Dec/10/2020

errata_c31w73_05

S1C31 Manual errata

ITEM: Appendix D Measures Against Noise			
Object manuals	Document codes	Items	Pages
S1C31D50/D51 Technical Manual	413699403	Appendix D Measures Against Noise	AP-D-1
S1C31W65 Technical Manual	414076300	Appendix D Measures Against Noise	AP-D-1
S1C31W73 Technical Manual	414076300	Appendix D Measures Against Noise	AP-D-1

（Error）

No description

（Correct）

Noise Measures for input terminals connected to signals with high drive capability such as power supplies

If there are terminals that are directly connected to the output of a power supply or a device with high drive capability, a large current may flow due to noise entering these terminals. In such a case insert a resistor of 30Ω or more in series to protect the terminals. Determine the resistance value after evaluation on the mounting board. When connecting the power supply directly to the VREFA terminal, insert a 100Ω resistor in series. In this case, there is no effect on the characteristics of the ADC.

Dec/10/2020

errata_c31w73_04

S1C31 Manual errata

ITEM: Limitation of changing RDWAIT settings

Object manuals	Document codes	Items	Pages
S1C31W65 Technical Manual	414063300	4.8 Control Register	4-10
S1C31W73 Technical Manual	414076300	4.9 Control Register	4-11
S1C31W74 Technical Manual	413374500	4.9 Control Register	4-10
S1C31D01 Technical Manual	413520400	4.8 Control Register	4-12
S1C31D50/D51 Technical Manual	413699403	4.8 Control Register	4-10

（Error）Control Register

FLASHC Flash Read Cycle Register

Bits 1-0 RDWAIT[1:0]

These bits set the number of bus access cycles for reading from the Flash memory.

Note: Be sure to set the FLASHCWAIT.RDWAIT[1:0] bits before the system clock is configured.

（Correct）Control Register

FLASHC Flash Read Cycle Register

Bits 1-0 RDWAIT[1:0]

These bits set the number of bus access cycles for reading from the Flash memory.

Note:・Be sure to set the FLASHCWAIT.RDWAIT[1:0] bits before the system clock is configured.

・When changing the setting of the FLASHCWAIT.RDWAIT [1: 0] bits from 0x2 to 0x1, insert two NOP instructions immediately after that.

(Example of program)

```
FLASHC->WAIT  b.RDWAIT = 1;
asm(“NOP”);
asm(“NOP”);
CLG->OSC  b.IOSCEN = 0;
```

Dec/10/2020

errata_c31w73_03

S1C31 Manual errata

ITEM: Instruction Cache

Object manuals	Document codes	Items	Pages
S1C31W65 Technical Manual	414063300	1.1 Features 4.7 Instruction Cache 4.8 Control Register	1-1 4-9 4-10
S1C31W73 Technical Manual	414076300	1.1 Features 4.7 Instruction Cache 4.9 Control Register	1-1 4-10 4-11
S1C31D50/D51 Technical Manual	413699403	1.1 Features 4.6 Instruction Cache 4.8 Control Register	1-1 4-9 4-10

（Error）Features

Embedded RAMs	
Instruction cache	512 bytes

（Correct）Features

Embedded RAMs	
Instruction cache	512 byte *It is prohibited to use in this product.

（Error）Instruction Cache

This IC includes an instruction cache. Enabling the cache function translates into reduced current consumption, as the Flash memory access frequency is decreased.

This function is enabled by setting the CASHECTL.CACHEEN bit to 1. Setting this bit to 0 clears the instruction codes stored in the cache.

（Correct）Instruction Cache

This IC includes an instruction cache. Enabling the cache function translates into reduced current consumption, as the Flash memory access frequency is decreased.

This function is enabled by setting the CASHECTL.CACHEEN bit to 1. Setting this bit to 0 clears the instruction codes stored in the cache.

Note: This function is prohibited to use in this product.

（Error）Control Register

CACHE Control Register

Bit 0 CACHEEN

This bit enables the instruction cache function.

1 (R/W): Enable instruction cache

0 (R/W): Disable instruction cache

（Correct）Control Register

CACHE Control Register

Bit 0 CACHEEN

This bit enables the instruction cache function.

1 (R/W): Enable instruction cache

0 (R/W): Disable instruction cache

Note: This function is prohibited to use in this product.

Dec/10/2020

errata_c31w73_02

S1C31 Manual errata

ITEM: Corrective operation when a value out of the effective range is set

Object manuals	Document codes	Items	Pages
S1C31W65 Technical Manual	414063300	10.4.2 Real-Time Clock Counter Operations	10-4
S1C31W73 Technical Manual	414076300	10.4.2 Real-Time Clock Counter Operations	10-4
S1C31W74 Technical Manual	413374500	10.4.2 Real-Time Clock Counter Operations	10-4
S1C31D01 Technical Manual	413520400	10.4.2 Real-Time Clock Counter Operations	10-4
S1C31D50/D51 Technical Manual	413699403	10.4.2 Real-Time Clock Counter Operations	10-4

(Error)

Corrective operation when a value out of the effective range is set

When a value out of the effective range is set to the year, day of the week, or hour (in 24H mode) counter, the counter will be cleared to 0 at the next count-up timing. When a such value is set to the month, day, or hour (in 12H mode) counter, the counter will be set to 1 at the next count-up timing.

(Correct)

Corrective operation when a value out of the effective range is set

When a value out of the effective range is set to the year, day of the week, or hour (in 24H mode) counter, the counter will be cleared to 0 at the next count-up timing of the counter. When a such value is set to the month, day, or hour (in 12H mode) counter, the counter will be set to 1 at the next count-up timing of the counter.

Note: RTCMON.RTCMOH bits=0 & RTCMON.RTCMOL[3:0] bits=0x0 are prohibited.

Dec/10/2020

errata_c31w73_01

S1C31 Manual errata

ITEM: FLASHC Flash Read Cycle Register

Object manuals	Document codes	Items	Pages
S1C31W73 Technical Manual	414076300	4.9 Control Registers FLASHC Flash Read Cycle Register	4-11

（Error）

Table 4.9.1 Setting Number of Bus Access Cycles for Flash Read

FLASHCWAIT. RDWAIT[1:0] bits	Number of bus access cycles	System clock frequency	
		PWGACTL. REGSEL bit = 0	PWGACTL. REGSEL bit = 1
0x3	4	2.1 MHz (max.)	33 MHz (max.)
0x2	3		
0x1	2		
0x0	1	1.05 MHz (max.)	16 MHz (max.)

（Correct）

Table 4.9.1 Setting Number of Bus Access Cycles for Flash Read

FLASHCWAIT. RDWAIT[1:0] bits	Number of bus access cycles	System clock frequency	
		PWGACTL. REGSEL bit = 0	PWGACTL. REGSEL bit = 1
0x3	4	2.2 MHz (max.)	33.3 MHz (max.)
0x2	3		
0x1	2		
0x0	1	1.2 MHz (max.)	17.1 MHz (max.)