Jul/12/2019

errata_c31d50_01

S1C31 Manual Errata

ITEM CLGSCLK.CLKDIV register initial value miss write			
Object manual	Document code	item	Page
S1C31D50 Technical Manual	413699400	2.6 Control Registers Appendix A **List of Peripheral Circuit Control Registers**	2-16 AP-A-1

(Error)

2.6 Control Registers

CLG System Clock Control Register

Regsiter name	Bit	Bit name	Initial	Reset	R/W	Remarks
CLGSCLK	15	WUPMD	0	H0	R/WP	–
	14	–	0	–	R	
	13–12	WUPDIV[1:0]	0x0	H0	R/WP	
	11–10	–	0	–	R	
	9–8	WUPSRC[1:0]	0x0	H0	R/WP	
	7–6	–	0x0	–	R	
	5–4	CLKDIV[1:0]	0x0	H0	R/WP	
	3–2	–	0x0	–	R	
	1–0	CLKSRC[1:0]	0x0	H0	R/WP	

Appendix A List of Peripheral Circuit Control Registers

0x0020 0040–0x0020 0050 Clock Generator (CLG)

Address	Regsiter name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x0020	CLGSCLK	15	WUPMD	0	H0	R/WP	–
0040		14	–	0	–	R	
		13–12	WUPDIV[1:0]	0x0	H0	R/WP	
		11–10	–	0	–	R	
		9–8	WUPSRC[1:0]	0x0	H0	R/WP	
		7–6	–	0x0	–	R	
		5–4	CLKDIV[1:0]	0x0	H0	R/WP	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/WP	

(Correct)

2.6 Control Registers

CLG System Clock Control Register

Regsiter name	Bit	Bit name	Initial	Reset	R/W	Remarks
CLGSCLK	15	WUPMD	0	H0	R/WP	–
	14	–	0	–	R	
	13–12	WUPDIV[1:0]	0x0	H0	R/WP	
	11–10	–	0	–	R	
	9–8	WUPSRC[1:0]	0x0	H0	R/WP	
	7–6	–	0x0	–	R	
	5–4	CLKDIV[1:0]	0x2	H0	R/WP	
	3–2	–	0x0	–	R	
	1–0	CLKSRC[1:0]	0x0	H0	R/WP	

Appendix A List of Peripheral Circuit Control Registers

0x0020 0040–0x0020 0050 **Clock Generator (CLG)**

Address	Regsiter name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x0020	CLGSCLK	15	WUPMD	0	H0	R/WP	–
0040		14	–	0	–	R	
		13–12	WUPDIV[1:0]	0x0	H0	R/WP	
		11–10	–	0	–	R	
		9–8	WUPSRC[1:0]	0x0	H0	R/WP	
		7–6	–	0x0	–	R	
		5–4	CLKDIV[1:0]	0x2	H0	R/WP	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/WP	