Dec/10/2020

errata_c31d01_05

S1C31 Manual errata

ITEM: Limitation of changing RDWAIT settings

Object manuals	Document codes	Items	Pages
S1C31W65 Technical Manual	414063300	4.8 Control Register	4-10
S1C31W73 Technical Manual	414076300	4.9 Control Register	4-11
S1C31W74 Technical Manual	413374500	4.9 Control Register	4-10
S1C31D01 Technical Manual	413520400	4.8 Control Register	4-12
S1C31D50/D51 Technical Manual	413699403	4.8 Control Register	4-10

（Error）Control Register

FLASHC Flash Read Cycle Register

Bits 1-0 RDWAIT[1:0]

These bits set the number of bus access cycles for reading from the Flash memory.

Note: Be sure to set the FLASHCWAIT.RDWAIT[1:0] bits before the system clock is configured.

（Correct）Control Register

FLASHC Flash Read Cycle Register

Bits 1-0 RDWAIT[1:0]

These bits set the number of bus access cycles for reading from the Flash memory.

Note:・Be sure to set the FLASHCWAIT.RDWAIT[1:0] bits before the system clock is configured.

・When changing the setting of the FLASHCWAIT.RDWAIT [1: 0] bits from 0x2 to 0x1, insert two NOP instructions immediately after that.

(Example of program)

```
FLASHC->WAIT  b.RDWAIT = 1;
asm(“NOP”);
asm(“NOP”);
CLG->OSC  b.IOSCEN = 0;
```

Dec/10/2020

errata_c31d01_04

S1C31 Manual errata

ITEM: Corrective operation when a value out of the effective range is set

Object manuals	Document codes	Items	Pages
S1C31W65 Technical Manual	414063300	10.4.2 Real-Time Clock Counter Operations	10-4
S1C31W73 Technical Manual	414076300	10.4.2 Real-Time Clock Counter Operations	10-4
S1C31W74 Technical Manual	413374500	10.4.2 Real-Time Clock Counter Operations	10-4
S1C31D01 Technical Manual	413520400	10.4.2 Real-Time Clock Counter Operations	10-4
S1C31D50/D51 Technical Manual	413699403	10.4.2 Real-Time Clock Counter Operations	10-4

(Error)

Corrective operation when a value out of the effective range is set

When a value out of the effective range is set to the year, day of the week, or hour (in 24H mode) counter, the counter will be cleared to 0 at the next count-up timing. When a such value is set to the month, day, or hour (in 12H mode) counter, the counter will be set to 1 at the next count-up timing.

(Correct)

Corrective operation when a value out of the effective range is set

When a value out of the effective range is set to the year, day of the week, or hour (in 24H mode) counter, the counter will be cleared to 0 at the next count-up timing of the counter. When a such value is set to the month, day, or hour (in 12H mode) counter, the counter will be set to 1 at the next count-up timing of the counter.

Note: RTCMON.RTCMOH bits=0 & RTCMON.RTCMOL[3:0] bits=0x0 are prohibited.

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errata_c31d01_03

S1C31 Manual errata

ITEM: Real-Time Clock (RTCA) Theoretical Regulation Function			
Object manuals	Document codes	Items	Pages
S1C31W74 Technical Manual	413374500	10.3.2 Theoretical Regulation Function	10-2
S1C31D01 Technical Manual	413520400	10.3.2 Theoretical Regulation Function	10-2

(Error)

10.3.2 Theoretical Regulation Function

The time-of-day clock loses accuracy if the OSC1 frequency f_{OSC1} has a frequency tolerance from 32.768 kHz. To correct this error without changing any external part, RTCA provides a theoretical regulation function. Follow the procedure below to perform theoretical regulation.

1. Measure the frequency tolerance "m [ppm]" of f_{OSC1}.
2. Determine the theoretical regulation execution cycle time "n seconds."
3. Determine the value to be written to the RTCCTL.RTCTRM[6:0] bits from the results in Steps 1 and 2.
4. Write the value determined in Step 3 to the RTCCTL.RTCTRM[6:0] bits periodically in n-second cycles using an RTCA alarm or second interrupt.
5. Monitor the RTC1S signal to check that every n-second cycle has no error included.

The correction value for theoretical regulation can be specified within the range from -64 to +63 and it should be written to the RTCCTL.RTCTRM[6:0] bits as a two's-complement number. Use Eq. 9.1 to calculate the correction value.

n: Theoretical regulation execution cycle time [second] (time interval to write the correct value to the RTCCTL.
RTCTRM[6:0] bits periodically via software)
m: OSC1 frequency tolerance [ppm]

(Correct)

10.3.2 Theoretical Regulation Function

The time-of-day clock loses accuracy if the OSC1 frequency f_{OSC1} has a frequency tolerance from 32.768 kHz. To correct this error without changing any external part, RTCA provides a theoretical regulation function. Follow the procedure below to perform theoretical regulation.

1. Determine the correction value of frequency tolerance "m [ppm] =- {(f_{OSC1}-32768[Hz]) / 32768[Hz]}×10^6" by measuring the f_{OSC1}.
2. Determine the theoretical regulation execution cycle time "n seconds."
3. Determine the value to be written to the RTCCTL.RTCTRM[6:0] bits from the results in Steps 1 and 2.
4. Write the value determined in Step 3 to the RTCCTL.RTCTRM[6:0] bits periodically in n-second cycles using an RTCA alarm or second interrupt.
5. Monitor the RTC1S signal to check that every n-second cycle has no error included.

The correction value for theoretical regulation can be specified within the range from -64 to +63 and it should be written to the RTCCTL.RTCTRM[6:0] bits as a two's-complement number. Use Eq. 9.1 to calculate the correction value.

n: Theoretical regulation execution cycle time [second] (time interval to write the correct value to the RTCCTL.
RTCTRM[6:0] bits periodically via software)
m: OSC1's correction value of frequency tolerance [ppm]

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S1C31 Manual errata

ITEM: Flash Memory Pin

Object manuals	Document codes	Items	Pages
S1C31D01 Technical Manual	413520400	1.3.3 Pin Descriptions	1-9
		4.3.1 Flash Memory Pin	4-2
		25 Basic External Connection Diagram	25-1

(Error)

1.3.3 Pin Descriptions

Table 1.3.3.1 Pin Description

P16	P16	I/O	Hi-Z	–	I/O port
	EXCL11	I			16-bit PWM timer Ch.1 event counter input 1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)

4.3.1 Flash Memory Pin

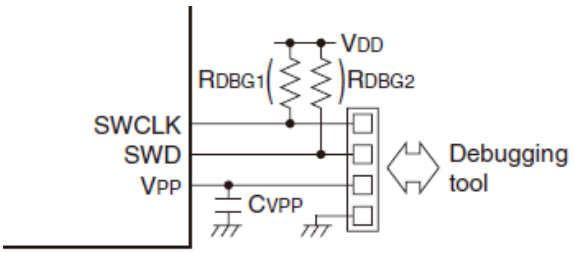
Table 4.3.1.1 Flash Memory Pin

Pin name	I/O	Initial status	Function
VPP	P	–	Flash programming power supply

For the VPP voltage, refer to "Recommended Operating Conditions, Flash programming voltage VPP" in the "Electrical Characteristics" chapter.

Note: Always leave the VPP pin open except when programming the Flash memory.

25 Basic External Connection Diagram



(Correct)

1.3.3 Pin Descriptions

Table 1.3.3.1 Pin Description

P16	P16 (ENVPP)	I/O	Hi-Z	–	I/O port (Flash programming control signal output)
	EXCL11	I			16-bit PWM timer Ch.1 event counter input 1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)

4.3.1 Flash Memory Pin

Table 4.3.1.1 Flash Memory Pin

Pin name	I/O	Initial status	Function
VPP	P	–	Flash programming power supply
(ENVPP)	O or Hi-Z	–	Flash programming control signal output

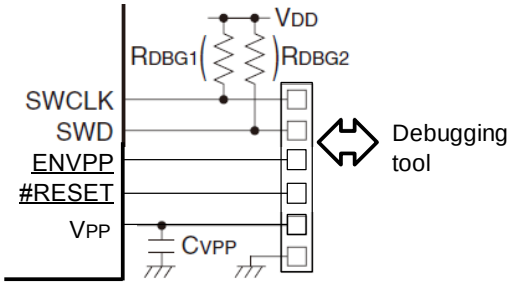
For the VPP voltage, refer to "Recommended Operating Conditions, Flash programming voltage VPP" in the "Electrical Characteristics" chapter.

Note: Always leave the VPP pin open except when programming the Flash memory.

The ENVPP pin outputs a control signal to the Bridge Board(S5U1C31001L) in flash programming.

Consider the influence of this signal on external circuit although it can be used as a normal pin.

25 Basic External Connection Diagram



Aug/07/2017

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S1C31 Manual Errata

ITEM Flash Programming

Object manual	Document code	item	Page
S1C31D01 Technical Manual	413520400	4.3.3 Flash Programming	4-3
		24.2 Recommended Operating Conditions	24-1
		Appendix C Mounting Precautions	AP-C-1

(Error)

4.3.3 Flash Programming

The Flash memory supports on-board programming, so it can be programmed using a flash loader.

The V_{PP} voltage can be supplied from either an external power supply or the internal voltage booster.

Choose the flash loader according to the V_{PP} power supply to be used.

Notes: · When the V_{PP} voltage is supplied externally, 2.4 V or more V_{DD} voltage is required.

· When the V_{PP} voltage is generated internally, 2.7 V or more V_{DD} voltage is required.

24.2 Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Capacitor between V_{SS} and V_{PP}	C_{VPP}	*5	-	0.1	-	µF

*5 C_{VPP} should be connected only when the V_{PP} voltage is not stable.

Appendix C Mounting Precautions

V_{PP} pin

If fluctuations in the Flash programming voltage V_{PP} is large, connect a capacitor C_{VPP} between the V_{SS} and V_{PP} pins to suppress fluctuations within V_{PP} ± 1 V. The C_{VPP} should be placed as close to the V_{PP} pin as possible and use a sufficiently thick wiring pattern that allows current of several tens of mA to flow.

(Correct)

4.3.3 Flash Programming

The Flash memory supports on-board programming, so it can be programmed using a flash loader.

The V_{PP} voltage can be supplied from either an external power supply or the internal voltage booster.

The V_{PP} voltage can also be generated by the internal power supply for generating the Flash programming voltage. Be sure to connect a capacitor C_{VPP} between the V_{SS} and V_{PP} pins for stabilizing the voltage when the V_{PP} voltage is supplied externally or for generating the voltage when the internal power supply

is used.

The V_{PP} pin must be left open except when programming the Flash memory. However, it is not necessary to disconnect the wire when using “Bridge Board (S5U1C31001L)” to supply the V_{PP} voltage, as Bridge Board controls the power supply so that it will be supplied during Flash programming only.

Notes: · When the V_{PP} voltage is supplied externally, 2.4 V or more V_{DD} voltage is required.

· When the V_{PP} voltage is generated internally, 2.7 V or more V_{DD} voltage is required

· Be sure to avoid using the V_{PP} pin output for driving external circuits when the V_{PP} voltage is generated internally.

24.2 Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Capacitor between V_{SS} and V_{PP}	C_{VPP}	~~*5~~	-	0.1	-	µF

~~*5 C_{VPP} should be connected only when the V_{PP} voltage is not stable.~~

Appendix C Mounting Precautions

V_{PP} pin

~~If fluctuations in the Flash programming voltage V_{PP} is large,~~ Connect a capacitor C_{VPP} between the V_{SS} and V_{PP} pins to suppress fluctuations within V_{PP} ± 1 V. The C_{VPP} should be placed as close to the V_{PP} pin as possible and use a sufficiently thick wiring pattern that allows current of several tens of mA to flow.