2006/10/11

IC Marketing & Engineering Section

S1C88655 Manual errata

ITEM　SERIAL INTERFACE		
Object manuals	Document code	Object page
S1C88655 Technical Manual	410757500	73,75,104

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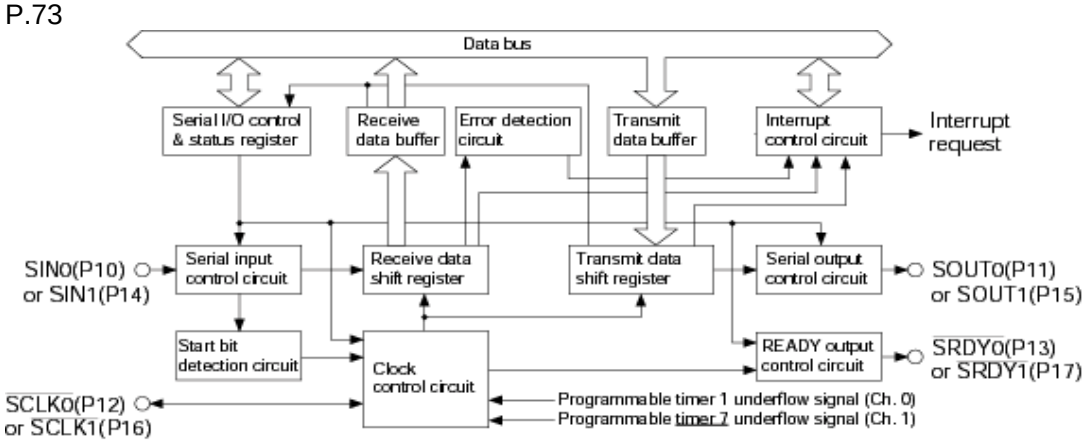

Fig. 11.1.1 Configuration of serial interface

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When the “programmable timer” is selected, the underflow signal of the programmable timer 1 for ch.0 or timer 7 for Ch.1 is divided by 2 and the divided signal is used as the clock source.

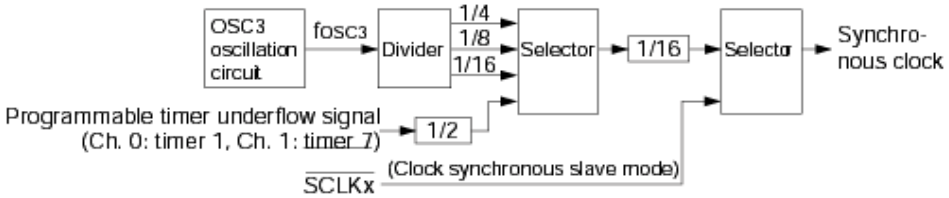

Fig. 11.4.1 Division of the synchronous clock

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The underflow signals of Timer 1 and Timer 7 can be used as the source clock for serial interface Ch.0 and Ch.1, respectively. The transfer rate is set using the registers PST1x and RDR1x for Ch. 0 or PST7x and RDR7x for Ch. 1. (since only the underflow signal is

used as the serial interface clock source, the CDR1x or CDR7x register value does not affect the transfer rates. It can be set to any value).

Since the underflow signal of Timer is divided by 32 in the serial interface, the value set in the register RDR1x or RDR7x which corresponds to the transfer rate is shown in the following expression:

$$RDR = \frac{fdiv}{32 \times bps} - 1$$

RDR: RDR1x or RDR7x set value
fdiv: Input clock frequency
(setting of PST1x or PST7x)
bps: Transfer rate

Table 13.7.1 Example of transfer rate setting

Transfer rate (bps)	OSC3 oscillation frequency / Programmable timer settings							
	fOSC3 = 2.4576 MHz		f OSC3 = 3.0720 MHz		f OSC3 = 3.6864 MHz		fOSC3 = 4.3008 MHz	
	PST1x PST7x	RDR1x RDR7x	PST1x PST7x	RDR1x RDR7x	PST1x PST7x	RDR1x RDR7x	PST1x PST7x	RDR1x RDR7x
19,200	00H	03H	00H	04H	00H	05H	00H	06H
9,600	00H	07H	00H	09H	00H	0BH	00H	0DH
4,800	00H	0FH	00H	13H	00H	17H	00H	1BH
2,400	00H	1FH	00H	27H	00H	2FH	00H	37H
1,200	00H	3FH	00H	4FH	00H	5FH	00H	6FH
600	00H	7FH	00H	9FH	00H	BFH	00H	DFH
300	02H	1FH	03H	09H	01H	BFH	01H	DFH
150	02H	3FH	03H	13H	02H	5FH	02H	6FH

* Since the underflow signal only is used as the clock source, the CDR1x or CDR7x register value does not affect the transfer rates.

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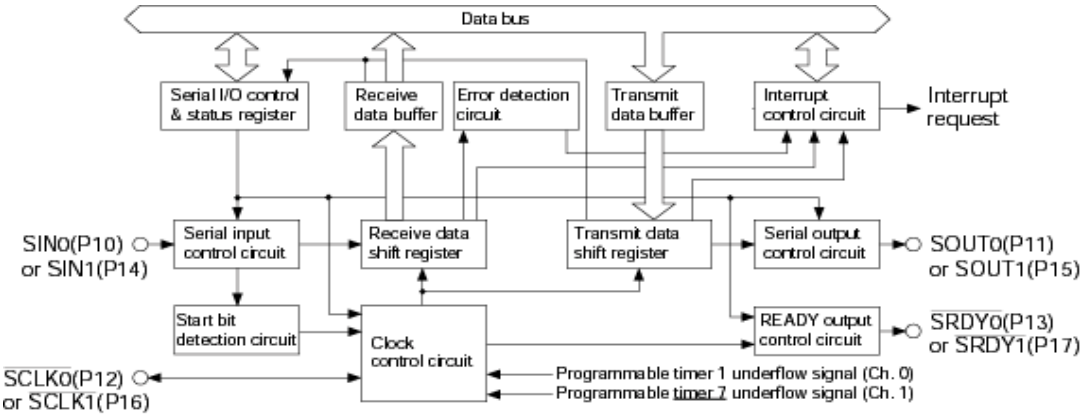

Fig. 11.1.1 Configuration of serial interface

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When the “programmable timer” is selected, the underflow signal of the programmable timer 1 for ch.0 or timer 5 for Ch.1 is divided by 2 and the divided signal is used as the clock source.

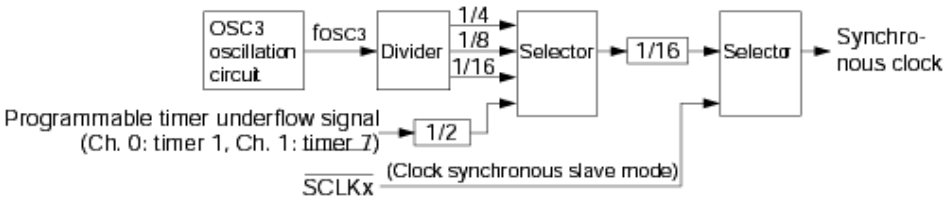

Fig. 11.4.1 Division of the synchronous clock

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The underflow signals of Timer 1 and Timer 5 can be used as the source clock for serial interface Ch.0 and Ch.1, respectively. The transfer rate is set using the registers PST1x and RDR1x for Ch. 0 or PST5x and RDR5x for Ch. 1. (since only the underflow signal is used as the serial interface clock source, the CDR1x or CDR7x register value does not affect the transfer rates. It can be set to any value).

Since the underflow signal of Timer is divided by 32 in the serial interface, the value set in the register RDR1x or RDR5x which corresponds to the transfer rate is shown in the following expression:

$$\mathbf{RDR} = \frac{\mathbf{fdiv}}{\mathbf{32} \times \mathbf{bps}} - \mathbf{1}$$

RDR: RDR1x or RDR7x set value
fdiv: Input clock frequency
(setting of PST1x or PST5x)
bps: Transfer rate

Table 13.7.1 Example of transfer rate setting

Transfer rate (bps)	OSC3 oscillation frequency / Programmable timer settings							
	fosc3 = 2.4576 MHz		f osc3 = 3.0720 MHz		f osc3 = 3.6864 MHz		fosc3 = 4.3008 MHz	
	PST1x PST5x	RDR1x RDR5x	PST1x PST5x	RDR1x RDR5x	PST1x PST5x	RDR1x RDR5x	PST1x PST5x	RDR1x RDR5x
19,200	00H	03H	00H	04H	00H	05H	00H	06H
9,600	00H	07H	00H	09H	00H	0BH	00H	0DH
4,800	00H	0FH	00H	13H	00H	17H	00H	1BH
2,400	00H	1FH	00H	27H	00H	2FH	00H	37H
1,200	00H	3FH	00H	4FH	00H	5FH	00H	6FH
600	00H	7FH	00H	9FH	00H	BFH	00H	DFH
300	02H	1FH	03H	09H	01H	BFH	01H	DFH
150	02H	3FH	03H	13H	02H	5FH	02H	6FH

* Since the underflow signal only is used as the clock source, the CDR1x or CDR5x register value does not affect the transfer rates.