S1C63 Manual errata

ITEM:			
Object manuals	Document codes	Items	Pages
S1C6F016 Technical Manual	411801400	C.2.3 Serial Programming Procedure	AP-C-3
S1C6F416 Technical Manual	404736203	A.2.3 Serial Programming Procedure	132
S1C6F632 Technical Manual	411707400a	B.2.3 Serial programming procedure	226
S1C6F666 Technical Manual	410963501	A.2.3 Serial programming procedure	208

(Error)

(4) Installing the USB-Serial conversion driver

(Required only when the USB-Serial On Board Writer is used)

When the USB-Serial On Board Writer (S5U1C88000W4) is connected for the first time, a dialog box appears on the PC screen to prompt the user to install the driver. Install the USB-Serial conversion driver by following the prompts. The USB-Serial conversion driver was copied in the "¥EPSON¥S1C63¥writer¥driver" folder when the S1C63 Family Assembler Package 2 (S5U1C63000A2) was installed. Specify this folder as the driver location.

(Correct)

(4) Installing the USB-Serial conversion driver

(Required only when the USB-Serial On Board Writer is used)

When the USB-Serial On Board Writer (S5U1C88000W4) is connected for the first time, a dialog box appears on the PC screen to prompt the user to install the driver. Install the USB-Serial conversion driver by following the prompts. The USB-Serial conversion driver was copied in the "¥EPSON¥S1C63¥writer¥driver" **and "¥EPSON¥S1C63¥writer¥driver1"** folder when the S1C63 Family Assembler Package 2 (S5U1C63000A2) was installed. Specify **as follows** folder as the driver location.

Serial number of S5U1C88000W4100 (written on the back side of the board	Location of the driver
0Z04W73001-0Z04W84050	/EPSON/S1C63/writer/driver
0Z04W87001 or later	/EPSON/S1C63/writer/driver1

S1C63 Manual errata

ITEM:			
Object manuals	Document codes	Items	Pages
S1C6F632	411707400a	4.13.8 Programming notes Add to (4)	P159
		6.2 Summary of Notes by Function R/f converter Add to (3)	P178

(Error)

(Correct)　Add

Reference/sensor oscillation frequency vs voltage deviation is increase under 2V, please take into account this characteristic.

S1C63 Manual errata

ITEM:			
Object manuals	Document codes	Items	Pages
S1C6F632	411707400a	4.5.9 Programming notes	P60
		6.2 Summary of Notes by Function I/O port	P176

(Error)

(1)

  C: terminal capacitance 5 pF + parasitic capacitance ? pF

  R: pull-down resistance 375 kO (Max.)

(Correct)

(1)

  C: terminal capacitance 15 pF + parasitic capacitance ? pF

  R: pull-down resistance 500 kO (Max.)

S1C63 Manual errata

ITEM:			
Object manuals	Document codes	Items	Pages
S1C6F632	411707400a	2.1.2 Internal power supply circuit Fig.2.1.2.1 Configuration of power supply circuit	P9
		4.2.1 Configuration of power supply circuit Fig.4.1.2.1 Built-in power supply circuit	P32

(Error)

Pin name

SEG0-63

(Correct)

Pin name

SEG0-47

S1C63 Manual errata

ITEM:			
Object manuals	Document codes	Items	Pages
S1C6F632	411707400a	1.2 Block Diagram Fig.1.2.1 Block Diagram	P3

(Error)

Pin name

(SEG48-63)COM16-31

(Correct)

Pin name

(SEG63-48)COM16-31

S1C63 Manual errata

ITEM: Additional explanation and note about execution of SLP instruction			
Object manuals	Document codes	Items	Pages
S1C6F632	411707400a	4.15 Interrupt and HALT/SLEEP 6.2 Summary of Notes by Function	162,171, 179
S1C63632	411863800a	4.15 Interrupt and HALT/SLEEP 5.2 Summary of Notes by Function	163,172, 178

(Error)   **- S1C6F632 (P162)   S1C63632 (P163)-**

<HALT/SLEEP>

When the CPU enters SLEEP status as the result of the SLP instruction, the CPU stops its operation and the OSC1 and OSC3 oscillation circuits are also stop.

Reactivating from SLEEP status can only be done by generation of a key input interrupt request from a P1x or P4x port. Therefore, set the following flag and the registers for the I/O port to be used to cancel SLEEP status before executing the SLP instruction.

• Interrupt flag (I flag) = "1" (interrupts are enabled)

• Interrupt select register SIPxx = "1" (the Pxx I/O port interrupt is selected)

• Interrupt mask register EIKxx = "1" (the Pxx I/O port interrupt is enabled)

• Noise rejector select register NRSPxx = "00" (noise rejector is bypassed)

(Correct)　**- S1C6F632 (P162)　S1C63632 (P163)-**

<HALT/SLEEP>

When the CPU enters SLEEP status as the result of the SLP instruction, the CPU stops its operation and the OSC1 and OSC3 oscillation circuits are also stop. Therefore, the power supply voltage booster/halver cannot generate VD2 in SLEEP mode. If it is used VD2 to drive the LCD system voltage regulator, it is necessary to switch VDD before executing the SLP instruction. And to prevent improper operation after the CPU wakes up, be sure to run the CPU with the OSC1 clock before setting the CPU in the SLEEP mode.

Reactivating from SLEEP status can only be done by generation of a key input interrupt request from a P1x or P4x port. ~~Therefore, set the following flag and the registers for the I/O port to be used to cancel SLEEP status before executing the SLP instruction.~~

~~• Interrupt flag (I flag) = "1" (interrupts are enabled)~~

~~• Interrupt select register SIPxx = "1" (the Pxx I/O port interrupt is selected)~~

~~• Interrupt mask register EIKxx = "1" (the Pxx I/O port interrupt is enabled)~~

~~• Noise rejector select register NRSPxx = "00" (noise rejector is bypassed)~~

Therefore, set and confirm the P1(4)x input level, the flag and the registers for the P1(4)x port, the CPU clock, and the power control according to the following procedures to be used to enter / cancel SLEEP status before executing the SLP instruction surely.

1. LCD system voltage regulator power source switch register VCSEL="0"
   Power supply voltage booster/halver boost mode On/Off register DBON="0"
   (LCD system voltage regulator is driven with VDD)
2. CPU system clock switching register CLKCHG = "0" (OSC1 CPU clock is selected)
3. Interrupt selection register SIPxx = "1" (the Pxx input port interrupt is selected)
4. Interrupt mask register EIKxx = "1" (the Pxx input port interrupt is enabled)
5. Noise rejector selection register NRSPxx = "00" (noise rejector is bypassed)
6. Reset the Pxx input interrupt factor flag register (write "1" to the IKxx register)
7. Interrupt flag (I flag) = "1" (interrupts are enabled)
8-1. Confirm the input to the P1(4)x port is surely HIGH level when the P1(4)x port interrupt polarity select register = "1"(interrupt request signal is generated at the falling edge)
8-2. Confirm the input to the P1(4)x port is surely LOW level when the P1(4)x port interrupt polarity select register = "0"(interrupt request signal is generated at the rising edge)
9. Execute SLP instruction

(Error) **- S1C6F632 (P171)   S1C63632 (P172)-**

4.15.5 Programming notes

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(4) When using the SLEEP function, set the interrupt flag and the registers for the I/O port to be used to cancel SLEEP status as below before executing the SLP instruction.
  • Interrupt flag (I flag) = "1" (interrupts are enabled)
  • Interrupt select register SIPxx = "1" (the Pxx I/O port interrupt is selected
  • Interrupt mask register EIKxx = "1" (the Pxx I/O port interrupt is enabled)
  • Noise rejector select register NRSPxx = "00" (noise rejector is bypassed)

(Correct) **- S1C6F632 (P171)   S1C63632 (P172)-**

4.15.5 Programming notes

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(4) When using the SLEEP function, ~~set the interrupt flag and the registers for the I/O port to be used to cancel SLEEP status as below before executing the SLP instruction.~~
  ~~• Interrupt flag (I flag) = "1" (interrupts are enabled)~~
  ~~• Interrupt select register SIPxx = "1" (the Pxx I/O port interrupt is selected~~
  ~~• Interrupt mask register EIKxx = "1" (the Pxx I/O port interrupt is enabled)~~
  ~~• Noise rejector select register NRSPxx = "00" (noise rejector is bypassed)~~

set and confirm the P1(4)x input level, the flag and the registers for the P1(4)x port, the CPU clock, and the power control according to the following procedures to be used to enter / cancel SLEEP status before executing the SLP instruction surely.

1. LCD system voltage regulator power source switch register VCSEL="0"
     Power supply voltage booster/halver boost mode On/Off register DBON="0"
     (LCD system voltage regulator is driven with VDD)

2. CPU system clock switching register CLKCHG = "0" (OSC1 CPU clock is selected)

3. Interrupt selection register SIPxx = "1" (the Pxx input port interrupt is selected)

4. Interrupt mask register EIKxx = "1" (the Pxx input port interrupt is enabled)

5. Noise rejector selection register NRSPxx = "00" (noise rejector is bypassed)

6. Reset the Pxx input interrupt factor flag register (write "1" to the IKxx register)

7. Interrupt flag (I flag) = "1" (interrupts are enabled)

8-1. Confirm the input to the P1(4)x port is surely HIGH level when the P1(4)x port interrupt polarity select register = "1"(interrupt request signal is generated at the falling edge)

8-2. Confirm the input to the P1(4)x port is surely LOW level when the P1(4)x port interrupt polarity select register = "0"(interrupt request signal is generated at the rising edge)

9. Execute SLP instruction

(Error)   **- S1C6F632 (P179)   S1C63632 (P178)-**

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(4)   When using the SLEEP function, set the interrupt flag and the registers for the I/O port to be used to cancel SLEEP status as below before executing the SLP instruction.
   • Interrupt flag (I flag) = "1" (interrupts are enabled)
   • Interrupt select register SIPxx = "1" (the Pxx I/O port interrupt is selected
   • Interrupt mask register EIKxx = "1" (the Pxx I/O port interrupt is enabled)
   • Noise rejector select register NRSPxx = "00" (noise rejector is bypassed)

(Correct)   **- S1C6F632 (P179)   S1C63632 (P178)-**

Interrupt

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(4)   When using the SLEEP function, ~~set the interrupt flag and the registers for the I/O port to be used to cancel SLEEP status as below before executing the SLP instruction.~~
   ~~• Interrupt flag (I flag) = "1" (interrupts are enabled)~~
   ~~• Interrupt select register SIPxx = "1" (the Pxx I/O port interrupt is selected~~
   ~~• Interrupt mask register EIKxx = "1" (the Pxx I/O port interrupt is enabled)~~
   ~~• Noise rejector select register NRSPxx = "00" (noise rejector is bypassed)~~

set and confirm the P1(4)x input level, the flag and the registers for the P1(4)x port, the CPU clock, and the power control according to the following procedures to be used to enter / cancel SLEEP status before executing the SLP instruction surely.

1.   LCD system voltage regulator power source switch register VCSEL="0"
      Power supply voltage booster/halver boost mode On/Off register DBON="0"
      (LCD system voltage regulator is driven with VDD)
2.   CPU system clock switching register CLKCHG = "0" (OSC1 CPU clock is selected)
3.   Interrupt selection register SIPxx = "1" (the Pxx input port interrupt is selected)
4.   Interrupt mask register EIKxx = "1" (the Pxx input port interrupt is enabled)
5.   Noise rejector selection register NRSPxx = "00" (noise rejector is bypassed)
6.   Reset the Pxx input interrupt factor flag register (write "1" to the IKxx register)
7.   Interrupt flag (I flag) = "1" (interrupts are enabled)
8-1. Confirm the input to the P1(4)x port is surely HIGH level when the P1(4)x port interrupt polarity select register = "1"(interrupt request signal is generated at the falling edge)
8-2. Confirm the input to the P1(4)x port is surely LOW level when the P1(4)x port interrupt polarity select register = "0"(interrupt request signal is generated at the rising edge)
9.   Execute SLP instruction

S1C6F632 Manual errata

ITEM: PWM output signal's output terminal			
Object manuals	Document codes	Items	Pages
S1C6F632	411707400a	4.9.5 PWM mode(Timers 0-7)	P102

(Error)

The generated PWM signal can be output from an I/O port (P12,P41,P42,P43) terminal (see Section 4.9.8).

(Correct)

The generated PWM signal can be output from an I/O port (P13,P31,P32,P33) terminal (see Section 4.9.8).