Feb/28/2014

errata_c33l27_5

S1C33 Manual errata

ITEM: The A0RAM operating condition at the time of cash use			
Object manuals	Document codes	Items	Pages
S1C33L27 Technical Manual	411911901	12.2 Cache Configuration	12-2

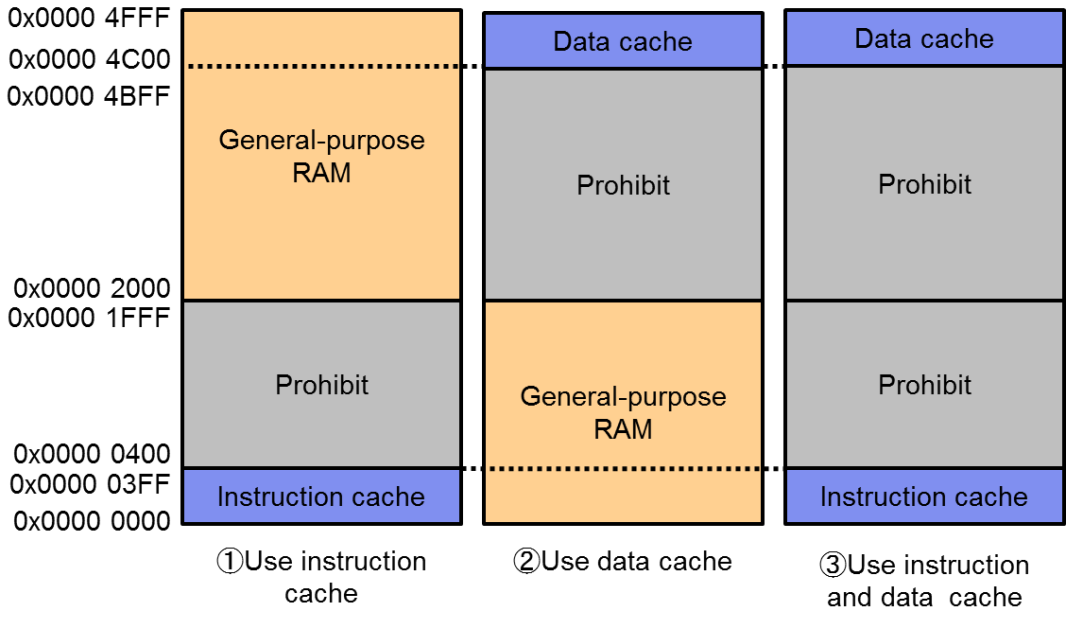
(Error)

The method of using A0RAM as general-purpose RAM at the time of cash use is not clear.

(Correct)

Add the following contents.

When you use A0RAM as general-purpose RAM at the time of cash use, please use it by the following allocation.



Jan/29/2014

errata_c33l27_4

S1C33 Technical Manual Errata

ITEM: USI/USIL AC Characteristics			
Object manual	Document code	Object ITEM	Page
S1C33L27 Technical Manual	411911901	32.8.4 USI/USIL AC Characteristics	32-11

32-11

(Error)

SPI master mode (normal mode)

Unless otherwise specified: LVDD = 1.65 to 1.95V, HVDD = 2.7 to 3.6V, VSS = 0V, Ta = -40 to 85°C

Item	Symbol	Min.	Typ.	Max.	Unit
spi_ck cycle time	tSPCK	42 + tPCLK	-	-	ns
spi_di setup time	tSDS	42 + tPCLK	-	-	ns

SPI master mode (fast mode)

Unless otherwise specified: LVDD = 1.65 to 1.95V, HVDD = 2.7 to 3.6V, VSS = 0V, Ta = -40 to 85°C

Item	記号	Min.	Typ.	Max.	Unit
spi_ck cycle time	tSPCK	44	-	-	ns
spi_di setup time	tSDS	44	-	-	ns

(Correct)

SPI master mode (normal mode)

Unless otherwise specified: LVDD = 1.65 to 1.95V, HVDD = 2.7 to 3.6V, VSS = 0V, Ta = -40 to 85°C

Item	Symbol	Min.	Typ.	Max.	Unit
spi_ck cycle time	tSPCK	**(42 + tPCLK) x 2**	-	-	ns
spi_di setup time	tSDS	42 + tPCLK	-	-	ns

SPI master mode (fast mode)

Unless otherwise specified: LVDD = 1.65 to 1.95V, HVDD = 2.7 to 3.6V, VSS = 0V, Ta = -40 to 85°C

Item	記号	Min.	Typ.	Max.	Unit
spi_ck cycle time	tSPCK	**44 x 2**	-	-	ns
spi_di setup time	tSDS	44	-	-	ns

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errata_c33l27_3

S1C33 Series Technical Manual Errata

ITEM Control and Operation of SDRAM Interface

Object manual	Document code	Object item	Page
S1C33E07 Technical Manual	410573604	II.4 SDRAM Controller (SDRAMC)	II-4-14, 15
S1C33E08 Technical Manual	410865100	II.4 SDRAM Controller (SDRAMC)	II-4-14, 15
S1C33L05 Technical Manual	405262000	VIII-2 SDRAM INTERFACE	VIII-2-15
S1C33L17 Technical Manual	411520600	II.4 SDRAM Controller (SDRAMC)	II-4-14, 15
S1C33L18 Technical Manual	411573200	II.4 SDRAM Controller (SDRAMC)	II-4-14, 15
S1C33L19 Technical Manual	411664200	II.4 SDRAM Controller (SDRAMC)	II-4-14, 15
S1C33L26 Technical Manual	411900101	10 SDRAM Controller (SDRAMC)	10-11, 12
S1C33L27 Technical Manual	411911901	10 SDRAM Controller (SDRAMC)	10-10, 11

Page II-4-14 S1C33E07 Technical Manual

Page II-4-14 S1C33E08 Technical Manual

Page VIII-2-15 S1C33L05 Technical Manual

Page II-4-14 S1C33L17 Technical Manual

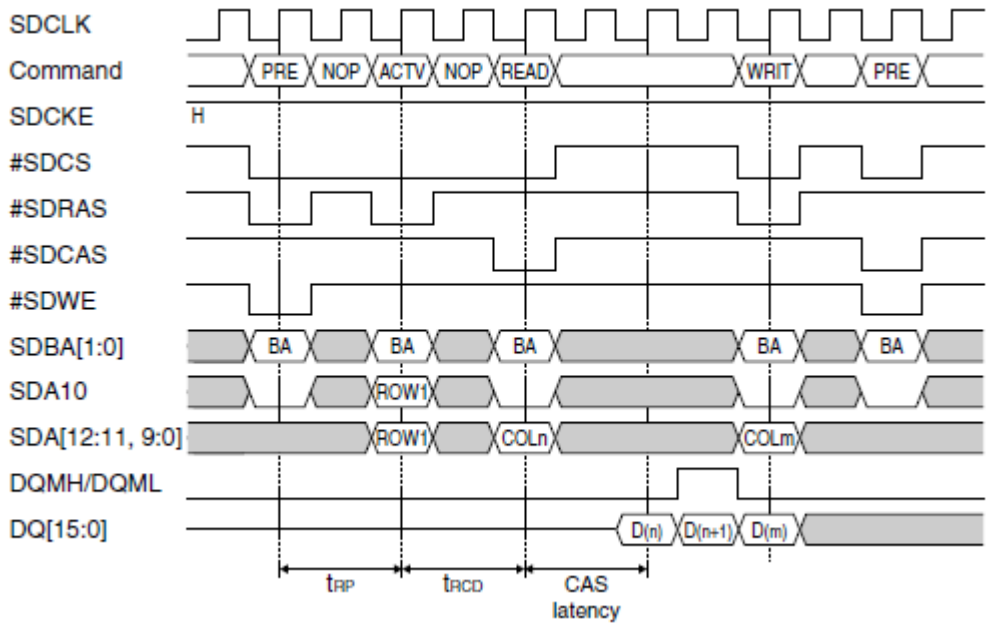
Page II-4-14 S1C33L18 Technical Manual

Page II-4-14 S1C33L19 Technical Manual

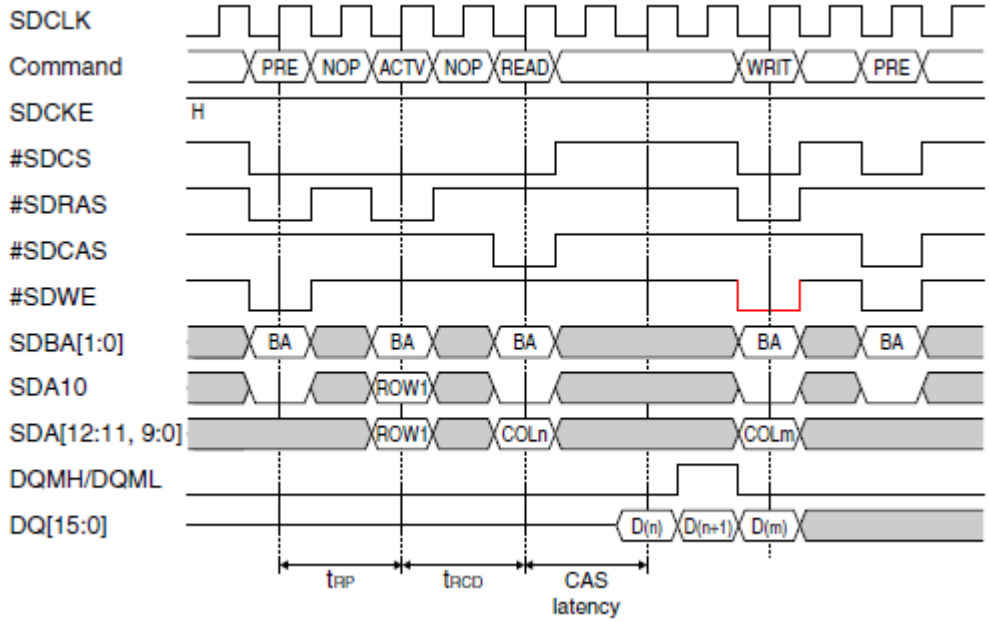
Page 10-11 S1C33L26 Technical Manual

Page 10-10 S1C33L27 Technical Manual

(Error)



(Correct)



Page II-4-15 S1C33E07 Technical Manual

Page II-4-15 S1C33E08 Technical Manual

Page II-4-15 S1C33L17 Technical Manual

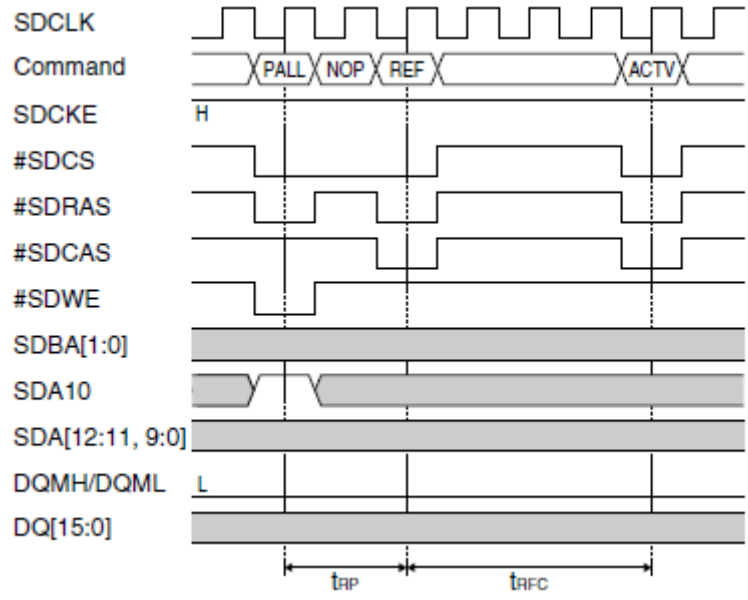
Page II-4-15 S1C33L18 Technical Manual

Page II-4-15 S1C33L19 Technical Manual

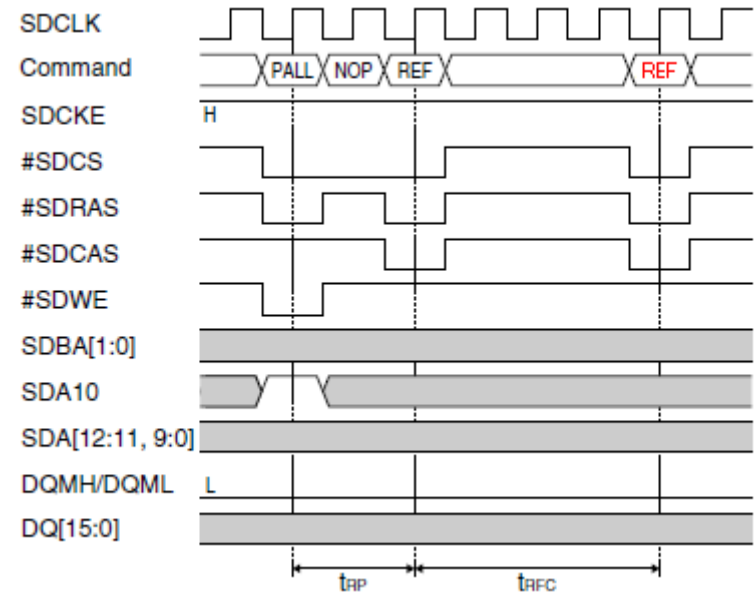
Page 10-12 S1C33L26 Technical Manual

Page 10-11 S1C33L27 Technical Manual

(Error)



(Correct)


SDCLK
Command
PALL
NOP
REF
REF
SDCKE
H
#SDCS
#SDRAS
#SDCAS
#SDWE
SDBA[1:0]
SDA10
SDA[12:11, 9:0]
DQMH/DQML
L
DQ[15:0]
tRP
tRFC

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errata_c33l27_2

S1C33 Manual errata

ITEM: SRAM AC Characteristics

Object manuals	Document codes	Items	Pages
S1C33L27 Technical Manual	411911901	32.8.2 SRAMC AC Characteristics	32-8

(Error)

Unless otherwise specified: LV_{DD} = 1.65 to 1.95V, HV_{DD} = 2.7 to 3.6V, V_{SS} = 0V, external load = 50pF, Ta = -40 to 85°C

Item	Symbol	Min.	Typ.	Max.	Unit
CMU_CLK output delay time	t_{CD}	–	–	24	ns
Address delay time	t_{AD}	–	–	7	ns
#CEx delay time	t_{CED}	–	–	7	ns
Write delay time	t_{WRD}	–	–	7	ns
Write data delay time	t_{WRDD}	–	–	7	ns
Write data hold time	t_{WRDH}	1	–	–	ns
Read delay time	t_{RDD}	–	–	7	ns
Read data setup time	t_{RDS}	7	–	–	ns
Read data hold time	t_{RDDH}	0	–	–	ns
Write signal pulse width	t_{WRW}	t_{CYC}(1 + WC) - 7	–	–	ns
Read signal pulse width	t_{RDW}	t_{CYC}(1 + WC) - 7	–	–	ns
Read address access time	t_{ACC}	–	–	t_{CYC}(1 + WC) - 14	ns
Chip enable access time	t_{CEAC}	–	–	t_{CYC}(1 + WC) - 14	ns
Read signal access time	t_{RDAC}	–	–	t_{CYC}(1 + WC) - 14	ns
#WAIT setup time	t_{WTS}	48	–	–	ns
#WAIT hold time	t_{WTH}	0	–	–	ns

WC: Number of wait cycles

(Correct)

Unless otherwise specified: LV_{DD} = 1.65 to 1.95V, HV_{DD} = 2.7 to 3.6V, V_{SS} = 0V, external load = 50pF, Ta = -40 to 85°C

Item	Symbol	Min.	Typ.	Max.	Unit
CMU_CLK output delay time	t_{CD}	–	–	24	ns
SRAM cycle time	t_{CYC}	*	–	–	ns
Address delay time	t_{AD}	–	–	7	ns
#CEx delay time	t_{CED}	–	–	7	ns
Write delay time	t_{WRD}	–	–	7	ns
Write data delay time	t_{WRDD}	–	–	7	ns
Write data hold time	t_{WRDH}	1	–	–	ns
Read delay time	t_{RDD}	–	–	7	ns
Read data setup time	t_{RDS}	7	–	–	ns
Read data hold time	t_{RDDH}	0	–	–	ns
Write signal pulse width	t_{WRW}	t_{CYC}(1 + WC) - 7	–	–	ns
Read signal pulse width	t_{RDW}	t_{CYC}(1 + WC) - 7	–	–	ns
Read address access time	t_{ACC}	–	–	t_{CYC}(1 + WC) - 14	ns
Chip enable access time	t_{CEAC}	–	–	t_{CYC}(1 + WC) - 14	ns
Read signal access time	t_{RDAC}	–	–	t_{CYC}(1 + WC) - 14	ns
#WAIT setup time	t_{WTS}	48	–	–	ns
#WAIT hold time	t_{WTH}	0	–	–	ns

WC: Number of wait cycles

* : The SRAM cycle time is same as SYSCLK.
The minimum cycle time to output CMU_CLK signal is Min.20.8ns

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errata_c33l27_1

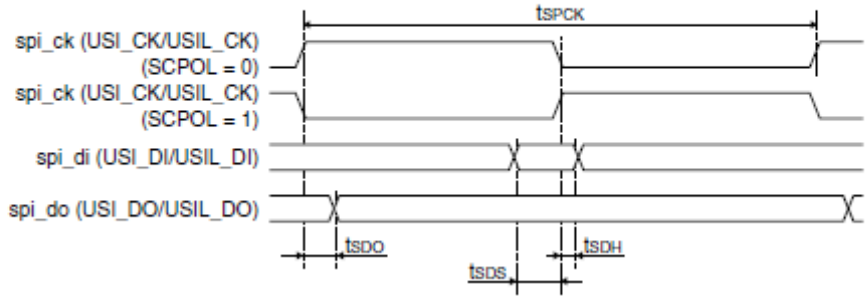
S1C33 Manual errata

ITEM: Modification AC Characteristics about USI SPI slave mode			
Object manuals	Document codes	Items	Pages
S1C33L27 Technical Manual	411911901	32.8.4 USI/USIL AC Characteristics	32-11

(Error)

32.8.4 USI/USIL AC Characteristics

SPI master/slave mode (USI/USIL)



. . .

SPI slave mode

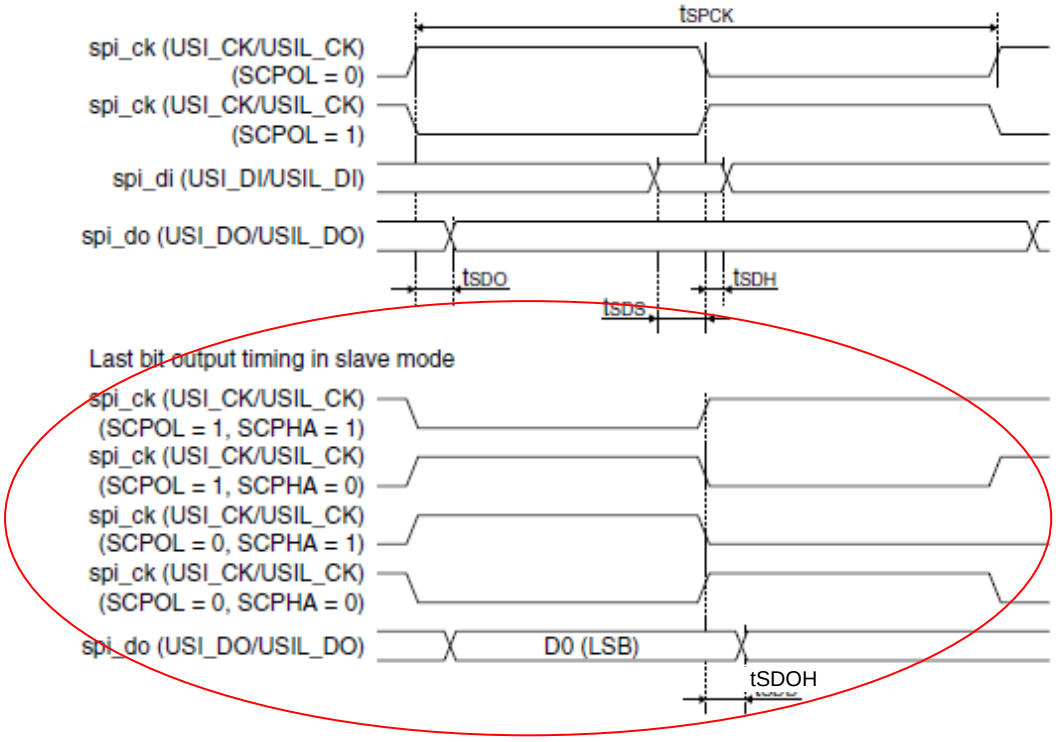
Unless otherwise specified: LV_{DD} = 1.65 to 1.95V, HV_{DD} = 2.7 to 3.6V, V_{SS} = 0V, Ta = -40 to 85°C

Item	Symbol	Min.	Typ.	Max.	Unit
spi_ck cycle time	t_{SPCK}	29 + t_{PCLK}	–	–	ns
spi_di setup time	t_{SDS}	20 + t_{PCLK}	–	–	ns
spi_di hold time	t_{SDH}	9	–	–	ns
spi_do output delay time	t_{SDO}	–	–	42	ns
spi_do output hold time	t_{SDOH}	–	–	2 × t_{PCLK} + 40.552	ns

t_{PCLK}: PCLK (peripheral module clock supplied from the CMU) clock cycle time

(Correct)

SPI master/slave mode (USI/USIL)



. . .

SPI slave mode

Unless otherwise specified: LV_{DD} = 1.65 to 1.95V, HV_{DD} = 2.7 to 3.6V, V_{SS} = 0V, Ta = -40 to 85°C

Item	Symbol	Min.	Typ.	Max.	Unit
spi_ck cycle time	t_{SPCK}	29 + t_{PCLK}	–	–	ns
spi_di setup time	t_{SDS}	20 + t_{PCLK}	–	–	ns
spi_di hold time	t_{SDH}	9	–	–	ns
spi_do output delay time	t_{SDO}	–	–	42	ns
spi_do output hold time	t_{SDOH}	2*tPCLK	–		ns

t_{PCLK}: PCLK (peripheral module clock supplied from the CMU) clock cycle time