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S1C33 Technical Manual Errata

ITEM: USI/USIL AC Characteristics

Object manual	Document code	Object ITEM	Page
S1C33L26 Technical Manual	411900101	31.8.4 USI/USIL AC Characteristics	31-11

31-11

(Error)

SPI master mode (normal mode)

Unless otherwise specified: LVDD = 1.65 to 1.95V, HVDD = 2.7 to 3.6V, VSS = 0V, Ta = -40 to 85°C

Item	Symbol	Min.	Typ.	Max.	Unit
spi_ck cycle time	tSPCK	85 + tPCLK	-	-	ns
spi_di setup time	tSDS	85 + tPCLK	-	-	ns

SPI master mode (fast mode)

Unless otherwise specified: LVDD = 1.65 to 1.95V, HVDD = 2.7 to 3.6V, VSS = 0V, Ta = -40 to 85°C

Item	記号	Min.	Typ.	Max.	Unit
spi_ck cycle time	tSPCK	85	-	-	ns
spi_di setup time	tSDS	85	-	-	ns

(Correct)

SPI master mode (normal mode)

Unless otherwise specified: LVDD = 1.65 to 1.95V, HVDD = 2.7 to 3.6V, VSS = 0V, Ta = -40 to 85°C

Item	Symbol	Min.	Typ.	Max.	Unit
spi_ck cycle time	tSPCK	**(85 + tPCLK) x 2**	-	-	ns
spi_di setup time	tSDS	85 + tPCLK	-	-	ns

SPI master mode (fast mode)

Unless otherwise specified: LVDD = 1.65 to 1.95V, HVDD = 2.7 to 3.6V, VSS = 0V, Ta = -40 to 85°C

Item	記号	Min.	Typ.	Max.	Unit
spi_ck cycle time	tSPCK	**85 x 2**	-	-	ns
spi_di setup time	tSDS	85	-	-	ns

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S1C33 Series Technical Manual Errata

ITEM Control and Operation of SDRAM Interface

Object manual	Document code	Object item	Page
S1C33E07 Technical Manual	410573604	II.4 SDRAM Controller (SDRAMC)	II-4-14, 15
S1C33E08 Technical Manual	410865100	II.4 SDRAM Controller (SDRAMC)	II-4-14, 15
S1C33L05 Technical Manual	405262000	VIII-2 SDRAM INTERFACE	VIII-2-15
S1C33L17 Technical Manual	411520600	II.4 SDRAM Controller (SDRAMC)	II-4-14, 15
S1C33L18 Technical Manual	411573200	II.4 SDRAM Controller (SDRAMC)	II-4-14, 15
S1C33L19 Technical Manual	411664200	II.4 SDRAM Controller (SDRAMC)	II-4-14, 15
S1C33L26 Technical Manual	411900101	10 SDRAM Controller (SDRAMC)	10-11, 12
S1C33L27 Technical Manual	411911901	10 SDRAM Controller (SDRAMC)	10-10, 11

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Page II-4-14 S1C33E08 Technical Manual

Page VIII-2-15 S1C33L05 Technical Manual

Page II-4-14 S1C33L17 Technical Manual

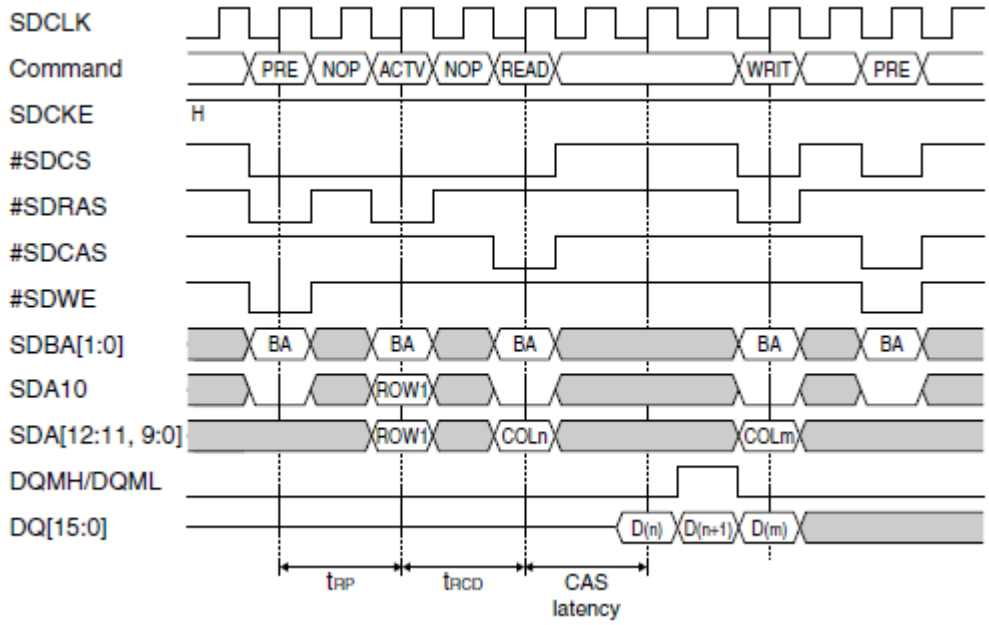
Page II-4-14 S1C33L18 Technical Manual

Page II-4-14 S1C33L19 Technical Manual

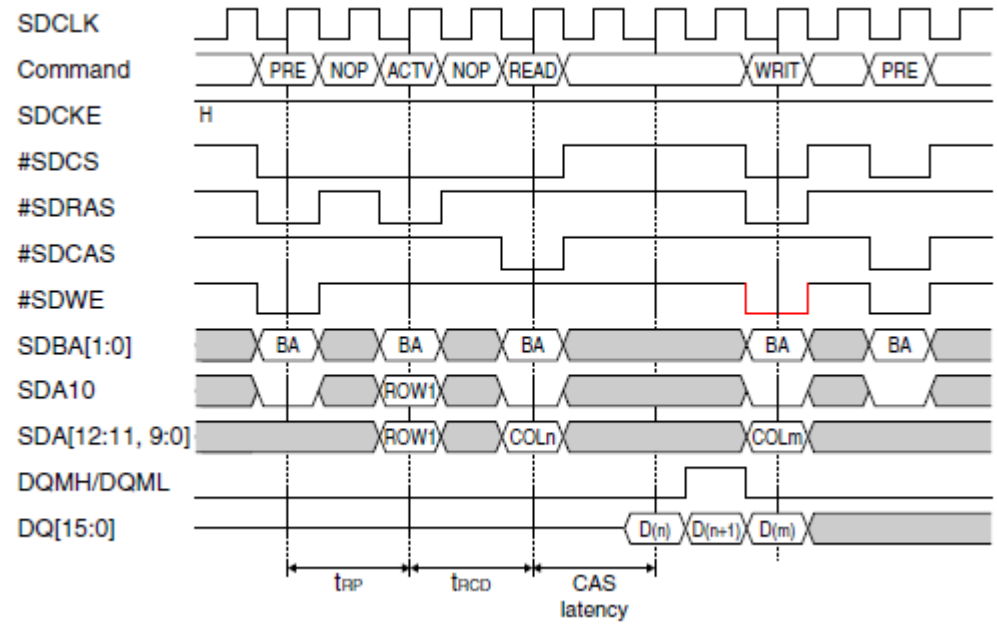
Page 10-11 S1C33L26 Technical Manual

Page 10-10 S1C33L27 Technical Manual

(Error)



(Correct)



Page II-4-15 S1C33E07 Technical Manual

Page II-4-15 S1C33E08 Technical Manual

Page II-4-15 S1C33L17 Technical Manual

Page II-4-15 S1C33L18 Technical Manual

Page II-4-15 S1C33L19 Technical Manual

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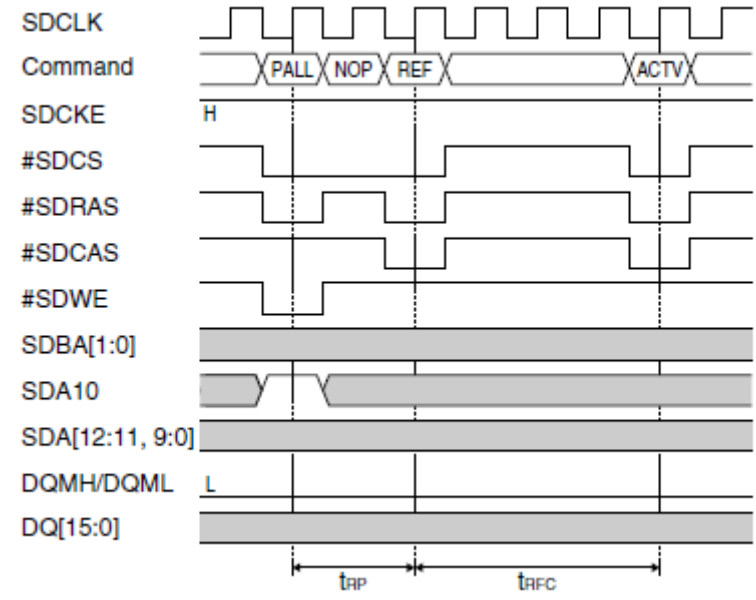
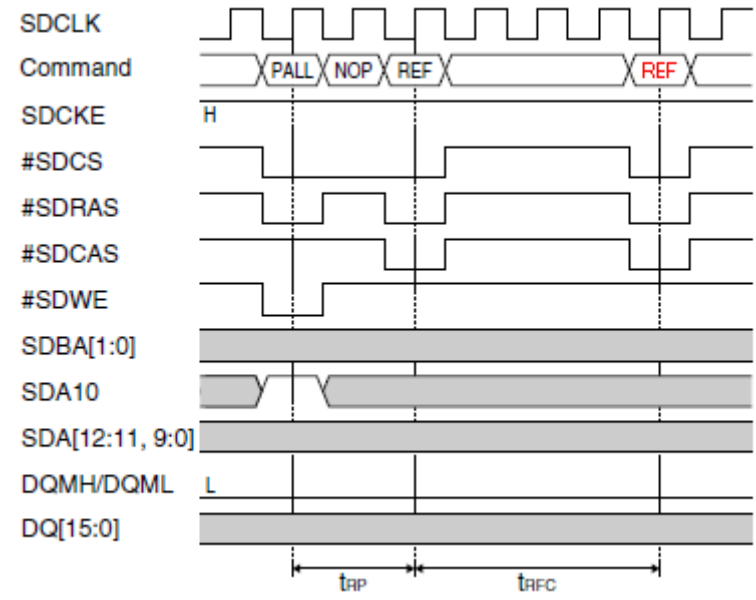
(Error)



(Correct)


SDCLK
Command
PALL
NOP
REF
REF
SDCKE
H
#SDCS
#SDRAS
#SDCAS
#SDWE
SDBA[1:0]
SDA10
SDA[12:11, 9:0]
DQMH/DQML
L
DQ[15:0]
tRP
tRFC

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S1C33 Technical Manual Errata

ITEM: Setting to the Horizontal Display Period Start Position			
Object manual	Document code	Object ITEM	Page
S1C33L26 Technical Manual	411900101	26.5.3 HR-TFT Panel Timing Parameters	26-12
		26.10 Control Register Details	26-39
		Appendix A List of I/O Registers	AP-A-51

26-12

(Error)

HDPS: Horizontal display period start position

Use HDPSCNT[9:0]/LCDC_HDPS register to set the horizontal display period start position for the HR-TFT panel.

HDPS = HDPCNT[9:0] + 1 [Ts]

(Correct)

HDPS: Horizontal display period start position

Use HDPSCNT[9:0]/LCDC_HDPS register to set the horizontal display period start position for the HR-TFT panel.

HDPS = HDPSCNT[9:0] + 1 [Ts]

26-39

(Error)

HDPS = HDPSCNT [Ts]

(Correct)

HDPS = HDPSCNT + 1 [Ts]

AP-A-51

(Error)

HDPS = HDPSCNT [Ts]

(Correct)

HDPS = HDPSCNT + 1 [Ts]

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S1C33 Technical Manual Errata

ITEM: Timing of transmit-buffer empty interrupt			
Object manual	Document code	Object ITEM	Page
S1C33L19 Technical Manual	411900101	20.6.3 Control and Operation of Clock-Synchronized Transfer	20-8

(Error)

(3) Terminating transmit operation

Upon completion of data transmission, write 0 to the transmit-enable bit TXEN to disable transmit operation.

This operation clears (initializes) the transmit data buffer (FIFO), therefore, make sure that the transmit data buffer does not contain any data waiting for transmission before writing 0 to TXEN.

(Correct)

(3) Terminating transmit operation

Upon completion of data transmission, write 0 to the transmit-enable bit TXEN to disable transmit operation.

This operation clears (initializes) the transmit data buffer (FIFO), therefore, make sure that the transmit data buffer does not contain any data waiting for transmission before writing 0 to TXEN.

Note: In clock-synchronized mode, TENDx becomes L when the bit7 of each byte data is transmitted. Therefore, the last of transmission cannot be detected only by judging the TENDx. The last of the transmission can be detected by polling to the pPx_PxD register until SCLKx level becomes High after TENDx was Low.

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S1C33 Technical Manual Errata

ITEM: Timing of transmit-buffer empty interrupt			
Object manual	Document code	Object ITEM	Page
S1C33L26 Technical Manual	411900101	20.9 FSIO Interrupts and DMA	20-21

(Error)

Transmit buffer empty interrupt

To use this interrupt, set TDBE_IE/FSIO_INTEx register to 1. If TDBE_IE is set to 0 (default), interrupt requests for this cause will not be sent to the ITC.

When transmit data written to the transmit data buffer is transferred to the shift register, the FSIO module sets TDBE_IF/FSIO_INTFx register to 1, indicating that the transmit data buffer is empty. If transmit buffer empty interrupts are enabled (TDBE_IE = 1), an interrupt request is sent simultaneously to the ITC.

(Correct)

Transmit buffer empty interrupt

To use this interrupt, set TDBE_IE/FSIO_INTEx register to 1. If TDBE_IE is set to 0 (default), interrupt requests for this cause will not be sent to the ITC.

When transmit data written to the transmit data buffer is transferred to the shift register and the transmit data buffer is empty , the FSIO module sets TDBE_IF/FSIO_INTFx register to 1, indicating that the transmit data buffer is empty. If transmit buffer empty interrupts are enabled (TDBE_IE = 1), an interrupt request is sent simultaneously to the ITC.

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S1C33 Technical Manual Errata

ITEM: Action of **TEND** in Clock-Synchronized Transfer			
Object manual	Document code	Object ITEM	Page
S1C33L26 Technical Manual	411900101	20.6.3 Control and Operation of Clock-Synchronized Transfer	20-7
		20.10 Details of Control Registers	20-24

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(Error)

The transmit shift register status can be checked using the transmit-completion flag (TEND/FSIO_STATUS*x* register). This flag goes 1 after the first bit is shifted out from the shift register and goes 0 after the last bit is shifted out.

When data is transmitted successively in clock-synchronized master mode, TEND maintains 1 until all data is shifted out (Figure 20.6.3.1). In slave mode, TEND goes 0 every time 1-byte data is shifted out (Figure 20.6.3.2).

(Correct)

The transmit shift register status can be checked using the transmit-completion flag (TEND/FSIO_STATUS*x* register). This flag goes 1 ~~after the first bit is shifted out from the shift register~~ while bit7-bit0 of data is being transmitted and goes 0 ~~after the last bit is shifted out~~ bit7 of data is transmitted (see Figure 20.6.3.1 and Figure 20.6.3.2).

~~When data is transmitted successively in clock-synchronized master mode, TEND maintains 1 until all data is shifted out (Figure 20.6.3.1). In slave mode, TEND goes 0 every time 1-byte data is shifted out (Figure 20.6.3.2)~~.

20-24

(Error)

D5 **TEND: Transmit Status Flag Bit**

Indicates the transmission status.

1 (R): Busy (during transmitting)

0 (R): End/idle (default)

TEND goes 1 after the first bit is shifted out from the shift register and goes 0 after the last bit is shifted out. When data is transmitted successively in clock-synchronized master mode or asynchronous mode, TEND maintains 1 until all data is shifted out (see Figure 20.6.3.1 and Figure 20.7.3.1). In clock-synchronized slave mode, TEND goes 0 every time 1-byte data is shifted out (see Figure 20.6.3.2).

(Correct)

D5 **TEND: Transmit Status Flag Bit**

Indicates the transmission status.

1 (R): Busy (during transmitting)

0 (R): End/idle (default)

TEND goes 1 ~~after the first bit is shifted out from the shift register~~ while bit7-bit0 of data is being transmitted and goes 0 ~~after the last bit is shifted out~~ bit7 of data is transmitted. When data is transmitted successively in ~~clock-synchronized master mode or~~ asynchronous mode,

TEND maintains 1 until all data is shifted out (see ~~Figure 20.6.3.1 and~~ Figure 20.7.3.1). In clock-synchronized ~~slave~~ mode, TEND goes 0 every time 1-byte data is shifted out (see Figure 20.6.3.1 and Figure 20.6.3.2).

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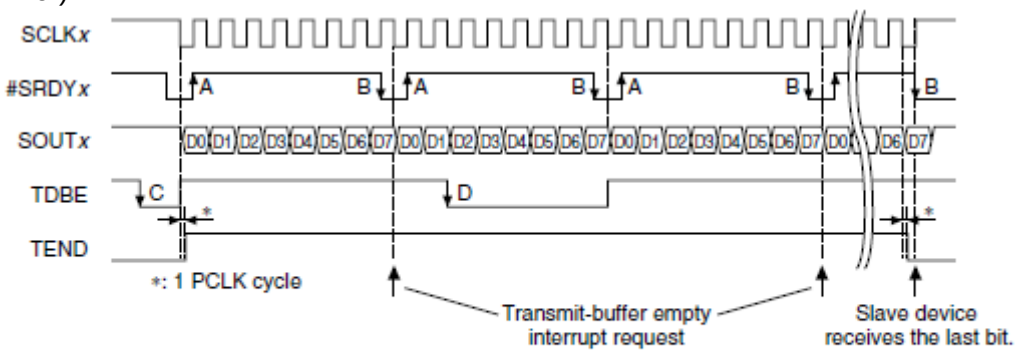
S1C33 Technical Manual Errata

ITEM: The change of the transmit timing chart in Clock-Synchronized Master Mode			
Object manual	Document code	Object ITEM	Page
S1C33L26 Technical Manual	411900101	20.6.3 Control and Operation of Clock-Synchronized Transfer	20-7

(Error)

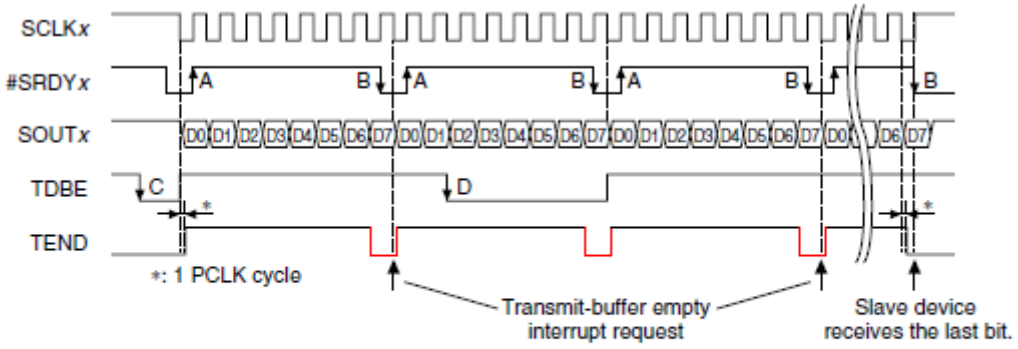


A Slave device receives the LSB. C First data is written. (2 bytes)
B Slave device receives the MSB. D Next data is written. (2 bytes)

Figure 20.6.3.1 Transmit Timing Chart in Clock-Synchronized Master Mode

(Correct)

(The changes are written **in red**.)



A Slave device receives the LSB. C First data is written. (2 bytes)
B Slave device receives the MSB. D Next data is written. (2 bytes)

Figure 20.6.3.1 Transmit Timing Chart in Clock-Synchronized Master Mode