October/06/2023

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S1C17 Manual errata

ITEM: Package			
Object manuals	Document codes	Items	Pages
S1C17624/604/622/602/621 Technical Manual	411914903	1.1 Features Table 1.1.1 Features Shipping form	1-2
		1.3.2 S1C17604 Pin Configuration Diagram	1-7
		1.3.4 S1C17602/621 Pin Configuration Diagram	1-13
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S1C17803 Technical Manual	411820401	1 Overview Table 1.1 Product Lineup	1-1
		1.1 Features Shipping Form	1-6
		1.3.1 Pin Arrangement	1-8
		1.3.2 Pin Functions	1-10-15
		1.3.4 Package	1-18
		4.1 Power Supply Pins	4-1

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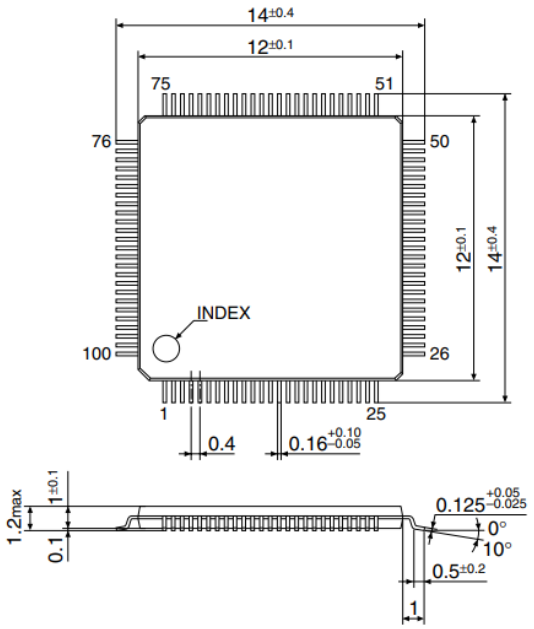
S1C17604/602/621
Page 1-2 1.1 Features Table 1.1.1 Features Shipping form
(Error) TQFP14-100pin (Correct) QFP14-100pin
Page 1-7 1.3.2 S1C17604 Pin Configuration Diagram
(Error) TQFP14-100pin (Correct) QFP14-100pin
Page 1-13 1.3.4 S1C17602/621 Pin Configuration Diagram
(Error) TQFP14-100pin (Correct) QFP14-100pin
Page 31-1 31 Package
(Error)

TQFP14-100pin package

(Unit: mm)



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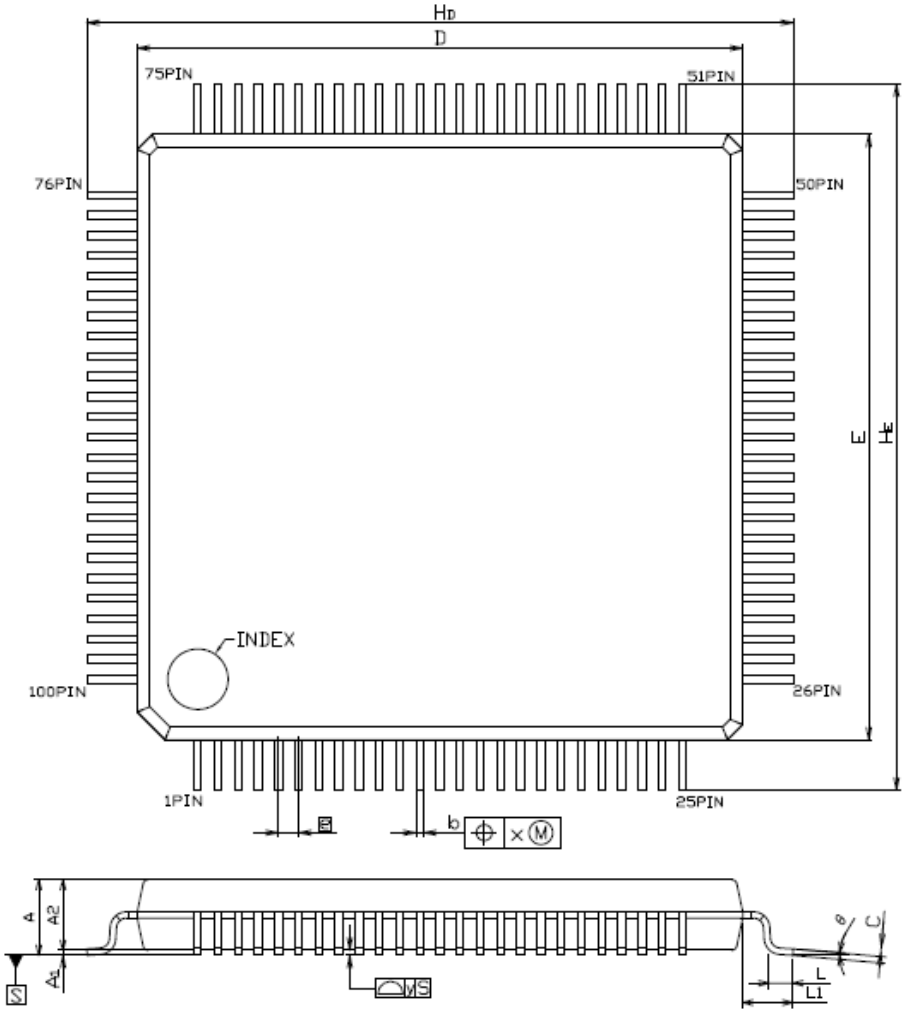
(Correct)

QFP14-100 pin package



Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.90	12.00	12.10
E	11.90	12.00	12.10
A	–	–	1.70
A_1	0.00	0.10	0.20
A_2	1.30	1.40	1.50
B	–	0.40	–
b	0.13	0.18	0.23
c	0.09	0.15	0.20
θ	0°	5°	10°
L	0.30	0.50	0.75
L_1	0.80	1.00	1.20
H_D	13.60	14.00	14.40
H_E	13.60	14.00	14.40
x	–	–	0.08
y	–	–	0.08

1 = 1mm

S1C17803
Page 1-1 1 Overview Table 1.1 Product Lineup
(Error) TQFP14-100 pin (Correct) QFP14-100pin
Page 1-6 1.1 Features Shipping Form
(Error) TQFP14-100 pin (Correct) QFP14-100 pin
Page 1-8 1.3.1 Pin Arrangement
(Error) TQFP14-100 pin (Correct) QFP14-100 pin
Page 1-10-15 1.3.2 Pin Functions
(Error) TQFP14-100 pin (Correct) QFP14-100 pin
Page 1-18 1.3.4 Package
(Error)

TQFP14-100pin Package (Unit: mm)

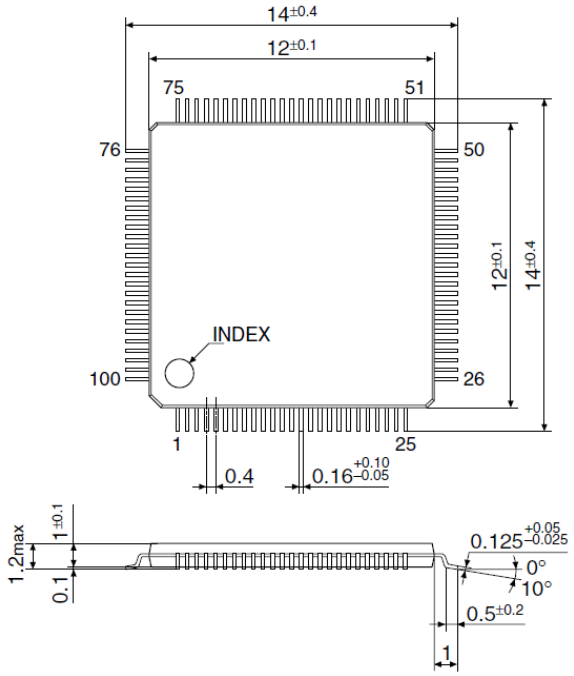
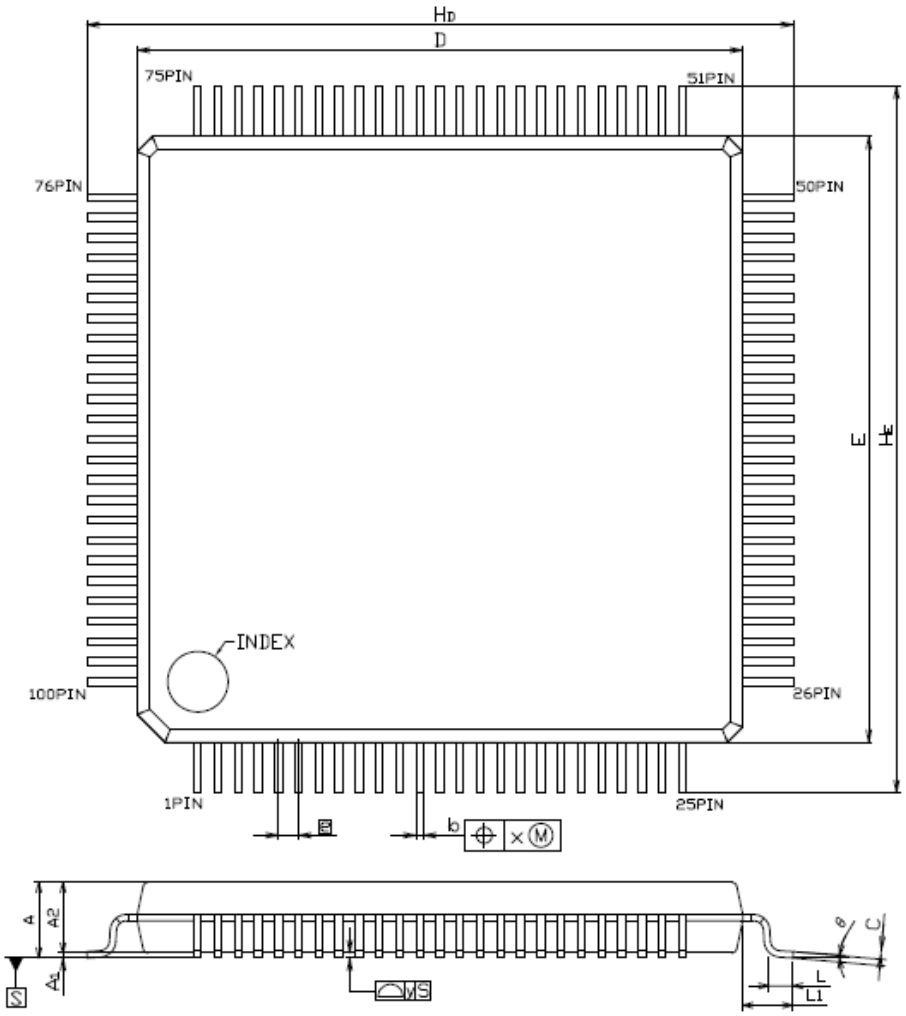


Figure 1.3.4.1 TQFP14-100pin Package Dimensions

(Correct)

QFP14-100 pin package



Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.90	12.00	12.10
E	11.90	12.00	12.10
A	–	–	1.70
A_1	0.00	0.10	0.20
A_2	1.30	1.40	1.50
e	–	0.40	–
b	0.13	0.18	0.23
c	0.09	0.15	0.20
θ	0°	5°	10°
L	0.30	0.50	0.75
L_1	0.80	1.00	1.20
H_D	13.60	14.00	14.40
H_E	13.60	14.00	14.40
x	–	–	0.08
y	–	–	0.08

1 = 1mm

Page 4-1 4.1 Power Supply Pins

(Error) TQFP14-100 pin (Correct) QFP14-100 pin

Jan/29/2014

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S1C17 Technical Manual Errata

ITEM: USI/USIL AC Characteristics			
Object manual	Document code	Object ITEM	Page
S1C17803 Technical Manual	411820401	30.7.3 USI AC Characteristics	30-10

30-10

(Error)

SPI master mode (8 or 9 bits, normal mode)

Unless otherwise specified: LVDD = 2.7 to 3.6V, IO1_VDD/IO2_VDD= 4.5 to 5.5V, VSS = 0V

Item	Symbol	Min.	Typ.	Max.	Unit
spi_sck cycle time	tSPCK	85 + tPCLK	-	-	ns
spi_sdi setup time	tSDS	85 + tPCLK	-	-	ns

Unless otherwise specified: LVDD = 2.7 to 3.6V, IO1_VDD/IO2_VDD= 2.7 to 3.6V, VSS = 0V

Item	Symbol	Min.	Typ.	Max.	Unit
spi_sck cycle time	tSPCK	85 + tPCLK	-	-	ns
spi_sdi setup time	tSDS	85 + tPCLK	-	-	ns

SPI master mode (8 or 9 bits, fast mode)

Unless otherwise specified: LVDD = 2.7 to 3.6V, IO1_VDD/IO2_VDD= 4.5 to 5.5V, VSS = 0V

Item	記号	Min.	Typ.	Max.	Unit
spi_sck cycle time	tSPCK	85	-	-	ns
spi_sdi setup time	tSDS	85	-	-	ns

Unless otherwise specified: LVDD = 2.7 to 3.6V, IO1_VDD/IO2_VDD= 2.7 to 3.6V, VSS = 0V

Item	記号	Min.	Typ.	Max.	Unit
spi_sck cycle time	tSPCK	85	-	-	ns
spi_sdi setup time	tSDS	85	-	-	ns

(Correct)

SPI master mode (8 or 9 bits, normal mode)

Unless otherwise specified: LVDD = 2.7 to 3.6V, IO1_VDD/IO2_VDD= 4.5 to 5.5V, VSS = 0V

Item	Symbol	Min.	Typ.	Max.	Unit
spi_sck cycle time	tSPCK	**(85 + tPCLK) x 2**	-	-	ns
spi_sdi setup time	tSDS	85 + tPCLK	-	-	ns

Unless otherwise specified: LVDD = 2.7 to 3.6V, IO1_VDD/IO2_VDD= 2.7 to 3.6V, VSS = 0V

Item	Symbol	Min.	Typ.	Max.	Unit
spi_sck cycle time	tSPCK	**(85 + tPCLK) x 2**	-	-	ns
spi_sdi setup time	tSDS	85 + tPCLK	-	-	ns

SPI master mode (8 or 9 bits, fast mode)

Unless otherwise specified: LVDD = 2.7 to 3.6V, IO1_VDD/IO2_VDD= 4.5 to 5.5V, VSS = 0V

Item	記号	Min.	Typ.	Max.	Unit
spi_sck cycle time	tSPCK	**85 x 2**	-	-	ns
spi_sdi setup time	tSDS	85	-	-	ns

Unless otherwise specified: LVDD = 2.7 to 3.6V, IO1_VDD/IO2_VDD= 2.7 to 3.6V, VSS = 0V

Item	記号	Min.	Typ.	Max.	Unit
spi_sck cycle time	tSPCK	**85 x 2**	-	-	ns
spi_sdi setup time	tSDS	85	-	-	ns

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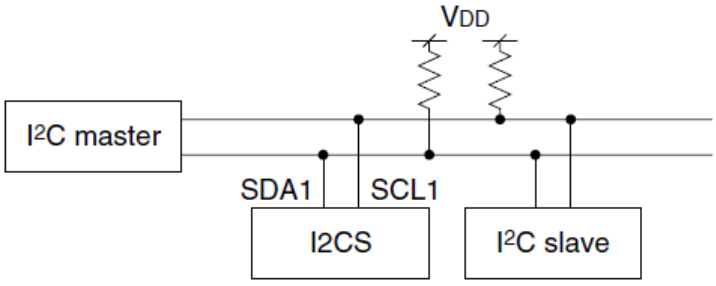
S1C17 Family Technical Manual Errata

ITEM **I2C Slave Input/Output Pins**

Object manual	Document code	Object item	Page
S1C17601 Technical Manual	411805701	21.2 I2C Slave Input/Output Pins	21-2
S1C17611 Technical Manual	411882301	21.2 I2C Slave Input/Output Pins	21-2
S1C17706 Technical Manual	412026401	18.2 I2CS Input/Output Pins	18-1
S1C17002 Technical Manual	411554402	V.3.2 I2C Slave I/O Pins	V-3-2
S1C17003 Technical Manual	411635102	21.2 I2C Slave Input/Output Pins	21-2
S1C17803 Technical Manual	411820401	21.2 I2CS Input/Output Pins	21-2

(Addition)

Note: The pins go to high impedance status when the port function is switched. The SCL and SDA pins do not output a high level, so these lines should be pulled up to VDDwith an external pull-up resistor. Be sure to avoid pulling these pins up to a voltage that exceeds the VDD level.



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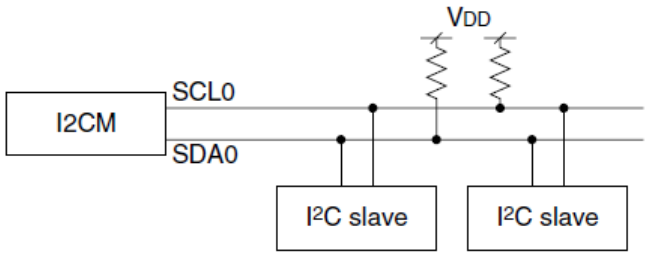
S1C17 Family Technical Manual Errata

ITEM **I2C Master Input/Output Pins**

Object manual	Document code	Object item	Page
S1C17601 Technical Manual	411805701	20.2 I2C Master Input/Output Pins	20-2
S1C17611 Technical Manual	411882301	20.2 I2C Master Input/Output Pins	20-2
S1C17701 Technical Manual	411089904	20.2 I2C I/O Pins	20-2
S1C17704 Technical Manual	411511903	20.2 I2C I/O Pins	20-2
S1C17706 Technical Manual	412026401	17.2 I2CM Input/Output Pins	17-1
S1C17001 Technical Manual	411412301	20.2 I2C Input/Output Pins	252
S1C17002 Technical Manual	411554402	V.2.2 I2C Master I/O Pins	V-2-2
S1C17003 Technical Manual	411635102	20.2 I2C Master Input/Output Pins	20-2
S1C17501 Technical Manual	411525602	VI.2.2 I2C I/O Pins	VI-2-2
S1C17801 Technical Manual	411390802	VI.2.2 I2C I/O Pins	VI-2-2
S1C17803 Technical Manual	411820401	20.2 I2CM Input/Output Pins	20-2

(Addition)

Note: The pins go to high impedance status when the port function is switched.
The SCL and SDA pins do not output a high level, so these lines should be pulled up to VDD with an external pull-up resistor. Be sure to avoid pulling these pins up to a voltage that exceeds the VDD level.



Dec/27/2011

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S1C17 Family Technical Manual Errata

ITEM About Power-on sequence			
Object manual	Document code	Object item	Page
S1C17803 Technical Manual	411820401	4.7 Precautions on Power Supply	4-4

Page 4-4 S1C17803 Technical Manual

(Error)

4.7 Precautions on Power Supply

Power-on sequence

In order to operate the device normally, supply power in accordance with the following timing.

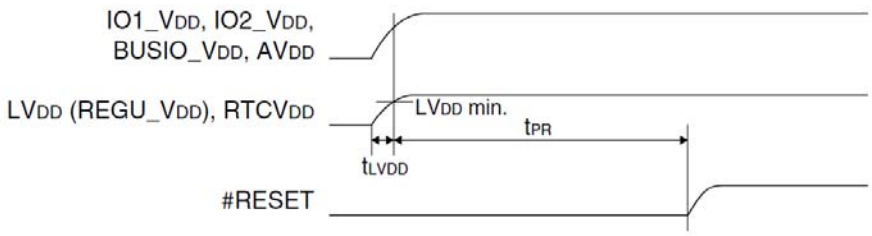

Figure 4.7.1 Power-On Sequence

(1) t_{LVDD}: Elapsed time until the power supply stabilizes after power-on

Supply power in the following sequence.

Power-on: 1. LV_{DD} (and $RTCV_{DD}$) or $REGU\_V_{DD}$

2. $BUSIO\_V_{DD}$, $IO1\_V_{DD}$, $IO2\_V_{DD}$, AV_{DD} (May be applied with 1 above at the same time.)

3. Apply the input signal

* The $RTCV_{DD}$ can be always supplied to the chip to operate the RTC and BBRAM.

(2) t_{PR}: Power-on-reset time

Keep the #RESET signal low for this period. See “Electrical Characteristics” for the power-on-reset time.

(Correct)

4.7 Precautions on Power Supply

Power-on sequence

In order to operate the device normally, supply power in accordance with the following timing.

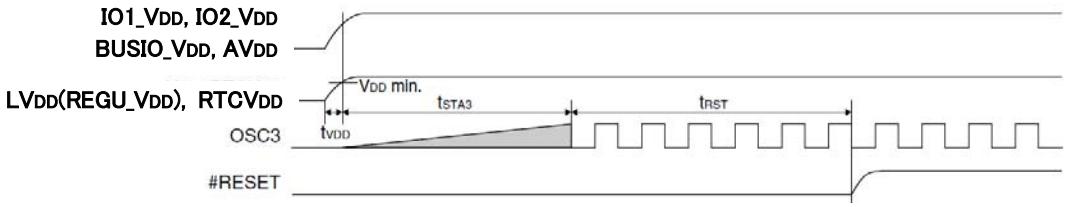

Figure 4.7.1 Power-On Sequence

(1) t_{LVDD}: Elapsed time until the power supply stabilizes after power-on
Supply power in the following sequence.
Power-on: 1. LV_{DD} (and $RTCV_{DD}$) or $REGU\_V_{DD}$
2. $BUSIO\_V_{DD}$, $IO1\_V_{DD}$, $IO2\_V_{DD}$, AV_{DD} (May be applied with 1 above at the same time.)
3. Apply the input signal
* The $RTCV_{DD}$ can be always supplied to the chip to operate the RTC and BBRAM.

(2) t_{STA3}: Time at which OSC3 oscillation starts

(3) t_{RST}: Minimum reset pulse width
Time at which the clock supplied to the chip stabilizes plus at least six clocks; Keep the #RESET signal low.