

## S1C17 Manual errata

ITEM: Package			
Object manuals	Document codes	Items	Pages
S1C17624/604/622/602/621 Technical Manual	411914903	1.1 Features Table 1.1.1 Features Shipping form	1-2
		1.3.2 S1C17604 Pin Configuration Diagram	1-7
		1.3.4 S1C17602/621 Pin Configuration Diagram	1-13
		31 Package	31-1
S1C17803 Technical Manual	411820401	1 Overview Table 1.1 Product Lineup	1-1
		1.1 Features Shipping Form	1-6
		1.3.1 Pin Arrangement	1-8
		1.3.2 Pin Functions	1-10-15
		1.3.4 Package	1-18
		4.1 Power Supply Pins	4-1

S1C17604/602/621

Page 1-2 1.1 Features Table 1.1.1 Features Shipping form

(Error) TQFP14-100pin (Correct) QFP14-100pin

Page 1-7 1.3.2 S1C17604 Pin Configuration Diagram

(Error) TQFP14-100pin (Correct) QFP14-100pin

Page 1-13 1.3.4 S1C17602/621 Pin Configuration Diagram

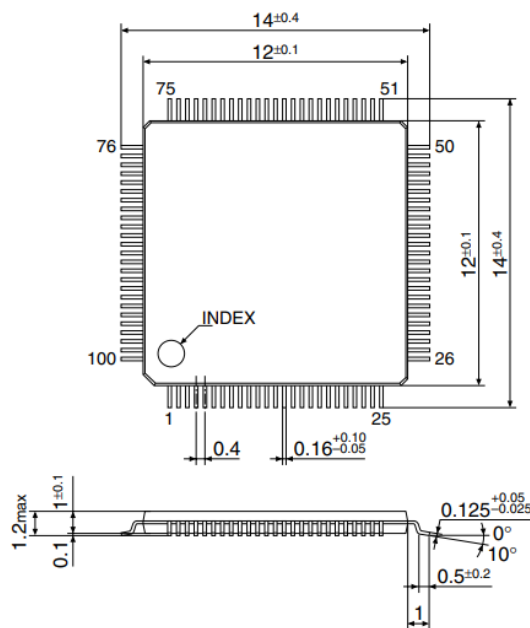
(Error) TQFP14-100pin (Correct) QFP14-100pin

Page 31-1 31 Package

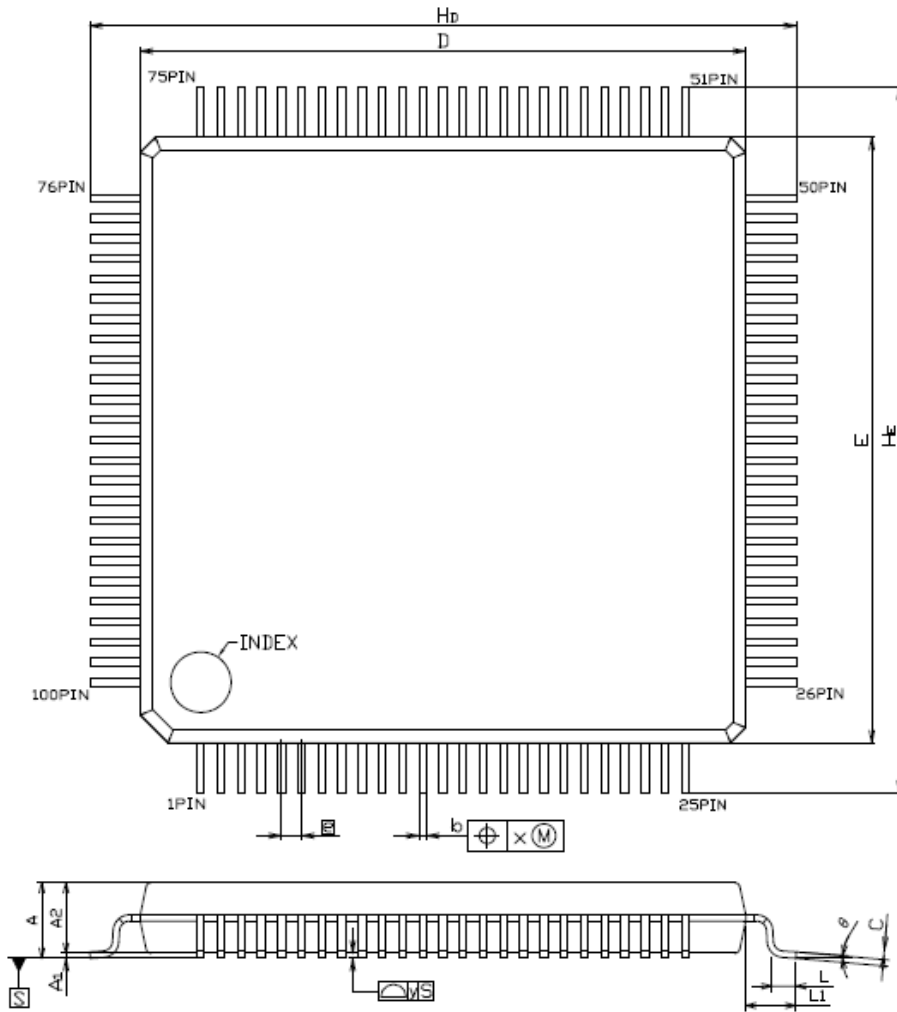
(Error)

**TQFP14-100pin package**

(Unit: mm)



(Correct)  
QFP14-100 pin package



Symbol	Dimension In Millimeters		
	Min	Nom	Max
$D$	11.90	12.00	12.10
$E$	11.90	12.00	12.10
$A$	-	-	1.70
$A_2$	0.00	0.10	0.20
$A_e$	1.30	1.40	1.50
$\text{M}$	-	0.40	-
$b$	0.13	0.18	0.23
$c$	0.09	0.15	0.20
$\theta$	0°	5°	10°
$L$	0.30	0.50	0.75
$L_1$	0.80	1.00	1.20
$H_b$	13.60	14.00	14.40
$H_e$	13.60	14.00	14.40
$x$	-	-	0.08
$y$	-	-	0.08

1 = 1mm

S1C17803

Page 1-1 1 Overview Table 1.1 Product Lineup

(Error) TQFP14-100 pin (Correct) QFP14-100pin

Page 1-6 1.1 Features Shipping Form

(Error) TQFP14-100 pin (Correct) QFP14-100 pin

Page 1-8 1.3.1 Pin Arrangement

(Error) TQFP14-100 pin (Correct) QFP14-100 pin

Page 1-10-15 1.3.2 Pin Functions

(Error) TQFP14-100 pin (Correct) QFP14-100 pin

Page 1-18 1.3.4 Package

(Error)

**TQFP14-100pin Package**

(Unit: mm)

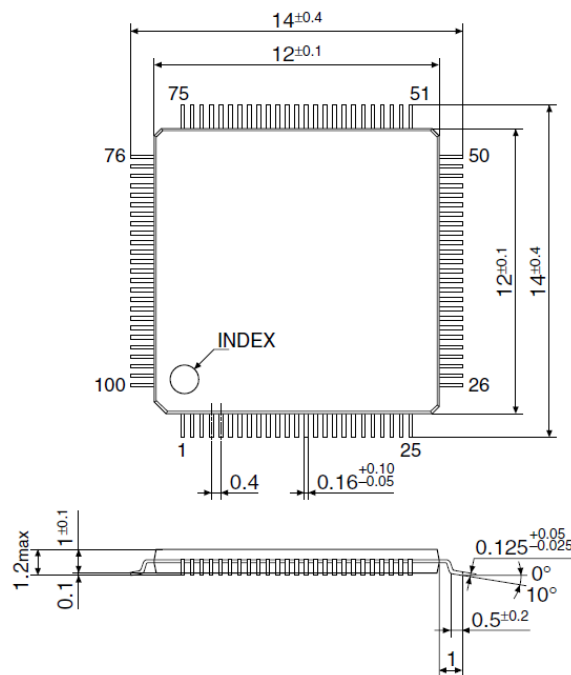
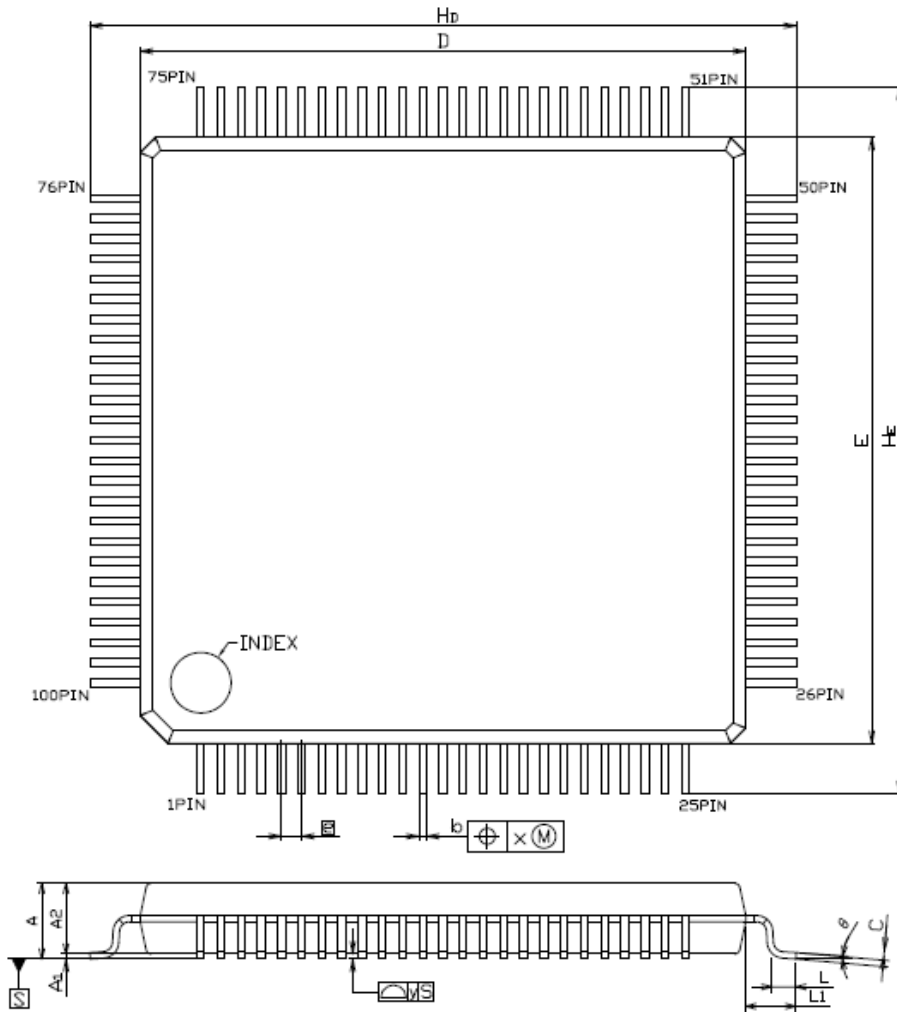


Figure 1.3.4.1 TQFP14-100pin Package Dimensions

(Correct)

QFP14-100 pin package



Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.90	12.00	12.10
E	11.90	12.00	12.10
A	-	-	1.70
A <sub>L</sub>	0.00	0.10	0.20
A <sub>P</sub>	1.30	1.40	1.50
⊠	-	0.40	-
b	0.13	0.18	0.23
c	0.09	0.15	0.20
θ	0°	5°	10°
L	0.30	0.50	0.75
L <sub>1</sub>	0.80	1.00	1.20
H <sub>D</sub>	13.60	14.00	14.40
H <sub>E</sub>	13.60	14.00	14.40
x	-	-	0.08
y	-	-	0.08

1 = 1mm

## S1C17 Family Technical Manual Errata

<b>ITEM    A part of shipping form is discontinued</b>				
Object manual	Document code	Object item	Page	
S1C17624/604/602/621 Technical Manual	411914903	Shipping form	1-2	
<b>1.1 Features</b>				
(Error)				
<b>Shipping form</b>				
1	TQFP15-128pin	TQFP14-100pin	TQFP15-128pin	TQFP14-100pin
2	Die form	Die form	Die form	Die form
3				VFBGA7H-144
Size/pitch	TQFP15-128pin (body size: 14 mm × 14 mm, lead pitch: 0.4 mm) TQFP14-100pin (body size: 12 mm × 12 mm, lead pitch: 0.4 mm) VFBGA7H-144 (body size: 7 mm × 7 mm, ball pitch: 0.5 mm) Die form (pad pitch: 100 μm)			
(Correct)				
<b>Shipping form</b>				
1	TQFP15-128pin	TQFP14-100pin	TQFP15-128pin	TQFP14-100pin
2	Die form	Die form	Die form	Die form
3				VFBGA7H-144 # 1
Size/pitch	TQFP15-128pin (body size: 14 mm × 14 mm, lead pitch: 0.4 mm) TQFP14-100pin (body size: 12 mm × 12 mm, lead pitch: 0.4 mm) VFBGA7H-144 (body size: 7 mm × 7 mm, ball pitch: 0.5 mm) # 1 Die form (pad pitch: 100 μm)			
<b># 1 : VFBGA7H-144 for S1C17602 &amp; S1C17621 is discontinued.</b>				

## S1C17 Family Technical Manual Errata

ITEM Features of OSC1 oscillator circuit			
Object manual	Document code	Object item	Page
S1C17624/604/622/602/621 Technical Manual	411914902	1.1 Features	1-1
(Error)			
<b>Clock generator</b>			
OSC1 oscillator circuit	32.768 kHz (typ.) crystal oscillator circuit Supports an external clock input.		
(Correct)			
<b>Clock generator</b>			
OSC1 oscillator circuit	32.768 kHz (typ.) crystal oscillator circuit <del>Supports an external clock input.</del>		

## S1C17 Family Technical Manual Errata

ITEM About the Fine mode setting of T16E.			
Object manual	Document code	Object item	Page
S1C17001 Technical Manual	411412303	13.6 Clock Output Control	150
S1C17003 Technical Manual	411635102	13.6 Clock Output Control	13-8
S1C17624/604/622/621 Technical Manual	411914902	12.7 Clock Output Control	12-6
S1C17701 Technical Manual	411089905	13.6 Controlling Clock Output	13-8
S1C17702 Technical Manual	411581702	13.6 Clock Output Control	13-8
S1C17704 Technical Manual	411511903	13.6 Controlling Clock Output	13-8
<p><b>Page 150</b> S1C17001 Technical Manual  <b>Page 13-8</b> S1C17003 Technical Manual  <b>Page 13-8</b> S1C17701 Technical Manual  <b>Page 13-8</b> S1C17702 Technical Manual  <b>Page 13-8</b> S1C17704 Technical Manual</p>			
<p>Add following comment at Precautions of "Setting fine mode for clock output".</p> <p><b>(3) Use the Fine mode only for T16EDF = 0x0 (PCLK-1/1).</b></p>			
<p><b>Page 12-6</b> S1C17623/604/622/621 Technical Manual</p>			
<p>Add following comment at Precautions of "Setting fine mode for clock output".</p> <p><b>(4) Use the Fine mode only for T16EDF = 0x0 (PCLK-1/1).</b></p>			



## S1C17 Family Technical Manual Errata

ITEM About Internal RAM size select.			
Object manual	Document code	Object item	Page
S1C17624/604/622/621 Technical Manual	411914902	3.3.1 Embedded RAM	3-6
<b>Page 3-6</b> S1C17623/604/622/621 Technical Manual			
(Error)			
<p>The S1C17624/604 enables the RAM size used to apply restrictions to 8KB, 4KB, or 2KB. The S1C17602 enables the RAM size used to apply restrictions to 4KB or 2KB. For example, when using the S1C17624/604/602 to develop an application for a built-in ROM model, you can set the RAM size to match that of the target model, preventing creating programs that seek to access areas outside the RAM areas of the target product. The RAM size is selected using IRAMSZ[2:0]/MISC_IRAMSZ register.</p>			
(Correct)			
<p>The S1C17624/604 enables the RAM size used to apply restrictions to 8KB, 4KB, or 2KB. The <b>S1C17622</b> enables the RAM size used to apply restrictions to 4KB or 2KB. For example, when using the S1C17624/604/<b>622</b> to develop an application for a built-in ROM model, you can set the RAM size to match that of the target model, preventing creating programs that seek to access areas outside the RAM areas of the target product. The RAM size is selected using IRAMSZ[2:0]/MISC_IRAMSZ register.</p>			

## S1C17 Family Technical Manual Errata

ITEM About Flash Protect Bits			
Object manual	Document code	Object item	Page
S1C17624/604/622/621 Technical Manual	411914902	3. Memory Map 3.2.3 Protect Bits	3-2, 3-5

**Page 3-2** S1C17623/604/622/621 Technical Manual

(Error-1)

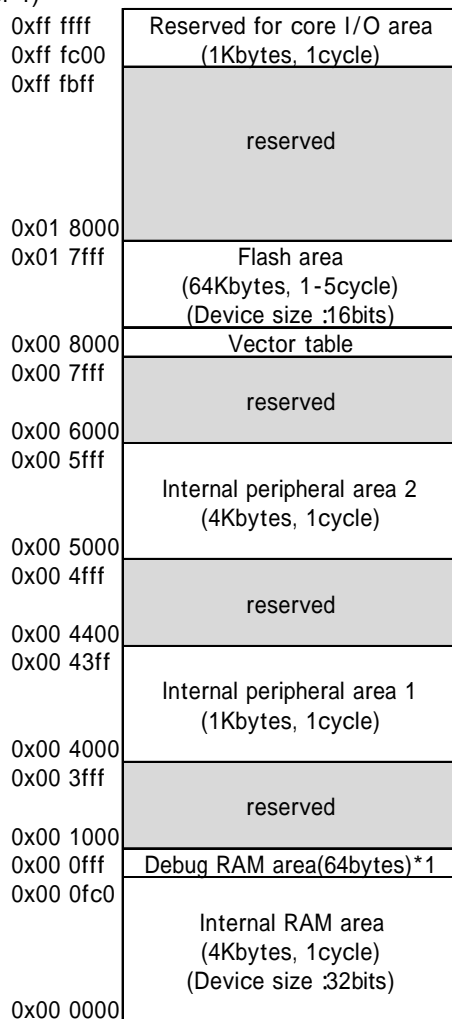


Figure3.2 S1C17622/602 Memory Map

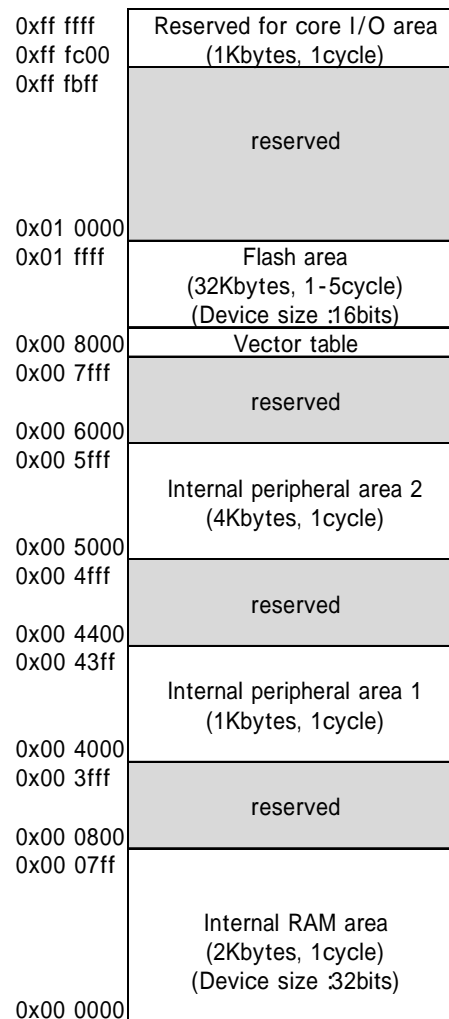


Figure3.3 S1C17621 Memory Map

(Correct-1)

0xff ffff	Reserved for core I/O area (1Kbytes, 1cycle)
0xff fc00	
0xff fbff	reserved
0x02 8000	
0x02 7fff	Flash Protect area *2
0x02 7ffc	
0x02 7ffb	reserved
0x01 8000	
0x01 7fff	Flash area (64Kbytes, 1-5cycle) (Device size :16bits)
0x00 8000	Vector table
0x00 7fff	reserved
0x00 6000	
0x00 5fff	Internal peripheral area 2 (4Kbytes, 1cycle)
0x00 5000	
0x00 4fff	reserved
0x00 4400	
0x00 43ff	Internal peripheral area 1 (1Kbytes, 1cycle)
0x00 4000	
0x00 3fff	reserved
0x00 1000	
0x00 0fff	Debug RAM area(64bytes)*1
0x00 0fc0	
	Internal RAM area (4Kbytes, 1cycle) (Device size :32bits)
0x00 0000	

Figure3.2 S1C17622/602 Memory Map

0xff ffff	Reserved for core I/O area (1Kbytes, 1cycle)
0xff fc00	
0xff fbff	reserved
0x01 8000	
0x01 7fff	
0x01 7ffc	Flash Protect area
0x01 7ffb	reserved
0x01 0000	
0x01 ffff	Flash area (32Kbytes, 1-5cycle) (Device size :16bits)
0x00 8000	Vector table
0x00 7fff	reserved
0x00 6000	
0x00 5fff	Internal peripheral area 2 (4Kbytes, 1cycle)
0x00 5000	
0x00 4fff	reserved
0x00 4400	
0x00 43ff	Internal peripheral area 1 (1Kbytes, 1cycle)
0x00 4000	
0x00 3fff	reserved
0x00 0800	
0x00 07ff	
	Internal RAM area (2Kbytes, 1cycle) (Device size :32bits)
0x00 0000	

Figure3.3 S1C17621 Memory Map

\*2 The address range from 0x27ffc to 0x27fff of the S1C17602 is a reserved area.

**Page 3-5 S1C17623/604/622/621 Technical Manual**

(Error-2)

**Flash Protect Bits (S1C17622/602)**

Address	Bit	Function	Setting			Init.	R/W	Remarks
0x17fc (16 bits)	D15-4	Reserved	-			-	-	
	D3	Flash write-protect bit for 0x14000-0x17fff	1	Writeable	0	Protected	1	R/W
	D2	Flash write-protect bit for 0x10000-0x13fff	1	Writeable	0	Protected	1	R/W
	D1	Flash write-protect bit for 0xc000-0xffff	1	Writeable	0	Protected	1	R/W
	D0	Flash write-protect bit for 0x8000-0xbfff	1	Writeable	0	Protected	1	R/W

Address	Bit	Function	Setting			Init.	R/W	Remarks
0x17fe (16 bits)	D15-4	Reserved	-					
	D3	Flash data-read-protect bit for 0x14000-0x17fff	1	Readable	0	Protected	1	R/W
	D2	Flash data-read-protect bit for 0x10000-0x13fff	1	Readable	0	Protected	1	R/W
	D1	Flash data-read-protect bit for 0xc000-0xffff	1	Readable	0	Protected	1	R/W
	D0	reserved	1			1	R/W	Always set to 1.

**Flash Protect Bits (S1C17621)**

Address	Bit	Function	Setting			Init.	R/W	Remarks
0xffc (16 bits)	D15-2	Reserved	-			-	-	
	D1	Flash write-protect bit for 0xc000-0xffff	1	Writeable	0	Protected	1	R/W
	D0	Flash write-protect bit for 0x8000-0xbfff	1	Writeable	0	Protected	1	R/W

Address	Bit	Function	Setting			Init.	R/W	Remarks
0xffe (16 bits)	D15-2	Reserved	-			-	-	
	D1	Flash data-read-protect bit for 0xc000-0xffff	1	Writeable	0	Protected	1	R/W
	D0	reserved	1			1	R/W	Always set to 1.

Notes: Be sure not to locate the area with data-read protection into the .data and .rodata sections.  
 Be sure to set D0 of address 0x27fe (S1C17624/604), 0x17fe (S1C17622/602), or 0xffe (S1C17621) to 1. If it is set to 0, the program cannot be booted.

(Correct-2)

**Flash Protect Bits (S1C17622)**

Address	Bit	Function	Setting		Init.	R/W	Remarks	
0x27ffc (16 bits)	D15-4	Reserved	-		-	-		
	D3	Flash write-protect bit for 0x14000-0x17fff	1	Writeable	0	Protected	1	R/W
	D2	Flash write-protect bit for 0x10000-0x13fff	1	Writeable	0	Protected	1	R/W
	D1	Flash write-protect bit for 0xc000-0xffff	1	Writeable	0	Protected	1	R/W
	D0	Flash write-protect bit for 0x8000-0xbfff	1	Writeable	0	Protected	1	R/W

Address	Bit	Function	Setting		Init.	R/W	Remarks	
0x27ffe (16 bits)	D15-4	Reserved	-					
	D3	Flash data-read-protect bit for 0x14000-0x17fff	1	Readable	0	Protected	1	R/W
	D2	Flash data-read-protect bit for 0x10000-0x13fff	1	Readable	0	Protected	1	R/W
	D1	Flash data-read-protect bit for 0xc000-0xffff	1	Readable	0	Protected	1	R/W
	D0	reserved	1		1	R/W	Always set to 1.	

**Flash Protect Bits (S1C17602)**

Address	Bit	Function	Setting		Init.	R/W	Remarks	
0x17ffc (16 bits)	D15-4	Reserved	-		-	-		
	D3	Flash write-protect bit for 0x14000-0x17fff	1	Writeable	0	Protected	1	R/W
	D2	Flash write-protect bit for 0x10000-0x13fff	1	Writeable	0	Protected	1	R/W
	D1	Flash write-protect bit for 0xc000-0xffff	1	Writeable	0	Protected	1	R/W
	D0	Flash write-protect bit for 0x8000-0xbfff	1	Writeable	0	Protected	1	R/W

Address	Bit	Function	Setting		Init.	R/W	Remarks	
0x17ffe (16 bits)	D15-4	Reserved	-					
	D3	Flash data-read-protect bit for 0x14000-0x17fff	1	Readable	0	Protected	1	R/W
	D2	Flash data-read-protect bit for 0x10000-0x13fff	1	Readable	0	Protected	1	R/W
	D1	Flash data-read-protect bit for 0xc000-0xffff	1	Readable	0	Protected	1	R/W
	D0	reserved	1		1	R/W	Always set to 1.	

**Flash Protect Bits (S1C17621)**

Address	Bit	Function	Setting		Init.	R/W	Remarks	
0x17ffc (16 bits)	D15-2	Reserved	-		-	-		
	D1	Flash write-protect bit for 0xc000-0xffff	1	Writeable	0	Protected	1	R/W
	D0	Flash write-protect bit for 0x8000-0xbfff	1	Writeable	0	Protected	1	R/W

Address	Bit	Function	Setting		Init.	R/W	Remarks	
0x17ffe (16 bits)	D15-2	Reserved	-		-	-		
	D1	Flash data-read-protect bit for 0xc000-0xffff	1	Writeable	0	Protected	1	R/W
	D0	reserved	1		1	R/W	Always set to 1.	

Notes: Be sure not to locate the area with data-read protection into the .data and .rodata sections.  
 Be sure to set D0 of address 0x27ffe (S1C17624/604/622) or 0x17ffe (S1C17602/621) to 1.  
 If it is set to 0, the program cannot be booted.

## S1C17 Series Technical Manual Errata

ITEM About the CBUFEN register of T16A/T16A2			
Object manual	Document code	Object Item	Page
S1C17624/604/622/602/621 Technical Manual	411914902	13.8 Control Register Details	13-14 13-15
S1C17705/703 Technical Manual	411706602	10.8 Control Register Details	10-19
S1C17706 Technical Manual	412026401	10.8 Control Register Details	10-17
S1C17711 Technical Manual	411905602	10.8 Control Register Details	10-14
S1C17554/564 Technical Manual	411914402	11.8 Control Register Details	11-14
S1C17651 Technical Manual	412120600	12.8 Control Register Details	12-13
<p><b>Page 13-14 13-15</b> S1C624/604/622/602/621 Technical Manual</p> <p><b>Page 10-17</b> S1C17706 Technical Manual</p> <p><b>Page 12-13</b> S1C17651 Technical Manual</p>			
<p>(Error)</p> <p><b>D3 CBUFEN: Compare Buffer Enable Bit</b></p> <p>Enables or disables writing to the compare buffer.</p> <p>1 (R/W): Enabled</p> <p>0 (R/W): Disabled (default)</p> <p>Setting CBUFEN to 1 enables the compare buffer. The compare A and B signals will be generated by comparing the counter values with the compare A and B buffer values instead of the compare A and B register values. The compare A and B register values written via software are loaded to the compare A and B buffers when the compare B signal is generated.</p> <p>Setting CBUFEN to 0 disables the compare buffer. The compare A and B signals will be generated by comparing the counter values with the compare A and B register values.</p> <p><b>Note:</b> Make sure the counter is halted (PRUN = 0) before setting CBUFEN.</p>			
<p>(Correct)</p> <p><b>D3 CBUFEN: Compare Buffer Enable Bit</b></p> <p>Enables or disables writing to the compare buffer.</p> <p>1 (R/W): Enabled</p> <p>0 (R/W): Disabled (default)</p> <p>Setting CBUFEN to 1 enables the compare buffer. The compare A and B signals will be generated by comparing the counter values with the compare A and B buffer values instead of the compare A and B register values. The compare A and B register values written via software are loaded to the compare</p>			

A and B buffers when the compare B signal is generated.

Setting CBUFEN to 0 disables the compare buffer. The compare A and B signals will be generated by comparing the counter values with the compare A and B register values.

**Note:** Make sure the counter is halted (**CLKEN** = 0) before setting CBUFEN.

**Page 13-14 13-15** S1C17705/703 Technical Manual

**Page 10-14** S1C17711 Technical Manual

**Page 11-14** S1C17554/564 Technical Manual

(Error)

**D3 CBUFEN: Compare Buffer Enable Bit**

Enables or disables writing to the compare buffer.

1 (R/W): Enabled

0 (R/W): Disabled (default)

When CBUFEN is set to 1, compare data is written via the compare data buffer. The buffer contents are loaded into the compare A and compare B registers when the compare B signal is generated.

When CBUFEN is set to 0, compare data is written directly to the compare A and compare B registers.

**Note:** Make sure the counter is halted (**PRUN** = 0) before setting CBUFEN.

(Correct)

**D3 CBUFEN: Compare Buffer Enable Bit**

Enables or disables writing to the compare buffer.

1 (R/W): Enabled

0 (R/W): Disabled (default)

When CBUFEN is set to 1, compare data is written via the compare data buffer. The buffer contents are loaded into the compare A and compare B registers when the compare B signal is generated.

When CBUFEN is set to 0, compare data is written directly to the compare A and compare B registers.

**Note:** Make sure the counter is halted (**CLKEN** = 0) before setting CBUFEN.