Aug/28/2013

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S1C17 Family Technical Manual Errata

ITEM **I2C Master Input/Output Pins**

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S1C17701 Technical Manual	411089904	20.2 I2C I/O Pins	20-2
S1C17704 Technical Manual	411511903	20.2 I2C I/O Pins	20-2
S1C17706 Technical Manual	412026401	17.2 I2CM Input/Output Pins	17-1
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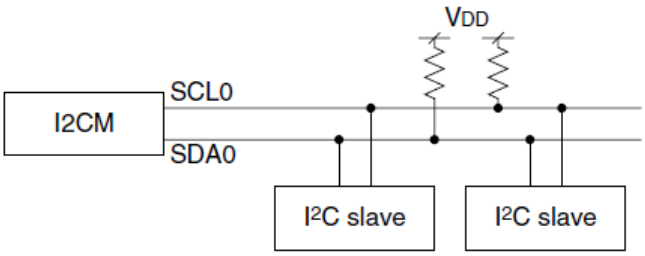
S1C17002 Technical Manual	411554402	V.2.2 I2C Master I/O Pins	V-2-2
S1C17003 Technical Manual	411635102	20.2 I2C Master Input/Output Pins	20-2
S1C17501 Technical Manual	411525602	VI.2.2 I2C I/O Pins	VI-2-2
S1C17801 Technical Manual	411390802	VI.2.2 I2C I/O Pins	VI-2-2
S1C17803 Technical Manual	411820401	20.2 I2CM Input/Output Pins	20-2

(Addition)

Note: The pins go to high impedance status when the port function is switched.
The SCL and SDA pins do not output a high level, so these lines should be pulled up to VDD with an external pull-up resistor. Be sure to avoid pulling these pins up to a voltage that exceeds the VDD level.



Dec/27/2011

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ITEM About Port Input Interrupt			
Object manual	Document code	Object item	Page
S1C17501 Technical Manual	411525602	IV.1 Interrupt Controller (ITC) VII.1.5 port Input Interrupt	IV-1-1 VII-1-3
S1C17801 Technical Manual	411390803	IV.1 Interrupt Controller (ITC) VII.1.5 port Input Interrupt	IV-1-1 VII-1-3

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(Error)

VII.1.5 Port Input Interrupt

The GPIO module has eight interrupt systems (port input interrupts 0 to 7) and a port can be selected for generating each cause of interrupt.

The interrupt condition can also be selected from between input signal edge (rising edge or falling edge) and input signal level (high level or low level) in the interrupt controller (ITC).

Figure VII.1.5.1 shows the configuration of the port input interrupt circuit.

(Correct)

VII.1.5 Port Input Interrupt

The GPIO module has eight interrupt systems (port input interrupts 0 to 7) and a port can be selected for generating each cause of interrupt.

The interrupt can be occurred from input signal level (high level or low level), and it is set in the interrupt controller (ITC).

Figure VII.1.5.1 shows the configuration of the port input interrupt circuit.

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(Error)

VII.1.5.2 Control Registers of the Interrupt Controller

Selecting the trigger mode and polarity

The interrupt controller (ITC) provides two trigger modes for the port interrupts, the pulse trigger mode and the level trigger mode, to accept either a pulse signal or a level signal as interrupt requests.
The trigger mode can be selected using the EITG*x* bit in the ITC_ELV*x* registers (0x4306 to 0x430c). When EITG*x* is set to 1, level trigger mode is selected; when EITG*x* is set to 0 (default), pulse trigger mode is selected.
The ITC allows these interrupt sources to select the polarity of the interrupt request signal to be sent to the ITC.
The signal polarity can be selected using the EITP*x* bit in the ITC_ELV*x* registers (0x4306 to 0x430c). When EITP*x* is set to 1, positive pulse/rising edge (in pulse trigger mode) or active high (in level mode) is selected; when EIPT*x* is set to 0 (default), negative pulse/falling edge (in pulse trigger mode) or active low (in level mode) is selected.

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With these registers, the port input interrupt condition is determined as shown in Table VII.1.5.2.2.

Table VII.1.5.2.2 Port Input Interrupt Condition

EITG*x*	EITP*x*	Port Input Interrupt Condition
1	1	High level
1	0	Low level
0	1	Rising edge
0	0	Falling edge

(Correct)

VII.1.5.2 Control Registers of the Interrupt Controller

Selecting the trigger mode and polarity

The interrupt controller (ITC) provides the level trigger mode for the port interrupts, to accept a level signal as interrupt requests.
The trigger mode can be selected using the EITG*x* bit in the ITC_ELV*x* registers (0x4306 to 0x430c). When EITG*x* is set to 1, level trigger mode is selected. The default of EITG*x* is 0. so when the port interrupt is used, EITG*x* is set to 1.
The ITC allows these interrupt sources to select the polarity of the interrupt request signal to be sent to the ITC.
The signal polarity can be selected using the EITP*x* bit in the ITC_ELV*x* registers (0x4306 to 0x430c). When EITP*x* is set to 1, active high (in level mode) is selected; when EIPT*x* is set to 0 (default), active low (in level mode) is selected.

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With these registers, the port input interrupt condition is determined as shown in Table VII.1.5.2.2.

Table VII.1.5.2.2 Port Input Interrupt Condition

EITG*x*	EITP*x*	Port Input Interrupt Condition
1	1	High level
1	0	Low level
0	1	No support
0	0	No support

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(Error)

VII.1.7 Precautions

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• When pulse trigger interrupt mode is selected, the input pulse width must be longer than 1 cycle of the system clock to be certain an interrupt will be generated.

(Correct)

VII.1.7 Precautions

.....

~~• When pulse trigger interrupt mode is selected, the input pulse width must be longer than 1 cycle of the system clock to be certain an interrupt will be generated.~~

• The handshaking is needed to the interrupt generating equipment when use the level mode of port interrupt. Please maintain the signal level of outside equipment until CPU accepts interrupt and return ack to the external equipment after the acceptance.

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The one that correction was removed from content published in (Correct).

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Table IV.1.2.1 Vector Table

Vector No.	Vector address	Hardware interrupt name	Cause of hardware interrupt	Priority
0 (0x00)	TTBR + 0x00	Reset	· Low input to the #RESET pin · Watchdog timer overflow *2	1
1 (0x01)	TTBR + 0x04	Address misaligned interrupt	Memory access instruction	2
–	(0xfffc00)	Debugging interrupt	brk instruction, etc.	3
2 (0x02)	TTBR + 0x08	NMI	· Low input to the #NMI pin · Watchdog timer overflow *2	4
3 (0x03)	TTBR + 0x0c	C compiler (reserved)	Used in emulation library for C compiler	5
4 (0x04)	TTBR + 0x10	Port input interrupt 0	P*x*0 input (~~rising/falling edge or~~ high/low level)	High *1
5 (0x05)	TTBR + 0x14	Port input interrupt 1	P*x*1 input (~~rising/falling edge or~~ high/low level)	↑
6 (0x06)	TTBR + 0x18	Port input interrupt 2	P*x*2 input (~~rising/falling edge or~~ high/low level)	
7 (0x07)	TTBR + 0x1c	Port input interrupt 3	P*x*3 input (~~rising/falling edge or~~ high/low level)	
8 (0x08)	TTBR + 0x20	MFT interrupt	· Compare-match · Period-match · ADC protection input · Port protection input	
9 (0x09)	TTBR + 0x24	reserved	–	
10 (0x0a)	TTBR + 0x28	A/D converter	Out of range results (upper-and lowerlimit)	
11 (0x0b)	TTBR + 0x2c		End of conversion	
12 (0x0c)	TTBR + 0x30	CLG_T16U0 timer interrupt	Timer underflow	
		Port input interrupt 4	P*x*4 input (~~rising/falling edge or~~ high/low level)	
13 (0x0d)	TTBR + 0x34	Port input interrupt 5	P*x*5 input (~~rising/falling edge or~~ high/low level)	
14 (0x0e)	TTBR + 0x38	CLG_T8S timer interrupt	Timer underflow	
		Port input interrupt 6	P*x*6 input (~~rising/falling edge or~~ high/low level)	
15 (0x0f)	TTBR + 0x3c	CLG_T8I timer interrupt	Timer underflow	
		Port input interrupt 7	P*x*7 input (~~rising/falling edge or~~ high/low level)	
16 (0x10)	TTBR + 0x40	UART with IrDA CH.0 interrupt	· Transmit buffer empty · Receive buffer full · Receive error	
		Port input interrupt 4	P*x*4 input (~~rising/falling edge or~~ high/low level)	
17 (0x11)	TTBR + 0x44	Port input interrupt 5	P*x*5 input (~~rising/falling edge or~~ high/low level)	
18 (0x12)	TTBR + 0x48	SPI CH.0 interrupt	· Transmit buffer empty · Receive buffer full	
		Port input interrupt 6	P*x*6 input (~~rising/falling edge or~~ high/low level)	
19 (0x13)	TTBR + 0x4c	I2C interrupt	· Transmit buffer empty · Receive buffer full	
		Port input interrupt 7	P*x*7 input (~~rising/falling edge or~~ high/low level)	
20 (0x14)	TTBR + 0x50	RTC interrupt	1/64 second, 1 second, 1 minute, or 1 hour count up	
21 (0x15)	TTBR + 0x54	PT8 CH.0 interrupt	Timer 0 underflow	
22 (0x16)	TTBR + 0x58	PT8 CH.1 interrupt	Timer 1 underflow	
23 (0x17)	TTBR + 0x5c	PT8 CH.2 interrupt	Timer 2 underflow	
24 (0x18)	TTBR + 0x60	PT8 CH.3 interrupt	Timer 3 underflow	
25 (0x19)	TTBR + 0x64	LCDC interrupt	· End of frame · End of SPI transfer · End of DMA transfer	
26 (0x1a)	TTBR + 0x68	SPI CH.1 interrupt	· Transmit buffer empty · Receive buffer full	
27 (0x1b)	TTBR + 0x6c	USB function controller interrupt	USB interrupt	
28 (0x1c)	TTBR + 0x70	I2S interrupt	· I2S FIFO empty	
29 (0x1d)	TTBR + 0x74		· I2S FIFO full	
30 (0x1e)	TTBR + 0x78	REMC interrupt	· Envelope counter underflow · REMC_IN rising edge detection · REMC_IN falling edge detection	↓
31 (0x1f)	TTBR + 0x7c	reserved	–	Low *1

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(Error)

The one that correction was removed from content published in (Correct).

(Correct)

Table IV.1.3.2.1 Causes of Hardware Interrupt and Interrupt Flags

Cause of hardware interrupt	Interrupt flag
I2C interrupt: transmit buffer empty/receive buffer full	IIFT7 (D15/ITC_IFLG register)
SPI CH.0 interrupt: transmit buffer empty/receive buffer full	IIFT6 (D14/ITC_IFLG register)
UART interrupt: transmit buffer empty/receive buffer full/receive error	IIFT4 (D12/ITC_IFLG register)
CLG_T8I timer interrupt: timer underflow	IIFT3 (D11/ITC_IFLG register)
CLG_T8S timer interrupt: timer underflow	IIFT2 (D10/ITC_IFLG register)
CLG_T16U0 timer interrupt: timer underflow	IIFT0 (D8/ITC_IFLG register)
Port input interrupt 7: P*x*7 ~~rising/falling edge or~~ high/low level input	EIFT7 (D7/ITC_IFLG register)
Port input interrupt 6: P*x*6 ~~rising/falling edge or~~ high/low level input	EIFT6 (D6/ITC_IFLG register)
Port input interrupt 5: P*x*5 ~~rising/falling edge or~~ high/low level input	EIFT5 (D5/ITC_IFLG register)
Port input interrupt 4: P*x*4 ~~rising/falling edge or~~ high/low level input	EIFT4 (D4/ITC_IFLG register)
Port input interrupt 3: P*x*3 ~~rising/falling edge or~~ high/low level input	EIFT3 (D3/ITC_IFLG register)
Port input interrupt 2: P*x*2 ~~rising/falling edge or~~ high/low level input	EIFT2 (D2/ITC_IFLG register)
Port input interrupt 1: P*x*1 ~~rising/falling edge or~~ high/low level input	EIFT1 (D1/ITC_IFLG register)
Port input interrupt 0: P*x*0 ~~rising/falling edge or~~ high/low level input	EIFT0 (D0/ITC_IFLG register)
Remote controller interrupt: envelope counter underflow/input rising edge/input falling edge	AIFT14 (D14/ITC_AIFLG register)
I2S interrupt: I2S FIFO full	AIFT13 (D13/ITC_AIFLG register)
I2S interrupt: I2S FIFO empty	AIFT12 (D12/ITC_AIFLG register)
USB interrupt: USB interrupt	AIFT11 (D11/ITC_AIFLG register)
SPI CH.1 interrupt: transmit buffer empty/receive buffer full	AIFT10 (D10/ITC_AIFLG register)
LCDC interrupt: end of frame/end of SPI transfer/end of DMA transfer	AIFT9 (D9/ITC_AIFLG register)
PT8 CH.3 interrupt: timer underflow	AIFT8 (D8/ITC_AIFLG register)
PT8 CH.2 interrupt: timer underflow	AIFT7 (D7/ITC_AIFLG register)
PT8 CH.1 interrupt: timer underflow	AIFT6 (D6/ITC_AIFLG register)
PT8 CH.0 interrupt: timer underflow	AIFT5 (D5/ITC_AIFLG register)
RTC interrupt: 1/64 second, 1 second, 1 minute, or 1 hour count up	AIFT4 (D4/ITC_AIFLG register)
ADC interrupt: end of conversion	AIFT3 (D3/ITC_AIFLG register)
ADC interrupt: out of range	AIFT2 (D2/ITC_AIFLG register)
Multi-function timer interrupt: compare-match/period-match/protection input	AIFT0 (D0/ITC_AIFLG register)

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IV.1.3.5 Interrupt Trigger Mode

The ITC provides two trigger modes for the port interrupts, the pulse trigger mode and the level trigger mode, to accept either a pulse signal or a level signal as interrupt requests.
The trigger mode can be selected using the EITG*x* bit in the ITC_ELV*x* registers (0x4306 to 0x430c). When EITG*x* is set to 1, level trigger mode is selected; when EITG*x* is set to 0 (default), pulse trigger mode is selected.
The ITC allows these interrupt sources to select the polarity of the interrupt request signal to be sent to the ITC. The signal polarity can be selected using the EITP*x* bit in the ITC_ELV*x* registers (0x4306 to 0x430c). When EITP*x* is set to 1, positive pulse/rising edge (in pulse trigger mode) or active high (in level mode) is selected; when EIPT*x* is set to 0 (default), negative pulse/falling edge (in pulse trigger mode) or active low (in level mode) is selected.

(Correct)

IV.1.3.5 Interrupt Trigger Mode

The ITC provides level trigger modes for the port interrupts, to accept a level signal as interrupt requests.
The trigger mode can be selected using the EITG*x* bit in the ITC_ELV*x* registers (0x4306 to 0x430c). When EITG*x* is set to 1, level trigger mode is selected; when EITG*x* is set to 0 (default), pulse trigger mode is selected.
The ITC allows these interrupt sources to select the polarity of the interrupt request signal to be sent to the ITC. The signal polarity can be selected using the EITP*x* bit in the ITC_ELV*x* registers (0x4306 to 0x430c). When EITP*x* is set to 1, ~~positive pulse/rising edge (in pulse trigger mode) or~~ active high (in level mode) is selected; when EIPT*x* is set to 0 (default), ~~negative pulse/falling edge (in pulse trigger mode) or~~ active low (in level mode) is selected.

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0x4306: External Interrupt Level Setup Register 0 (ITC_ELV0)

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
External	**0x4306**	D15–14	**–**	reserved	–	–	–	0 when being read.
Interrupt Level	(16 bits)	D13	**EITP1**	Port interrupt 1 trigger polarity	1 Positive 0 Negative	0	R/W	
Setup Register0		D12	**EITG1**	Port interrupt 1 trigger mode	1 Level 0 Pulse	0	R/W	
(ITC_ELV0)		D11	**–**	reserved	–	–	–	0 when being read.
		D10–8	**EILV1[2:0]**	Port interrupt 1 level	0 to 7	0x0	R/W	
		D7–6	**–**	reserved	–	–	–	0 when being read.
		D5	**EITP0**	Port interrupt 0 trigger polarity	1 Positive 0 Negative	0	R/W	
		D4	**EITG0**	Port interrupt 0 trigger mode	1 Level 0 Pulse	0	R/W	
		D3	**–**	reserved	–	–	–	0 when being read.
		D2–0	**EILV0[2:0]**	Port interrupt 0 level	0 to 7	0x0	R/W	

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D13 EITP1: Port Interrupt 1 Trigger Polarity Bit

Selects the polarity of the port interrupt 1 signal.
1 (R/W): Positive/active high
0 (R/W): Negative/active low (default)

In pulse trigger mode, the port outputs a positive pulse for an interrupt request to the ITC when this bit is set to 1 or a negative pulse when this bit is set to 0.
In level trigger mode, the port outputs an active high signal for an interrupt request to the ITC when this bit is set to 1 or a active low signal when this bit is set to 0.

D12 EITG1: Port Interrupt 1 Trigger Mode Bit

Selects the trigger mode of the port interrupt 1.
1 (R/W): Level trigger mode
0 (R/W): Pulse trigger mode (default)

In pulse trigger mode, the ITC samples interrupt signals at the rising edge of the system clock. When a pulse with the specified polarity is sampled, the ITC sets the interrupt flag (EIFT*x*) to 1 and stops sampling of that interrupt signal. The ITC resumes the sampling operation for the interrupt signal after the interrupt flag (EIFT*x*) is reset to 0 in the application program (interrupt handler).
In level trigger mode, the ITC continuously samples interrupt signals at every rising edge of the system clock. The interrupt flag (EIFT*x*) is set to 1 when the specified active level is sampled and is reset to 0 when the inactive level is sampled. In this mode, writing 1 cannot reset the interrupt flag (EIFT*x*). Therefore, the interrupt source module must hold the interrupt signal to high until the S1C17 Core accepts the interrupt request and must reset the interrupt signal after that.

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D5 EITP0: Port Interrupt 0 Trigger Polarity Bit

Selects the polarity of the port interrupt 0 signal.
1 (R/W): Positive/active high
0 (R/W): Negative/active low (default)

See the description of EITP1 (D13).

D4 EITG0: Port Interrupt 0 Trigger Mode Bit

Selects the trigger mode of the port interrupt 0.
1 (R/W): Level trigger mode
0 (R/W): Pulse trigger mode (default)

See the description of EITG1 (D12).

(Correct)

0x4306: External Interrupt Level Setup Register 0 (ITC_ELV0)

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
External Interrupt Level Setup Register0 (ITC_ELV0)	0x4306 (16 bits)	D15–14	–	reserved	–	–	–	0 when being read.
		D13	EITP1	Port interrupt 1 trigger polarity	1 Active high 0 Active low	0	R/W	
		D12	EITG1	Port interrupt 1 trigger mode	1 Level 0 No support	0	R/W	
		D11	–	reserved	–	–	–	0 when being read.
		D10–8	EILV1[2:0]	Port interrupt 1 level	0 to 7	0x0	R/W	
		D7–6	–	reserved	–	–	–	0 when being read.
		D5	EITP0	Port interrupt 0 trigger polarity	1 Active high 0 Active low	0	R/W	
		D4	EITG0	Port interrupt 0 trigger mode	1 Level 0 No support	0	R/W	
		D3	–	reserved	–	–	–	0 when being read.
		D2–0	EILV0[2:0]	Port interrupt 0 level	0 to 7	0x0	R/W	

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D13 EITP1: Port Interrupt 1 Trigger Polarity Bit

Selects the polarity of the port interrupt 1 signal.
1 (R/W): ~~Positive/~~Active high
0 (R/W): ~~Negative/~~Active low (default)

~~In pulse trigger mode, the port outputs a positive pulse for an interrupt request to the ITC when this bit is set to 1 or a negative pulse when this bit is set to 0.~~
In level trigger mode, the port outputs an active high signal for an interrupt request to the ITC when this bit is set to 1 or a active low signal when this bit is set to 0.

D12 EITG1: Port Interrupt 1 Trigger Mode Bit

Selects the trigger mode of the port interrupt 1.
1 (R/W): Level trigger mode
0 (R/W): No support (default)

~~In pulse trigger mode, the ITC samples interrupt signals at the rising edge of the system clock. When a pulse with the specified polarity is sampled, the ITC sets the interrupt flag (EIFT*x*) to 1 and stops sampling of that interrupt signal. The ITC resumes the sampling operation for the interrupt signal after the interrupt flag (EIFT*x*) is reset to 0 in the application program (interrupt handler).~~
In level trigger mode, the ITC continuously samples interrupt signals at every rising edge of the system clock. The interrupt flag (EIFT*x*) is set to 1 when the specified active level is sampled and is reset to 0 when the inactive level is sampled. In this mode, writing 1 cannot reset the interrupt flag (EIFT*x*). Therefore, the interrupt source module must hold the interrupt signal to high until the S1C17 Core accepts the interrupt request and must reset the interrupt signal after that.

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D5 EITP0: Port Interrupt 0 Trigger Polarity Bit

Selects the polarity of the port interrupt 0 signal.
1 (R/W): ~~Positive/~~Active high
0 (R/W): ~~Negative/~~Active low (default)

See the description of EITP1 (D13).

D4 EITG0: Port Interrupt 0 Trigger Mode Bit

Selects the trigger mode of the port interrupt 0.
1 (R/W): Level trigger mode
0 (R/W): No support (default)

See the description of EITG1 (D12).

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0x4308: External Interrupt Level Setup Register 1 (ITC_ELV1)

Register name	Address	Bit	Name	Function	Setting				Init.	R/W	Remarks
External	0x4308	D15–14	–	reserved	–				–	–	0 when being read.
Interrupt Level	(16 bits)	D13	EITP3	Port interrupt 3 trigger polarity	1	Positive	0	Negative	0	R/W	
Setup Register1		D12	EITG3	Port interrupt 3 trigger mode	1	Level	0	Pulse	0	R/W	
(ITC_ELv1)		D11	–	reserved	–				–	–	0 when being read.
		D10–8	EILV3[2:0]	Port interrupt 3 level	0 to 7				0x0	R/W	
		D7–6	–	reserved	–				–	–	0 when being read.
		D5	EITP2	Port interrupt 2 trigger polarity	1	Positive	0	Negative	0	R/W	
		D4	EITG2	Port interrupt 2 trigger mode	1	Level	0	Pulse	0	R/W	
		D3	–	reserved	–				–	–	0 when being read.
		D2–0	EILV2[2:0]	Port interrupt 2 level	0 to 7				0x0	R/W	

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D13 EITP3: Port Interrupt 3 Trigger Polarity Bit

Selects the polarity of the port interrupt 3 signal.
1 (R/W): Positive/active high
0 (R/W): Negative/active low (default)

See the description of EITP1 (D13) in the ITC_ELV0 register (0x4306).

D12 EITG3: Port Interrupt 3 Trigger Mode Bit

Selects the trigger mode of the port interrupt 3.
1 (R/W): Level trigger mode
0 (R/W): Pulse trigger mode (default)

See the description of EITG1 (D12) in the ITC_ELV0 register (0x4306).

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D5 EITP2: Port Interrupt 2 Trigger Polarity Bit

Selects the polarity of the port interrupt 2 signal.
1 (R/W): Positive/active high
0 (R/W): Negative/active low (default)

See the description of EITP1 (D13) in the ITC_ELV0 register (0x4306).

D4 EITG2: Port Interrupt 2 Trigger Mode Bit

Selects the trigger mode of the port interrupt 2.
1 (R/W): Level trigger mode
0 (R/W): Pulse trigger mode (default)

See the description of EITG1 (D12) in the ITC_ELV0 register (0x4306).

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0x4308: External Interrupt Level Setup Register 1 (ITC_ELV1)

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
External Interrupt Level Setup Register1 (ITC_ELv1)	**0x4308** (16 bits)	D15–14	**–**	reserved	–	–	–	0 when being read.
		D13	**EITP3**	Port interrupt 3 trigger polarity	1 Active high 0 Active low	0	R/W	
		D12	**EITG3**	Port interrupt 3 trigger mode	1 Level 0 No support	0	R/W	
		D11	**–**	reserved	–	–	–	0 when being read.
		D10–8	**EILV3[2:0]**	Port interrupt 3 level	0 to 7	0x0	R/W	
		D7–6	**–**	reserved	–	–	–	0 when being read.
		D5	**EITP2**	Port interrupt 2 trigger polarity	1 Active high 0 Active low	0	R/W	
		D4	**EITG2**	Port interrupt 2 trigger mode	1 Level 0 No support	0	R/W	
		D3	**–**	reserved	–	–	–	0 when being read.
		D2–0	**EILV2[2:0]**	Port interrupt 2 level	0 to 7	0x0	R/W	

……

D13 EITP3: Port Interrupt 3 Trigger Polarity Bit

Selects the polarity of the port interrupt 3 signal.
1 (R/W): ~~Positive/~~Active high
0 (R/W): ~~Negative/~~Active low (default)

See the description of EITP1 (D13) in the ITC_ELV0 register (0x4306).

D12 EITG3: Port Interrupt 3 Trigger Mode Bit

Selects the trigger mode of the port interrupt 3.
1 (R/W): Level trigger mode
0 (R/W): No support (default)

See the description of EITG1 (D12) in the ITC_ELV0 register (0x4306).

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D5 EITP2: Port Interrupt 2 Trigger Polarity Bit

Selects the polarity of the port interrupt 2 signal.
1 (R/W): ~~Positive/~~Active high
0 (R/W): ~~Negative/~~Active low (default)

See the description of EITP1 (D13) in the ITC_ELV0 register (0x4306).

D4 EITG2: Port Interrupt 2 Trigger Mode Bit

Selects the trigger mode of the port interrupt 2.
1 (R/W): Level trigger mode
0 (R/W): No support (default)

See the description of EITG1 (D12) in the ITC_ELV0 register (0x4306).

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(Error)

0x430a: External Interrupt Level Setup Register 2 (ITC_ELV2)

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
External	**0x430a**	D15–14	**–**	reserved	–	–	–	0 when being read.
Interrupt Level	(16 bits)	D13	**EITP5**	Port interrupt 5 trigger polarity	1 Positive 0 Negative	0	R/W	
Setup Register 2		D12	**EITG5**	Port interrupt 5 trigger mode	1 Level 0 Pulse	0	R/W	
(ITC_ELV2)		D11	**–**	reserved	–	–	–	0 when being read.
		D10–8	**EILV5[2:0]**	Port interrupt 5 level	0 to 7	0x0	R/W	
		D7–6	**–**	reserved	–	–	–	0 when being read.
		D5	**EITP4**	Port interrupt 4 trigger polarity	1 Positive 0 Negative	0	R/W	
		D4	**EITG4**	Port interrupt 4 trigger mode	1 Level 0 Pulse	0	R/W	
		D3	**–**	reserved	–	–	–	0 when being read.
		D2–0	**EILV4[2:0]**	Port interrupt 4 level	0 to 7	0x0	R/W	

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D13 EITP5: Port Interrupt 5 Trigger Polarity Bit

Selects the polarity of the port interrupt 5 signal.
1 (R/W): Positive/active high
0 (R/W): Negative/active low (default)

See the description of EITP1 (D13) in the ITC_ELV0 register (0x4306).

D12 EITG5: Port Interrupt 5 Trigger Mode Bit

Selects the trigger mode of the port interrupt 5.
1 (R/W): Level trigger mode
0 (R/W): Pulse trigger mode (default)

See the description of EITG1 (D12) in the ITC_ELV0 register (0x4306).

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D5 EITP4: Port Interrupt 4 Trigger Polarity Bit

Selects the polarity of the port interrupt 4 signal.
1 (R/W): Positive/active high
0 (R/W): Negative/active low (default)

See the description of EITP1 (D13) in the ITC_ELV0 register (0x4306).

D4 EITG4: Port Interrupt 4 Trigger Mode Bit

Selects the trigger mode of the port interrupt 4.
1 (R/W): Level trigger mode
0 (R/W): Pulse trigger mode (default)

See the description of EITG1 (D12) in the ITC_ELV0 register (0x4306).

(Correct)

0x430a: External Interrupt Level Setup Register 2 (ITC_ELV2)

Register name	Address	Bit	Name	Function	Setting				Init.	R/W	Remarks
External Interrupt Level Setup Register 2 (ITC_ELV2)	0x430a (16 bits)	D15–14	–	reserved	–				–	–	0 when being read.
		D13	EITP5	Port interrupt 5 trigger polarity	1	Active high	0	Active low	0	R/W	
		D12	EITG5	Port interrupt 5 trigger mode	1	Level	0	No support	0	R/W	
		D11	–	reserved	–				–	–	0 when being read.
		D10–8	EILV5[2:0]	Port interrupt 5 level	0 to 7				0x0	R/W	
		D7–6	–	reserved	–				–	–	0 when being read.
		D5	EITP4	Port interrupt 4 trigger polarity	1	Active high	0	Active low	0	R/W	
		D4	EITG4	Port interrupt 4 trigger mode	1	Level	0	No support	0	R/W	
		D3	–	reserved	–				–	–	0 when being read.
		D2–0	EILV4[2:0]	Port interrupt 4 level	0 to 7				0x0	R/W	

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D13 EITP5: Port Interrupt 5 Trigger Polarity Bit

Selects the polarity of the port interrupt 5 signal.
1 (R/W): ~~Positive/~~Active high
0 (R/W): ~~Negative/~~Active low (default)

See the description of EITP1 (D13) in the ITC_ELV0 register (0x4306).

D12 EITG5: Port Interrupt 5 Trigger Mode Bit

Selects the trigger mode of the port interrupt 5.
1 (R/W): Level trigger mode
0 (R/W): No support (default)

See the description of EITG1 (D12) in the ITC_ELV0 register (0x4306).

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D5 EITP4: Port Interrupt 4 Trigger Polarity Bit

Selects the polarity of the port interrupt 4 signal.
1 (R/W): ~~Positive/~~Active high
0 (R/W): ~~Negative/~~Active low (default)

See the description of EITP1 (D13) in the ITC_ELV0 register (0x4306).

D4 EITG4: Port Interrupt 4 Trigger Mode Bit

Selects the trigger mode of the port interrupt 4.
1 (R/W): Level trigger mode
0 (R/W): No support (default)

See the description of EITG1 (D12) in the ITC_ELV0 register (0x4306).

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0x430c: External Interrupt Level Setup Register 3 (ITC_ELV3)

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
External	**0x430c**	D15–14	**–**	reserved	–	–	–	0 when being read.
Interrupt Level	(16 bits)	D13	**EITP7**	Port interrupt 7 trigger polarity	1 Positive 0 Negative	0	R/W	
Setup Register3		D12	**EITG7**	Port interrupt 7 trigger mode	1 Level 0 Pulse	0	R/W	
(ITC_ELV3)		D11	**–**	reserved	–	–	–	0 when being read.
		D10–8	**EILV7[2:0]**	Port interrupt 7 level	0 to 7	0x0	R/W	
		D7–6	**–**	reserved	–	–	–	0 when being read.
		D5	**EITP6**	Port interrupt 6 trigger polarity	1 Positive 0 Negative	0	R/W	
		D4	**EITG6**	Port interrupt 6 trigger mode	1 Level 0 Pulse	0	R/W	
		D3	**–**	reserved	–	–	–	0 when being read.
		D2–0	**EILV6[2:0]**	Port interrupt 6 level	0 to 7	0x0	R/W	

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D13 EITP7: Port Interrupt 7 Trigger Polarity Bit

Selects the polarity of the port interrupt 7 signal.
1 (R/W): Positive/active high
0 (R/W): Negative/active low (default)

See the description of EITP1 (D13) in the ITC_ELV0 register (0x4306).

D12 EITG7: Port Interrupt 7 Trigger Mode Bit

Selects the trigger mode of the port interrupt 7.
1 (R/W): Level trigger mode
0 (R/W): Pulse trigger mode (default)

See the description of EITG1 (D12) in the ITC_ELV0 register (0x4306).

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D5 EITP6: Port Interrupt 6 Trigger Polarity Bit

Selects the polarity of the port interrupt 6 signal.
1 (R/W): Positive/active high
0 (R/W): Negative/active low (default)

See the description of EITP1 (D13) in the ITC_ELV0 register (0x4306).

D4 EITG6: Port Interrupt 6 Trigger Mode Bit

Selects the trigger mode of the port interrupt 6.
1 (R/W): Level trigger mode
0 (R/W): Pulse trigger mode (default)

See the description of EITG1 (D12) in the ITC_ELV0 register (0x4306).

(Correct)

0x430c: External Interrupt Level Setup Register 3 (ITC_ELV3)

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
External Interrupt Level Setup Register3 (ITC_ELV3)	0x430c (16 bits)	D15–14	–	reserved	–	–	–	0 when being read.
		D13	EITP7	Port interrupt 7 trigger polarity	1 Active high 0 Active low	0	R/W	
		D12	EITG7	Port interrupt 7 trigger mode	1 Level 0 No support	0	R/W	
		D11	–	reserved	–	–	–	0 when being read.
		D10–8	EILV7[2:0]	Port interrupt 7 level	0 to 7	0x0	R/W	
		D7–6	–	reserved	–	–	–	0 when being read.
		D5	EITP6	Port interrupt 6 trigger polarity	1 Active high 0 Active low	0	R/W	
		D4	EITG6	Port interrupt 6 trigger mode	1 Level 0 No support	0	R/W	
		D3	–	reserved	–	–	–	0 when being read.
		D2–0	EILV6[2:0]	Port interrupt 6 level	0 to 7	0x0	R/W	

……

D13 EITP7: Port Interrupt 7 Trigger Polarity Bit

Selects the polarity of the port interrupt 7 signal.
1 (R/W): ~~Positive/~~Active high
0 (R/W): ~~Negative/~~Active low (default)

See the description of EITP1 (D13) in the ITC_ELV0 register (0x4306).

D12 EITG7: Port Interrupt 7 Trigger Mode Bit

Selects the trigger mode of the port interrupt 7.
1 (R/W): Level trigger mode
0 (R/W): No support (default)

See the description of EITG1 (D12) in the ITC_ELV0 register (0x4306).

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D5 EITP6: Port Interrupt 6 Trigger Polarity Bit

Selects the polarity of the port interrupt 6 signal.
1 (R/W): ~~Positive/~~Active high
0 (R/W): ~~Negative/~~Active low (default)

See the description of EITP1 (D13) in the ITC_ELV0 register (0x4306).

D4 EITG6: Port Interrupt 6 Trigger Mode Bit

Selects the trigger mode of the port interrupt 6.
1 (R/W): Level trigger mode
0 (R/W): No support (default)

See the description of EITG1 (D12) in the ITC_ELV0 register (0x4306).

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(Error)

The one that correction was removed from content published in (Correct).

(Correct)

Table IV.1.8.1 Clock Settings Required for Generating Interrupts

Clock system	Mode in which the CMU register settings are effective	Clock supply status			Clock settings required for generating interrupts																					
		Normal mode	HALT mode	SLEEP mode	Normal/HALT mode																		SLEEP mode			
					AMI	DBG	NMI	MFT	ADC	T16	T8	UART	SPI	I^2C	PORT	RTC	PT8	LCDC	SPI	USB	I^2S	REMC	DBG	NMI	PORT	RTC
PCLK	Normal/HALT	REG	REG	Stop				○	○	○	○	○	○	○	○	○	○	○	○	○	○	○			○	○
LCDC_SAPB_CLK	Normal/HALT	REG	REG	Stop														○								
LCDC_HIF	Normal/HALT	REG	REG	Stop														○								
USB_CLK	Normal/HALT	REG	REG	Stop																*6						
USB_SAPB_CLK	Normal/HALT	REG	REG	Stop																*6						
FLASHC	HALT	Cannot be stopped	REG	Stop																						
MFT_CLK	Normal/HALT	REG	REG	Stop				○																		
PT8_CLK	Normal/HALT	REG	REG	Stop													○									
SRAMC_CLK	HALT	Cannot be stopped	REG	Stop																						
RTC_SAPB_CLK	Normal/HALT	REG	REG	Stop												○										○
PORT_CLK	Normal/HALT	REG	REG	Stop											~~*4~~										*5	
WDT_CLK	Normal/HALT	REG	REG	Stop			*3																			
ADC_CLK	Normal/HALT	REG	REG	Stop					○																	
REMC_CLK	Normal/HALT	REG	REG	Stop																		○				
SPI_CLK	Normal/HALT	REG	REG	Stop															○							
CPU	–	Cannot be stopped	Stop	Stop	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
RTC	–	Cannot be stopped *1	Cannot be stopped *1	Cannot be stopped *1												○										○
OSC1 oscillator	–	Cannot be stopped *2	Cannot be stopped *2	Cannot be stopped *2	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7	○	*7	*7	*7	*7	*7	*7	*7	*7	*7	○
OSC3 oscillator	Normal/HALT	REG	REG	REG	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7

REG: Configurable with the register
○: Clock absolutely required for generating interrupts
AMI: Address misaligned interrupt
*1: Stops when the function is disabled in the peripheral module.
*2: Cannot be oscillated if the external input signal level is fixed.
*3: The clock must be supplied to generate NMI from WDT.
~~*4: Required only when pulse trigger interrupt is configured.~~
*5: Not required after the registers have been configured. (Level trigger interrupt only)
*6: Not required for generating a VBUS_Changed or NonJ interrupt in Snooze status. Required for other interrupts.
*7: The OSC1 or OSC3 oscillator circuit, which is used as the system clock source, must always be active except in SLEEP mode.

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(Error)

The one that correction was removed from content published in (Correct).

(Correct)

Table IV.1.8.1 Clock Settings Required for Generating Interrupts

Clock system	Mode in which the CMU register settings are effective	Clock supply status			Clock settings required for generating interrupts																				
		Normal mode	HALT mode	SLEEP mode	Normal/HALT mode																	SLEEP mode			
					AMI	DBG	NMI	MFT	ADC	T16	T8	UART	SPI	I²C	PORT	RTC	PT8	SPI	USB	I²S	REMC	DBG	NMI	PORT	RTC
PCLK	Normal/HALT	REG	REG	Stop				○	○	○	○	○	○	○	○	○	○	○	○	○	○			○	○
USB_CLK	Normal/HALT	REG	REG	Stop															*6						
USB_SAPB_CLK	Normal/HALT	REG	REG	Stop															*6						
FLASHC	HALT	Cannot be stopped	REG	Stop																					
MFT_CLK	Normal/HALT	REG	REG	Stop				○																	
PT8_CLK	Normal/HALT	REG	REG	Stop													○								
SRAMC_CLK	HALT	Cannot be stopped	REG	Stop																					
RTC_SAPB_CLK	Normal/HALT	REG	REG	Stop												○									○
PORT_CLK	Normal/HALT	REG	REG	Stop											~~*4~~									*5	
WDT_CLK	Normal/HALT	REG	REG	Stop			*3																		
ADC_CLK	Normal/HALT	REG	REG	Stop					○																
REMC_CLK	Normal/HALT	REG	REG	Stop																	○				
SPI_CLK	Normal/HALT	REG	REG	Stop														○							
CPU	–	Cannot be stopped	Stop	Stop	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
RTC	–	Cannot be stopped *1	Cannot be stopped *1	Cannot be stopped *1												○									○
OSC1 oscillator	–	Cannot be stopped *2	Cannot be stopped *2	Cannot be stopped *2	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7	○	*7	*7	*7	*7	*7	*7	*7	*7	○
OSC3 oscillator	Normal/HALT	REG	REG	REG	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7	*7

REG: Configurable with the register
○: Clock absolutely required for generating interrupts
AMI: Address misaligned interrupt
*1: Stops when the function is disabled in the peripheral module.
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*6: Not required for generating a VBUS_Changed or NonJ interrupt in Snooze status. Required for other interrupts.
*7: The OSC1 or OSC3 oscillator circuit, which is used as the system clock source, must always be active except in SLEEP mode.