Aug/28/2013

errata_c17003_19

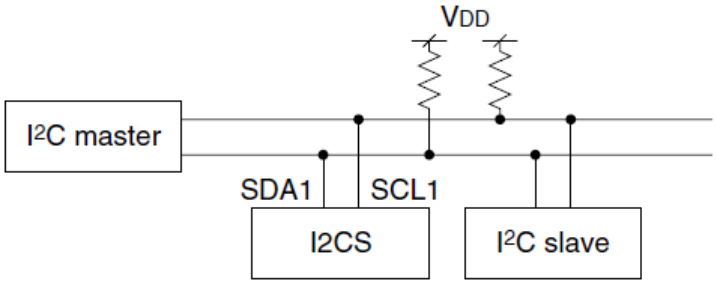
S1C17 Family Technical Manual Errata

ITEM **I2C Slave Input/Output Pins**

Object manual	Document code	Object item	Page
S1C17601 Technical Manual	411805701	21.2 I2C Slave Input/Output Pins	21-2
S1C17611 Technical Manual	411882301	21.2 I2C Slave Input/Output Pins	21-2
S1C17706 Technical Manual	412026401	18.2 I2CS Input/Output Pins	18-1
S1C17002 Technical Manual	411554402	V.3.2 I2C Slave I/O Pins	V-3-2
S1C17003 Technical Manual	411635102	21.2 I2C Slave Input/Output Pins	21-2
S1C17803 Technical Manual	411820401	21.2 I2CS Input/Output Pins	21-2

(Addition)

Note: The pins go to high impedance status when the port function is switched. The SCL and SDA pins do not output a high level, so these lines should be pulled up to VDDwith an external pull-up resistor. Be sure to avoid pulling these pins up to a voltage that exceeds the VDD level.



Aug/28/2013

errata_c17003_18

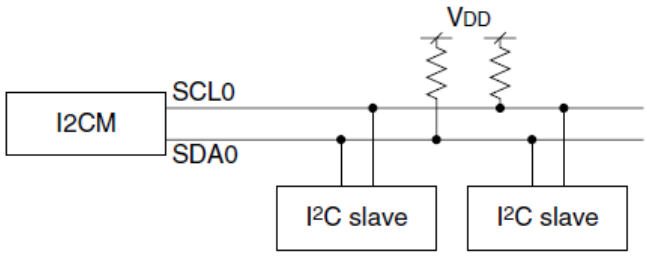
S1C17 Family Technical Manual Errata

ITEM **I2C Master Input/Output Pins**

Object manual	Document code	Object item	Page
S1C17601 Technical Manual	411805701	20.2 I2C Master Input/Output Pins	20-2
S1C17611 Technical Manual	411882301	20.2 I2C Master Input/Output Pins	20-2
S1C17701 Technical Manual	411089904	20.2 I2C I/O Pins	20-2
S1C17704 Technical Manual	411511903	20.2 I2C I/O Pins	20-2
S1C17706 Technical Manual	412026401	17.2 I2CM Input/Output Pins	17-1
S1C17001 Technical Manual	411412301	20.2 I2C Input/Output Pins	252
S1C17002 Technical Manual	411554402	V.2.2 I2C Master I/O Pins	V-2-2
S1C17003 Technical Manual	411635102	20.2 I2C Master Input/Output Pins	20-2
S1C17501 Technical Manual	411525602	VI.2.2 I2C I/O Pins	VI-2-2
S1C17801 Technical Manual	411390802	VI.2.2 I2C I/O Pins	VI-2-2
S1C17803 Technical Manual	411820401	20.2 I2CM Input/Output Pins	20-2

(Addition)

Note: The pins go to high impedance status when the port function is switched.
The SCL and SDA pins do not output a high level, so these lines should be pulled up to VDD with an external pull-up resistor. Be sure to avoid pulling these pins up to a voltage that exceeds the VDD level.



Dec/26/2012

errata_c17003_17

S1C17 Family Technical Manual Errata

ITEM Recommended values for external parts (for the OSC1 oscillator circuit)			
Object manual	Document code	Object item	Page
S1C17002 Technical Manual	411554403	I.8 Basic External Wiring Diagram	I-8-1
S1C17003 Technical Manual	411635102	27 Basic External Wiring Diagram	27-1

Page I-8-1 S1C17002 Technical Manual

Page 27-1 S1C17003 Technical Manual

(Error)

Recommended values for external parts

External parts the OSC1 oscillator circuit

Symbol	Resonator	Recommended manufacturer	Frequency [Hz]	Product number	Recommended values				Recommended operating condition
					C_{O1} [pF]	C_{G1} [pF]	R_{f1} [O]	R_{d1} [O]	Temperature range [℃]
X'tal1	Crystal	Epson Toyocom Corporation	32.768k	MC-146(C_L=7.0pF)	7	7	**1M**	0	-40 to 85

(Correct)

Recommended values for external parts

External parts the OSC1 oscillator circuit

Symbol	Resonator	Recommended manufacturer	Frequency [Hz]	Product number	Recommended values				Recommended operating condition
					C_{O1} [pF]	C_{G1} [pF]	R_{f1} [O]	R_{d1} [O]	Temperature range [℃]
X'tal1	Crystal	Seiko Epson Corporation	32.768k	MC-146(C_L=7.0pF)	7	7	**10M**	0	-40 to 85

Nov/09/2012

errata_c17003_16

S1C17 Family Technical Manual Errata

ITEM About the Fine mode setting of T16E.			
Object manual	Document code	Object item	Page
S1C17001 Technical Manual	411412303	13.6 Clock Output Control	150
S1C17003 Technical Manual	411635102	13.6 Clock Output Control	13-8
S1C17624/604/622/621 Technical Manual	411914902	12.7 Clock Output Control	12-6
S1C17701 Technical Manual	411089905	13.6 Controlling Clock Output	13-8
S1C17702 Technical Manual	411581702	13.6 Clock Output Control	13-8
S1C17704 Technical Manual	411511903	13.6 Controlling Clock Output	13-8

Page 150 S1C17001 Technical Manual

Page 13-8 S1C17003 Technical Manual

Page 13-8 S1C17701 Technical Manual

Page 13-8 S1C17702 Technical Manual

Page 13-8 S1C17704 Technical Manual

Add following comment at Precautions of “Setting fine mode for clock output”.

(3) Use the Fine mode only for T16EDF = 0x0 (PCLK-1/1).

Page 12-6 S1C17623/604/622/621 Technical Manual

Add following comment at Precautions of “Setting fine mode for clock output”.

(4) Use the Fine mode only for T16EDF = 0x0 (PCLK-1/1).

Dec/27/2011

errata_c17003_15

S1C17 Series Technical Manual Errata

ITEM Transmission buffer empty interrupt at SPI slave mode			
Object manual	Document code	Object Item	Page
S1C17003 Technical Manual	411635102	19.6 SPI Interrupts	19-8
		19.7 Control Register Details	19-13
		19.8 Precautions	19-15
S1C17705/703 Technical Manual	411706602	19.6 SPI Interrupts	15-5
		19.7 Control Register Details	15-8

Page 19-8 S1C17003 Technical Manual

(Error)

Transmit buffer empty interrupt

To use this interrupt, set SPTIE (D4/SPI_CTL register) to 1. If SPTIE is set to 0 (default), interrupt requests for this factor will not be sent to the ITC.

* **SPTIE**: Transmit Data Buffer Empty Interrupt Enable Bit in the SPI Control (SPI_CTL) Register (D4/0x4326)

When transmission data written to the transmit data buffer is transferred to the shift register, the SPI module sets the SPTBE bit (D0/SPI_ST register) to 1, indicating that the transmit data buffer is empty. If transmit buffer empty interrupts are permitted (SPTIE = 1), an interrupt request pulse is sent simultaneously to the ITC.

* **SPTBE**: Transmit Data Buffer Empty Flag in the SPI Status (SPI_ST) Register (D0/0x4320)

An interrupt occurs if other interrupt conditions are met.

You can inspect the SPTBE flag in the SPI interrupt processing routine to determine whether the SPI interrupt is attributable to a transmit buffer empty. If SPTBE is 1, the next transmission data can be written to the transmit data buffer by the interrupt processing routine.

(Correct)

Transmit buffer empty interrupt

To use this interrupt, set SPTIE (D4/SPI_CTL register) to 1. If SPTIE is set to 0 (default), interrupt requests for this factor will not be sent to the ITC.

* **SPTIE**: Transmit Data Buffer Empty Interrupt Enable Bit in the SPI Control (SPI_CTL) Register (D4/0x4326)

When transmission data written to the transmit data buffer is transferred to the shift register, the SPI module sets the SPTBE bit (D0/SPI_ST register) to 1, indicating that the transmit data buffer is empty. If transmit buffer empty interrupts are permitted (SPTIE = 1), an interrupt request pulse is sent

simultaneously to the ITC.

* **SPTBE**: Transmit Data Buffer Empty Flag in the SPI Status (SPI_ST) Register (D0/0x4320)

An interrupt occurs if other interrupt conditions are met.

You can inspect the SPTBE flag in the SPI interrupt processing routine to determine whether the SPI interrupt is attributable to a transmit buffer empty. If SPTBE is 1, the next transmission data can be written to the transmit data buffer by the interrupt processing routine.

Note: the transmit buffer empty interrupt can only be used in master mode.

Page 19-13 S1C17003 Technical Manual

(Error)

D4 SPTIE: Transmit Data Buffer Empty Interrupt Enable Bit

Permits or prohibits transmit data buffer empty SPI interrupts.

1 (R/W): Permitted

0 (R/W): Prohibited (default)

Setting SPTIE to 1 permits the output of SPI interrupt requests to the ITC due to a transmit data buffer empty. These interrupt requests are generated when the data written to the transmit data buffer is transferred to the shift register (when transmission starts). SPI interrupts are not generated by transmit data buffer empty if SPTIE is set to 0.

(Correct)

D4 SPTIE: Transmit Data Buffer Empty Interrupt Enable Bit

Permits or prohibits transmit data buffer empty SPI interrupts.

1 (R/W): Permitted

0 (R/W): Prohibited (default)

Setting SPTIE to 1 permits the output of SPI interrupt requests to the ITC due to a transmit data buffer empty. These interrupt requests are generated when the data written to the transmit data buffer is transferred to the shift register (when transmission starts). SPI interrupts are not generated by transmit data buffer empty if SPTIE is set to 0.

Note: the transmit buffer empty interrupt can only be used in master mode.

Page 19-15 S1C17003 Technical Manual

(Error)

• Do not access the SPI_CTL register (0x4326) while the SPBY flag (D2/SPI_ST register) is set to 1, or the SPRBF flag (D1/SPI_ST register) is set to 1 (while sending or receiving data).

* **SPBSY**: Transfer Busy Flag in the SPI Status (SPI_ST) Register (D2/0x4320)

* **SPRBF**: Receive Data Buffer Full Flag in the SPI Status (SPI_ST) Register (D1/0x4320)

• Do not gain write access to read registers (the SPI_ST and SPI_RXD registers) while sending/receiving data via SPI.

(Correct)

• Do not access the SPI_CTL register (0x4326) while the SPBY flag (D2/SPI_ST register) is set to 1, or the SPRBF flag (D1/SPI_ST register) is set to 1 (while sending or receiving data).

  * **SPBSY**: Transfer Busy Flag in the SPI Status (SPI_ST) Register (D2/0x4320)

  * **SPRBF**: Receive Data Buffer Full Flag in the SPI Status (SPI_ST) Register (D1/0x4320)

• Do not gain write access to read registers (the SPI_ST and SPI_RXD registers) while sending/receiving data via SPI.

• The transmit buffer empty interrupt can only be used in master mode.

Page 15-5 S1C17705/703 Technical Manual

(Error)

Transmit buffer empty interrupt

To use this interrupt, set SPTIE/SPI_CTLx register to 1. If SPTIE is set to 0 (default), interrupt requests for this factor will not be sent to the ITC.

When transmission data written to the transmit data buffer is transferred to the shift register, the SPI module sets the SPTBE/SPI_STx register to 1, indicating that the transmit data buffer is empty. If transmit buffer empty interrupts are permitted (SPTIE = 1), an interrupt request pulse is sent simultaneously to the ITC.

An interrupt occurs if other interrupt conditions are met. You can inspect the SPTBE flag in the SPI interrupt handler routine to determine whether the SPI interrupt is attributable to a transmit buffer empty. If SPTBE is 1, the next transmit data can be written to the transmit data buffer by the interrupt handler routine.

(Correct)

Transmit buffer empty interrupt

To use this interrupt, set SPTIE/SPI_CTLx register to 1. If SPTIE is set to 0 (default), interrupt requests for this factor will not be sent to the ITC.

When transmission data written to the transmit data buffer is transferred to the shift register, the SPI module sets the SPTBE/SPI_STx register to 1, indicating that the transmit data buffer is empty. If transmit buffer empty interrupts are permitted (SPTIE = 1), an interrupt request pulse is sent simultaneously to the ITC.

An interrupt occurs if other interrupt conditions are met. You can inspect the SPTBE flag in the SPI interrupt handler routine to determine whether the SPI interrupt is attributable to a transmit buffer empty. If SPTBE is 1, the next transmit data can be written to the transmit data buffer by the interrupt handler routine.

Note: the transmit buffer empty interrupt can only be used in master mode.

Page 15-8 S1C17705/703 Technical Manual

(Error)

D4 SPTIE: Transmit Data Buffer Empty Interrupt Enable Bit

Enables or disables SPI transmit data buffer empty interrupts.

1 (R/W): Enabled

0 (R/W): Disabled (default)

Setting SPTIE to 1 enables the output of SPI interrupt requests to the ITC due to a transmit data buffer empty. These interrupt requests are generated when the data written to the transmit data buffer is transferred to the shift register (when transmission starts).

SPI interrupts are not generated by transmit data buffer empty if SPTIE is set to 0.

(Correct)

D4 SPTIE: Transmit Data Buffer Empty Interrupt Enable Bit

Enables or disables SPI transmit data buffer empty interrupts.

1 (R/W): Enabled

0 (R/W): Disabled (default)

Setting SPTIE to 1 enables the output of SPI interrupt requests to the ITC due to a transmit data buffer empty. These interrupt requests are generated when the data written to the transmit data buffer is transferred to the shift register (when transmission starts).

SPI interrupts are not generated by transmit data buffer empty if SPTIE is set to 0.

Note: the transmit buffer empty interrupt can only be used in master mode.