Epson ASIC proposal

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The product features in this presentation is as of Dec. 2025 and may change without notification.

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1. About Epson ASIC

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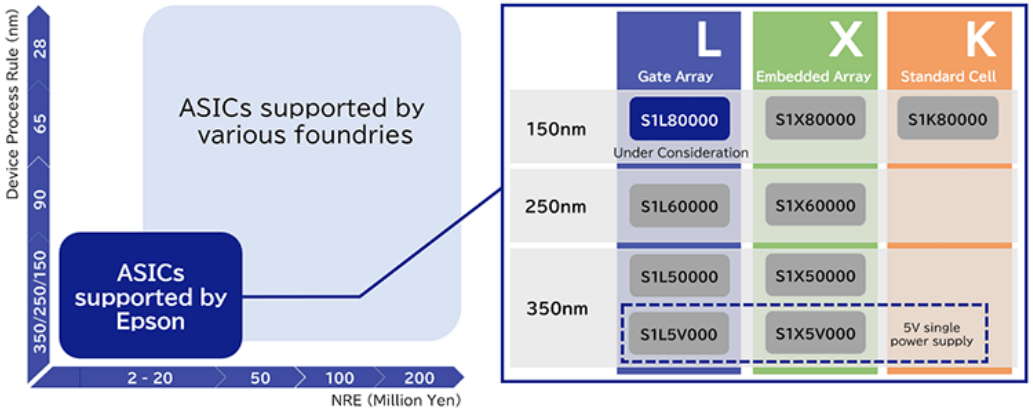
■ Key features

・Started ASIC business on 1982, have many design experiences and shipment records.

・Various lineup of Gate array/Embedded array/Standard cell

・Have own fabs and provide IDM solution from design to production and testing.



■ Major usage

・Reproduction of discontinued ASIC or PLD(FPGA, CPLD)

・Redevelopment to respond to market supply constraints or price increase

・Custom IC development which cannot realize by standard MCU or PLD
(ex. Constraints of Supply voltage, size, power consumption…)

■ Application examples

・Product which required long product lifecycle

・Industrial applications
(PLC, Industrial displays, Servo, Inverter, CNC, etc.)

・Measurement instruments

2. Product features

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Free pin assignment

Realize pin-to-pin compatible when you replace from discontinued IC

5V single power operation

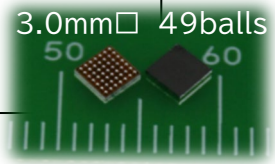
Suitable for legacy system or products which require noise immunity.

Wide range voltage operation

Can operate at different voltage level with single products. (i.e. 3.3V and 5V, or 2.0V and 3.3V)

Small package support

4mm□～ VFBGA/SQFN
2.4mm□～ WL-CSP
Suitable for small products



Power supply separation

・I/O：Can interface between different voltage devices
・Core：Realize low power operation or battery backup

Power consumption measurement

Can measure actual developed ASIC power consumption with LSI tester to compare with original IC.(Optional)

Customization of I/O characteristics

Customize DC, AC characteristics of I/O to support original IC’s interface standard.(Optional)

LVDS IO

Tx and Rx can be installed in pairs.
Wide amplitude low-voltage differential signaling (WA-LVDS) is available.

※Contents of this slide differ for each ASIC series.

2. Product features: Series lineups

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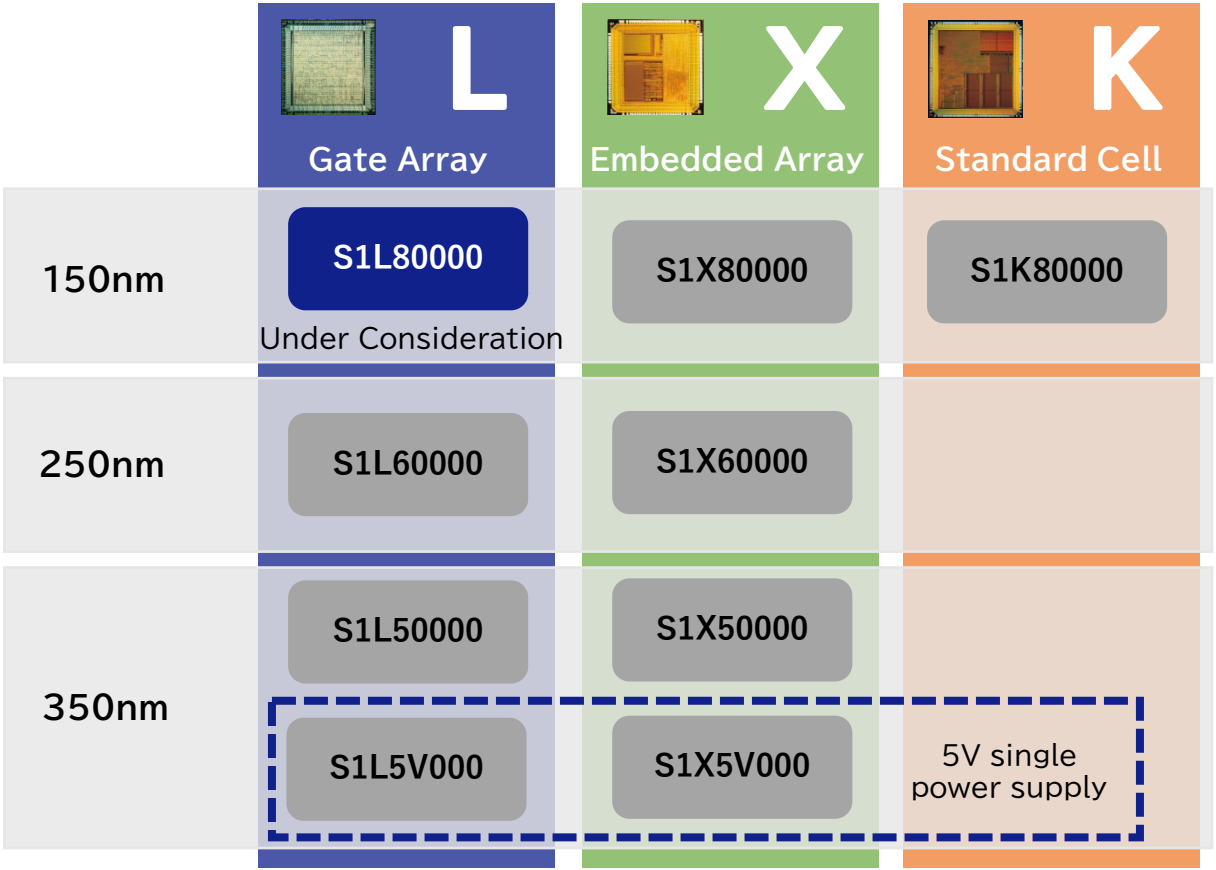

Macro cells
For E/A, S/C

PLL
- 32kHz -> 200MHz
- 5MHz -> 200MHz

SRAM
- 1-port
- 2-port (1R+1W)
- Dual port (2R+2W)

ROM
- 1k to 256k-bit
- 1k to 512k-bit/0.15um

LVDS
- FPD-Link
- LVDS-IO
- (Wide Amplitude LVDS)

2. Product features: Target of replacement

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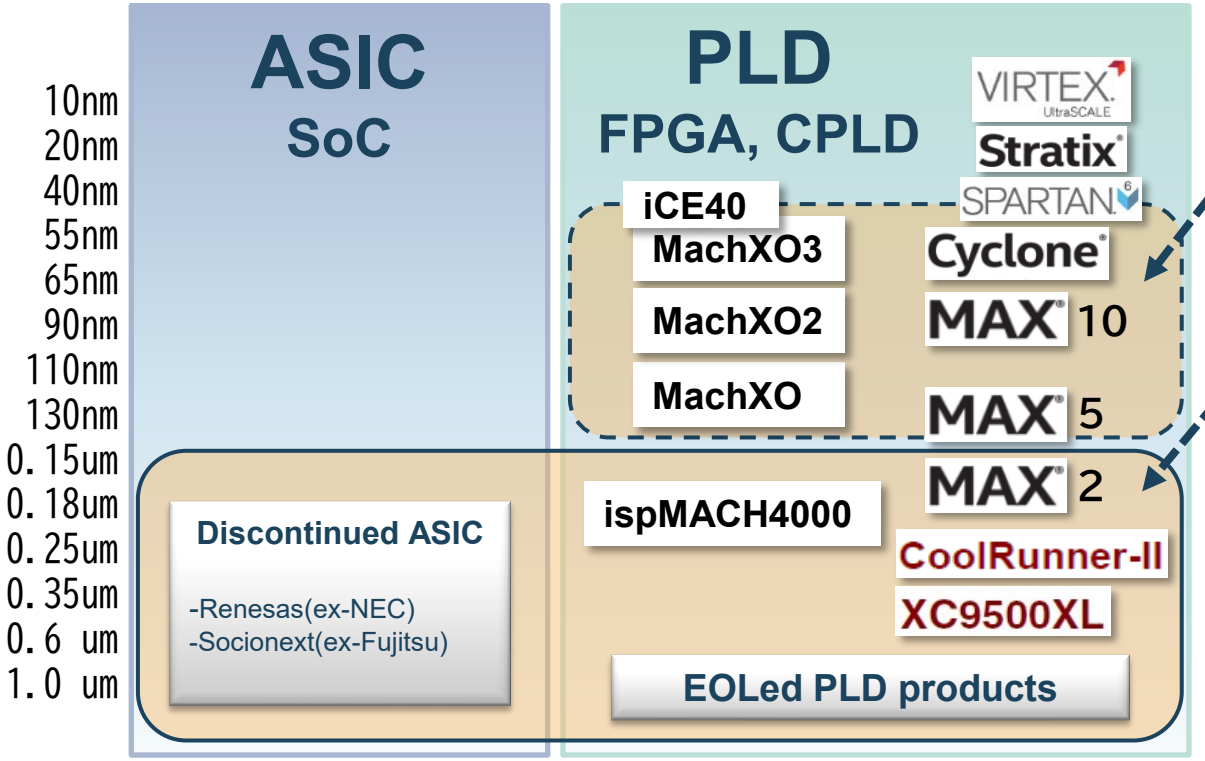

Able to replace depending on actual usage of PLD(logic size, IP etc.)

Target of Epson ASIC

- User logic size : ~800k gates
- Pins : ~280
- Supply voltage : 5V~1.8V

0.15um	S1X80000/S1K80000
0.25um	S1L60000/S1X60000
0.35um	S1L50000/S1X50000
	S1L5V000(5V single)

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3. Use case examples: Reproduction of discontinued ASIC

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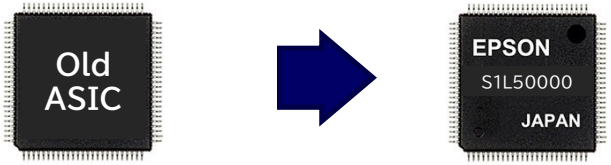
Realize short development time with low cost NRE

・Reproduction of discontinued IC



Other vendors discontinued ASIC　　Epson ASIC

・Power supply voltage, pin assignment, function compatible
・Can adjust I/O characteristics to be the same as original IC
・Design support for low power consumption, and verify by the measurement of actual sample.
・Can support legacy system which require 5V power supply
・Not only just copy original, re-development with additional function

3. Use case examples: Replacement from PLD to ASIC

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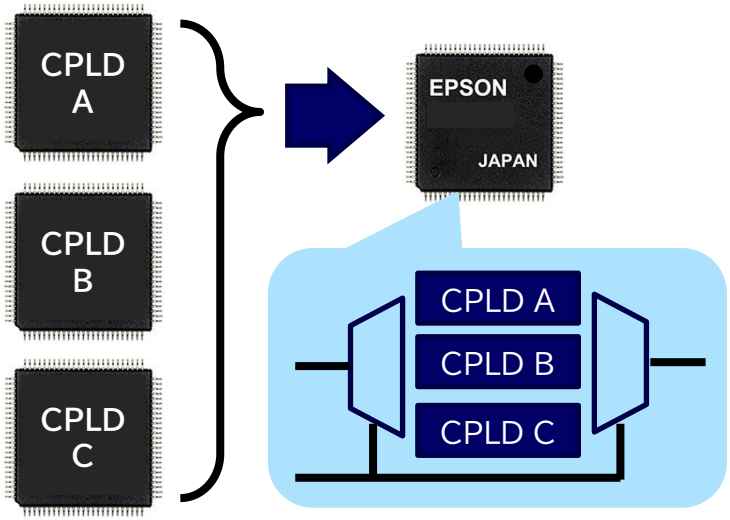
・Reproduction for EOLed PLD　・Replacement due to supply issues

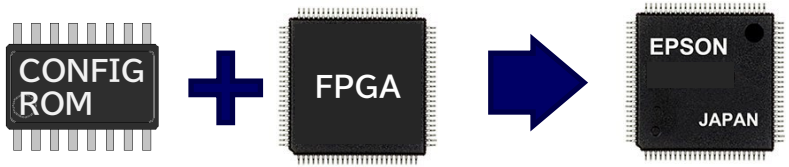
➡Solution for the stable supply and improving profitability

Multiple CPLDs into one ASIC



CPLD A/B/C selection is realized by PKG bonding option or dedicated external signal

FPGA to ASIC



FPGA
I/O 3.3V/
Core 1.2V

ASIC
3.3V
w/o 1.2V

footprint compatible
without config ROM
without 1.2V Power supply

3. Use case examples: Actual replacement projects

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Replacement target		ASICs	Packages
Low-cost FPGA	Spartan	S1L5V042 S1L51253 S1L60284 S1X50000	P-LQFP100-1414-0.50 P-LQFP100-1414-0.50 P-TQFP080-1212-0.50 P-TQFP128-1414-0.40
Low-cost FPGA	Cyclone	S1L50553 S1X50000	P-LQFP144-2020-0.50 P-LQFP100-1414-0.50
Small-size FPGA	MAX10	S1L5V254	P-LQFP080-1212-0.50
CPLD	MAX2 MAX5	S1L50552 S1L50282	P-LQFP144-2020-0.50 P-TQFP100-1414-0.50
CPLD	MACH	S1L5V012 S1L50122 S1L50282 S1L50552	P-LQFP048-0707-0.50 P-TFBGA-096-0606-0.50 P-LQFP100-1414-0.50 P-LQFP144-2020-0.50
Low-cost FPGA Small-size FPGA		S1L80000	*Planning new product:* *0.15um Gate array S1L80000 series*

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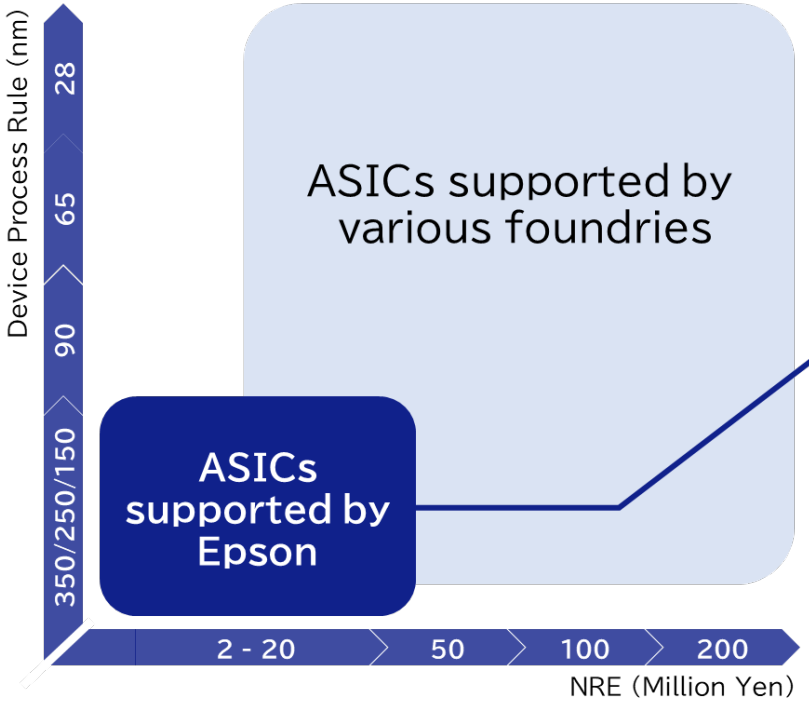
3. Use case examples: NRE images



	L Gate Array	X Embedded Array	K Standard Cell
150nm	S1L80000 Under Consideration	S1X80000	S1K80000
250nm	S1L60000	S1X60000	
350nm	S1L50000	S1X50000	
	S1L5V000	S1X5V000	5V single power supply

Gate Array	2~ Million Yen
Embedded Array	10~ Million Yen
Standard Cell	20~ Million Yen

4. New product idea: S1L80000 series (0.15um Gate Array)

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- New Gate Array product idea to replace existing PLD, now under planning
- Can realize 0.15um ASIC with cheaper NRE, and able to support reasonable MOQ

tentative	*S1L8010*	*S1L8020*	*S1L8030*
Usable gates 4LM	120K	230K	400K
Usable gates 5LM	135K	255K	450K
Usable pads	100	180	248
Available PKG examples Line up	QFP48, 64, 100 VFBGA5H-81 VFBGA6H-121	QFP48, 64, 100, 144 VFBGA6H-121 PFBGA10U-121	QFP64, 100, 144, 208, 256 PFBGA14U-256 PBGA1UE256
Power supply voltage	Dual: Core 1.8V, I/O 3.3V Single: 3. 3V	Dual: Core 1.8V, I/O 3.3V	Dual: Core 1.8V, I/O 3.3V
Target operating frequency	Dual: 120MHz, Single: 40MHz	Dual: 120MHz	Dual: 120MHz
LDO w/external capacitor	Core 1.8V up to 30mA	-	-
PLL 5M->200MHz	1pc	2pcs	2pcs
Embedded SRAM	-	-	DP-RAM: 16b x 256w x 24pcs
LVDS-IO	-	Tx 4pairs/Rx 4pairs	Tx 8pairs/Rx 8pairs
Device characteristics S1X80000	Internal gate delay: 34.5ps/1.8V 2-input NAND Typ. Power consumption: 0.063uW/MHz/gate 2-input NAND typ. Drivability of output buffer: IOL=2, 4, 8, 12mA at 3.3V		
Others	Gate array configurable SRAM 1port/2port, OSC buffers for external x' tal		

4. New product idea: Features of LVDS-Tx

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◆ Epson's proprietary LVDS transmitter

WA-LVDS Wide Amplitude LVDS

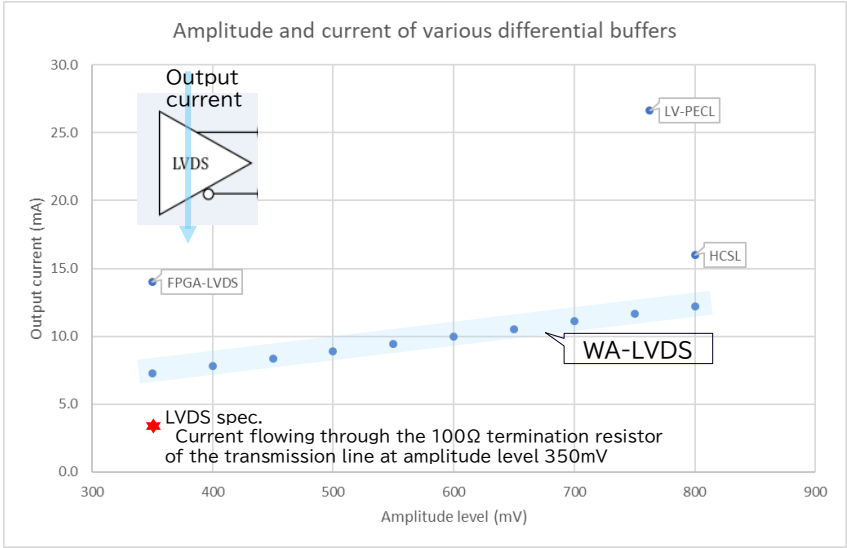
News Release　Technical Note

Supports
B-LVDS(Bus LVDS), M-LVDS(Multipoint LVDS)

Graph showing characteristics
(@100MHz, typical conditions, not guaranteed values)
X-axis: Amplitude level (mV)
Y-axis: Output current (mA)
FPGA-LVDS, WA-LVDS, HCSL, LV-PECL

When the differential output amplitude level is 350mV current consumption of each output buffers
FPGA-LVDS 2.5V　35mW/2.5V=14mA
(Reference values based on the power consumption estimate sheet published by a PLD supplier)
WA-LVDS　7.25mA (Simulation value)

Item	Specification
Power supply	3.3V±0.3V
Amplitude voltage	350~800mV 10 step setting
Offset voltage	0.9, 1.25, 1.5, 1.65V 4 step setting



4. New product idea: PLD examples for package compatible

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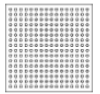
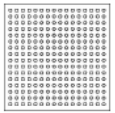
QFP15-100PIN P-LQFP100-1414-0.50	Lattice TQFP	LCMXO	LCMXO256	LCMXO640	LCMXO1200	LCMXO2280		
		LCMXO2	XO2-256	XO2-640	XO2-1200	XO2-2000		
	Intel TQFP	MAX II	EPM240	EPM570				
		MAX V	5M80Z	5M160Z	5M240Z	5M570Z		
QFP20-144PIN P-LQFP144-2020-0.50	Lattice TQFP	LCMXO	LCMXO640	LCMXO1200	LCMXO2280			
		LCMXO2	XO2-640U	XO2-1200	XO2-2000	XO2-4000	XO2-7000	
		ECP5	LFE5U-12	LFE5U-25	LFE5U-45			
	Intel TQFP	MAX II	EPM570	EPM1270				
		MAX V	5M240Z	5M570Z	5M1270Z			
		MAX 10	10M02SC	10M04SC	10M08SC	10M16SC	10M25SC	10M40SA 10M50SA
		Cyclone10	10CL006	10CL010	10CL016	10CL025		
		Cyclone4	EP4CE6	EP4CE10	EP4CE15	EP4CE22		
	AMD TQG	Spartan-6	XC6SLX4	XC6SLX9				
VFBGA6H-121 P-VFBGA-121-0606-0.50	Lattice csfBGA	LCMXO3	XO3L-640	XO3L-1300	XO3L-2100	XO3L-4300		
		iCE40 LP	LP1K					
PFBGA14U-256 P-TFBGA-256-1414-0.80	Lattice caBGA	LCMXO	LCMXO640	LCMXO1200	LCMXO2280			
		LCMXO2	XO2-2000	XO2-4000	XO2-7000			
		LCMXO3	XO3L-1300	XO3L-2100	XO3L-4300	XO3L-6900	XO3L-9400	
		ECP5	LFE5U-12	LFE5U-25	LFE5U-45			
		iCE40 HX	HX8K					
	Intel UBGA	Cyclone10	10CL006	10CL010	10CL016	10CL025		
		Cyclone4	EP4CE6	EP4CE10	EP4CE15	EP4CE22		
PBGA1UE256 P-LBGA-0256-1717-1.00	Lattice ftBGA	LCMXO	LCMXO640	LCMXO1200	LCMXO2280			
		LCMXO2	XO2-1200U	XO2-2000	XO2-4000	XO2-7000		
	Intel FBGA	MAX II	EPM1270	EPM2210				
		MAX V	5M570Z	5M2210Z	5M1270Z			
		MAX 10	10M04DA	10M08DA	10M16DA	10M25DA	10M40DA	10M50DA
		Cyclone V	5CEBA2	5CEBA4				
		Cyclone4	EP4CE6	EP4CE10	EP4CE15	EP4CE22		
	AMD FTG	Spartan-6	XC6SLX9	XC6SLX16	XC6SLX25			

PKG Type		Body Size (mm)	Lead Pitch (mm)
QFP15-100PIN		14 x 14 x 1.7	0.5
QFP20-144PIN		20 x 20 x 1.7	0.5

PKG Type		Body Size (mm)	Ball Pitch (mm)
VFBGA6H-121		6 x 6 x 1.0	0.5
PFBGA14U-256		14 x 14 x 1.2	0.8
PBGA1UE256		17 x 17 x 1.7	1.0

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5. Others: ASIC Design interface

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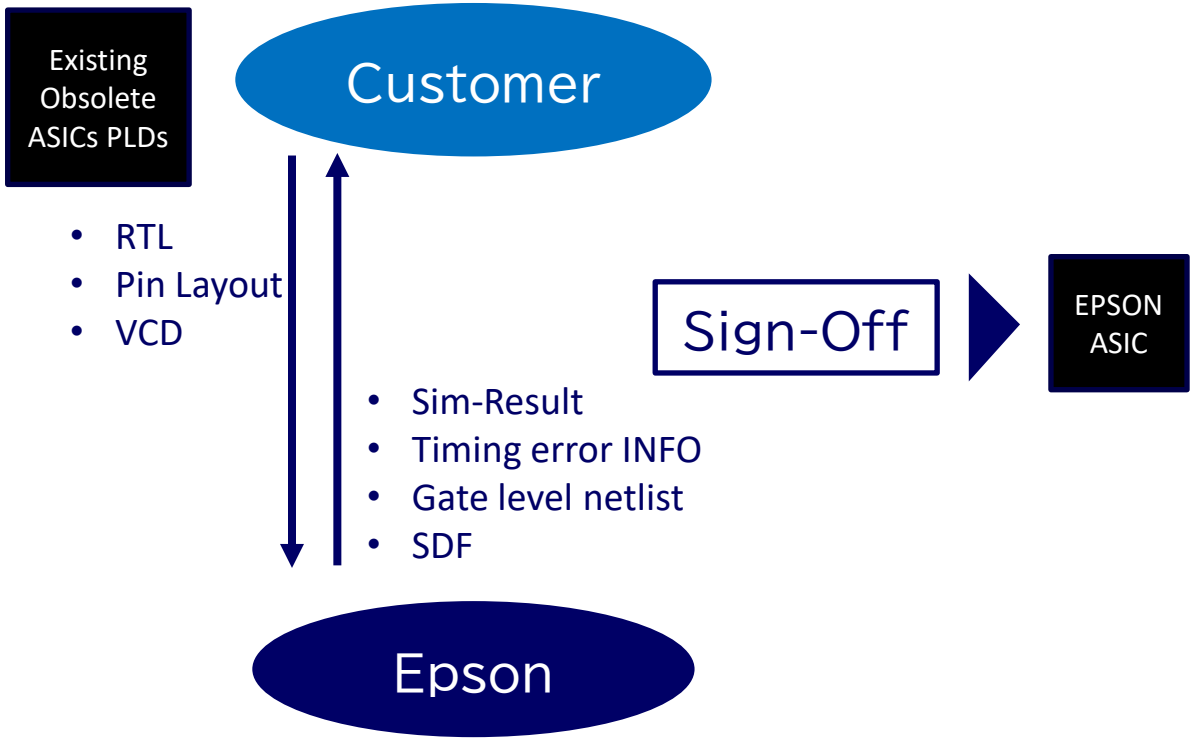
Users only need to send us RTL and VCD files of simulation results obtained with their test bench.



5. Others: ASIC website

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ASIC top page

https://global.epson.com/products and drivers/semicon/products/asic/

ASIC Development Interface

https://global.epson.com/products and drivers/semicon/products/asic/development.html

Pamphlet PDF 32MB

https://global.epson.com/products and drivers/semicon/pdf/id000456.pdf

5. Others: Fab location

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Wafer Process

Wafer Size	Technology	Capacity (wf/month)	Location	Operation Start
8 inch (T wing)	0.15 - 0.35 µm	25K	Tohoku Epson Corp.	1997
6 inch (S wing)	0.35 - 1.2 µm	20K	Tohoku Epson Corp.	1991


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TEG outline specifications

EPSON

ASIC
S1L80305

PKG
PFBGA14U-256 14x14 0.8mm ball pitch

Power supply
3.3V 1.8V dual power supply

Usable logic gates
400K gates

LVDS
RX 5ch left + 3ch right
TX 3ch left + 5ch right **Wide Amplitude-LVDS**

PLL
IN 25MHz/OUT 100MHz

SRAM
Dual Port 256word x 16bit x 24 total 約12KBytes

Target PLD example
LCMXO3L-4300C-5BG256I