EPSON
EXCEED YOUR VISION

QFN
Package Mount Manual

This manual describes notes on using Epson QFN products. It is the responsibility of the customer to optimize the process to obtain the desired results.

Rev.1.0

SEIKO EPSON CORPORATION

NOTICE

The content of this document is subject to change without notice.

1. This document may not be copied, reproduced, or used for any other purpose, in whole or in part, without the consent of Seiko Epson Corporation (“Epson”).
2. Before purchasing or using Epson products, check with our sales representative for the latest information. Always consult Epson web site or other sources for the latest information.
3. Information provided in this document is for reference only. Epson makes no guarantees against any infringements of or damages to a third party intellectual property rights or any other rights resulting from the information. Epson does not give any licenses to use the intellectual property rights or any other rights of a third party or Epson under this document.
4. When using Epson products, evaluate mounting and soldering thoroughly, and use the Epson products within the guarantee range specified by Epson. Epson shall have no liability for malfunctions, accidents resulting in injury or death, fire accident or social damages arising out of the use of Epson products beyond such specified by Epson.
5. Epson has prepared this document carefully and accurately as much as possible, but Epson does not guarantee that the information presented herein is error-free. Epson assumes no responsibility for any damages caused by the customers resulting from information errors in this document.
6. Epson products listed in this document and their associated technologies may not be used in equipment or systems that are prohibited to manufacture, use or sell under the laws, regulations, or rules in Japan or any other countries. Furthermore, Epson products and their associated technologies may not be used for the development, etc., of weapons of mass destruction, for military uses, or other military applications. If exporting Epson products or their associated technologies, be sure to comply with the Foreign Exchange and Foreign Trade Control Act in Japan and other export-related laws and ordinances in Japan and any other countries. And follow the required procedures as provided by the relevant laws and ordinances.
7. Epson assumes no responsibility if our products are used in violation of conditions listed in this document and such use results in damage.
8. For details of environmental compatibility etc. of Epson products, check Epson's web site.
9. Epson assumes no responsibility if our products' failure or characteristic fluctuation occurs due to external factors (electrostatic breakdown ESD, overvoltage / overcurrent EOS, thermal stress, mechanical stress, environmental atmosphere) in the product handling, mounting, and customer's process.

   Also, follow the conditions of individual specifications such as storage time before opening, storage time after opening, etc. for products that require moisture-proof packaging.

Table of Contents

1. Outline 5

1.1 QFN Package Structure 5

1.2 QFN Photo 5

1.3 QFN Line-up 6

1.4 Wettable Flank QFN (Option) 7

2. Soldering 8

2.1 Surface Mount Technology 8

2.2 Reflow Soldering Process flow 9

3. PCB Design Guide 10

3.1 Precautions for PCB Design 10

3.2 Land Pattern and Solder Resist Design, NSMD and SMD 10

3.3 PCB Land Pattern Design 11

3.4 PCB Land Design for Exposed Die Pad 12

3.5 PCB Land Surface Treatment 13

3.6 PCB Warp 13

4. Solder Printing 14

4.1 Solder Paste 14

4.2 Stencil Design 15

4.2.1 Stencil Design for Exposed Die Pad 16

4.3 Solder paste supply 17

4.4 Squeegee 17

4.4.1 Polyurethane Rubber Squeegee 17

4.4.2 Metal Squeegee 17

4.4.3 Plastic Squeegee 17

4.5 Solder Printing 18

5. Mounting 19

5.1 Precautions for Mounting QFN 19

5.1.1 Taking out from Carrier Tape or Tray 19

5.1.2 Mounting on PCB 19

6. Reflow Soldering 20

6.1 Reflow Soldering Oven 20

6.1.1 Preheating Zone 20

6.1.2 Reflow Zone 20

6.1.3 Cooling Zone 20

6.2 Reflow Profile 21

6.3 Recommended Reflow Soldering Conditions 22

7. Cleaning 23

7.1 Cleaning after QFN Soldering 23

7.2 General PCB Cleaning 23
7.2.1 PCB Cleaning 23
7.2.2 Cleaning Method 23
7.2.3 Water Cleaning 23
7.2.4 No Cleaning 23
7.3 Others 23
8. Rework 24
9. General Precautions for Use of Semiconductor Devices 25
9.1 Introduction 25
9.2 Storage 25
9.3 Design and Handling 25
Revision History 27

1. Outline

QFN (Quad Flat Non-leaded package) is a "Peripheral package", and has terminal pads along the four edges of the bottom and side surface. Unlike the QFP (Quad Flat Package) which is also peripheral package, connection terminals of the QFN do not protrude outside the package. QFN has a smaller mounting area and thinner package thickness than QFP, so QFN is a compact package suitable for high-density application.

Epson QFN is SQFN (Saw singulation QFN) which singulation is done by saw dicing method after molding process. In the molding process, multi-chip substrate is molded by using a single mold cavity. This process is called mold-array process (MAP).

Also, if you want to improve the visibility of the visual inspection after soldering, wettable flanks QFN is prepared as an option. Regarding wettable flanks QFN, please see Section 1.4.

1.1 QFN Package Structure

QFN has a structure in which one surface of the die pad of the copper lead frame is exposed. This exposed part is called Exposed Die Pad (Ex-DP), and the electric potential of the silicon substrate of the IC chip is connected externally through Ex-DP.

By soldering this Ex-DP to the PCB, it becomes possible to improve the electric potential stability of the IC chip, the heat dissipation characteristics of the package and the solder joint strength.

Consideration of the electric potential of the mounting PCB land is necessary when QFN Ex-DP is to be connected to the PCB. Also, even in the case of no connection of Ex-DP, attention must be paid to the PCB wiring under Ex-DP area. Please refer to Section 3.4 "PCB Land Design for Exposed Die Pad".

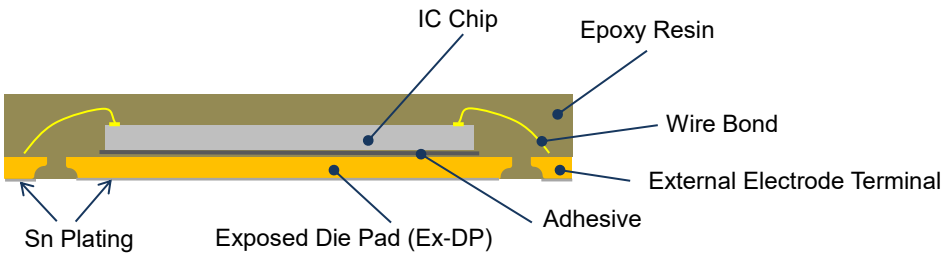
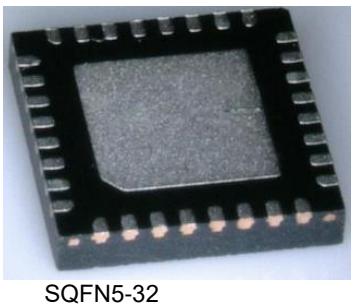


Fig 1.1 QFN Package Structure

1.2 QFN Photo

SQFN6-36

Fig 1.2 Package Top Surface



SQFN5-32

Fig 1.3 Package Bottom Surface

1.3 QFN Line-up

The table below shows Epson's standard line-up for QFN package. For detailed specifications, dimensions, and package drawings, please refer to our website, brochure, delivery specifications, and/or package outline drawing.

Table 1.1 QFN Package Lineup *1)

QFN Type	Package body size	Pin count	Pin pitch *2)	Package name
SQFN4	4mm□ t=1mm	16pin	0.65mm	SQFN4-16
		24pin	0.50mm	SQFN4-24
		32pin	0.40mm	SQFN4-32
SQFN5	5mm□ t=1mm	32pin	0.50mm	SQFN5-32
SQFN6	6mm□ t=1mm	36pin	0.50mm	SQFN6-36
SQFN7	7mm□ t=1mm	48pin	0.50mm	SQFN7-48
SQFN9	9mm□ t=1mm	64pin	0.50mm	SQFN9-64
		76pin	0.40mm	SQFN9-76
		80pin	0.40mm	SQFN9-80

*1) Some packages have the wettable flanks structure as an option. Please consult with Epson sales if necessary.
*2) The repeated pitch of external electrode terminals.

1.4 Wettable Flank QFN (Option)

Since Epson QFN singulation is done by saw dicing method, the copper surface is exposed at the side of the package. For this reason, depending on the storage environment of QFN and/or the conditions during soldering of the PCB, solder fillets may not be formed on the package side electrode terminal due to the copper oxide film on the package side electrode terminal. To obtain stable solder fillets on the package side electrode terminal, Epson has wettable flanks QFN option.

Epson wettable flanks QFN has tin (Sn) plating on package side electrode terminals, so forming of solder fillets is easier during soldering time, and it is possible to obtain the following merits. *1)

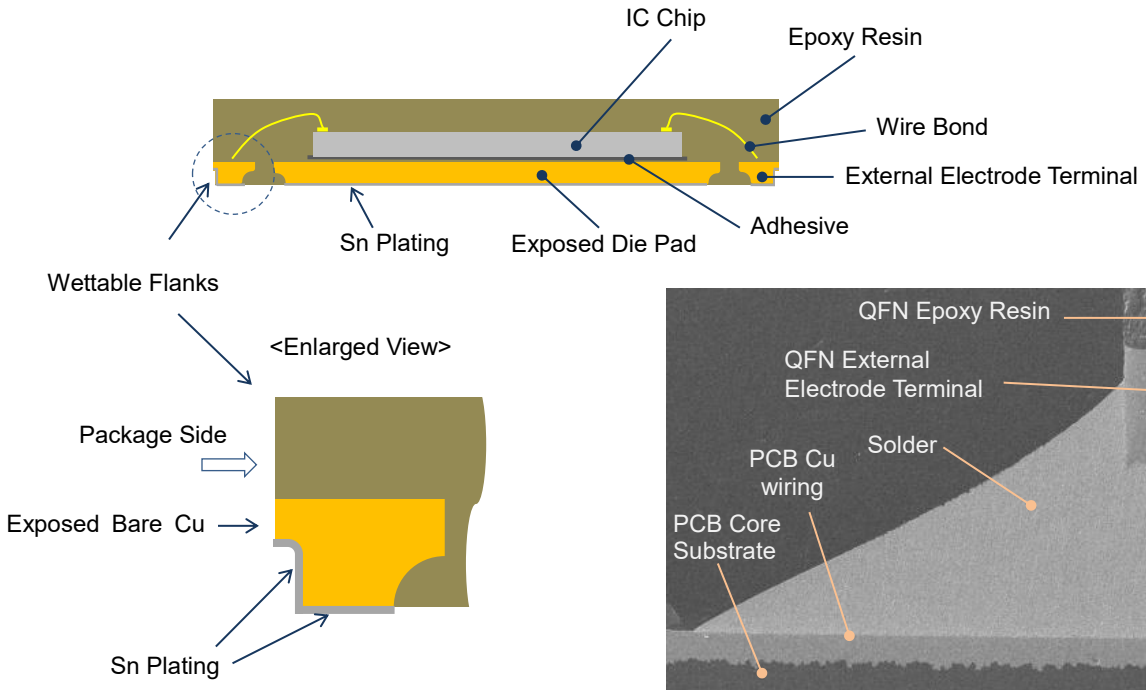


Fig 1.4 Wettable Flanks Sectional View

Fig 1.5 Sectional View after Soldering (SEM)

(1) Wettable flanks will facilitate solder wetting on the side of the package, making it easier to obtain a three-dimensional solder connection structure between PCB land and the sides of the QFN terminals.

(2) Wettable flanks are modifications to the fully-exposed terminal ends, which promote solder wetting for the formation of a solder fillet. With the solder fillet, automatic visual inspection (AVI) can be applied for the inspection of soldering quality.

*1) The solder fillets obtained by wettable flanks may not be in ideal shape because of the package storage condition and/or soldering parameter setting. Obtaining the ideal fillets shape cannot be guaranteed only by using the wettable flanks. Please perform sufficient evaluation and set appropriate parameters by the customer.

2. Soldering

2.1 Surface Mount Technology

As the soldering method for QFN package that is one of the surface mount devices (SMD), reflow process is recommended generally. Reflow process is as follows. Firstly solder paste is printed on PCB, then surface mount devices are mounted on the PCB, and then the PCB with SMD is soldered by the heat of a reflow oven. This technology is called “Surface mount technology” (SMT), and SMT is generally used for SMD. Reflow heating methods include infrared (IR) method, hot air method (convection method), infrared (IR) hot air combined method, hot plate method, and so on.

In the reflow soldering process, SMD soldering accuracy does not depend on SMD mounting accuracy. Soldering accuracy depends on solder self-alignment by the solder surface tension. *1) Therefore, when designing PCB, it is necessary to design the land and PCB considering the characteristics of this self-alignment function.

For QFN package soldering, hot air method or IR hot air combined method is recommended. If only IR is used, solder and the terminals on the bottom surface of the QFN are hard to obtain enough heat for soldering, because IR might be blocked by the molded package body, especially for large size QFN packages.

*1) Solder self-alignment: A certain level of SMD mounting shift will be corrected by the solder surface tension force during reflow soldering. Solder self-alignment depends on the solder surface tension force and package weight, so it’s effective for light packages. But solder self-alignment effect might not occur, when there is a huge offset between PCB land and QFN terminal.

2.2 Reflow Soldering Process flow

The table below shows the typical and most regular used reflow soldering process flow for QFN package soldering.

Table 2.2 Reflow Soldering Process Flow

	Process	Material	Machine, Jig, etc.
1	**Printing** [Chapter 4]	PCB [Chapter 3] Solder paste [Section 4.1, 4.3]	Printing machine Stencil [Section 4.2] Squeegee [Section 4.4]
(2)	(Printing inspection)	———	Inspection unit SPI
3	**Mounting** [Chapter 5]	SMD QFN, Chip components, Connector, etc.	SMD mounter
4	**Reflow soldering** [Chapter 6] Preheating [Section 6.1.1] Reflow [Section 6.1.2] Cooling [Section 6.1.3]	PCB after SMD mounted.	Reflow oven Reflow profile [Section 6.2] N2 gas
5	**Cleaning** [Chapter 7]	PCB after soldering.	Cleaning machine Cleaner
(6)	(Function test)	———	In-circuit tester
(7)	(Visual inspection)	———	Inspection unit AVI

* For details of each process, please refer to the explanation page.
(2), (6) and (7) are the inspection process, so explanation is omitted.

3. PCB Design Guide

3.1 Precautions for PCB Design

There are two types of PCB mounting pad, Non-Solder Mask Defined (NSMD) and Solder Mask Defined (SMD).

In general, it is said that the solder joint strength of NSMD is higher than that of SMD, because in NSMD, solder joint exists not only land pattern surface but also land pattern side wall. But sometimes solder printability for SMD is better than that for NSMD because of printing parameter and/or stencil design. So please select NSMD or SMD according to the application.

3.2 Land Pattern and Solder Resist Design, NSMD and SMD

In NSMD, land size is defined by the land pattern size. And in SMD, land size is defined by the solder resist opening size.

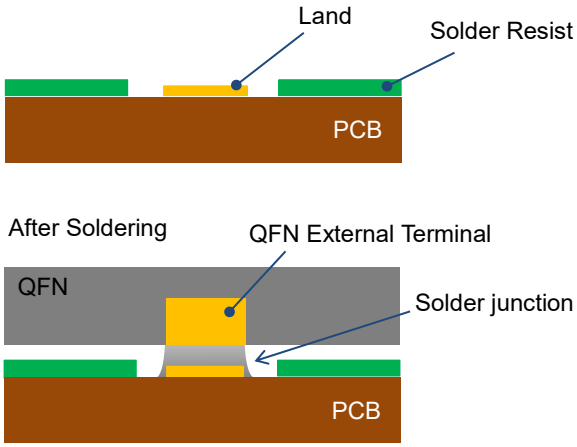


Fig. 3.1 NSMD Sectional View

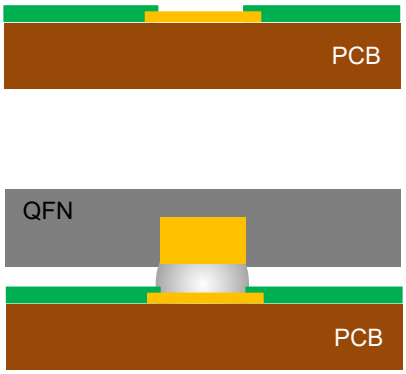


Fig. 3.2 SMD Sectional View

Table 3.1 (Reference) Joint Strength Comparison of NSMD and SMD

Joint strength between land and PCB *1)	**NSMD <= SMD**
Joint strength between land and solder *2)	**NSMD >= SMD**

*1) As the land pattern is covered by solder resist, joint strength between land and PCB of SMD is higher than that of NSMD.

*2) As solder covers not only land pattern top surface but also land pattern side wall, joint strength between land and solder of NSMD is higher than that of SMD.

3.3 PCB Land Pattern Design

Regarding PCB land pattern design for QFN, please refer to the figure below and the table below. (Conforming to JEITA ED-4702C)

However, since Epson QFN has Exposed Die Pad (Ex-DP), in order to prevent solder bridges and electrical short-circuit (including migration) between the Ex-DP and the PCB electrode lands, it is recommended to design with L2 and L_{DP} equal to zero.

As these problems are also affected by the amount of solder paste and the printing area, customers should perform a comprehensive mounting evaluation to finalize the dimensions.

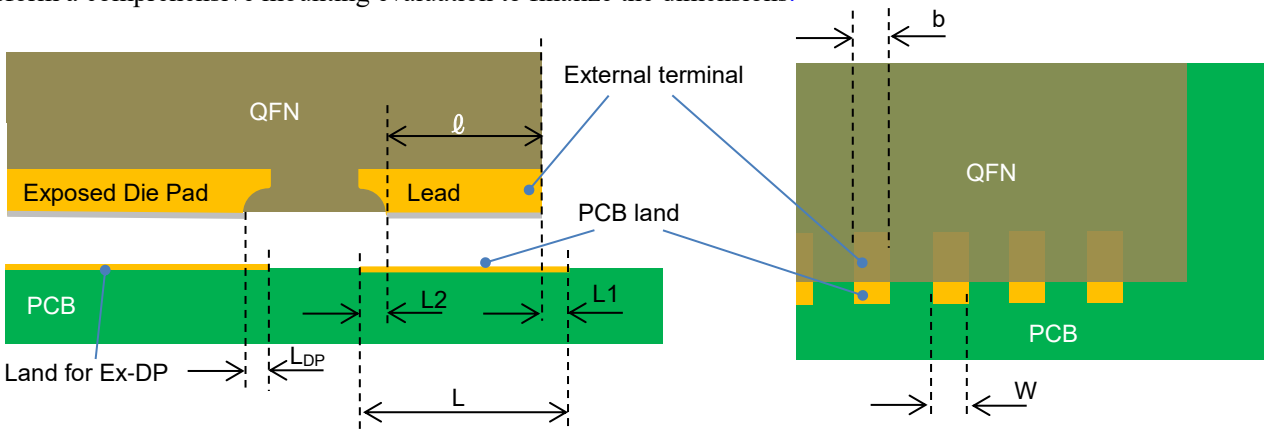


Fig. 3.3 PCB Land Design

Table 3.2 PCB Land Design

Symbol	Item	Reference dimension *1)
ℓ	Package external lead length	Refer to package outline drawing
b	Package external lead width	Refer to package outline drawing
L	PCB mount land length	ℓ+L1+L2
L1	———	0.30±0.05
L2	———	0.00
W	PCB mount land width	b±0.05
L_{DP}	———	0.00

*1) Dimensions are for reference only.

3.4 PCB Land Design for Exposed Die Pad

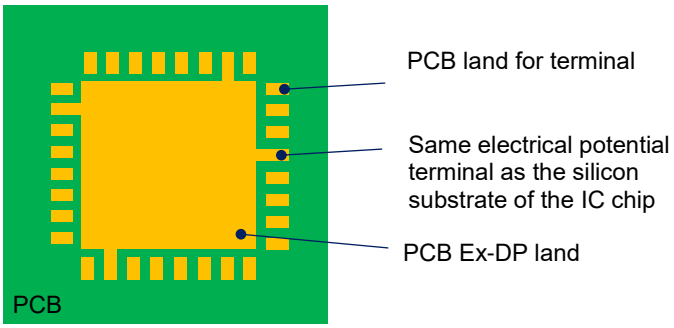
In Epson QFN, the electric potential of the silicon substrate of IC chip inside the package is exposed externally through Exposed Die Pad (Ex-DP). Therefore, depending on the PCB design for the Ex-DP land, IC may not function correctly. Based on the electrical potential specification of Ex-DP of the product, please design the Ex-DP land appropriately.

For the electrical potential specification of Ex-DP, please refer to the technical manual, delivery specification or consult with Epson sales staff.

Proper design of Ex-DP connection to the PCB is crucial to stabilize the electric potential of the IC chip, reduce the noise (EMI/EMC) and improve the heat dissipation characteristics.

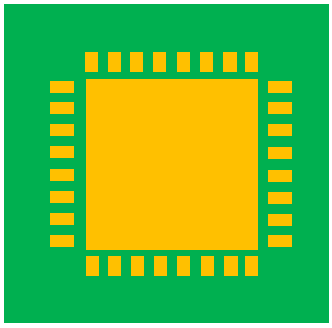
Table 3.3 Precautions for PCB Land Design for Exposed Die Pad

Exposed die pad connection	Precautions
In the case of connecting Ex-DP to PCB land by solder. Refer to Fig.3.4 and Fig.3.5	Design the PCB so that PCB's Ex-DP connection land has the same electrical potential as the silicon substrate potential of the IC chip. Or, design without electrical connecting. The connection between different electrical potential may lead to electrical short, high leak current and other problem.
In the case of no soldering Ex-DP to PCB land. Refer to Fig.3.6	Please do not design electrical wiring on the PCB under the Ex-DP of QFN. Unexpected foreign object intrusion may cause leakage current and/or migration between Ex-DP and PCB.



*) Connect Ex-DP land to the same electrical potential terminals as the silicon substrate of the IC chip

Fig. 3.4 (Example) Ex-DP Connection Land



*) Not connecting Ex-DP land to the terminals

Fig. 3.5 (Example) Ex-DP Open Land

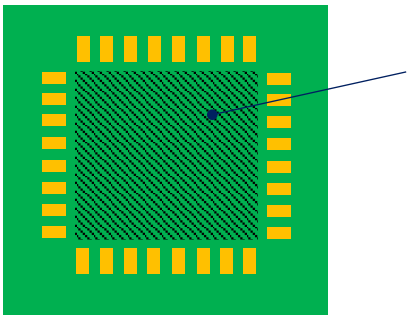


Fig. 3.6 Land Design for Ex-DP without Soldering

3.5 PCB Land Surface Treatment

Leaving PCB in the atmosphere might oxidize the land surface of PCB, and this oxidation may affect the solder wettability during soldering. It is better to use protective film coating or plating to prevent this oxidation. In general, Organic Solderability Preservatives (OSP) and Ni/Au plating are used for PCB land surface oxidation prevention treatment. So adoption of these treatments is strongly recommended.

3.6 PCB Warp

Solder connection between the component and the PCB may not be obtained or the solder joint reliability may be adversely affected, if the warp of the PCB is large during and after reflow. In the PCB designing, please select the material with high warpage resistance, and equalize the ratio occupied by the conductor on each layer of the PCB.

Additionally, in PCB components layout design, please do not place SMD including QFN near the place with stress concentration during soldering and actual use. Stress concentration places are, for example, in the vicinity of switches and connectors, on the backside of switches and connectors, and the movable part such as the hinge.

4. Solder Printing

4.1 Solder Paste

Solder paste consists of solder particles, flux, surfactant, thixotropic agent and so on. Since there are many kinds of solder paste, for each solder paste it is necessary to determine the reflow temperature profile individually.

The composition and size of the solder particles in the solder paste are determined depending on the application, mount land pitch and so on. Solder paste with narrow particle distribution has better soldering stability.

Full attention is required for selecting the particle size of solder paste. Smaller solder particle tends to have surface more oxidation during storage, printing and reflow. This may worsen the solder wettability.

In addition, please refer to the above and select a suitable solder paste based on the result from sufficient evaluation of solder wettability, the state of generation of intermetallic compounds and so on.

Table 4.1 (Reference) Solder Paste Structure

Component	Function
Solder particle	As the solder particles melt and the solder wetting progresses, the solder particles in solder paste and the solder plating of QFN terminals melt together uniformly. As a result, electrical connection and mechanical joint strength are obtained after cooling.
Flux	Flux reduces the oxide film on each terminal surface, and prevents re-oxidation of the solder surface during reflow heating, and accelerates molten solder fluidity.
Surfactant	The surfactant is added a small amount to mix the flux, solder and other components uniformly.
Thixotropic agent	Thixotropic agent is added to the solder paste to keep the shape of the solder paste after printing and to hold the mounted components.

Table 4.2 (Reference) Solder Melting Point

Solder paste composition	Melting temperature (°C)		
	Solidus	Peak temperature *1)	Liquidus-line
Sn - 3.5Ag - 0.75Cu	218	219	219
Sn - 3.0Ag - 0.5Cu	217	219	220
Sn - 1.0Ag - 0.5Cu	217	219	227

*1) Peak temperature: Temperature at the maximum heat absorption point of DSC curve.

4.2 Stencil Design

Since the design of the stencil greatly affects the SMT process quality (solderability, standoff, solder bridge and so on), proper stencil design is necessary. The volume and stability of solder paste to be transferred to PCB is determined by the design of stencil specifications, such as stencil thickness, opening size for solder filling, planar shape and cross-sectional shape.

In typical solder printing process, to obtain the stable solder paste transfer volume, stencil property such as small physical variation material and excellence stencil releasing after solder printing should be selected. Also, when mounting multiple SMDs, special attention is required on designing for printing stencil due to optimum solder paste volume and thickness that might be different in each component.

Excessive or insufficient and unstable of solder paste might occur, if the selection of stencil property and design are incorrect. This causes defective solder joint. Stencil selection and design based on the sufficient evaluation of mounting and soldering are necessary.

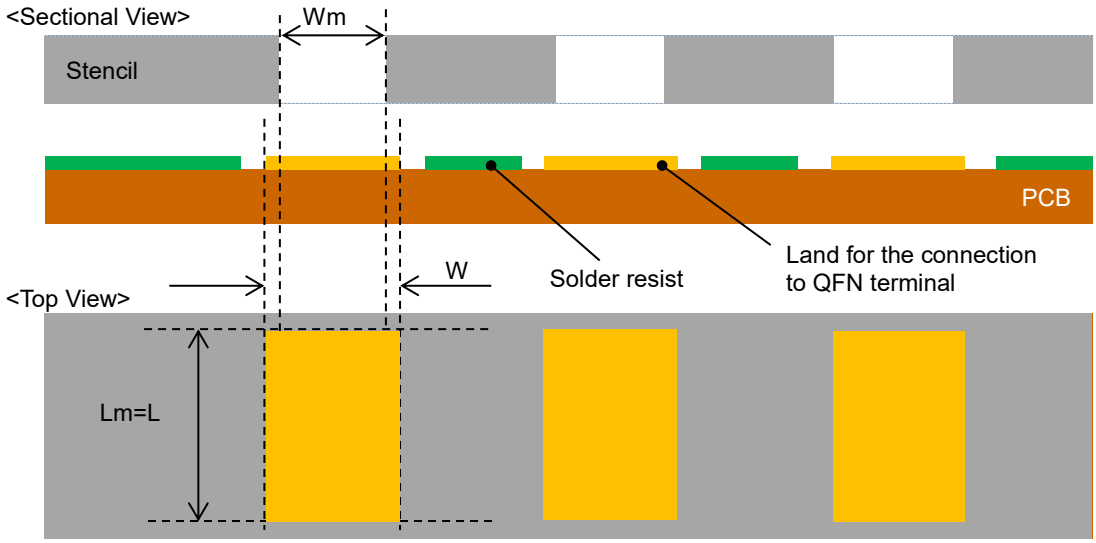


Fig. 4.1 Sectional/Top View of Stencil and PCB

Table 4.3 (Reference) Stencil Design

PWB land size	Stencil opening dimension for length direction Lm	Stencil opening dimension for width direction Wm	Stencil thickness
L,W (Refer to Table 3.2)	Lm=L	Wm=W・100%～90%	100um~150um

*) In order to prevent solder bridge between adjacent terminals, please set the appropriate value within the range of 100% to 90% of the QFN terminal dimension in the width direction.

Table 4.4 (Reference) Failure Mode Caused by Solder Paste Printing

Solder paste printing condition	Main failure mode
Excessive solder paste	> Solder bridge > Solder ball scattering > Component tilt/lifting
Insufficient solder paste	> Solder no joint > Solder bad wetting

4.2.1 Stencil Design for Exposed Die Pad

When excessive solder paste is printed to the large PCB land for Exposed Die Pad (Ex-DP) soldering, solder bridge between Ex-DP land and electrode terminal land and/or floating of the package may occur. So it is necessary to properly design the printing area of solder paste and control the amount of solder.

Generally, solder printing pattern as shown in the figure below might provide a good. This pattern has the effect of preventing the products from occurring solder bridge by spreading of solder paste caused by pressing during QFN mounting. Also, this may prevent QFN from floating up due to the surface tension generated by solder melting during reflow mounting.

Optimum solder printing area may vary depending on the thickness of the stencil. Please obtain the optimum stencil design with sufficient evaluation. As a rule of thumb, solder printing area is about 60% of the QFN's Ex-DP area.

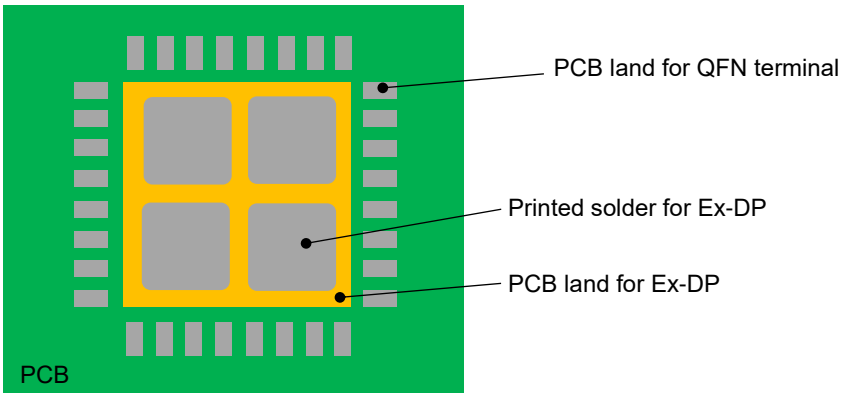


Fig. 4.2 (Reference) Solder Printing for QFN PCB

4.3 Solder paste supply

Solder paste should be stored under supplier's recommended conditions and use solder paste within supplier's guaranteed life time. Once the container is opened and the solder paste is exposed to the environment, please use solder paste under supplier's warranty conditions and recommended conditions.

Please refer to general precautions for using the solder paste below.
> Please open the solder paste container after the temperature of solder paste reaches to near room temperature.
> Please stir solder paste 10 to 20 times by spatula, or please print a trial printing several times after supplying adequate solder paste on the stencil.
> Please don't return solder paste once used for printing to the original container. Please discard it.

4.4 Squeegee

As there are various types of the squeegee, please select the optimum according to the PCB, solder paste and printing machine.

Table 4.5 (Reference) Squeegee Material Comparison

Squeegee material	Use for uneven surface	Amount of printed solder	Stencil life	Squeegee life
Polyurethane rubber	◎	△	◎	△
Metal	△	◎	△	◎
Plastic	△	◎	○	○

*) Above is the relative comparison in general. (◎: Excellent, ○: Good, △: Acceptable)

4.4.1 Polyurethane Rubber Squeegee

By using polyurethane rubber as the squeegee material, it is possible to extend the lifetime of the stencil, but there is a tendency that the volume of printed solder paste becomes lesser than expected.
By using this type squeegee on the uneven PCB, it is possible to obtain good solder printing.

4.4.2 Metal Squeegee

By using metal material as the squeegee material, it is good for printed solder paste volume, but it tends to shorten the lifetime of the stencil.
By using this type squeegee on the even PCB, it is possible to obtain good solder printing.

4.4.3 Plastic Squeegee

By using plastic material as the squeegee material, it is possible to keep the amount of printed solder equivalent to that of the metal squeegee and to extend the lifetime of the stencil, but the lifetime of the squeegee itself is inferior to the metal squeegee.

4.5 Solder Printing

Solder paste is printed on the PCB solder connection land designated for mounted components including QFN. In general, solder paste is filled in the stencil hole with a squeegee, and transferred to the required position, with the required thickness through a stencil separation process.

In order to achieve good quality of solder paste printing, solder paste handling, printing machine maintenance and setting, such as stencil clearance, printing pressure, and squeegee speed are important. Particularly, solder paste property varies depending on the environment such as temperature, humidity, atmospheric convection and so on, it is necessary to pay attention to those environmental factors.

After solder printing, please complete the solder reflow process as soon as possible by following solder paste supplier recommendation.

5. Mounting

QFN is to be mounted on the land where the solder paste is printed. For QFN mounting, please use general component mounting equipment, SMD mounter.

In the reflow soldering method, the final components accuracy after reflow soldering does not reflect the components mounting accuracy. The shift of alignment in components mounting process, to some extent, is corrected by the self-alignment during reflow soldering process. So please mount the components within the range where the position can be corrected by "self-alignment".

Firstly small chip components such as ceramic chip capacitor and so on, should be mounted. Then the large components such as QFP and so on, should be mounted last. Please decide the mounting order in consideration of the size of the mounting components and QFN.

5.1 Precautions for Mounting QFN

5.1.1 Taking out from Carrier Tape or Tray

Please be careful not to apply excessive load or impact during component pickup.

5.1.2 Mounting on PCB

When mounting QFN on the PCB, it is necessary to push the QFN into the printed solder paste on the PCB land appropriately. But excessive loading and/or pressing may cause the solder bridge failure between QFN terminals and the solder ball scattering failure, due to the solder paste collapse.

Impact and pressing beyond limit may result in the breakage of QFN package. So please decide the mounting parameters after sufficient evaluation.

6. Reflow Soldering

6.1 Reflow Soldering Oven

The outline of the reflow soldering oven that is used for SMD soldering in general, is as follows. The reflow oven has the following temperature zone arrangement, and it is necessary to set optimum temperature profile and circumstances for each zone.

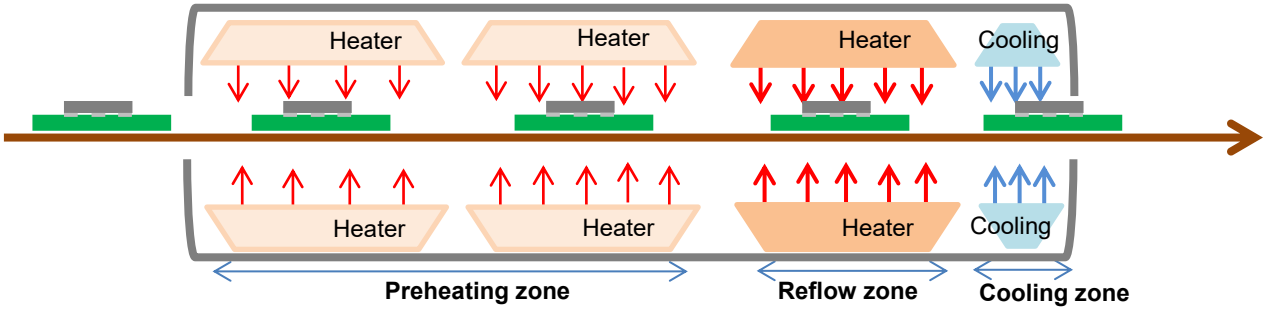


Fig. 6.1 Sketch of Reflow Soldering Oven

6.1.1 Preheating Zone

PCB and mounted components are preheated in the preheating zone. Temperature is from about 140 degrees to about 200 degrees in general.

The purpose of preheating is to equalize the temperature of components with various heat capacity mounted on the PCB, to relieve the sudden thermal shock stress to the components, to activate the flux, and to vaporize the organic solvent, in order to obtain stable solder joints.

6.1.2 Reflow Zone

Temperature is then raised to the solder melting point, in general from 220 degrees to 260 degrees, for a short duration.

As the solder melting point depends on the solder composition, the reflow temperature for lead-free solder must be higher than that for conventional lead solder. However, when the reflow heating temperature becomes higher, oxidation will be accelerated and the wettability tends to become worse. For stable soldering, in order to prevent accelerated oxidation at high temperature, it is necessary to keep the oxygen concentration low.

And also lead-free reflow profile may not be suitable for some components mounted at the same time. Heatproof guarantee temperature of some components may bring down lead-free reflow profile temperature. So it is necessary to confirm the heatproof temperature of each component beforehand.

6.1.3 Cooling Zone

Although natural cooling is common, it is recommended to cool down rapidly in order to release the mounted components from the thermal stress quickly and to obtain a thin and uniform intermetallic compound at the solder joint.

6.2 Reflow Profile

The figure below shows the reflow temperature profile for typical lead-free solder, Sn-Ag-Cu alloy solder. The temperature of the soldering position of the mounted components during reflow soldering, is affected by the following. The structure of mounted components (for example, area array package or peripheral package), surrounding components layout, components position in the PCB, mounted components density and its heat capacity will affect the temperature. So please verify the temperature profile at multiple solder joint positions on the PCB.

When setting reflow profile by the customer, please refer to the recommended reflow profile from solder paste supplier, check the temperature profile by using actual reflow soldering oven and actual PCB, and set the optimum temperature parameter.

In general, reflow heating under nitrogen environment is highly recommended because this gives a better result of soldering stability and wettability.

For Epson QFN, please refer to “6.3 Recommended Reflow Soldering Conditions".

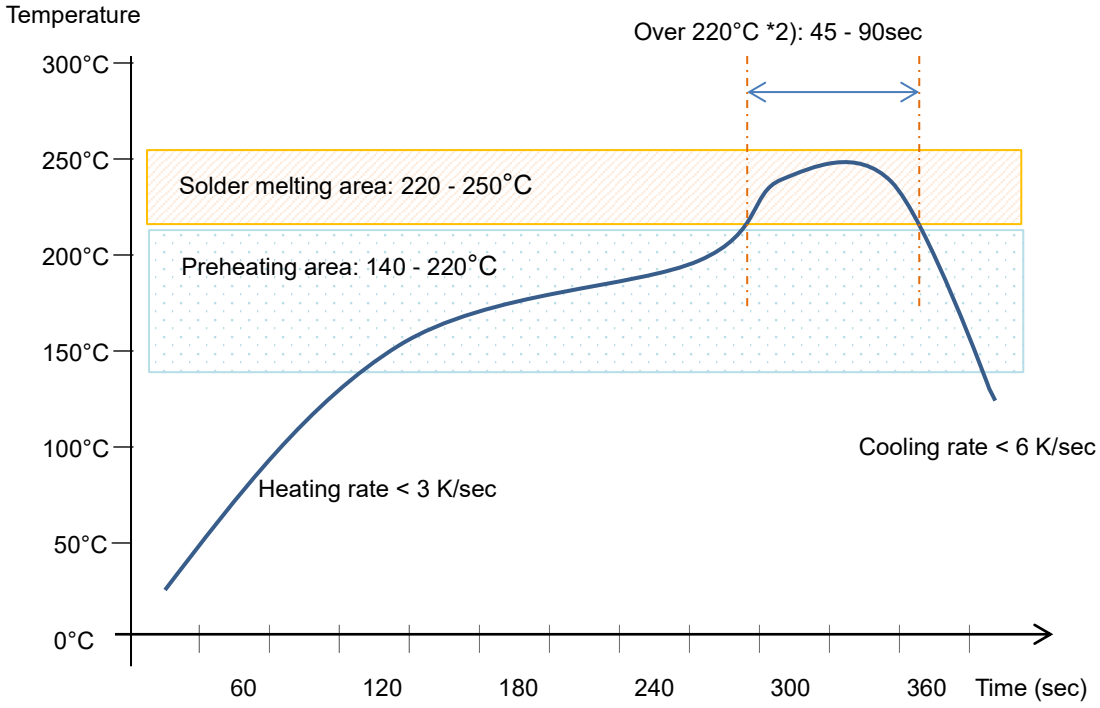


Fig. 6.2 (Reference) Typical Reflow Temperature Profile *1)

*1) Reprint from “JEITA ET-7407B Fig. 3 Sn-3.0AG-0.5Cu”. About detail, please refer to JEITA standard.
*2) Allowable soldering temperature and soldering time depend on the components and the packages.
Please check the specification of components and packages.

6. Reflow Soldering

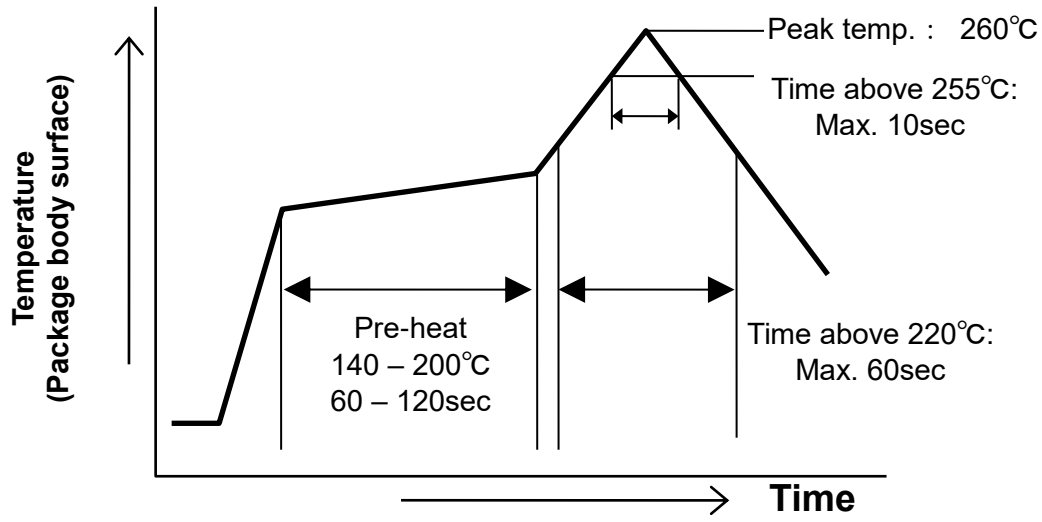
6.3 Recommended Reflow Soldering Conditions

This package is surface mount device (SMD).
The resistance to soldering heat with SMD depends on storage conditions, soldering methods, and soldering conditions.
Please assemble packages according to the following conditions.

Recommended storage conditions

	Conditions	Time
Before opening dry pack:	≦30℃85％RH	1 year
After opening dry pack:	≦30℃70％RH	1 month (720 hours)

Recommended reflow profile



This package should be assembled with IR reflow, full convection, or IR/convection.
The allowable number of time with the reflow is max. 2 times. This must be done in the above-mentioned condition (after opening dry pack).
Nitrogen reflow is recommended to inhibit the effects of oxidation and improve wettability.
* Hand soldering using a soldering iron should be performed under the following conditions:
<Temperature: less than 350 °C, Time: less than 5 sec, Times: twice or less>
Pay sufficient attention not to let a soldering iron contact any parts other than leads.

Recommended bake conditions

When packages exceed the above-mentioned storage conditions after opening the dry pack, please bake them according to the following conditions:

Temperature	Time	Number of times
125±5℃	20 - 36 hours	Max. 2 times

Storage conditions from the baking to the reflow soldering are the same as the above-mentioned storage conditions.

*if products are shipped in tape & reel, please transfer them to heatproof trays before baking.

(Storage rank: MSL2a)

7. Cleaning

7.1 Cleaning after QFN Soldering

Since QFN standoff *1) is very narrow after soldering, it is very difficult to remove the solder paste flux residue between the QFN and the PCB. Solder paste that does not require cleaning after soldering is recommended.

Also, when selecting the solder paste that requires cleaning, cleaning condition need to be decided after detail discussion with solder paste supplier.

*1) Standoff: The distance between QFN mounted PCB surface and QFN package bottom surface.

7.2 General PCB Cleaning

7.2.1 PCB Cleaning

The flux residue after PCB production process may cause the leakage or migration between terminals. These may affect the reliability. Cleaning is effective in removing flux sticking on the components and connection terminals that require flux cleaning. Also, cleaning is effective in removing scattered solder balls that occurred during reflow soldering. If “no-clean solder” is not used, it is still recommended to perform flux cleaning after reflow soldering.

7.2.2 Cleaning Method

Standard cleaning methods for PCB include immersion cleaning, ultrasonic cleaning, spray cleaning, vapor cleaning and so on. Hot water immersion ultrasonic cleaning is widely used. Regarding detail cleaning method, please follow the recommendation from solder paste supplier and cleaning fluid supplier.

7.2.3 Water Cleaning

In case of using water-soluble solder paste, in order to prevent moisture absorption, it is necessary to control the staging time between solder paste printing and components mounting and reflow soldering. Regarding operation time management, please follow the recommendation from solder paste supplier.

7.2.4 No Cleaning

For eliminating “Cleaning process” after reflow soldering, it is necessary to check the effect of halogen content, especially chlorine content, in flux and to use solder paste with less flux residue. Before “no cleaning” is implemented, please check that the solder is “no-clean solder” type and perform mounting evaluation and reliability test by using actual PCB.

7.3 Others

(1) Cleaning time should be short, and the cleaning temperature should be as low as possible.
(2) Please be sure to check the quality (effect on the terminal) after cleaning.
(3) If water adheres and remains on the QFN terminal after cleaning, there is a risk of causing troubles, so please perform drying treatment thoroughly.
(4) Please evaluate the influence by cleaning agent, diluent, water and pure water on the PCB and mounted components thoroughly. Influence by acid, alkali, organic solvent and water should be considered as well.

8. Rework

Reuse of the QFN that is removed from the PCB after reflow soldering, will void the warranty. Please do not reuse the removed QFN.

Also, in case of re-mounting new QFN on the PCB from which the old QFN is removed, please perform soldering of new QFN after cleaning the PCB surface and reapplying new solder paste.

The method of removing mounted QFN is as follows. Use a dedicated jig for removing the components, and remove the QFN by melting solder connection while locally heating by high-temperature air. Before heating the QFN, preheat the QFN area and its surrounding. Preheating reduces the high-temperature heating time required for removal, and minimizes the distortion and the deformation of the PCB.

Additionally in case of PCB rework and reuse, please check the influence of damage, deformation, reliability and so on of the PCB thoroughly by the customer.

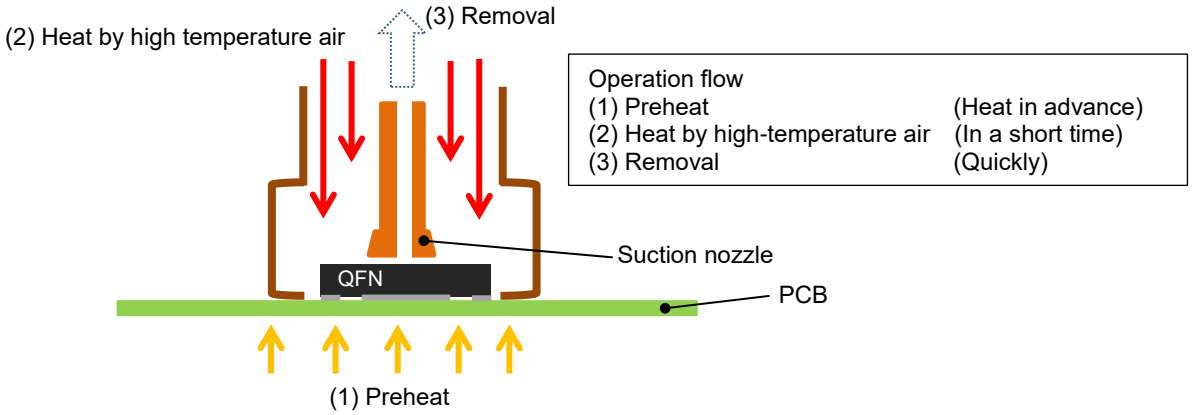


Fig 8.1 (Reference) Sketch of QFN Rework

9. General Precautions for Use of Semiconductor Devices

Please follow the precautions of our semiconductor products mentioned below. For details on QFN, please also check the notes mentioned in each chapter in this document.

9.1 Introduction

Epson's semiconductor devices are designed and manufactured to assure trouble-free operation when used under normal operating conditions. All products are subjected to stringent electrical and mechanical testing to ensure reliability, but users are strongly recommended to observe the following precautions when designing systems, handling or storing devices to minimize the chance of failure.

9.2 Storage

(1) Take care so that packages are not subjected to impact, vibration or water leakage.

(2) Do not store and use the product under the environment in which moisture condensation may be formed due to rapid changes in temperature. Also, please do not apply load to the products during storage.

(3) When storing, avoid dusty locations and corrosive gases.

(4) Before opening moisture-proof bag, please make sure that the moisture-proof bag is not broken or scratched. Also check the silica gel in the bag has not absorbed moisture, after the bag is opened.

(5) When using after a long term of storage, use after confirming that terminal discoloration, solderability deterioration and so on, does not occur.

9.3 Design and Handling

(1) Use ICs within the rated ranges of operating voltage, temperature, input/output voltage and current. Devices may sometimes work properly for a short period of time even when used outside of rated ranges, but their failure ratio may increase. Even within the rated conditions, failure ratio will change depending on the operating temperature and voltage of embedded systems. This must be fully considered when designing systems.

(2) When a noise such as spark and electrostatic is given from an input terminals, IC may malfunction. Pay sufficient attention in product designing. Electromagnetic can cause ICs to operate erratically. Shield all interference sources in equipment that uses ICs.

(3) Excessive electrical noise occurred to a power or input/output pin can cause ICs to latch up, resulting in device malfunction or damage. If this occurs, turn off the power, solve the problem, then supply power again.

(4) Although all pins are equipped with an anti-electro static circuit, electro static beyond the capacity may lead to breakage. Take appropriate countermeasures for ESD when handling ICs.

(5) Avoid using packing and transporting containers made of plastic, use electrically conductive containers. Also, special care must be taken when handling ICs, by wearing an antistatic wrist strap or taking other possible measures.

(6) Use a soldering iron and test circuits without high voltage leakage and use those with grounding.

(7) Storage conditions after opening a moisture proof-bag, soldering method and soldering temperature must meet the requirements specified by Epson for respective products.

(8) Minimize mechanical stress to a printed circuit board during or after soldering.

(9) As for a surface mount device, the land of a PCB and the lead of a package will be soldered with those both surfaces in contact. Although Epson is shipping products securing sufficient lead flatness for soldering, when handling, take care not to apply force which leads to deformation of the lead.

(10) Use the IC under the proper temperature and humidity. The humidity must not be more than 85% (no dew condensation). In the environment where the IC is directly exposed to acid gas such as SO2, or exposed to dust or salt, it may cause electrical leakage between leads or corrosion. In order to prevent such problems, in above environment, apply corrosion-proof coatings to PCB and ICs.

(11) Avoid the following as much as possible, since mechanical vibration, shock, continuous stress, sudden temperature change and so on, may cause package cracks and/or wire breakage.

(12) In some packages, a part of the signal line is exposed on the surface of the package. Pay attention to contamination of the package when using these products. Also avoid handling products with bare hands.

(13) Light irradiation to ICs may cause the characteristics change of IC. To prevent IC from malfunction, consider following points for IC mounted PCB and IC used products.

> In product design and assembly, consider the product structure so that IC (especially IC chip) is shielded from light in actual use.

> In testing process, provide light-shielded environment for the semiconductor device under test.

> Regarding light shielding of IC, consider the light shielding for the surface, back, and side of IC chip.

Revision History

Attachment-1

Rev. No.	Date	Page	Category	Contents
Rev 1.0	2018/08/10	All	New	New release.

EPSON

International Sales Operations

America

Epson America, Inc.

Headquarter:
3840 Kilroy Airport Way
Long Beach, California 90806-2452 USA
Phone: +1-562-290-4677

San Jose Office:
214 Devcon Drive
San Jose, CA 95112 USA
Phone: +1-800-228-3964 or +1-408-922-0200

Europe

Epson Europe Electronics GmbH
Riesstrasse 15, 80992 Munich,
Germany
Phone: +49-89-14005-0 FAX: +49-89-14005-110

Asia

Epson (China) Co., Ltd.
4th Floor, Tower 1 of China Central Place, 81 Jianguo Road, Chaoyang District, Beijing 100025 China
Phone: +86-10-8522-1199 FAX: +86-10-8522-1120

Shanghai Branch
Room 1701 & 1704, 17 Floor, Greenland Center II,
562 Dong An Road, Xu Hui District, Shanghai, China
Phone: +86-21-5330-4888 FAX: +86-21-5423-4677

Shenzhen Branch
Room 804-805, 8 Floor, Tower 2, Ali Center,No.3331
Keyuan South RD(Shenzhen bay), Nanshan District, Shenzhen
518054, China
Phone: +86-10-3299-0588 FAX: +86-10-3299-0560

Epson Taiwan Technology & Trading Ltd.
15F, No.100, Songren Rd, Sinyi Dist, Taipei City 110. Taiwan
Phone: +886-2-8786-6688

Epson Singapore Pte., Ltd.
1 HarbourFront Place,
#03-02 HarbourFront Tower One, Singapore 098633
Phone: +65-6586-5500 FAX: +65-6271-3182

Seiko Epson Corp.
Korea Office
19F, KLI 63 Bldg, 60 Yoido-dong,
Youngdeungpo-Ku, Seoul 150-763, Korea
Phone: +82-2-784-6027 FAX: +82-2-767-3677

Seiko Epson Corp.
Sales & Marketing Division

Device Sales & Marketing Department
421-8, Hino, Hino-shi, Tokyo 191-8501, Japan
Phone: +81-42-587-5816 FAX: +81-42-587-5116

Document Code: 3990-0003
First Issue August 2018 in JAPAN