S1C17W11 (rev1.0)

EPSON

16-bit Single Chip Microcontroller

- Low-voltage operation from 1.2V possible using a single alkaline or silver oxide button cell battery.
- Sleep mode power consumption of 109nA (all registers, SRAM, and terminal states are retained.)
- Equipped with an R/F converter (RFC2) for high-resolution measurements even in low-voltage environments.
- A power supply voltage doubling circuit (max. 5V) can be used to boost the buzzer volume or drive a white LED.
- Equipped with 128 bytes of EEPROM for storing sensor calibration values and measurement values.

■ Overview

The S1C17W11 is a 16-bit MCU featuring low power consumption. It incorporates various serial interfaces, an LCD driver, and a CR oscillation-type A/D converter (R/F converter). Combined with the powerful processing capability of a 16-bit CPU, it is best suited for battery-powered equipment requiring LCD and resistance measurement functions (such as thermometers, water quality meters, and salinity meters). In addition, it includes a charge pump regulator for driving a buzzer and LEDs, allowing for white LED illumination and increased buzzer volume.

■ Features

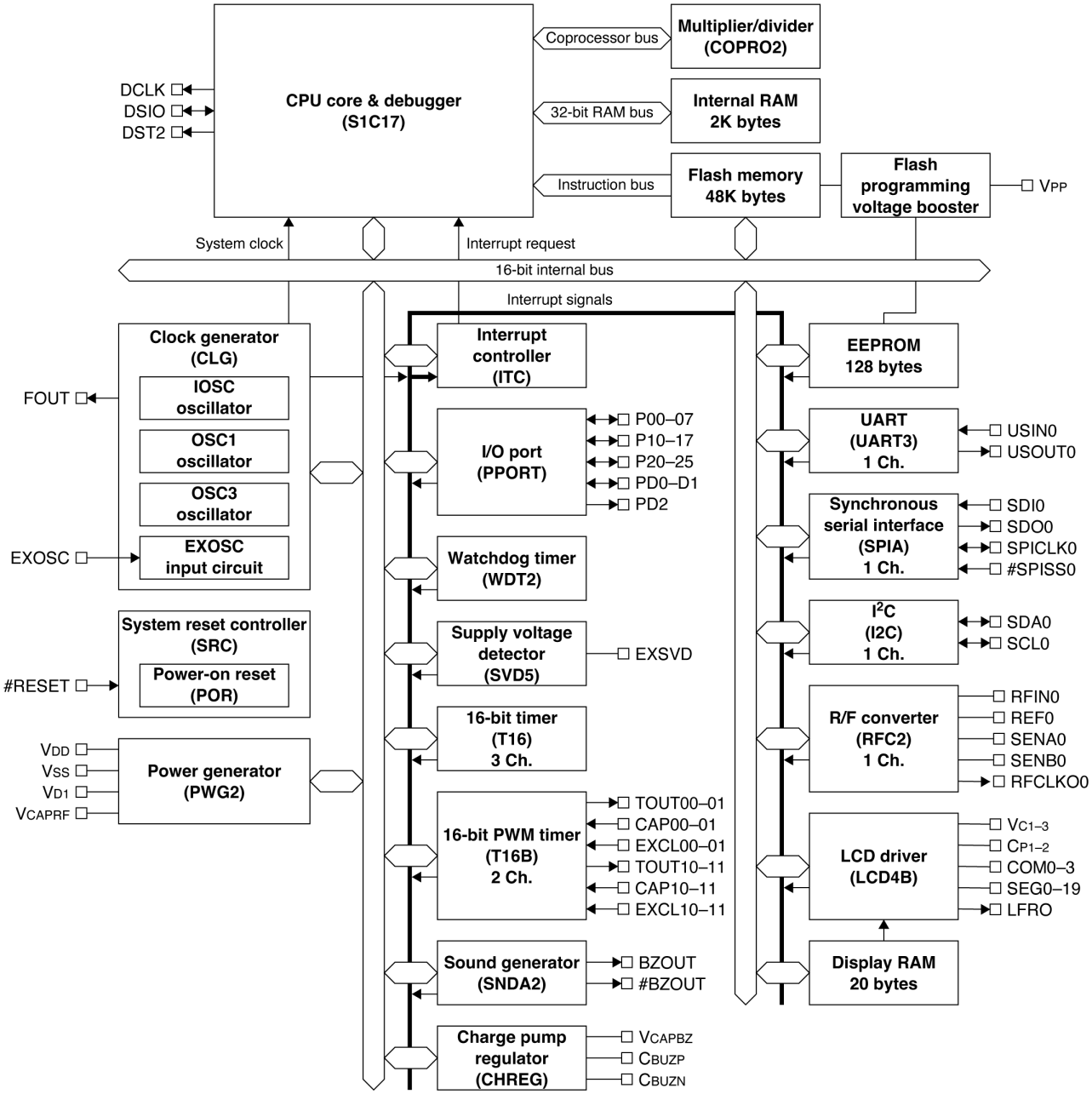
Model	S1C17W11
CPU	
CPU core	Seiko Epson original 16-bit RISC CPU core S1C17
Other	On-chip debugger
Embedded Flash memory	
Capacity (for both instructions and data)	48K bytes
Erase/program count	1,000 times (min.) * Programming by the debugging tool ICDmini
Other	Security function to protect from reading/programming by ICDmini
	On-board programming function using ICDmini * An external smoothing capacitor is required.
	Flash programming voltage can be generated internally.
Embedded EEPROM	
Capacity	128 bytes
Erase/program count	100,000 times (min.)
Embedded RAM	
Capacity	2K bytes
Embedded display RAM	
Capacity	20 bytes (4 COM x 20 SEG x 2 screens)
Clock generator (CLG)	
System clock source	4 sources (IOSC/OSC1/OSC3/EXOSC)
System clock frequency (operating frequency)	4.2 MHz (max.)
IOSC oscillator circuit (boot clock source)	700 kHz (typ.) embedded oscillator
	23 µs (max.) starting time (time from cancelation of SLEEP state to vector table read by the CPU)
OSC1 oscillator circuit	32 kHz (typ.) embedded oscillator
OSC3 oscillator circuit	4 MHz (max.)/2 MHz/1 MHz/500 kHz/384 kHz/250 kHz embedded oscillator
EXOSC clock input	4.2 MHz (max.) square or sine wave input
Other	Configurable system clock division ratio
	Configurable system clock used at wake up from SLEEP state
	Operating clock frequency for the CPU and all peripheral circuits is selectable.

Model		S1C17W11
I/O port (PPORT)		
Number of general-purpose ports	Input/output port	24 bits (max.), 2 bits can also be used as debug ports (DSIO / DST2).
	Output port	1 bit (max.), Can also be used as a debug port (DCLK).
	Other	Pins are shared with the peripheral I/O.
Number of input interrupt ports		22 bits (max.)
Number of ports that support universal port multiplexer (UPMUX)		16 bits
		A peripheral circuit I/O function selected via software can be assigned to each port. Applicable functions: I2C, SPIA, UART3, T16B
LED drive output ports		2 bits, Nch open-drain, maximum output current 10 mA
Timers		
Watchdog timer (WDT2)		Generates NMI or hardware reset.
		Programmable NMI/reset generation cycle
16-bit timer (T16)		3 channels
		Generates the SPIA master clock.
16-bit PWM timer (T16B)		2 channels
		Event counter/capture function
		PWM waveform generation function
		Number of PWM output or capture input ports: 2 ports (per channel)
Supply voltage detector (SVD5)		
Detection voltage		V_{DD} or external voltage (One external voltage input port is provided, and an external voltage level can be detected even if it exceeds V_{DD}.)
Detection level		32 levels (1.15 to 3.2 V)
Other		Intermittent operation mode
		Generates an interrupt or reset according to the detection level evaluation.
Serial interfaces		
UART (UART3)		1 channel
		Baud-rate generator included, IrDA1.0 supported
		Open drain output, signal polarity, and baud rate division ratio are configurable.
		Infrared communication carrier modulation output function
Synchronous serial interface (SPIA)		1 channel
		2 to 16-bit variable data length
		The 16-bit timer (T16) can be used for the baud-rate generator in master mode.
I^2C (I2C) [*1]		1 channel
		Baud-rate generator included
Sound generator (SNDA2)		
Buzzer output function		512 Hz to 16 kHz output frequencies
		One-shot output function
Melody generation function		Pitch: 128 Hz to 16 kHz ≈ C3 to C6
		Duration: 7 notes/rests (Half note/rest to thirty-second note/rest)
		Tempo: 16 tempos (30 to 480)
		Tie may be specified.
Charge pump regulator (CHREG)		
Output voltage		V_{DD} x 2 ≤ 5.0 V (typ.)
Other		Used for the I/O voltage of the SNDA2 output (BZOUT, #BZOUT)
		Can be used as the LED drive power supply, 10 mA (max.) output current
LCD driver (LCD4B)		
LCD output (max value.)		20SEG x 1 to 4COM (max.)
LCD power supply		1/3 bias power supply included (internal step-up/resistive divider selectable).
		An external voltage can be applied. (Internal resistors are provided to divide the external source voltage.)
LCD contrast		29 levels (Only when the internal voltage booster is enabled.)

Model	S1C17W11
R/F converter (RFC2)	
Conversion method	CR oscillation type with 24-bit counters
Number of conversion channels	1 channel
Supported sensors	DC-bias resistive sensors
	AC-bias resistive sensors
Number of connectable sensors	2 (max.) in DC resistive sensor mode
	1 (max.) in AC resistive sensor mode
Reference power supply for measurement	Internally generated by dedicated power circuit
Multiplier/divider (COPRO2)	
Arithmetic functions	16-bit x 16-bit multiplier
	16-bit x 16-bit + 32-bit multiply and accumulation unit
	32-bit ÷ 32-bit divider
Reset	
#RESET pin	Reset when the reset pin is set to low.
Power-on reset	Reset at power on.
Key entry reset	Reset when the P10 to P11/P12/P13 keys are pressed simultaneously (can be enabled/disabled using a register).
Watchdog timer reset	Reset when the watchdog timer overflows (can be enabled/disabled using a register).
Supply voltage detector reset	Reset when the supply voltage detector detects the set voltage level (can be enabled/disabled using a register).
Interrupt	
Non-maskable interrupt	4 systems (Reset, address misaligned interrupt, debug, NMI)
Programmable interrupt	External interrupt: 1 system (8 levels)
	Internal interrupt: 14 systems (8 levels)
Power supply voltage	
V_{DD} operating voltage	1.2 to 3.6 V
Internal logic voltage	Selectable among 1.2 V/1.4 V/1.8 V
V_{DD} operating voltage for Flash programming	2.2 to 3.6 V (Programming voltage V_{PP}: 7.5 V supplied externally or generated internally)
V_{DD} operating voltage for EEPROM programming	2.2 to 3.6 V (Programming voltage V_{PP}: generated internally)
Operating temperature	
Operating temperature range	-40 to 85°C
Current consumption (typ. value)	
SLEEP mode	109 nA (VDD=1.5V), 116 nA (VDD=3.0V) IOSC = OFF, OSC1 = OFF, OSC3 = OFF, V_{D1}=1.2V
HALT mode	1.28 µA OSC1 = 32 kHz, V_{D1}=1.2V
RUN mode	3.82 µA OSC1 = 32 kHz, CPU = OSC1, V_{D1}=1.2V
	75.6 µA IOSC = 700kHz, CPU = IOSC, V_{D1}=1.2V
	156 µA OSC3 = 1MHz, CPU = OSC3, V_{D1}=1.2V
Shipping form	
1	SQFN7-48pin (P-VQFN048-0707-0.50, 7 × 7 mm, t = 1.0 mm, 0.5 mm pitch) *2
2	Bare chip

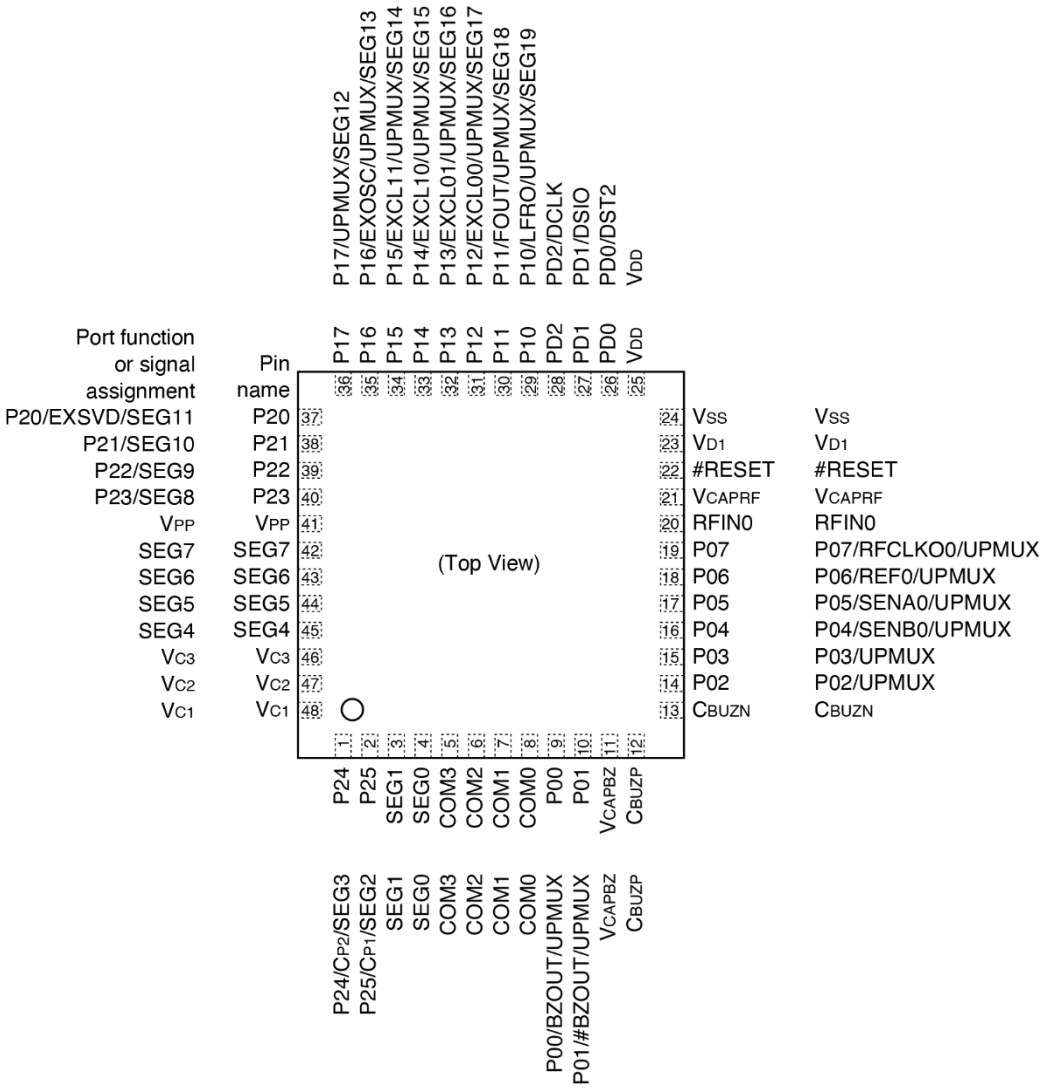
*1 The input filter in I2C (SDA and SCL inputs) does not comply with the standard for removing noise spikes less than 50 ns.
*2 Shown in parentheses is the JEITA package name.

Block Diagram

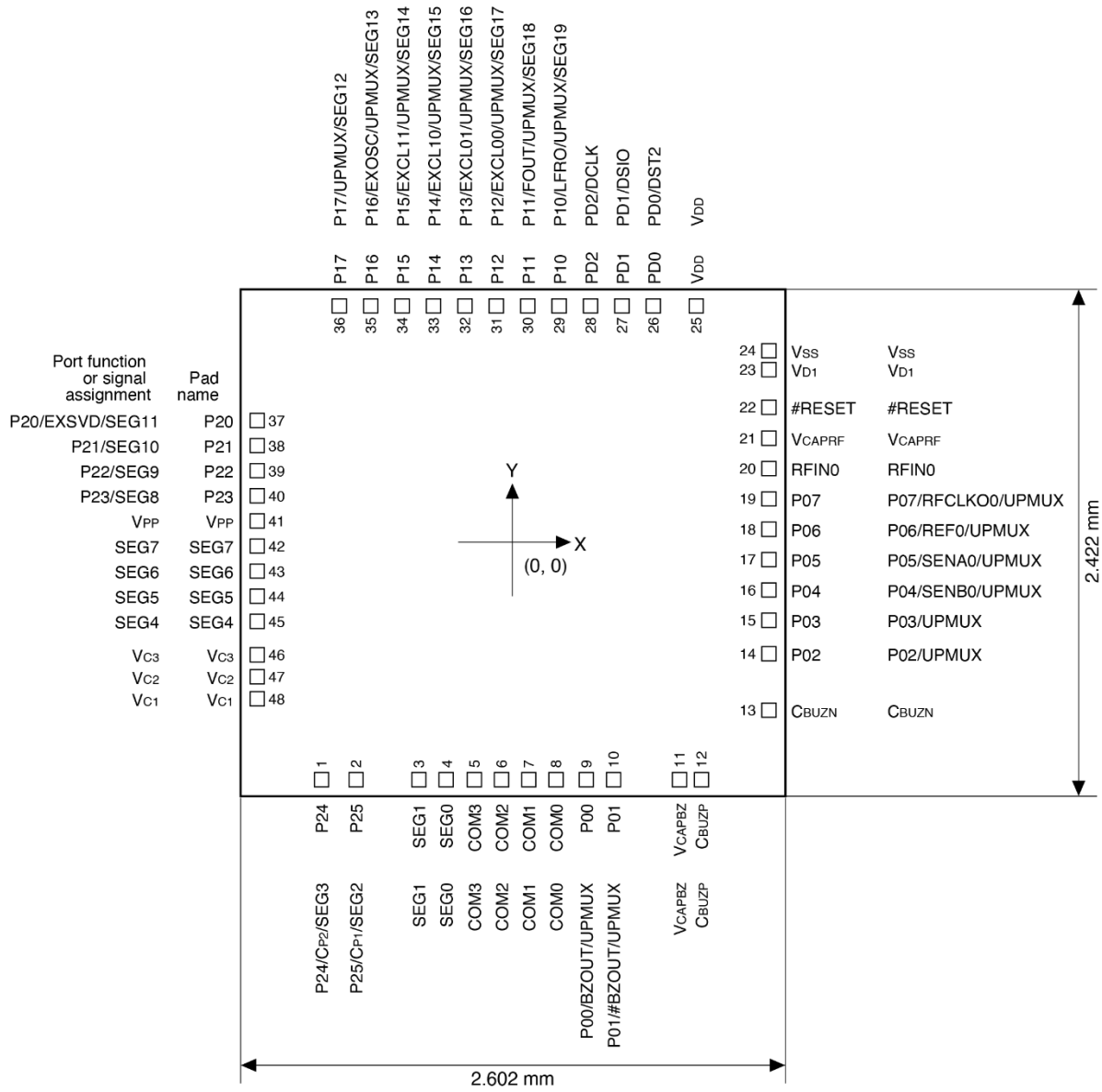


Pin Configuration Diagram

SQFN7-48pin



Chip



Pad opening: X = 68 µm, Y = 68 µm
Chip thickness: 400 µm

No.	Xµm	Yµm	No.	Xµm	Yµm	No.	Xµm	Yµm	No.	Xµm	Yµm
1	-915.0	-1131.5	13	1221.5	-800.0	25	875.0	1131.5	37	-1221.5	585.0
2	-750.0	-1131.5	14	1221.5	-530.0	26	670.0	1131.5	38	-1221.5	465.0
3	-450.0	-1131.5	15	1221.5	-370.0	27	520.0	1131.5	39	-1221.5	345.0
4	-320.0	-1131.5	16	1221.5	-225.0	28	370.0	1131.5	40	-1221.5	225.0
5	-185.0	-1131.5	17	1221.5	-80.0	29	220.0	1131.5	41	-1221.5	105.0
6	-55.0	-1131.5	18	1221.5	65.0	30	70.0	1131.5	42	-1221.5	-15.0
7	75.0	-1131.5	19	1221.5	210.0	31	-80.0	1131.5	43	-1221.5	-135.0
8	205.0	-1131.5	20	1221.5	355.0	32	-230.0	1131.5	44	-1221.5	-255.0
9	350.0	-1131.5	21	1221.5	500.0	33	-380.0	1131.5	45	-1221.5	-375.0
10	480.0	-1131.5	22	1221.5	647.5	34	-530.0	1131.5	46	-1221.5	-534.5
11	795.0	-1131.5	23	1221.5	827.5	35	-680.0	1131.5	47	-1221.5	-639.5
12	900.0	-1131.5	24	1221.5	917.5	36	-830.0	1131.5	48	-1221.5	-744.5

Pin Descriptions

Symbol meanings

Assigned signal:
The signal listed at the top of each pin is assigned in the initial state. The pin function must be switched via software to assign another signal (see the “I/O Ports” chapter).

I/O:
- I = Input
- O = Output
- I/O = Input/output
- P = Power supply
- A = Analog signal
- Hi-Z = High impedance state

Initial state:
- I (Pull-up) = Input with pulled up
- I (Pull-down) = Input with pulled down
- Hi-Z = High impedance state
- O (H) = High level output
- O (L) = Low level output

Tolerant fail-safe structure:
- ✓ = Over voltage tolerant fail-safe type I/O cell included (see the “I/O Ports” chapter)

Pin name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function
V_{DD}	V_{DD}	P	-	-	Power supply (+)
V_{SS}	V_{SS}	P	-	-	GND
V_{PP}	V_{PP}	P	-	-	Flash programming power supply
V_{D1}	V_{D1}	A	-	-	DC-DC converter output
V_{C1-3}	V_{C1-3}	P	-	-	LCD panel drive power supply
#RESET	#RESET	I	I (Pull-up)	-	Reset input
V_{CAPBZ}	V_{CAPBZ}	P	Hi-Z	-	Buzzer/LED drive voltage output
C_{BUZP}	C_{BUZP}	A	Hi-Z	-	Buzzer/LED drive power supply boost capacitor connection pin
C_{BUZN}	C_{BUZN}	A	Hi-Z	-	Buzzer/LED drive power supply boost capacitor connection pin
V_{CAPRF}	V_{CAPRF}	A	-	-	R/F converter regulator output
RFIN0	RFIN0	A	Hi-Z	-	R/F converter Ch.0 oscillation input
P00	P00	I/O	Hi-Z	✓	I/O port
	BZOUT	O			Sound generator buzzer output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P01	P01	I/O	Hi-Z	✓	I/O port
	#BZOUT	O			Sound generator inverted buzzer output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P02	P02	I/O	Hi-Z	✓	I/O port (open-drain type)
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P03	P03	I/O	Hi-Z	✓	I/O port (open-drain type)
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P04	P04	I/O	Hi-Z	✓	I/O port
	SENB0	A			R/F converter Ch.0 sensor B oscillation pin
	UPMUX	I/O			User-selected I/O (universal port multiplexer)

Pin name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function
P05	P05	I/O	Hi-Z	✓	I/O port
	SENA0	A			R/F converter Ch.0 sensor A oscillation pin
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P06	P06	I/O	Hi-Z	✓	I/O port
	REF0	A			R/F converter Ch.0 reference oscillation pin
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P07	P07	I/O	Hi-Z	✓	I/O port
	RFCLKO0	A			R/F converter Ch.0 clock monitor output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P10	P10	I/O	Hi-Z	✓	I/O port
	LFRO	O			LCD frame signal monitor output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	SEG19	A			LCD segment output 19
P11	P11	I/O	Hi-Z	✓	I/O port
	FOUT	O			Clock generator clock external output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	SEG18	A			LCD segment output 18
P12	P12	I/O	Hi-Z	✓	I/O port
	EXCL00	I			16-bit PWM timer Ch.0 event counter input 0
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	SEG17	A			LCD segment output 17
P13	P13	I/O	Hi-Z	✓	I/O port
	EXCL01	I			16-bit PWM timer Ch.0 event counter input 1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	SEG16	A			LCD segment output 16
P14	P14	I/O	Hi-Z	✓	I/O port
	EXCL10	I			16-bit PWM timer Ch.1 event counter input 0
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	SEG15	A			LCD segment output 15
P15	P15	I/O	Hi-Z	✓	I/O port
	EXCL11	I			16-bit PWM timer Ch.1 event counter input 1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	SEG14	A			LCD segment output 14
P16	P16	I/O	Hi-Z	✓	I/O port
	EXOSC	I			Clock generator external clock input
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	SEG13	A			LCD segment output 13
P17	P17	I/O	Hi-Z	✓	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	SEG12	A			LCD segment output 12
P20	P20	I/O	Hi-Z	✓	I/O port
	EXSVD	A			External power supply voltage detection input
	SEG11	A			LCD segment output 11
P21	P21	I/O	Hi-Z	✓	I/O port
	SEG10	A			LCD segment output 10
P22	P22	I/O	Hi-Z	✓	I/O port
	SEG9	A			LCD segment output 9
P23	P23	I/O	Hi-Z	✓	I/O port
	SEG8	A			LCD segment output 8
P24	P24	O	Hi-Z	✓	I/O port

Pin name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function
	C_{P2}	A			LCD drive voltage boost capacitor connection pin
	SEG3	A			LCD segment output 3
P25	P25	I/O	Hi-Z	✓	I/O port
	C_{P1}	A			LCD drive voltage boost capacitor connection pin
	SEG2	A			LCD segment output 2
PD0	DST2	O	O (L)	✓	On-chip debugger status output
	PD0	I/O			I/O port
PD1	DSIO	I/O	I (Pull-up)	✓	On-chip debugger data input/output
	PD1	I/O			I/O port
PD2	DCLK	O	O (H)	-	On-chip debugger clock output
	PD2	O			Output port
COM0-3	COM0-3	A	Hi-Z	-	LCD common outputs
SEG0-1	SEG0-1	A	Hi-Z	-	LCD segment outputs
SEG4-7	SEG4-7				

Note: In the peripheral circuit descriptions, the assigned signal name is used as the pin name.

Universal port multiplexer (UPMUX)

The universal port multiplexer (UPMUX) allows software to select the peripheral circuit input/output function to be assigned to each pin from those listed below.

Peripheral Circuit Input/output Function Selectable by UPMUX

Peripheral circuit	Signal to be assigned	I/O	Channel number *n*	Function
Synchronous serial interface (SPIA)	SDI*n*	I	*n* = 0	SPIA Ch.*n* data input
	SDO*n*	O		SPIA Ch.*n* data output
	SPICLK*n*	I/O		SPIA Ch.*n* clock input/output
	#SPISS*n*	I		SPIA Ch.*n* slave-select input
I²C (I2C)	SCL*n*	I/O	*n* = 0	I2C Ch.*n* clock input/output
	SDA*n*	I/O		I2C Ch.*n* data input/output
UART (UART3)	USIN*n*	I	*n* = 0	UART3 Ch.*n* data input
	USOUT*n*	O		UART3 Ch.*n* data output
16-bit PWM timer (T16B)	TOUT*n*0/CAP*n*0	I/O	*n* = 0, 1	T16B Ch.*n* PWM output/capture input 0
	TOUT*n*1/CAP*n*1	I/O		T16B Ch.*n* PWM output/capture input 1

Note: Do not assign a function to two or more pins simultaneously.

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