RF Transmitter IC

S1S77100

Data Sheet

SEIKO EPSON CORPORATION

Table of Contents

1. Overview

RF transmitter IC S1S77100 is a wireless transmitter IC for the UHF range. This IC houses a PLL and a Power Amp in a 4 mm x 4 mm SQFN package. The S1S77100 can be configured in combination with an external crystal oscillator. So, it is suitable for small wireless devices.

- Output frequency range: 300 MHz to 465 MHz (0.25 kHz Step), 600 MHz to 930 MHz (0.49 kHz Step)
- Δ-Σ fractional-N PLL
- Programmable power amplifier (PA) output power: -15 dBm to 1dBm, -5 dBm to 11 dBm for each 64 steps
- Modulation types: ASK/OOK/FSK with Soft-ASK and/or Soft FSK shaping.
- Multi-channel (up to 4 channels), channel hopping capability
- 3-wire/4-wire SPI interface for Special Function Register (SFR)
- SFR (Special Function Register)
- Fail-safe mechanism (PLL Loss of Lock: LOL, VCO auto-calibration error, Under Voltage Detection: UVD)
- External 32 MHz crystal oscillator by clipped sine input
- Synchronous transmission mode with input clock
- Dividing clock output via CKOUT
- Programmable voltage threshold of Under Voltage Detection (UVD): 4 step (1.8 V to 2.4 V)
- 24-pin 4 mm x 4 mm SQFN (Saw Quad Flat Non-leaded) package
- Supply voltage 1.8 V to 3.6 V
- Operating temperature: -40°C to +85°C
- Pb-free/RoHS-compliant

2. Block Diagram

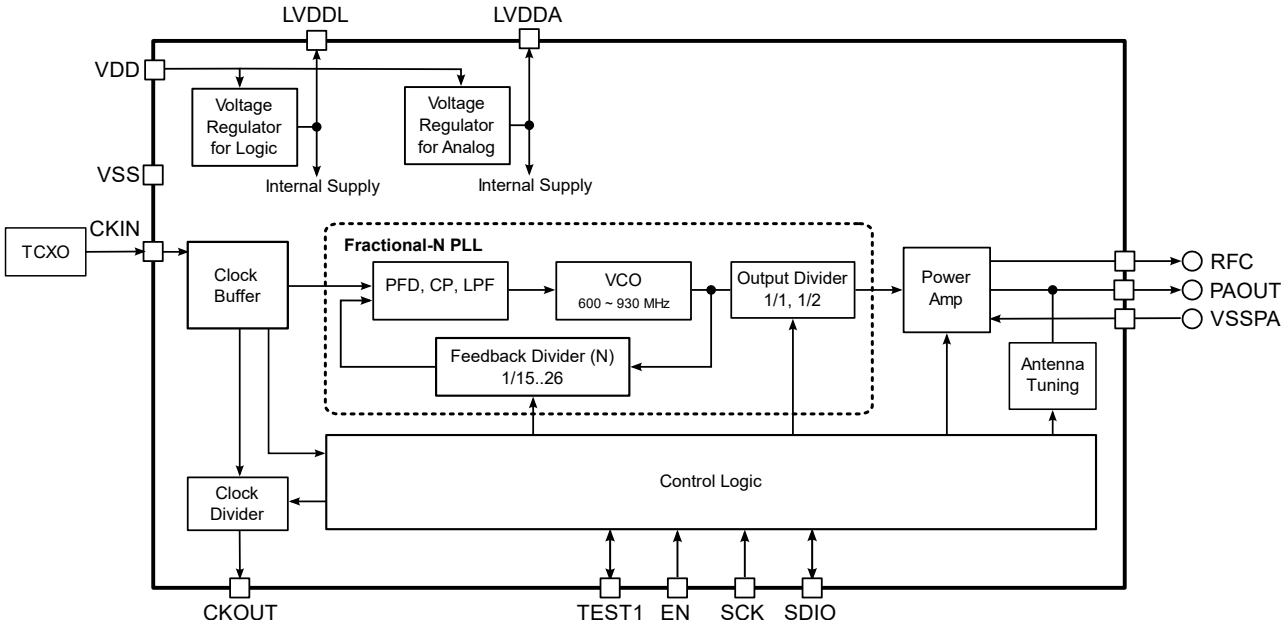
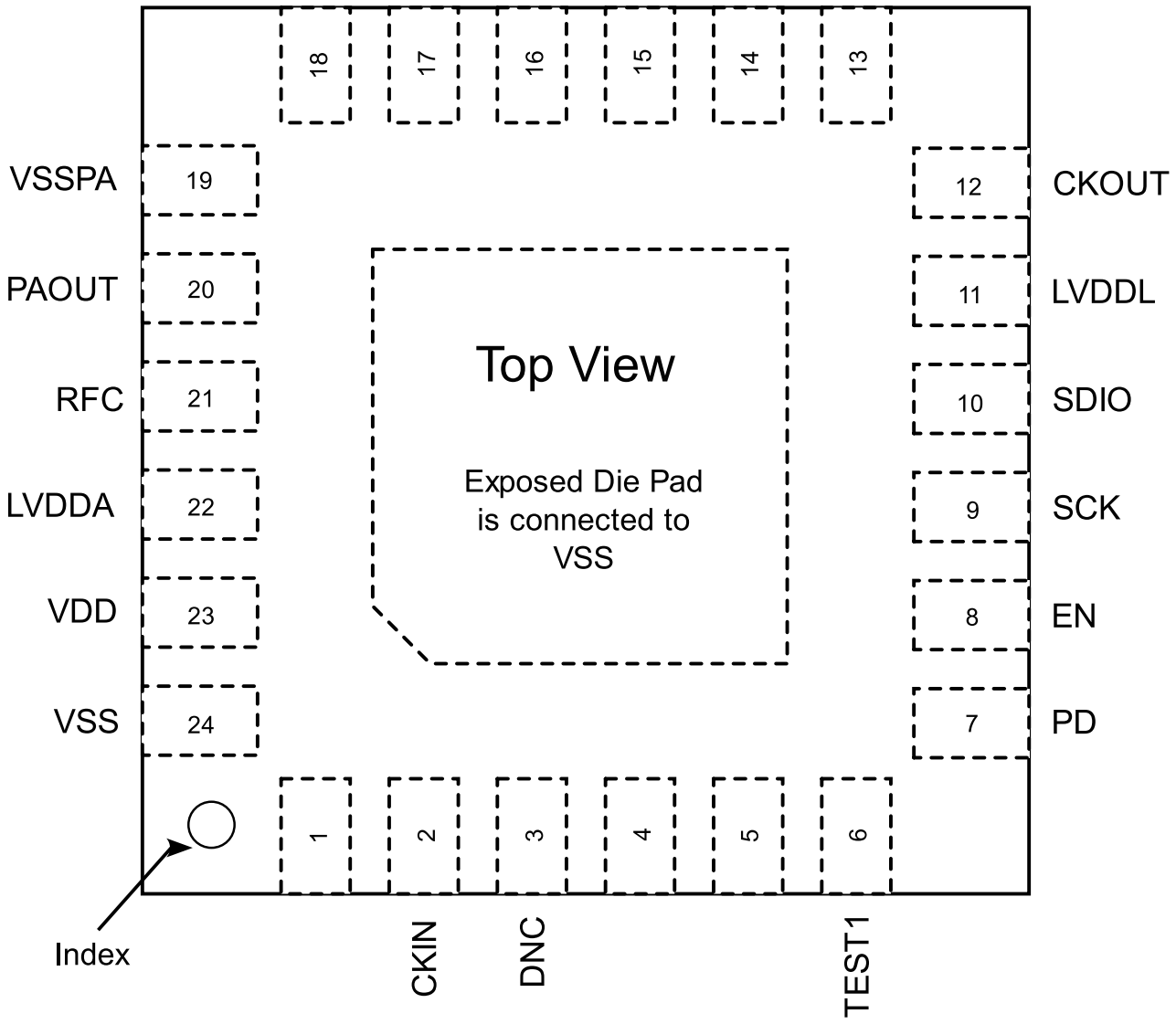


Figure 2.1 S1S77100 Block Diagram

3. Pin Assignments

Package type：SQFN 4



* Pins without names (1, 4, 5, 13 to 18) are NC (no wire connection to the built-in IC).
* When soldering the EDP (Exposed Die Pad) to the mounting board, connect it to a wire with the same power as VSS.

4. Pin Descriptions

Table 4.1 Pin Descriptions

No.	Pin Name	Type		Function
1	NC	-	-	Unconnected pin, connected to VSS for power stabilization
2	CKIN	Input	-	Crystal oscillator input, direct connected to clipped sine output
3	DNC	Input/Output	-	Our test pin, must be unconnected, prohibit VSS connection
4	NC	-	-	Unconnected pin, connected to VSS for power stabilization
5	NC	-	-	Unconnected pin, connected to VSS for power stabilization
6	TEST1	Input/Output	Pull-down	Test pin/ TxDATA input / SPI interface pin Leave floating and make no external connections to this pin if the function of this pin is unused.
7	PD	Input	Pull-down	Our test pin, connected to VSS for noise countermeasures
8	EN	Input	Pull-down	Enable input, SPI interface pin
9	SCK	Input	Pull-down	SPI clock input
10	SDIO	Input/Output	Pull-down	SPI data input/output
11	LVDDL	Output	-	Built-in power supply monitor pin for digital circuits When connecting a bypass capacitor, it should be 1000pF or less
12	CKOUT	Output	-	Clock output
13	NC	-	-	Unconnected pin, connected to VSS for power stabilization
14	NC	-	-	Unconnected pin, connected to VSS for power stabilization
15	NC	-	-	Unconnected pin, connected to VSS for power stabilization
16	NC	-	-	Unconnected pin, connected to VSS for power stabilization
17	NC	-	-	Unconnected pin, connected to VSS for power stabilization
18	NC	-	-	Unconnected pin, connected to VSS for power stabilization
19	VSSPA	Power	-	GND for PA
20	PAOUT	Output	-	Power Amp output
21	RFC	Output	-	RF choke coil
22	LVDDA	Output	-	Built-in power supply monitor pin for analog circuits When connecting a bypass capacitor, it should be 1000pF or less.
23	VDD	Power	-	Positive power supply
24	VSS	Power	-	GND
EDP	VSS	Power	-	GND

※EDP： Exposed Die Pad

5. Electrical Characteristics

5.1. Absolute Maximum Rating

Table 5.1 Absolute Maximum Rating

Item	Symbol	Condition	Standard			Unit
			Min.	Typ.	Max.	
Supply voltage	VDD	VSS = 0 V	-0.3	-	4.0	V
Input voltage	V_{in1}	VSS = 0 V, except CKIN pin	VSS – 0.3	-	VDD + 0.3	V
	V_{in2}	VSS = 0 V, CKIN pin	VSS – 0.3	-	1.8	V
Storage temperature	Tstg	Store as bare product	-40	-	+125	°C

5.2. DC Characteristics

Table 5.2 Power Supply, Operating Temperature

VSS = 0 V, Ta = -40°C to +85°C

Item	Symbol	Condition	Standard			Unit
			Min.	Typ.	Max.	
Supply voltage	VDD	-	1.8	3.0	3.6	V
Supply current Powerdown Mode	I_{DDPD}	VDD = 3.0 V, Ta = 25°C	-	20	100	nA
		VDD = 3.6 V, Ta = 85°C*1	-	-	900	
Supply current CKBUF-Active Mode	I_{DDAT}	-	-	860	1100	µA
Supply current PLL-Active Mode	I_{DDPLL}	F_{TX} = 315 MHz, F_{PLL} = 630 MHz	-	2.2	2.5	mA
		F_{TX} = 915 MHz, F_{PLL} = 915 MHz*1	-	2.5	2.8	mA
Supply current Transmitter-Active Mode	I_{DDTMA}	F_{TX} = 315 MHz, HPWR = 1, PADUTY = 10b				
		Pout = 5 dBm, AM* = 0x1A*1	-	10.0	11.0	mA
		Pout = 8 dBm, AM* = 0x29*1	-	12.7	13.7	
		Pout = 10 dBm, AM* = 0x36	-	15.0	16.0	
		F_{TX} = 433MHz, HPWR = 1, PADUTY = 10b				
		Pout = 5 dBm, AM* = 0x16*1	-	10	11	mA
		Pout = 8 dBm, AM* = 0x24*1	-	12.5	13.5	
		Pout = 10 dBm, AM* = 0x30*1	-	14.5	15.5	
		F_{TX} = 868 MHz, HPWR = 1, PADUTY = 01b				
		Pout = 5 dBm, AM* = 0x19*1	-	11.7	12.7	mA
		Pout = 8 dBm, AM* = 0x28*1	-	14.4	15.4	
		Pout = 10 dBm, AM* = 0x35*1	-	16.5	17.5	
		F_{TX} = 915 MHz, HPWR = 1, PADUTY = 01b				
		Pout = 5 dBm, AM* = 0x19*1	-	11.8	12.8	mA
		Pout = 8 dBm, AM* = 0x27*1	-	14.4	15.4	
		Pout = 10 dBm, AM* = 0x34*1	-	16.5	17.5	
CKOUT clock output current	I_{DDCK}	Load capacitance is 15 pF				
		SR = 11b, F_{CKOUT} = 32 MHz*1	-	-	3.0	mA
		SR = 00b, F_{CKOUT} = 2 MHz*1	-	-	0.3	
Operating temperature*1	Ta	-	-40	-	+85	°C
*1 Guaranteed by design, characterization, and/or simulation only and not by production test.						

Table 5.3 Logic I/O, CLK input

VDD = 1.8 V to 3.6 V, VSS = 0 V, Ta = -40 °C to +85 °C

Item	Symbol	Condition	Standard			Unit
			Min.	Typ.	Max.	
High level input voltage	V_{IH}	EN, SCK, SDIO, TEST1	VDD x 0.8	-	VDD + 0.3	V
Low level input voltage	V_{IL}	EN, SCK, SDIO, TEST1	-0.3	-	VDD x 0.2	V
Input clock voltage amplitude	V_{CLK}	Peak-Peak voltage amplitude of the signal input to CKIN	0.5	-	1.5	V
High level output voltage	V_{OH1}	SDIO, TEST1, Io = -0.4 mA	VDD x 0.9	-	-	V
	V_{OH2}	CKOUT, If the SR = 11b is set, Io = -1 mA If the SR = 10b is set, Io = -0.7 mA If the SR = 01b is set, Io = -0.5 mA If the SR = 00b is set, Io = -0.2 mA	VDD x 0.9	-	-	V
Low level output voltage	V_{OL1}	SDIO, TEST1 (4-wire SPI mode), Io = 0.4 mA	-	-	VDD x 0.1	V
	V_{OL2}	CKOUT, If the SR = 11b is set, Io = 1 mA If the SR = 10b is set, Io = 0.7 mA If the SR = 01b is set, Io = 0.5 mA If the SR = 00b is set, Io = 0.2 mA	-	-	VDD x 0.1	V
Pull-down resistor*1	R_{DOWN}	EN, SCK, SDIO, TEST1	-	250	-	kΩ
Input capacitance*1	C_{IN}	EN, SCK, SDIO, TEST1	-	5	-	pF
*1 Guaranteed by design, characterization, and/or simulation only and not by production test.						

Table 5.4 Under Voltage Detector Characteristics

VSS = 0 V, Ta = -40 °C to +85 °C

Item	Symbol	Condition		Standard			Unit
				Min.	Typ.	Max.	
Detector threshold	V_{DECT}	VDD Falling	VDET = 00b	1.75	1.80	1.85	V
			VDET = 01b	1.95	2.00	2.05	V
			VDET = 10b	2.15	2.20	2.25	V
			VDET = 11b	2.35	2.40	2.45	V
Detector release threshold	V_{RELE}	VDD Rising	VDET = 00b	1.95	2.00	2.05	V
			VDET = 01b	2.15	2.20	2.25	V
			VDET = 10b	2.35	2.40	2.45	V
			VDET = 11b	2.55	2.60	2.65	V

5.3. AC Characteristics

Table 5.5 Transmitter Characteristics

VDD = 1.8 V to 3.6 V, VSS = 0 V, Ta = -40 °C to +85 °C

Item	Symbol	Condition	Standard			Unit
			Min.	Typ.	Max.	
Carrier frequency bands	F_{TX}	32MHz clock signal input	300	-	465	MHz
			600	-	930	
Modulation types	-	-	ASK / OOK / FSK			
ASK bit rate*1	R_{ASK}	NRZ	-	-	100	kbps
FSK bit rate*1	R_{FSK}	NRZ	-	-	50	kbps
Carrier frequency resolution	F_{STEP}	Carrier frequency = 300 MHz to 465 MHz	-	-	244	Hz
		Carrier frequency = 600 MHz to 930 MHz	-	-	488	Hz
FSK deviation	F_{DEV}	-	±0.49	-	±996.1	kHz
ASK modulation index*1	A_{DEV}	In OOK setting Ratio between ON and OFF	90	-	-	%
Internal crystal frequency	F_{OSC}	-	-	32	-	MHz
CKOUT output frequency	F_{CKOUT}	See Figure 6.20	0.00049	-	32	MHz
CKOUT rise/fall time*1	tr / tf	Load capacitance15 pF, 20 to 80% VDD				
		SR = 11b	-	-	5	ns
		SR = 10b	-	-	7	ns
		SR = 01b	-	-	10	ns
		SR = 00b	-	-	20	ns
CKOUT symmetry*1	SYM	SR = 11b, load capacitance 15 pF F_{CKOUT} = 32MHz	45	-	55	%
PLL settling time*1	t_{FSTE}	See Figure **6.9** and Figure **6.10**.	-	-	100	µs
SSB phase noise*1 *3	F_{CN}	F_{TX} = 315 MHz				
		1 kHz offset	-	-106	-	
		10 kHz offset	-	-110	-	
		100 kHz offset	-	-106	-	
		1 MHz offset	-	-96	-	
		10 MHz offset	-	-104	-	
		F_{TX} = 915 MHz				
		1 kHz offset	-	-97	-	
		10 kHz offset	-	-103	-	
		100 kHz offset	-	-96	-	
		1 MHz offset	-	-88	-	
		10 MHz offset	-	-99	-	

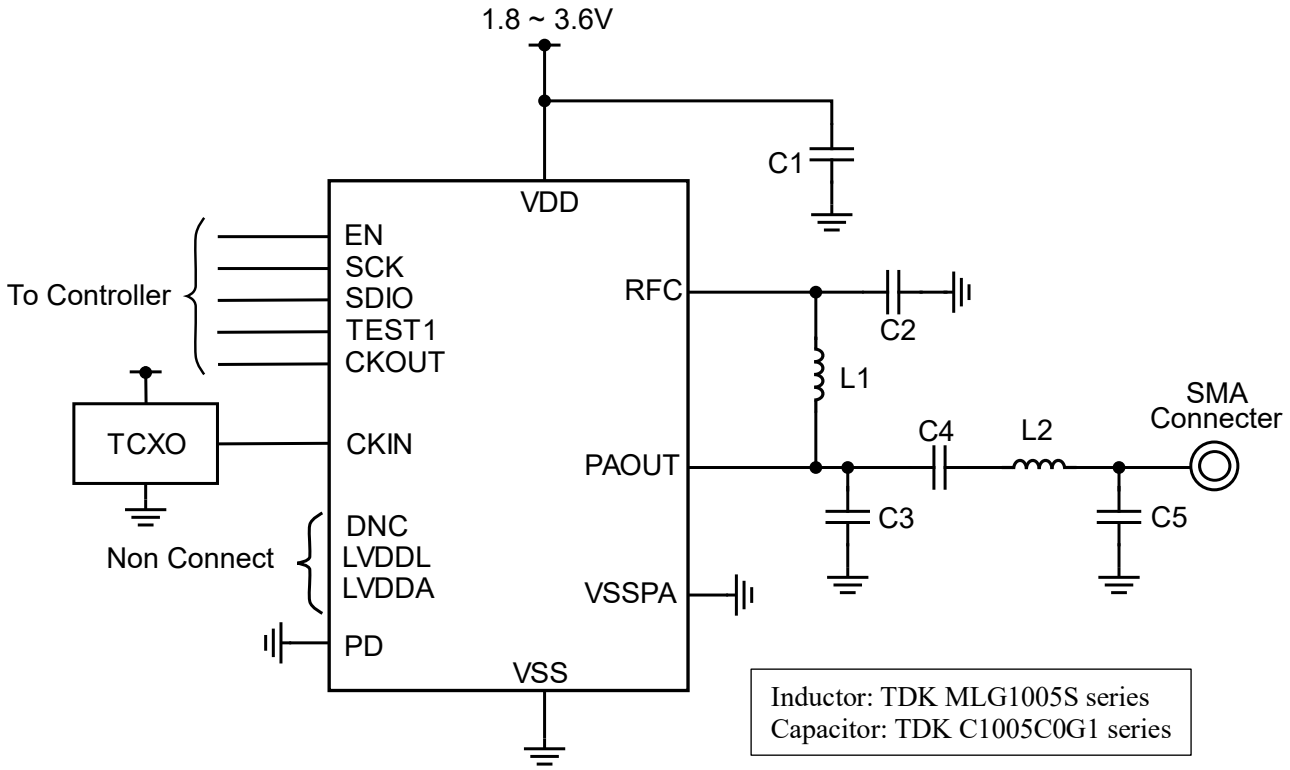
*1 Guaranteed by design, characterization, and/or simulation only and not by production test.
*2 Without aging.
*3 The evaluation results are based on the recommended connection diagram shown in Figure 5.1.

Table 5.6 PA Characteristics

VSS = 0 V

Item	Symbol	Condition	Standard			Unit
			Min.	Typ.	Max.	
Nominal output power*[1, 2, 3]	P_{OUT}	Ta = 25°C, VDD = 3.0 V, F_{TX} = 315 MHz, HPWR = 1, PADUTY = 10b				
		AM* = 0x3F	10.0	11.0	12.0	dBm
		AM* = 0x01	-6.5	-5.5	-4.5	
		Ta = 25°C, VDD = 3.0 V, F_{TX} = 433 MHz, HPWR = 1, PADUTY = 10b				
		AM* = 0x3F	10.5	11.5	12.5	dBm
		AM* = 0x01	-6.0	-5.0	-4.0	
		Ta = 25°C, VDD = 3.0 V, F_{TX} = 868 MHz, HPWR = 1, PADUTY = 01b				
		AM* = 0x3F	9.5	11	12.5	dBm
		AM* = 0x01	-7.0	-5.5	-4.0	
		Ta = 25°C, VDD = 3.0 V, F_{TX} = 915 MHz, HPWR = 1, PADUTY = 01b				
		AM* = 0x3F	9.5	11	12.5	dBm
		AM* = 0x01	-7.0	-5.5	-4.0	
		Ta = 25°C, VDD = 3.0 V, F_{TX} = 315 MHz, HPWR = 0, PADUTY = 10b				
		AM* = 0x3F	1.0	2.0	3.0	dBm
		AM* = 0x01	-16.0	-15.0	-14.0	
Output power temperature dependence*[1, 2]	P_{TMP}	Ta = -40°C to +85°C, VDD = 3.0 V	-1	-	1	dB
Output power supply voltage dependence*[1, 2]	P_{VDD}	Ta = 25°C, VDD = 1.8 V to 3.6 V, VDD = 3.0V				
		AM* > 0x20	-4	-	1	dB
		AM* ≦ 0x20	-1	-	1	dB
Harmonics level*[1, 2]	P_{dBc}	Ta = 25°C, VDD = 3.0 V, AM* = 0x1F, HPWR = Ratio of the 1st and 2nd harmonics				
		F_{TX} = 315 / 433 MHz, PADUTY = 10b	-	-34	-	dBc
		F_{TX} = 868 / 915 MHz PADUTY = 01b	-	-40	-	dBc

*1 Guaranteed by design, characterization, and/or simulation only and not by production test.
*2 Test circuit is shown in Figure 5.1.
*3 Without aging.



F_{TX}	C1	C2	C3	C4	C5	L1	L2
315 MHz	0.1 µF	560 pF	7 pF	82 pF	10 pF	100 nH	39 nH
433 MHz	0.1 µF	560 pF	7 pF	22 pF	10 pF	82 nH	27 nH
868 MHz	0.1 µF	100 pF	3 pF	33 pF	5pF	22 nH	10 nH
915 MHz	0.1 uF	100 pF	3 pF	22 pF	5pF	22 nH	10 nH

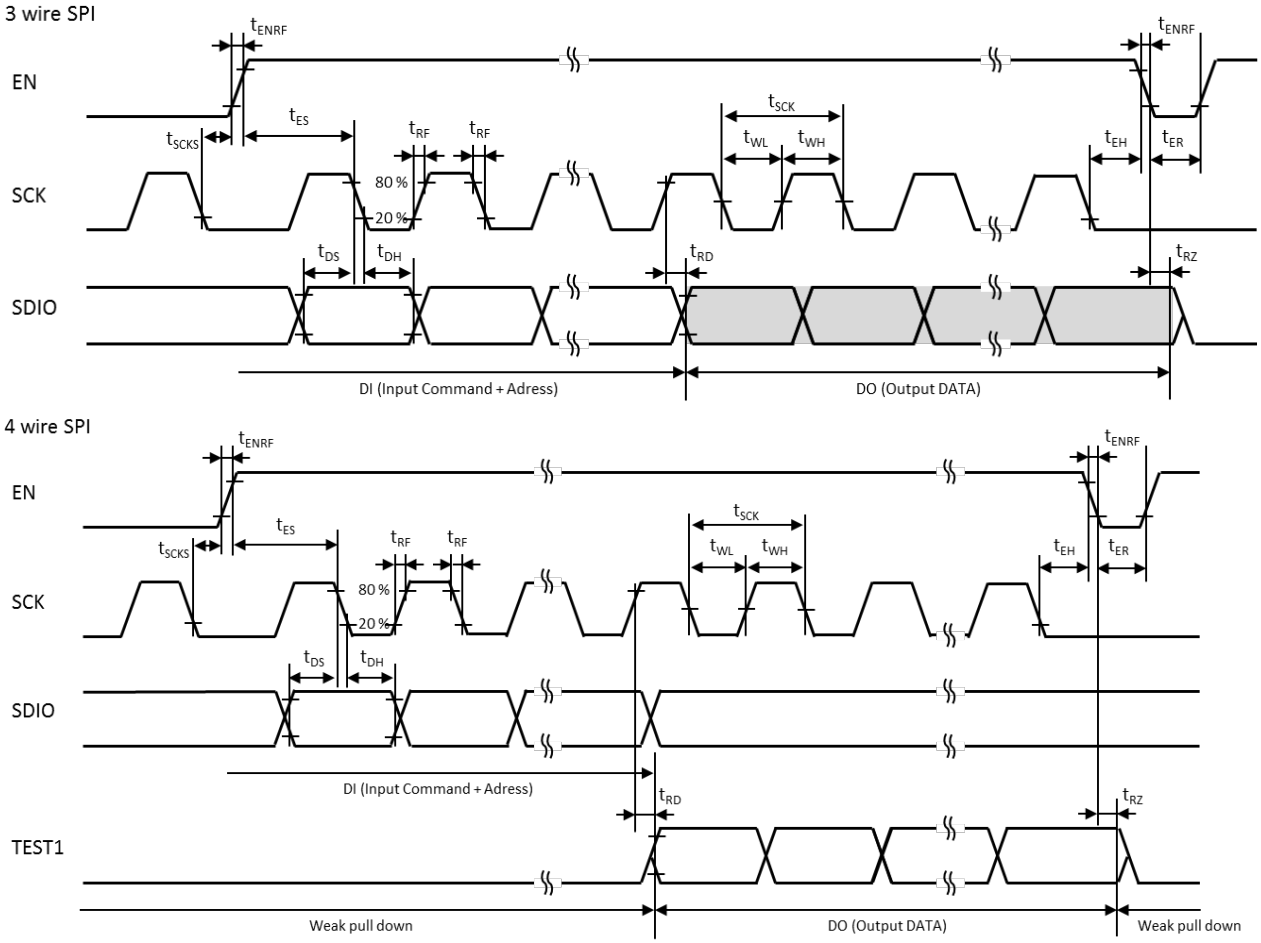
TCXO Recommended product:
Seiko Epson TG2016SMN 32.000000MHz xCGNNx (without ST)
Seiko Epson TG2016SLN 32.000000MHz xCGSNx (with ST）

Figure 5.1 PAOUT AC Test Circuit

Table 5.7 SPI Interface Characteristics

VDD = 1.8 V to 3.6 V, VSS = 0 V, Ta = -40°C to +85°C

Item	Symbol	Condition	Standard			Unit
			Min.	Typ.	Max.	
SCK clock cycle	tSCK	-	330	-	-	ns
SCK H pulse width	tWH	-	150	-	-	ns
SCK L pulse width	tWL	-	150	-	-	ns
SCK rise and fall time	tRF	-	-	-	20	ns
SCK setup time	tSCKS	-	100	-	-	ns
EN setup time	tES	-	150	-	-	ns
EN hold time	tEH	-	100	-	-	ns
EN recovery time	tER	-	100	-	-	ns
EN rise and fall time	tENRF	-	-	-	30	ns
Write data setup time	tDS	-	20	-	-	ns
Write data hold time	tDH	-	20	-	-	ns
Read data delay time	tRD	CL = 50 pF	0	-	100	ns
SDIO output disable time	tRZ	CL = 50 pF	0	-	100	ns



6. Function Description

6.1. Outline

RF transmitter IC S1S77100 is a wireless transmitter IC for the UHF range. This IC houses a PLL and a Power Amp in a 4 mm x 4 mm SQFN package. The S1S77100 can be configured in combination with an external crystal oscillator. So, it is suitable for small wireless devices.

As you can control the wireless transmitter settings via the SPI interface, the S1S77100 supports carrier frequency of 300-465 MHz, 600-930 MHz. You can select ASK, OOK, or FSK modulation. Soft-ASK and Soft-FSK are provided to reduce modulation bandwidth.

This module has a fail-safe function. If a failure is detected, it shuts down the power supply to PA.

The signals of the dividing clock are outputted from the CKOUT pin. They can be used as clock source and interrupt signal for an MCU.

6.2. SPI Interface

The S1S77100 has a 3-wire/4-wire SPI interface.
It is used to access SFR, which controls operations, and to transmit modulated signals using transmit commands.

EN

The EN pin is used to input SPI enable signal, control SPI communications, and input the timing to latch transmission data.
When the EN pin rises, the mode of the S1S77100 is transited from Powerdown mode to CKBUF-Active mode, and 2 MHz (32 MHz divided by 16) is outputted from the CKOUT pin by inputting the clock from an external crystal oscillator. When the EN pin falls, the SPI interface is initialized. If the EN pin is kept low at least 8.2 ms (2^{18} input clocks), the state transits to Powerdown mode.
After sending the transmit command (if bit "B" = 1), the EN pin additional function is available. The SDIO signal is latched as transmission data at the falling edge of the EN signals.

SCK

The SCK pin is the clock input for SPI. This pin is used for loading SDIO data, synchronized with the SCK falling edge.

SDIO

The SDIO pin is the bi-directional data input/output pin for 3-wire SPI mode. It also works as data input pin for 4-wire SPI mode.
The SDIO pin is used for RF transmission data input during RF data transfer. If you select RF transmission data input through the TEST1 pin, the SDIO signals do not affect RF data transmission. See section 6.2.4 for details.

TEST1

The TEST1 pin is used for data output in 4-wire SPI mode.
If you select this pin to data input for RF data transmission, this TEST1 pin becomes the data input pin. See section 6.2.4 for details.

6.2.1. **SPI interface mode change**

The SPI interface mode is changed by setting IFSEL[1:0], which is assigned to SFR address 0x15. (See Table **6.1** and Figure **6.1**.)
When connecting the S1S77100 with MCU in 4-wire SPI mode, you can write data without setting IFSEL[1:0]. To read data, set IFSEL[1:0].

Table 6.1 Interface Mode Setting

IFSEL[1:0]	SPI mode	Transmission data input pin
00b	3-wire SPI mode (default)	SDIO
01b	4-wire SPI mode	SDIO
10b	3-wire SPI mode	TEST1
11b	Invalid	

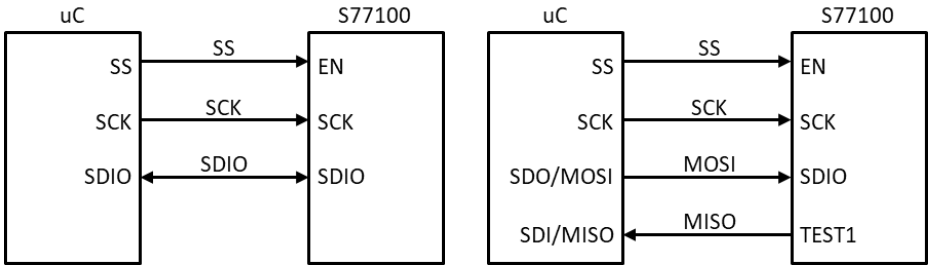


Figure 6.1 HOST Interface Example

6.2.2. **SFR access command**

You can access SFR using 3-wire and 4-wire SPI mode.
Figure 6.2 depicts the timing for writing access in 3-wire and 4-wire SPI modes, **Figure 6.3** shows the timing for read access in 3-wire SPI mode, and **Figure 6.4** shows the timing for read access in 4-wire SPI mode.

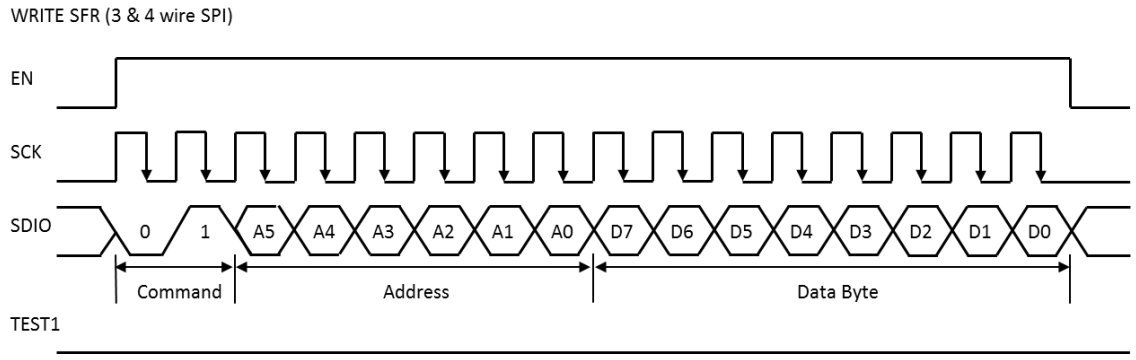


Figure 6.2 Write Access to SFR

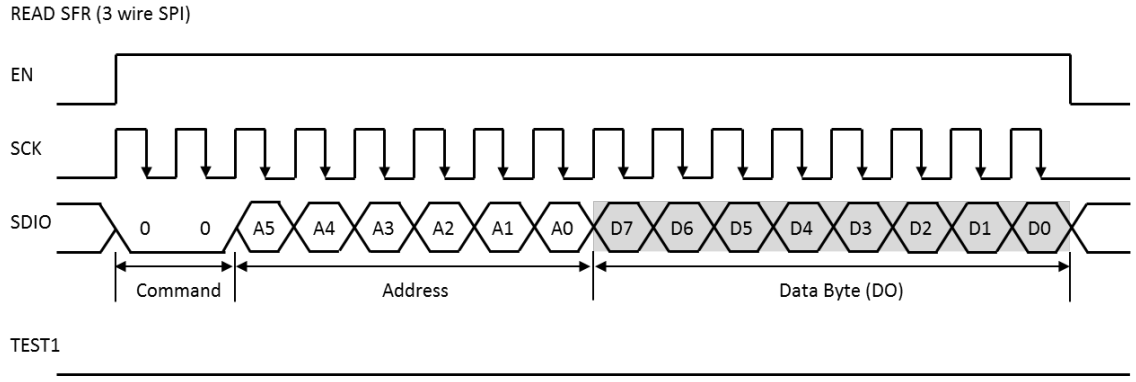


Figure 6.3 3-wire SPI Read Access to SFR

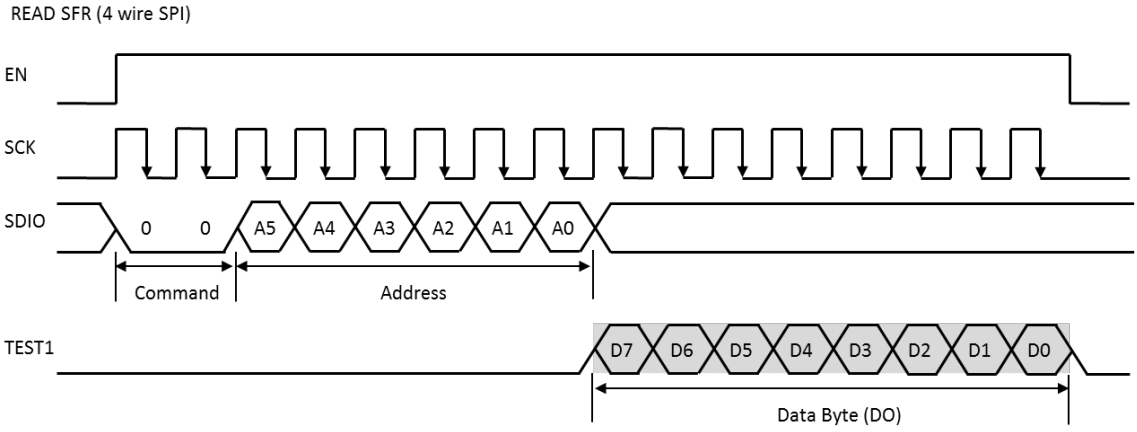


Figure 6.4 4-wire SPI Read Access to SFR

As the loading of data is synchronized with SCK falling, the output data is updated with the SCK rising edge. After the rising of the EN pin, write the 2 bits of the command bit shown in **Table 6.2** and the 6 bits of the address. If the command is SFR writing, the host may continue sending data to be written on SFR. If the command is SFR reading, this device shifts out the data of SFR.

Table 6.2 Command Bit

Command bit	Function
00b	SFR reading
01b	SFR writing
10b	Not available
11b	Transmit command

The S1S77100 supports burst write and read. **Figure 6.5** depicts the timing for burst write access in 3-wire and 4-wire SPI modes, **Figure 6.6** shows the timing for burst read access in 3-wire SPI mode, and **Figure 6.7** shows the timing for burst read access in 4-wire SPI mode. While burst writing & reading, the SFR address is incremented automatically from any address sent by the command address bit.

It is recommended to reset the SFR communication by setting EN pin low after SFR access is finished.
If the EN pin is not set to low, external noise may cause unintentional write access.

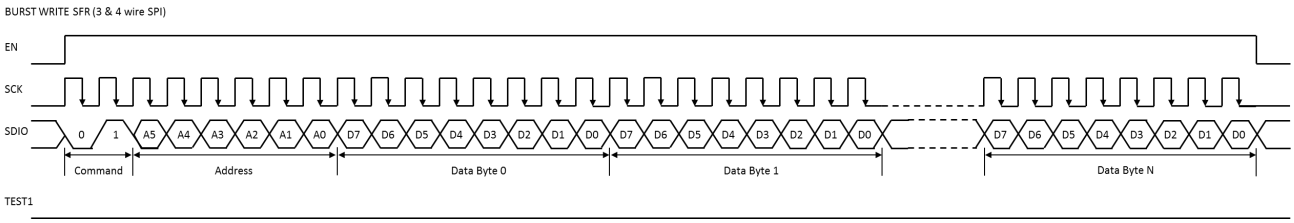


Figure 6.5 Burst Write Access to SFR

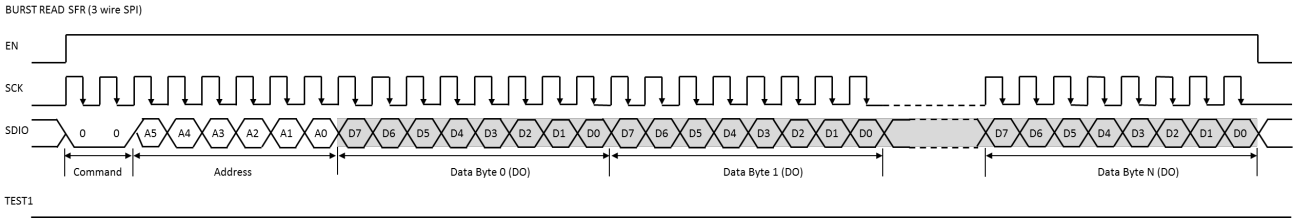


Figure 6.6 3-wire SPI Burst Read Access to SFR

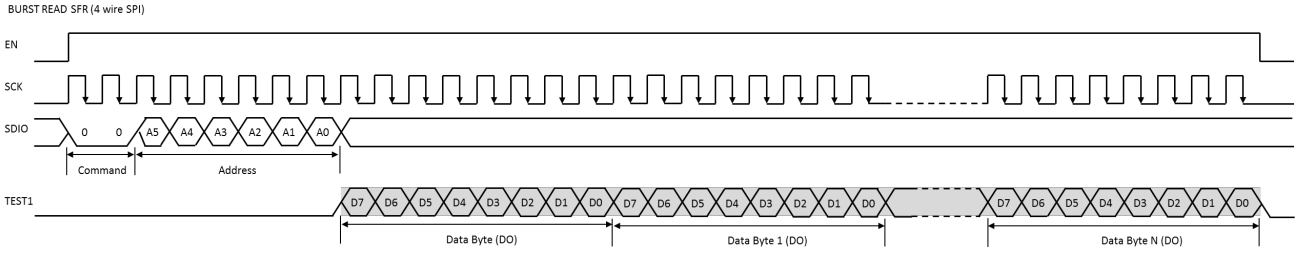


Figure 6.7 4-wire SPI Burst Read Access to SFR

6.2.3. **SPI checksum**

SPI checksum is available (**Figure 6.8**).
The XOR arithmetic calculation of command + address 8 bits and data 8 bits is operated during SFR write access. The checksum result is stored in 0x16 SFR address. The checksum is reset by transiting to Powerdown mode or writing any data to checksum register (address 0x16).

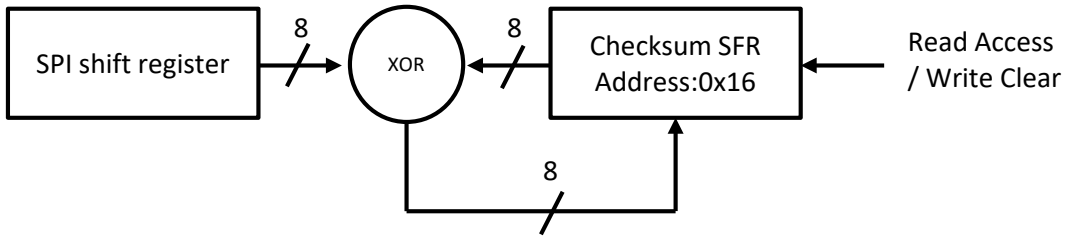


Figure 6.8 SPI Checksum Process Block Diagram

Table 6.3 shows SPI checksum example. If you write 0x02 in address 0x04 and 0x01 in address 0x05, the value 0x02 is stored in checksum register.

Table 6.3 SPI Checksum Calculation Example

Transmission byte by SPI	Checksum result
0100 0100 (Write + Address)	0100 0100
0000 0010 (Data)	0100 0110
0100 0101 (Write + Address)	0000 0011
0000 0001 (Data)	0000 0010

6.2.4. **Transmit command**

The Transmit command is activated when the SPI command bit is set to 11b. The six bits (A to F) that follow the command bit specify the transmit function structure. (See **Table 6.4**) The Transmit command is available only in PLL-Standby mode described in section 6.3.1.

Table 6.4 Details on Transmit Function

Bit	Function	Value, description
A	Data Sync	0: Asynchronous Transmission 1: Synchronous Transmission
B	Power Amp mode	0: PA is turned off with the falling edge of EN pin 1: The SDIO signal is latched as transmission data at the falling edge of EN pin
C	Encoding	0: NRZ 1: Manchester code (Bit "A" must be set to 1.)
D	ASK Modulation Control Setting Selection	0: ASKMC0 1: ASKMC1
E, F	Frequency Channel selection	00: Frequency channel 1 01: Frequency channel 2 10: Frequency channel 3 11: Frequency channel 4

After sending transmit command, wait for PLL settling time (t_{FSTE}), rise SCK. PA is activated, and RF data transmission starts. If you rise SCK before PLL is settled (t_{FSTE}), an unexpected frequency RF signal may be outputted.

Wireless transmission has both an asynchronous transmission mode and synchronous transmission mode. The mode can be selected by bit "A" of the transmission command.

Asynchronous transmission

Figure 6.9 shows asynchronous transmission. In asynchronous transmission mode, the SDIO signals are directly input into the modulator, and the carrier is modulated into ASK/OOK/FSK by transmitting signal.

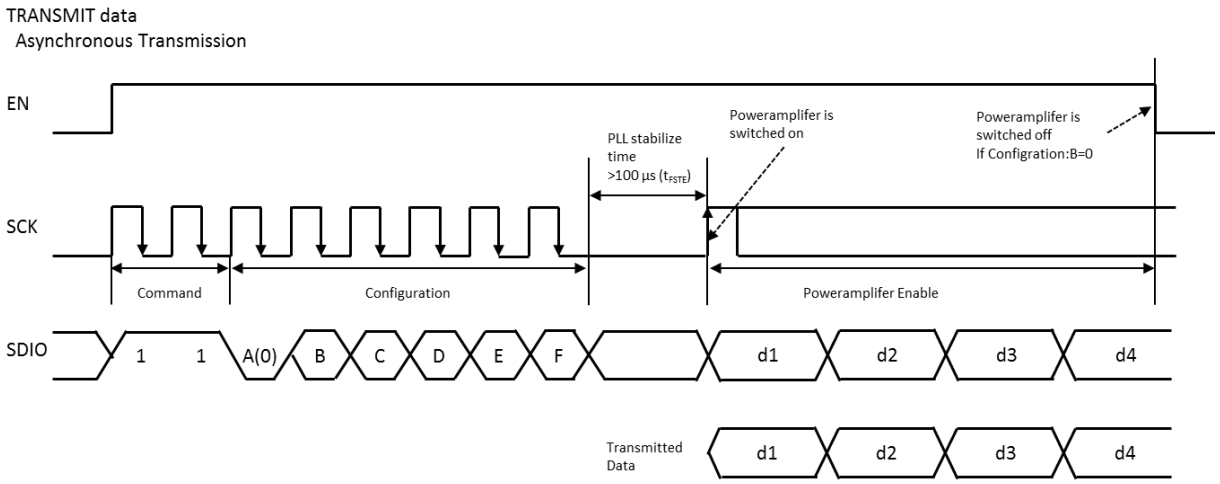


Figure 6.9 Asynchronous Transmission Timing

Synchronous transmission mode

Synchronous transmission timing is shown in **Figure 6.10**. In synchronous transmission mode, SDIO signals are latched by the bitrate signals, and the latched signals are transmitted. The bitrate signal for latch is formed by dividing the frequency for the external crystal oscillator, thus the bitrate signal has same accuracy as the input clock.

Users can output divide clock synchronized with the bitrate signal from CKOUT pin.

If divided clock are supplied to MCU as system clock, please note that clock pulse width may be changed by divider initialization with PA start-up. There may be 1 prescaler clock delay in bitrate signal initialization. See section 6.8 for more details of CKOUT function.

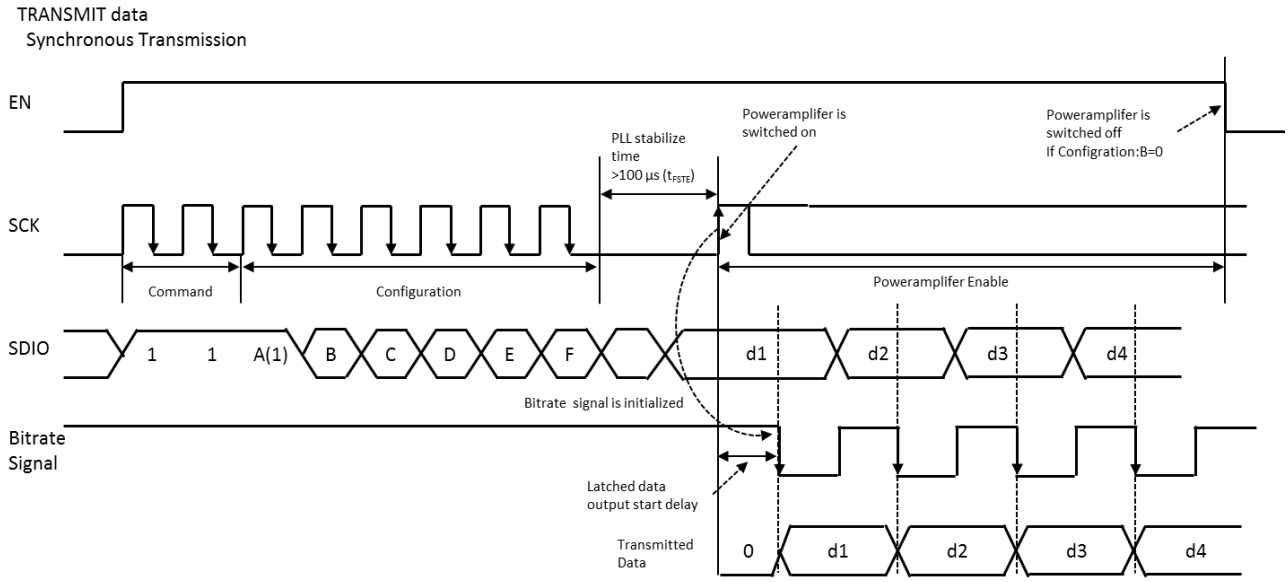


Figure 6.10 Synchronous Transmission Timing

Figure 6.11 shows synchronous transmission example in the following settings: Synchronous transmission (bit "A" = 1), PA is OFF (bit "B" = 0) when EN falls, transmission sign is Manchester code (bit "C" = 1), CKSRC [2:0] = 010b, ASC [2:0] = 1. See section 6.8 for CKOUT settings and details.

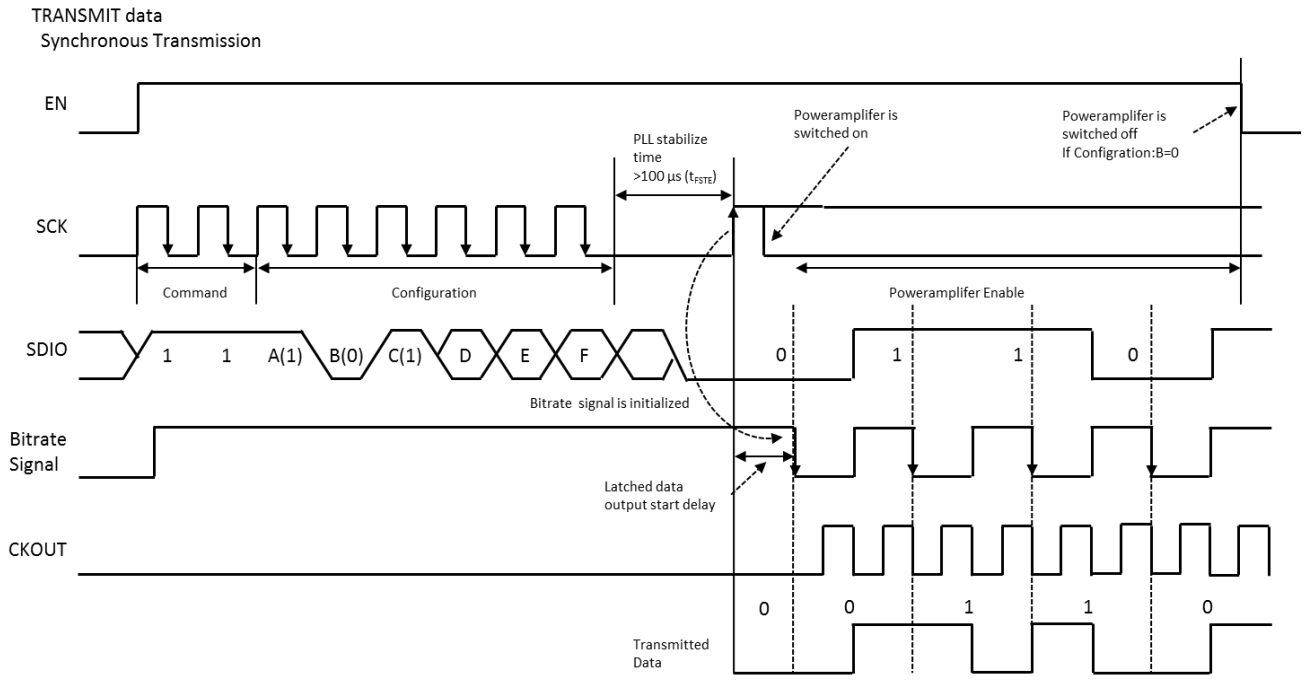


Figure 6.11 Synchronous Transmission Example

Transmission data input process

Transmission signal input method is selected by IFSEL[1:0] setting. Both pins are available in both the synchronous transmission mode and the asynchronous transmission mode. See **Figure 6.12** for transmission signal input timing details through the SDIO pin and **Figure 6.13** for transmission signal input timing details through the TEST1 pin.

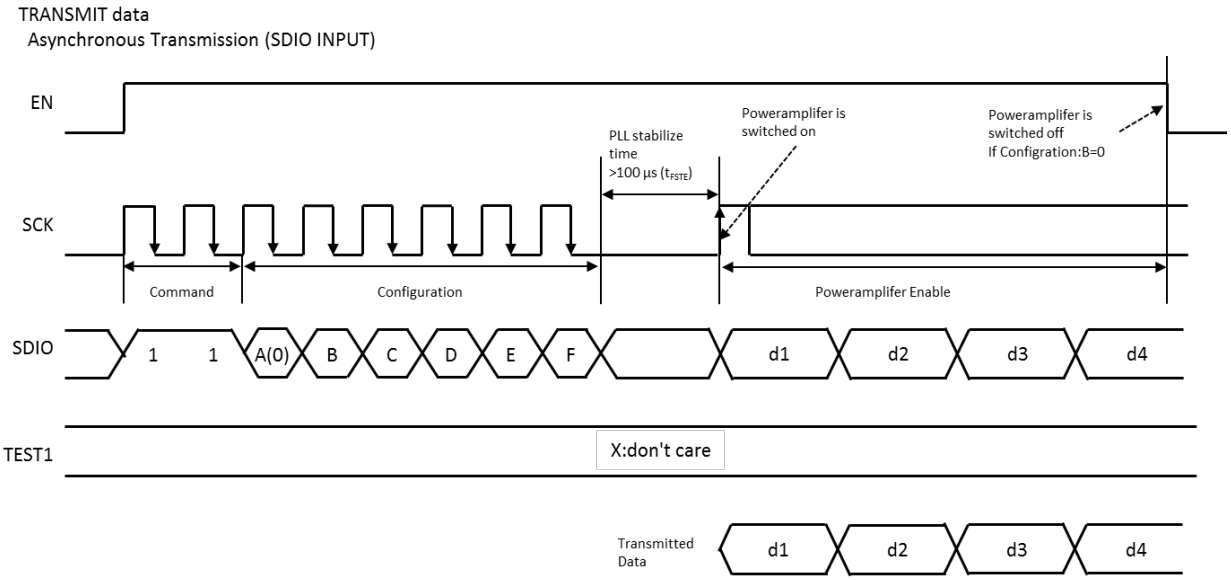


Figure 6.12 Transmission Signal Input Timing Details through SDIO Pin

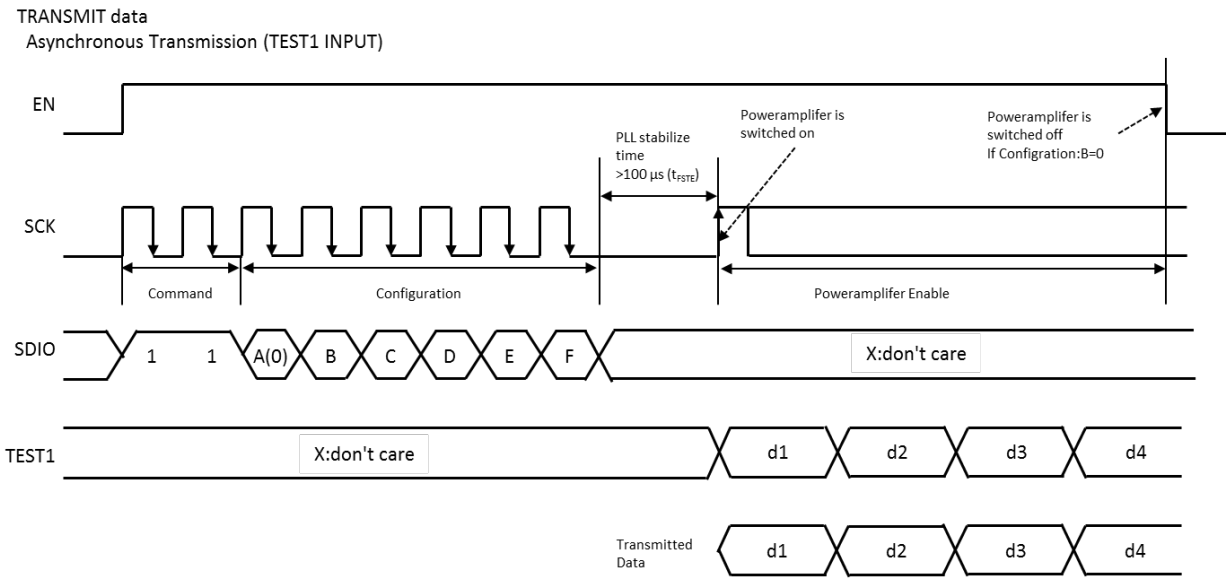


Figure 6.13 Transmission Signal Input Timing Details through TEST1 Pin

6.3. Operating Modes

6.3.1. State transition

The S1S77100 has 4 modes, and you can control state transition using pins or SPI command. The state diagram is shown in **Figure 6.14**. See the section below for details of each mode.

Powerdown mode

In Powerdown mode, minimum required circuits are powered on, and the current consumption is lowest. If the EN pin is kept low for at least 8.2 ms (2^{18} crystal clocks), the mode is transited from any mode to Powerdown mode, and the S1S77100 is reset.
If you want to enter Powerdown mode immediately after the EN pin is set low, write "1" in the bit "PD" in SFR address 0x15.
SFR values related to control are reset, and other SFR values are retained. However, their retention is not guaranteed because the under voltage detection is disabled in Powerdown mode. It is strongly recommended to reprogram all SFR values after exiting from Powerdown mode.
Please note that in states other than the Powerdown state, a clock input to the CKIN pin is required for state transition.

CKBUF-Active mode

In CKBUF-Active mode, the internal voltage regulator, the input clock buffer, and the under voltage detection circuit are activated. With rising edge of the EN pin, the S1S77100 transits from Powerdown mode to CKBUF-Active mode, it takes 100 µs for the clock signal input from the crystal oscillator. After transition to CKBUF-Active mode, 2 MHz (32 MHz divided by 16) is outputted from CKOUT. Users can set other dividing frequency and stop CKOUT with SFR settings. See section 6.8 for more details of CKOUT.
SFR can be accessed through SPI interface even if the input clock.

The S1S77100 enters CKBUF-Active mode when it turns on. Therefore, even if the EN pin is set low before the S1S77100 is turned on, CKOUT outputs clock signals for 8.2 ms (2^{18} crystal oscillator clock) after the clock input.

PLL-Standby mode

The internal voltage regulator, the input clock buffer, and the under voltage detect circuit are activated, and PLL circuit enters stand-by mode. The S1S77100 enters PLL-Standby mode by setting the bit "PLLEN" in SFR address 0x15 to 1.

Transmitter-Active mode

The internal voltage regulator, the input clock buffer, the under voltage detect circuit, PLL circuit and PA are activated, and RF signals are outputted from the PAOUT pin. The S1S77100 enters Transmitter-Active mode by sending a transmit command in PLL-Standby mode. See section 6.2.4 for more details of transmit command.
If the fail-safe function detects a fail while the PA is running in Transmitter-Active mode, the PA can be switched off. (See section 6.7 for details.)
In Transmitter-Active mode, SFR write access is not available. If you want to change SFR settings, change the mode to CKBUF-Active mode or PLL-Standby mode to write SFR values.

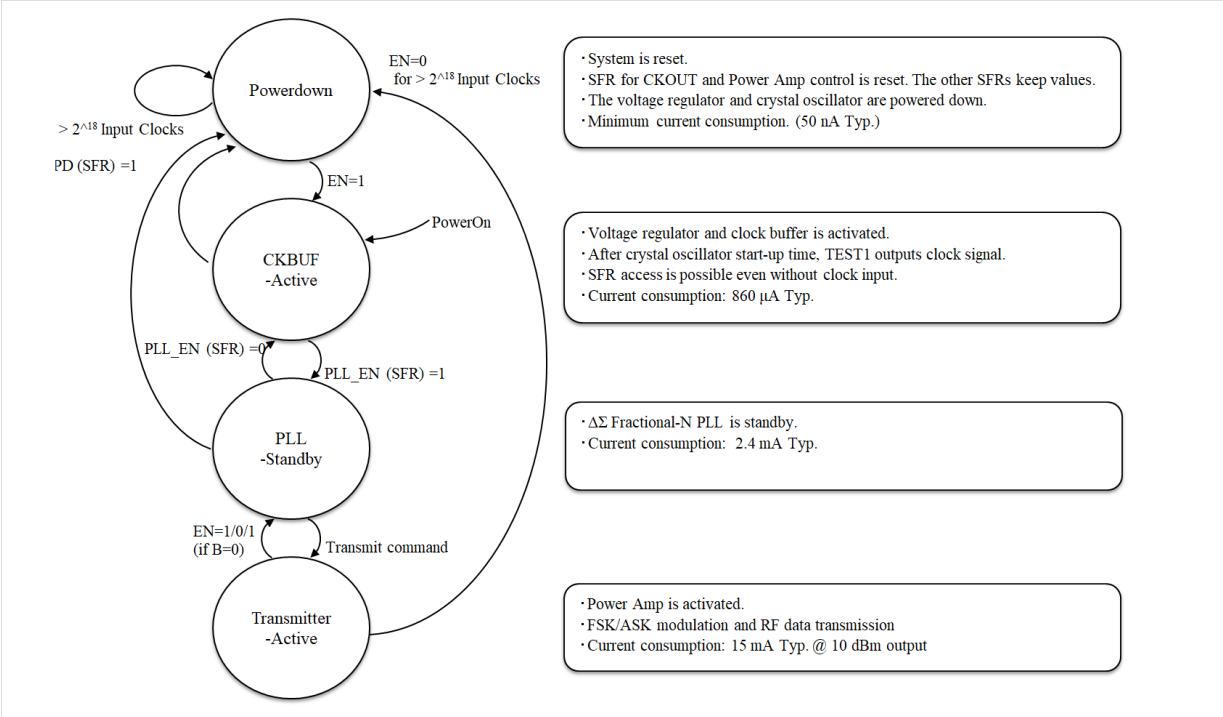


Figure 6.14 State Diagram

6.3.2. **Control signal timing**

An example of control signal timing is shown in **Figure 6.15**.**Figure 6.15** shows a wireless transmission sequence that starts from and goes back to Powerdown mode.
First, the mode is changed from Powerdown mode to CKBUF-Active mode when the EN pin rises. After the EN pin is turned on, the built-in voltage regulator starts up. It is recommended to start clock input from the CKIN pin after 50us when the voltage regulator has stabilized. After inputting the clock, a maximum of 100us is required until the clock is output from CKOUT.
After the transition to CKBUF-Active mode, and transition to PLL-Standby mode becomes available. Since PLL_EN is set to 1 in the SFR_Init process in **Figure 6.15**, the mode is changed to PLL-Standby mode immediately.
The mode is changed to Transmitter-Active mode when a transmit command is sent and the PA is activated by having SCK rise after t_{FSTE} (PLL settling time) has elapsed. The PA stops 100 ns after the falling edge of the EN pin, and the mode is changed to PLL-Standby mode. If the EN pin is kept low for 8.2 ms (2^{18} input clock), the mode is change to Powerdown mode.
If you want to enter Powerdown mode immediately after the EN pin is set low, write "1" in the bit ”PD” in SFR address 0x15.

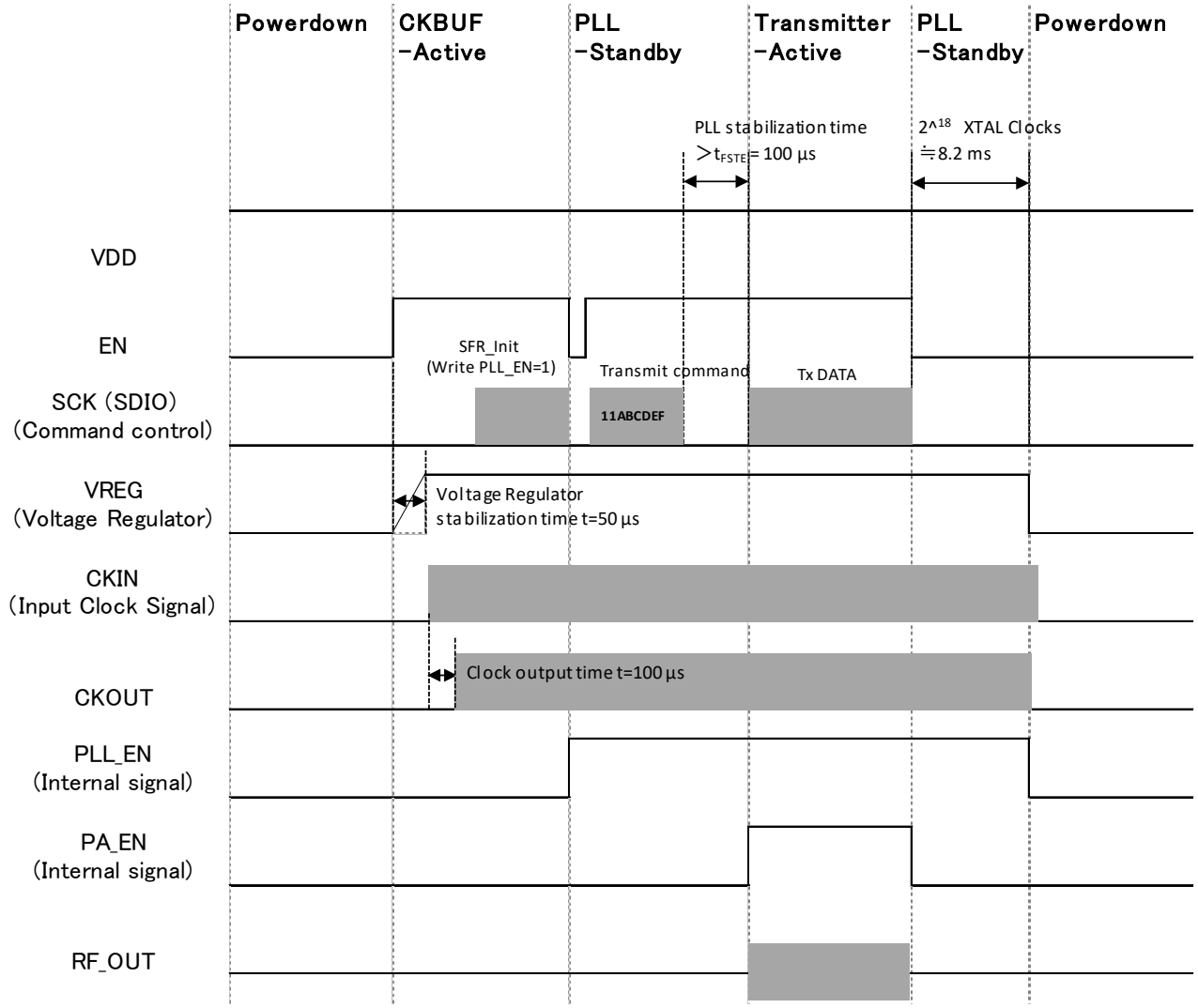


Figure 6.15 Control Signal Timing

6.4. Output Frequency Setting

6.4.1. **Calculation for the frequency setting value**

Carrier frequency (F_{TX}) is determined by the VCO frequency (F_{VCO}) and the division ratio of output divider (ODIV) as shown in formula (1).

$$F_{TX} = \frac{F_{VCO}}{ODIV} \quad \textbf{(1)}$$

VCO frequency (F_{VCO}) must be 600 MHz to 930 MHz. The output divider (ODIV) is determined by this rule and F_{TX} in formula (1). See **Table 6.5** for details.

Table 6.5 f_O and FnODIV

F_{TX} [MHz]	ODIV	FnODIV (SFR address 0x0A)
300 to 465	2	1
600 to 930	1	0

VCO frequency (F_{VCO}) is determined by the reference frequency (F_{REF}), which is supplied from input clock, and the division ratio of feedback divider (N). The division ratio of feedback divider is determined by the integral setting for 4 bits (N_{INT}) and the fractional setting for 16 bits (N_{FRAC}) that enable highly stable frequency settings. The VCO frequency (F_{VCO}) is calculated by formula (2):

$$F_{VCO} = F_{REF} \times N = F_{REF} \times \left(N_{INT} + \frac{4 \times N_{FRAC} + 3}{2^{18}}\right) \quad \textbf{(2)}$$

Output frequency (F_{TX}) is calculated by formula (3):

$$F_{TX} = \frac{F_{VCO}}{ODIV} = F_{REF} \frac{\left(N_{INT} + \frac{4 \times N_{FRAC} + 3}{2^{18}}\right)}{ODIV} \quad \textbf{(3)}$$

For example, if reference frequency (F_{REF}) is 32 MHz and output frequency should be 315 MHz, ODIV is calculated to be "2" by **Table 6.5**. Then the division settings of feedback divider (N, N_{INT}, and N_{FRAC}) are calculated by formulas (4) to (6) based on formula (2).

$$N = N_{INT} + \frac{4 \times N_{FRAC} + 3}{2^{18}} = \frac{F_{OUT} \times ODIV}{F_{REF}} = \frac{315 \times 10^6 \times 2}{32 \times 10^6} = 19.6875 \quad \textbf{(4)}$$

$$N_{INT} = floor(N) = floor(19.6875) = 19 \quad \textbf{(5)}$$

$$N_{FRAC} = \frac{(N - N_{int}) \times 2^{18} - 3}{4} = \frac{(19.6875 - 19) \times 2^{18} - 3}{4} \cong 45055 = 0xAFFF \quad \textbf{(6)}$$

Table 6.6 shows N_{INT} and SFR parameters.
N_{INT} is 4 bits and N_{FRAC} is 16 bits. You can set different N_{INT} values and N_{FRAC} values in each frequency channel of the SFR. (SFR address 0x00 to 0x09).
For example, if you want to set N_{INT} and N_{FRAC}, which are calculated by formula (6), to the channel 1, make the following settings:
SFR address 0x00, F1FRAC[15:8] = 0xAF
SFR address 0x01, F1FRAC[7:0] = 0xFF
SFR address 0x04, F1INT[3:0] = 0x03
See chapter 7 for details.

Table 6.6 N_{INT} and SFR Parameters

N_{INT}	FnINT[3:0] (SFR address 0x04, 0x09)
16	0x0
17	0x1
18	0x2
19	0x3
20	0x4
21	0x5
22	0x6
23	0x7
24	0x8
25	0x9
26	0xA
27	0xB
28	0xC
29	0xD
30	0xE
31	0xF

6.5. FSK Modulator

6.5.1. **FSK deviation setting**

You can set FSK deviation in SFR address 0x0B. FSK modulation (F_{DEV}) is calculated by formula (7). F_{REF} is the reference frequency of crystal oscillator. FDEV, FDEV4X and FDEV2X are SFR setting values.

$$F_{DEV} = \pm \frac{F_{REF} \times FDEV}{2^{16}} \times 4^{FDEV4X} \times 2^{FDEV2X} \quad \textbf{(7)}$$

For example, if you set FDEV to 31, FDEV4X to 0, and FDEV2X to 0, FSK deviation (F_{DEV}) is calculated by formula (8).

$$F_{DEV} = \pm \frac{F_{REF} \times FDEV}{2^{16}} \times 4^{FDEV4X} \times 2^{FDEV2X} = \pm \frac{32 \times 10^6 \times 31}{2^{16}} \times 4^0 \times 2^0 \cong \pm 15.136\ kHz \quad \textbf{(8)}$$

Carrier frequency is modulated to $F_{TX} + F_{DEV}$ in high level data transmission and to $F_{TX} - F_{DEV}$ in low level data transmission.

6.5.2. **Soft-FSK**

Soft-FSK function is implemented to reduce FSK modulation bandwidth. In Soft-FSK, modulation is applied in ramp shape shown in **Figure 6.16**.

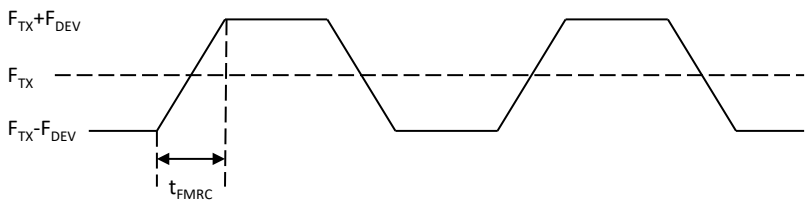


Figure 6.16 Soft-FSK Modulation Wave

t_{FMRC} shown in **Figure 6.16** is calculated by formula (9). The FMRC in formula (9) determines the inclination of ramp shape and is assigned to SFR address 0x10.

$$t_{FMRC} = 0DIV \times 2 \times FDEV \times FMRC \times \frac{1}{F_{REF}} \quad \textbf{(9)}$$

6.6. Output Power Setting

6.6.1. **ASK modulation**

You can make settings for PA output power and ASK modulation in SFR address 0x0C to 0x0E. See chapter 7 for details of SFR addresses. This section provides the details of each bit.

ASKMC0/ASKMC1 selection

8 bits are assigned to SFR address 0x0C (ASKMC0) and 0x0D (ASKMC1). The ASKMC means ASK Modulation Control. The 8 bits consist of ASK/FSK modulation setting, output power range setting, and output power minor adjustment.
You can select ASKMC0 or ASKMC1 using the transmit command bit "D" just before transmission.

ASKn

ASKn switches ASK modulation and FSK modulation (n = 0/1, ASK0 or ASK1). See **Table 6.7** for details.

Table 6.7 ASKn Settings

ASKn	Modulation method
0	FSK
1	ASK

HPWRn

HPWRn switches output power range (n = 0/1, HPWR0 or HPWR1). See **Table 6.8** for details.

Table 6.8 HPWRn Settings

HPWRn	Output power range
0	-15 dBm to 0 dBm
1	-5 dBm to 11 dBm

AMHn[5:0]

AMHn[5:0] is output power setting in H level data transmission for ASK (n = 0/1, AMH0[5:0] or AMH1[5:0]). It is also output power setting for FSK.

AML[5:0]

AML[5:0] is output power setting in L level data transmission for ASK modulation. If you set AML[5:0] = 000000b, the PAOUT pin goes OFF, which means OOK mode.

PADUTY[1:0]

The function of changing duty cycle is implemented to improve the PA efficiency. See **Table 6.9** for setting values and nominal duty cycle. You may improve PA efficiency by making the shape duty small and the on-time in output transistor small. However, since harmonics spurious is also changed, check output power, current consumption, and harmonics spurious before use if you change recommended values.
Recommended values based on the test circuit shown in **Figure 5.1**: 10bfor F_{TX} = 300 MHz to 465 MHz, 01b for F_{TX} = 600 MHz to 930 MHz.

Table 6.9 PADUTY[1:0] Setting

PADUTY[1:0]	Nominal duty cycle	
	F_{TX} = 300 MHz to 465 MHz	F_{TX} = 600 MHz to 930 MHz
00b	50%	50%
01b	45%	36%
10b	36%	Not available
11b	30%	Not available

6.6.2. **Soft-ASK**

Soft-ASK function is implemented to reduce the ASK modulation bandwidth. In Soft-ASK, modulation is applied in ramp shape shown in **Figure 6.17**.

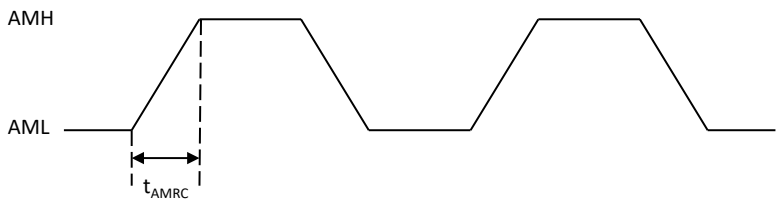


Figure 6.17 Soft-ASK Modulation Wave

t_{AMRC} shown in **Figure 6.17** is calculated by formula (10). The AMRC of formula (10) determines the inclination of ramp shape and is assigned to SFR address 0x0F.

$$t_{AMRC} = (\mathrm{AMH} - \mathrm{AML}) \times AMRC \times \frac{1}{F_{REF}} \quad \textbf{(10)}$$

The AMRC setting also works for FSK modulation. The load for power supply is reduced by applying ramp shape to start-up PA current consumption.

6.6.3. **Antenna tuning**

The PA has a variable capacitor array for antenna tuning. It is connected between the PAOUT pin and the VSS pin. Its capacitance is controlled by ATT [4:0] in SFR address 0x13. See **Table 6.10** for setting values and capacitance.

Table 6.10 ATT [4:0] Settings

ATT [4:0]	Capacitance
0	184 fF
1	223 fF
2	262 fF
- -	- -
31	1393 fF

6.7. Fail-safe Function

The S1S77100 has three kinds of fail-safe functions. If a fail is detected, the PA is turned off according to fail-safe settings.
This function detects PLL loss of lock, VCO auto-calibration errors, and under voltage. Error results are stored in SFR address 0x14 and can be read out. Error results are reset by transition to Powerdown mode or writing any data to SFR address 0x14.
You can change PA control using the bit "FSOFF" in SFR address 0x15. If the FSOFF = 0, PA turns off when a fail is detected. If the FSOFF = 1, PA does not turn off when a fail is detected.
When FSOFF = 0 and a fail is detected, PA does not turn on after transition to Transmitter-Active mode if error flags are not reset.

6.7.1. PLL Loss of Lock detection

The Loss of Lock detector works in the Transmitter-Active mode. It always compares the reference signal frequency and the feedback signal frequency, which are input in the phase frequency detector in the PLL, using logic counter. If PLL locks, the frequencies of reference signals and feedback signals are the same. If the frequency difference between reference signals and feedback signals exceeds threshold, the detector judges it as an error. Error detection results are stored in the PLLDER in SFR address 0x14.

6.7.2. VCO auto-calibration error detection

After sending transmit command, VCO in the PLL is automatically calibrated during t_{FSTE} (100 μs). If the result of this calibration exceeds the threshold, it is determined that oscillation frequency is not correct, and an error is detected. Error detection results are stored in the VCOCER in SFR address 0x14.

6.7.3. Under voltage detection

The supply voltage is always monitored in CKBUF-Active mode, PLL-Standby mode, and Transmitter-Active mode. If the supply voltage becomes lower than detecting threshold, an error is detected until the supply voltage exceeds release threshold. You can set the detecting threshold and release threshold using VDET [1:0] in SFR address 0x13.
See Table **5.3** for details.
Error detection results are stored in the VDETER in SFR address 0x14.
Figure 6.18 and **Figure 6.19** show the details of under voltage and VDETER reset timing. Error results are reset by SFR write clear in **Figure 6.18** and by transition to Powerdown mode in **Figure 6.19**.

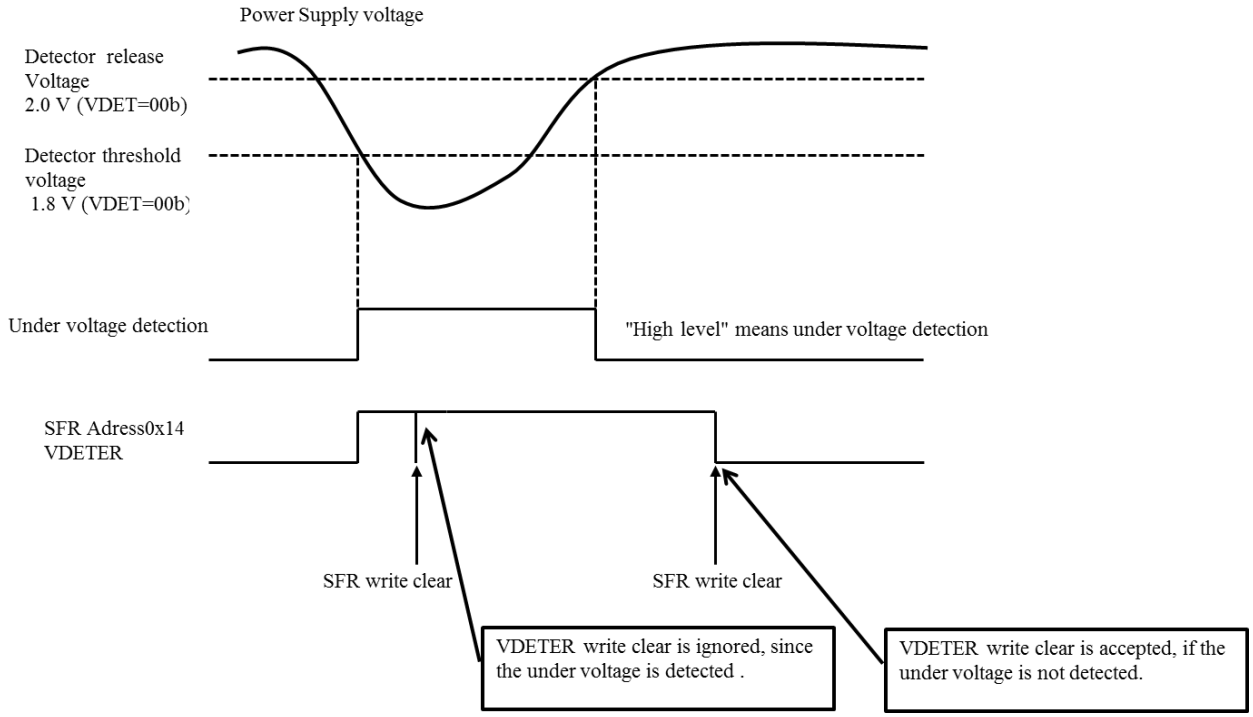


Figure 6.18 Reset of Under Voltage Detection Results by SFR Write Clear

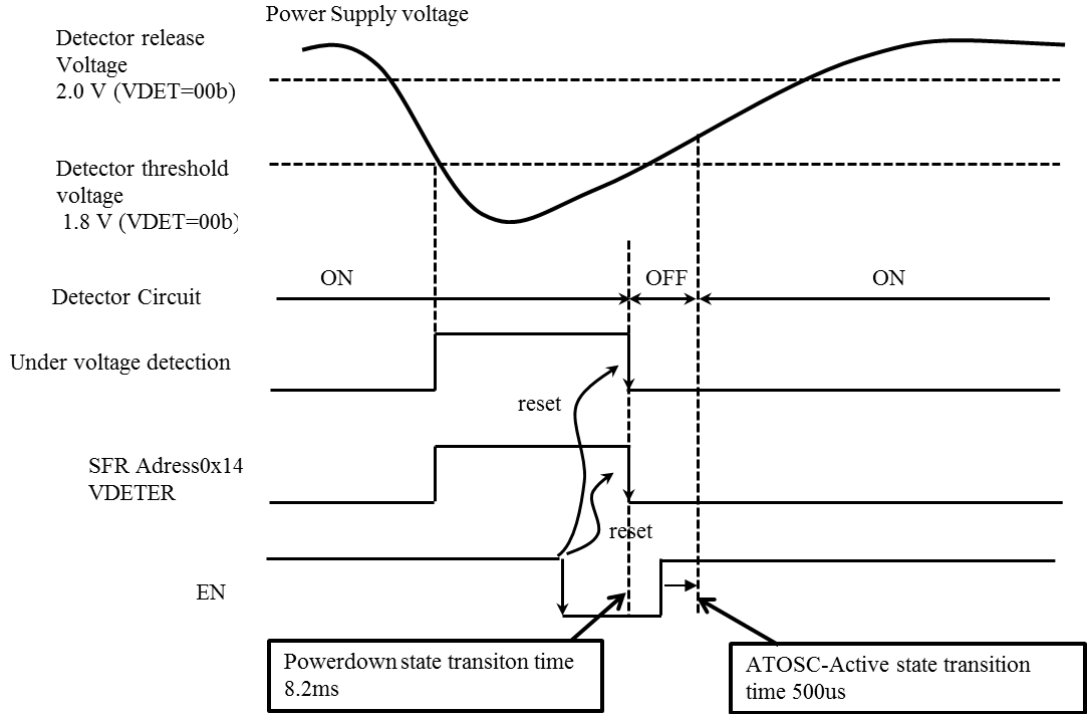


Figure 6.19 Reset of Under Voltage Detection Results by Transition to Powerdown Mode

6.8. Clock Output (CKOUT) Function

6.8.1. **Frequency divider**

The frequency divider structure for CKOUT/bitrate signal is shown in **Figure 6.20**. The frequency divider for CKOUT/bitrate signal consists of three programmable dividers and two fixed dividers.
You can select signals output from the CKOUT using CKSRC[2:0] in SFR address 0x12h. The detail of CKSRC[2:0] is shown in **Table 6.11**. CKSRC[2:0] is reset to 000b when the mode is changed to Powerdown mode. Therefore, 2 MHz (Fref/16) is outputted from the CKOUT pin right after the mode is changed from Powerdown mode to CKBUF-Active mode.

The “Bitrate Signal” shown in **Figure 6.20** is a signal for latch of SDIO pin data in synchronous communication mode. It is same as the "Bitrate Signal" shown in **Figure 6.10** and **Figure 6.11**.

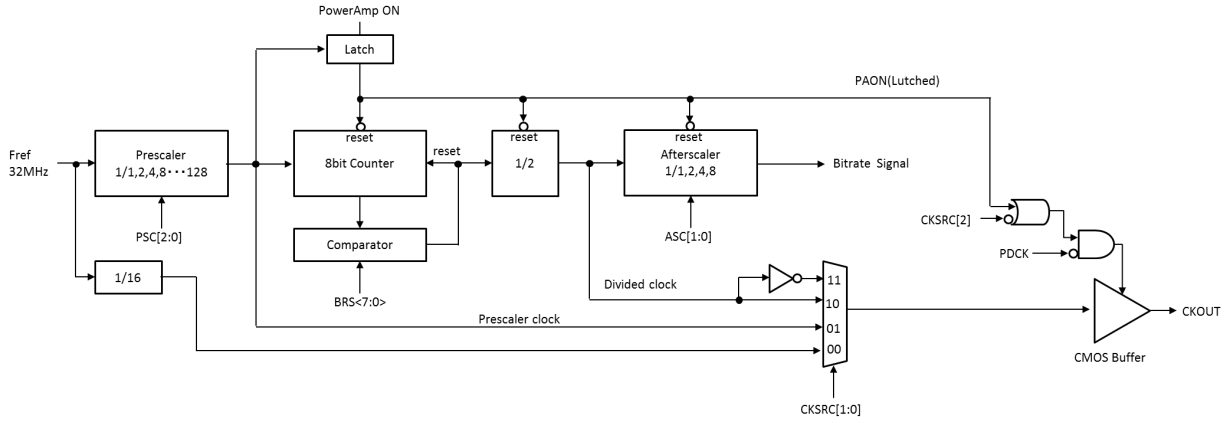


Figure 6.20 Frequency Divider Structure for CKOUT/Bitrate Signal

Table 6.11 CKSRC[2:0] Setting

CKSRC[2:0]	CKOUT
000b	Fref / 16
001b	Prescaler clock
010b	PAON: 0 "Low" PAON: 1 Divided clock
011b	PAON: 0 "High" PAON: 1 Inverted divided clock
100b	PAON: 0 High-Z PAON: 1 Fref / 16
101b	PAON: 0 High-Z PAON: 1 Prescaler clock
110b	PAON: 0 High-Z PAON: 1 Divided clock
111b	PAON: 0 High-Z PAON: 1 Inverted divided clock

6.8.2. **Frequency divider setting**

The settings for "Prescaler" shown in **Figure 6.20** is made in PSC[2:0] in SFR address 0x12. See **Table 6.12** for details.

Table 6.12 PSC[2:0] Setting

PSC[2:0]	Division ratio
0	1/1
1	1/2
2	1/4
3	1/8
4	1/16
5	1/32
6	1/64
7	1/128

The settings for "Comparator" shown in **Figure 6.20** is made in BRS[7:0] in SFR address 0x11. See **Table 6.13**.

Table 6.13 BSC[7:0] Setting

BRS[7:0]	Division ratio
0	1/1
1	1/2
2	1/3
3	1/4
4	1/5
-	-
-	-
255	1/256

The settings for "Afterscaler" shown in **Figure 6.20** is made in ASC[2:0] in SFR address 0x12. See **Table 6.14** for details.

Table 6.14 ASC[2:0] Setting

ASC[2:0]	Division ratio
0	1/1
1	1/2
2	1/4
3	1/8

6.8.3. Output CMOS driver

The slew rate of CMOS driver for CKOUT pin is selectable. Make settings in SR[1:0] in SFR address 0x0A. 00b is the minimum, and 11b is the maximum.
The SR[1:0] is reset to 00b when the mode is changed to Powerdown mode. 2 MHz (Fref/16) is outputted from the CKOUT pin when the mode is changed from Powerdown mode to CKBUF-Active mode. SR[1:0] = 00b is optimum for 2 MHz output. After that, if you want to output higher frequency signals from the CKOUT pin, make SR[1:0] settings for required rise/fall time.
Table 6.15 shows division ratio and recommended SR[1:0] values for respective frequencies.

Table 6.15 Recommended SR[1:0] Setting

CKOUT frequency [MHz]	PSC[2:0]	Division ratio	SR[1:0] recommended setting*
32	0	1/1	11b
16	1	1/2	10b
8	2	1/4	01b
4	3	1/8	00b
2	4	1/16	00b

* CKOUT pin load capacitance = 15 pF

6.9. Status Monitor

6.9.1. Transition counter

The TXCOUNT[3:0] in SFR address 0x14 stores the number of transition to Transmitter-Active mode. Users can check the number by reading SFR. The value is reset to zero when the counter overflows.
It is reset by transition to Powerdown mode or by writing any data in the SFR address 0x14.

6.9.2. Oscillation status monitor

The S1S77100 has a circuit that detects crystal oscillator amplitude. Detection results are stored in the OSCDET in SFR address 0x14. This function enables stable output clock signals by controlling the start of output from the CKOUT pin based on the detection results.

7. SFR (Special Function Register)

7.1. SFR List

Name	Description	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Reset Value
F1FRAC1	Freq1 Fractional setting 1	0x00	F1FRAC[15:8]								xxxx xxxx b
F1FRAC0	Freq1 Fractional setting 0	0x01	F1FRAC [7:0]								xxxx xxxx b
F2FRAC1	Freq2 Fractional setting 1	0x02	F2FRAC [15:8]								xxxx xxxx b
F2FRAC0	Freq2 Fractional setting 0	0x03	F2FRAC [7:0]								xxxx xxxx b
F1_2INT	Freq1/Freq2 Integer setting	0x04	F1INT[3:0]				F2INT[3:0]				xxxx xxxx b
F3FRAC1	Freq3 Fractional setting 1	0x05	F3FRAC [15:8]								xxxx xxxx b
F3FRAC0	Freq3 Fractional setting 0	0x06	F3FRAC [7:0]								xxxx xxxx b
F4FRAC1	Freq4 Fractional setting 1	0x07	F4FRAC [15:8]								xxxx xxxx b
F4FRAC0	Freq4 Fractional setting 0	0x08	F4FRAC [7:0]								xxxx xxxx b
F3_4INT	Freq3/Freq4 Integer setting	0x09	F3INT[3:0]				F4INT[3:0]				xxxx xxxx b
ODIV	Output Divider Setting	0x0A	FDEV4X	FDEV2X	SR1[1:0]		F1ODIV	F2ODIV	F3ODIV	F4ODIV	xx00 xxxx b
FDEV	FSK Deviation	0x0B	FDEV[7:0]								xxxx xxxx b
ASKMC0	ASK Modulation Control 0	0x0C	ASK0	HPWR0	AMH0[5:0]						xxxx xxxx b
ASKMC1	ASK Modulation Control 1	0x0D	ASK1	HPWR1	AMH1[5:0]						xxxx xxxx b
ASKMC2	ASK Modulation Control 2	0x0E	PADUTY[1:0]		AML[5:0]						xxxx xxxx b
PARAMP	ASK Modulation Ramp Control	0x0F	AMRC[7:0]								xxxx xxxx b
FSKRAMP	FSK Modulation Ramp Control	0x10	FMRC[7:0]								xxxx xxxx b
BRS1	Bitrate Setting 1	0x11	BRS[7:0]								xxxx xxxx b
BRS2	Bitrate Setting 2	0x12	CKSRC[2:0]			PSC[2:0]			ASC[1:0]		000x xxxx b
ATUNE	VDET setting / Antenna Tuning	0x13	-	VDET[1:0]		ATT[4:0]					xxxx xxxx b
TXSTAT	Transmitter Status Register	0x14	TXCOUNT[3:0]				OSCDET	VDETER	VCOCER	PLLDER	0000 x000 b
TXCON	Transmitter Control	0x15	PD	PDCK	FSOFF	IFSEL[1:0]		-	-	PLLEN	0000 0xx0 b
SPICKSUM	SPI Checksum register	0x16	SPICKSUM[7:0]								0000 0000 b

Note: Do not write values in the addresses not listed above.
Write zero to unidentified bits.
The “Reset Value” shows the values reset when the mode is changed to Powerdown mode. The “x” means that the values are retained and not reset). However, their retention is not guaranteed in Powerdown mode. Write desirable values again in all SFR addresses after exiting from Powerdown mode.

The register types described in the following sections:
R/W: Read/Write
R/O: Read only
W/O: Write only
R/C: Read only/Write clear

7.2. PLL Fractional Setting: Frequency Channel 1

Address	Register name	Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	F1FRAC1	F1FRAC[15:8]							
0x01	F1FRAC0	F1FRAC[7:0]							
Type		R/W							
Default		0	0	0	0	0	0	0	0

Bit	Name	Function
7:0	F1FRAC[15:8] F1FRAC[7:0]	**Fractional portion of the feedback divider (N_{FRAC}) of frequency channel 1** e.g. If N_{FRAC} is 0x1234: F1FRAC[15:8] = 0x12 F1FRAC[7:0] = 0x34

7.3. PLL Fractional Setting: Frequency Channel 2

Address	Register name	Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x02	F2FRAC1	F2FRAC[15:8]							
0x03	F2FRAC0	F2FRAC[7:0]							
Type		R/W							
Default		0	0	0	0	0	0	0	0

Bit	Name	Function
7:0	F2FRAC[15:8] F2FRAC[7:0]	**Fractional portion of the feedback divider (N_{FRAC}) of frequency channel 2** e.g. If N_{FRAC} is 0x5678: F2FRAC[15:8] = 0x56 F2FRAC[7:0] = 0x78

7.4. PLL Integer Setting: Frequency Channel 1 and 2

Address	Register name	Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x04	F1_2INT	F1INT[3:0]				F2INT[3:0]			
Type		R/W							
Default		0	0	0	0	0	0	0	0

Bit	Name	Function
7:4	F1INT[4:0]	**Integer portion of the feedback divider (N_{INT}) of frequency channel 1**
3:0	F2INT[4:0]	**Integer portion of the feedback divider (N_{INT}) of frequency channel 2**

FnINT[4:0] setting and integer portion (N_{INT})

0x0: 16	0x4: 20	0x8: 24	0xC: 28
0x1: 17	0x5: 21	0x9: 25	0xD: 29
0x2: 18	0x6: 22	0xA: 26	0xE: 30
0x3: 19	0x7: 23	0xB: 27	0xF: 31

7.5. PLL Fractional Setting: Frequency Channel 3

Address	Register name	Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x05	F3FRAC1	F3FRAC[15:8]							
0x06	F3FRAC0	F3FRAC[7:0]							
Type		R/W							
Default		0	0	0	0	0	0	0	0

Bit	Name	Function
7:0	F3FRAC[15:8] F3FRAC[7:0]	**Fractional portion of the feedback divider (N_{FRAC}) of frequency channel 3** e.g. If NFRAC is 0x9ABC: F3FRAC[15:8] = 0x9A F3FRAC[7:0] = 0xBC

7.6. PLL Fractional Setting: Frequency Channel 4

Address	Register name	Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x07	F4FRAC1	F4FRAC[15:8]							
0x08	F4FRAC0	F4FRAC[7:0]							
Type		R/W							
Default		0	0	0	0	0	0	0	0

Bit	Name	Function
7:0	F4FRAC[15:8] F4FRAC[7:0]	**Fractional portion of the feedback divider (N_{FRAC}) of frequency channel 4** e.g. If NFRAC is 0xDEF0: F4FRAC[15:8] = 0xDE F4FRAC[7:0] = 0xF0

7.7. PLL Integer Setting: Frequency Channel 3 and 4

Address	Register name	Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x09	F3_4INT	F3INT[3:0]				F4INT[3:0]			
Type		R/W							
Default		0	0	0	0	0	0	0	0

Bit	Name	Function
7:4	F3INT[4:0]	**Integer portion of the feedback divider (N_{INT}) of frequency channel 3**
3:0	F4INT[4:0]	**Integer portion of the feedback divider (N_{INT}) of frequency channel 4**

FnINT[4:0] setting and integer portion (N_{INT})

0x0: 16	0x4: 20	0x8: 24	0xC: 28
0x1: 17	0x5: 21	0x9: 25	0xD: 29
0x2: 18	0x6: 22	0xA: 26	0xE: 30
0x3: 19	0x7: 23	0xB: 27	0xF: 31

7.8. FSK Deviation Setting, Output Divider Setting, and CKOUT Slew Rate Control Setting

Address	Register name	Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0A	ODIV	FDEV4X	FDEV2X	SR[1:0]		F1ODIV	F2ODIV	F3ODIV	F4ODIV
Type		R/W							
Default		0	0	0	0	0	0	0	0

Bit	Name	Function
7	FDEV4X	**FSK deviation setting** $F_{DEV} = \pm \frac{F_{REF} \times FDEV}{2^{16}} \times 4^{FDEV4X} \times 2^{FDEV2X}$
6	FDEV2X	
5:4	SR[1:0]	**Slew rate of the CMOS driver of the CKOUT pin** 0 – Tr/Tf = 20 ns max 1 – Tr/Tf = 10 ns max 2 – Tr/Tf = 7 ns max 3 – Tr/Tf = 5 ns max
3	F1ODIV	**Settings for output divider of frequency channel 1**
2	F2ODIV	**Settings for output divider of frequency channel 2**
1	F3ODIV	**Settings for output divider of frequency channel 3**
0	F4ODIV	**Settings for output divider of frequency channel 4**

FnODIV settings and output divider ratio (ODIV)

0	1/1
1	1/2

7.9. FSK Deviation Setting

Address	Register name	Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0B	FDEV	FDEV[7:0]							
Type		R/W							
Default		0	0	0	0	0	0	0	0

Bit	Name	Function
7:0	FDEV[7:0]	**FSK deviation setting** $F_{DEV} = \pm \frac{F_{REF} \times FDEV}{2^{16}} \times 4^{FDEV4X} \times 2^{FDEV2X}$

0	FDEV = ± 0 kHz
1	FDEV = ± 0.49 kHz
2	FDEV = ± 0.98 kHz
-	-
-	-
255	FDEV = ± 124.51 kHz

*FDEV4X = 0, FDEV2X = 0

7.10. ASK Modulation Control 0

Address	Register name	Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0C	ASKMC0	ASK0	HPWR0	AMH0[5:0]					
Type		R/W							
Default		0	0	0	0	0	0	0	0

Bit	Name	Function
7	ASK0	**Modulation type** 0: FSK 1: ASK
6	HPWR0	**PA output power range** 0: -15 dBm to 0 dBm 1: -4 dBm to 11 dBm
5:0	AMH0[5:0]	**PA output power** In ASK, this setting is applied for High level transition data. In FSK, this setting is applied for the output power. 1: Min, 63: Max. See **Table 5.5**.
ASKMC0 ASKMC0 is selected when the bit "D" of transmit command is 0. See section 6.2.4 for details.		

7.11. ASK Modulation Control 1

Address	Register name	Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0D	ASKMC1	ASK1	HPWR1	AMH1[5:0]					
Type		R/W							
Default		0	0	0	0	0	0	0	0

Bit	Name	Function
7	ASK1	**Modulation type** 0: FSK 1: ASK
6	HPWR1	**PA output power range** 0: -15 dBm to 0 dBm 1: -4 dBm to 11 dBm
5:0	AMH1[5:0]	**PA output power** In ASK, this setting is applied for High level transition data. In FSK, this setting is applied for the output power. 1: Min, 63: Max. See **Table 5.5**.
ASKMC1 ASKMC0 is selected when the bit "D" of transmit command is 1. See section 6.2.4 for details.		

7.12. ASK Modulation Control 2

Address	Register name	Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0E	ASKMC2	PADUTY[1:0]		AML[5:0]					
Type		R/W							
Default		0	0	0	0	0	0	0	0

Bit	Name	Function
7:6	PADUTY[1:0]	**Output signal duty cycle setting** PADUTY[1:0] / Nominal duty cycle: F_{TX} = 300 MHz to 465 MHz / F_{TX} = 600 MHz to 930 MHz 00b: 50% / 50% 01b: 45% / 36% 10b: 36% / Not available 11b: 30% / Not available
5:0	AML[5:0]	**PA output power setting** In ASK, this setting is applied for High level transition data. In FSK, this setting is not used. 1: Min, 63: Max. See **Table 5.5**. 0: The PAOUT pin goes OFF, which means OOK mode.

7.13. Soft-ASK Modulation Setting

Address	Register name	Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0F	PARAMP	AMRC[7:0]							
Type		R/W							
Default		0	0	0	0	0	0	0	0

Bit	Name	Function
7:0	AMRC[7:0]	**Soft-ASK modulation setting** You can set AMRC calculated as follows. See section 6.6.2 for details. $$t_{AMRC} = (\mathrm{AMH} - \mathrm{AML}) \times AMRC \times \frac{1}{F_{REF}}$$

7.14. Soft-FSK Modulation Setting

Address	Register name	Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x10	FSKRAMP	FMRC[7:0]							
Type		R/W							
Default		0	0	0	0	0	0	0	0

Bit	Name	Function
7:0	FMRC[7:0]	**Soft-FSK Modulation setting** You can set FMRC calculated as follows. See section 6.5.2 for details. $t_{FMRC} = 0DIV \times 2 \times FDEV \times FMRC \times \frac{1}{F_{REF}}$

7.15. CKOUT / Bitrate Signal Divider Setting 1

Address	Register name	Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x11	BRS1	BRS[7:0]							
Type		R/W							
Default		0	0	0	0	0	0	0	0

Bit	Name	Function
7:0	BRS[7:0]	Compare settings for CKOUT/bitrate signal divider

0	1/1
1	1/2
2	1/3
3	1/4
4	1/5
- -	- -
255	1/256

7.16. CKOUT / Bitrate Signal Divider Setting 2

Address	Register name	Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x12	BRS2	CKSRC[2:0]			PSC[2:0]			ASC[1:0]	
Type		R/W							
Default		0	0	0	0	0	0	0	0

Bit	Name	Function
7:5	CKSRC[2:0]	**Clock source setting** 000b: Fref / 16 001b: Prescaler clock 010b: PAON: 0 "Low"; PAON: 1 Divided clock 011b: PAON: 0 "High"; PAON: 1 Inverted divided clock 100b: PAON: 0 High-Z; PAON: 1 Fref / 16 101b: PAON: 0 High-Z; PAON: 1 Prescaler clock 110b: PAON: 0 High-Z; PAON: 1 Divided clock 111b: PAON: 0 High-Z; PAON: 1 Inverted divided clock *Note PAON: 0 PA is disabled. PAON: 1 PA is enabled.
4:2	PSC[2:0]	**Prescaler setting for CKOUT/bitrate signal divider** 0: 1/1 1: 1/2 2: 1/4 3: 1/8 4: 1/16 5: 1/32 6: 1/64 7: 1/128
1:0	ASC[2:0]	**Afterscaler setting for CKOUT/bitrate signal divider** 0: 1/1 1: 1/2 2: 1/4 3: 1/8

7.17. Under Voltage Detection / Antenna Tuning Setting

Address	Register name	Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x13	ATUNE	-	VDET[1:0]		ATT[4:0]				
Type		R/W							
Default		0	0	0	0	0	0	0	0

Bit	Name	Function
6:5	VDET[1:0]	**Under voltage detection/release setting** 0: Detection threshold 1.8 V, Release threshold 2.0 V 1: Detection threshold 2.0 V, Release threshold 2.2 V 2: Detection threshold 2.2 V, Release threshold 2.4 V 3: Detection threshold 2.4 V, Release threshold 2.6 V
4:0	ATT[4:0]	**Antenna tuning capacitance array setting** About 40fF divide capacitance available 0: 184 fF 1: 223 fF 2: 262 fF - : - - : - 31: 1393 fF

7.18. Error Detection Status

Address	Register name	Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x14	TXSTAT	TXCOUNT[3:0]				OSCDET	VDETER	VCOCER	PLLDER
Type		R/C				R/O	R/C		
Default		0	0	0	0	0	0	0	0

Bit	Name	Function
7:4	TXCOUNT[3:0]	**Function for counting the number of transitions to Transmitter-Active mode** The value is reset to zero when the counter overflows.
3	OSCDET	**Crystal oscillation amplitude check result** 0 – Not enough amplitude 1 – Enough amplitude
2	VDETER	**Under voltage detection flag** 0 – No under voltage 1 – Under voltage detected
1	VCOCER	**VCO auto-calibration error flag** 0 – No VCO auto-calibration error 1 – VCO auto-calibration error detected
0	PLLDER	**PLL Loss of Lock flag** 0 – No PLL loss of lock 1 – PLL loss of lock detected

7.19. Transmitter Control

Address	Register name	Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x15	TXCON	PD	PDCK	FSOFF	IFSEL[1:0]		-	-	PLLEN
Type		W/O	R/W						
Default		0	0	0	0	0	0	0	0

Bit	Name	Function
7	PD	**Transition to Powerdown mode** 0: If EN pin is kept low for 8.2 ms (2^{18} crystal clocks), the S1S77100 transits to Powerdown mode. 1: If EN pin goes low, the S1S77100 immediately transits to Powerdown mode
6	PDCK	**CKOUT output disable setting** 0: Enable output 1: CKOUT pin is Hi-Z
5	FSOFF	**Fail safe function disable** If the fail-safe function is disabled, PA does not stop even if an error is detected. 0: Enable fail-safe function 1: Disable fail-safe function
4:3	IFSEL[1:0]	**Interface mode setting** 00b: 3-wire SPI mode (default), SDIO 01b: 4-wire SPI mode, SDIO 10b: 3-wire SPI mode, TEST1 11b: Invalid
0	PLLEN	**Transition to PLL-Standby mode** If PLLEN is set to 1 in CKBUF-Active mode, the S1S77100 transits to PLL-Standby mode. If PLLEN is set to 0 in PLL-Standby mode, the S1S77100 transits to CKBUF-Active mode.

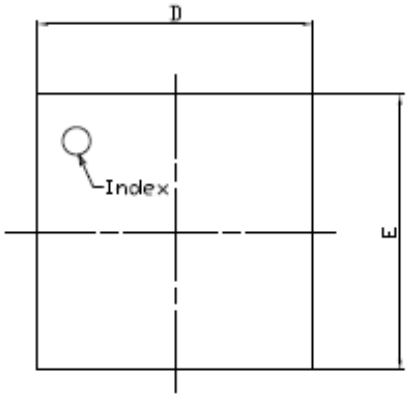
7.20. SPI Checksum

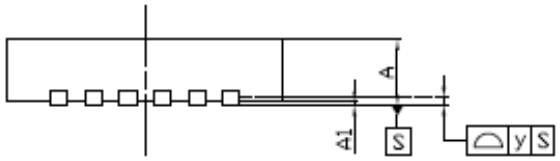
Address	Register name	Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x16	SPICKSUM	SPICKSUM[7:0]							
Type		R/C							
Default		0	0	0	0	0	0	0	0

Bit	Name	Function
7:0	SPICKSUM	**SPI checksum calculation result** The XOR result of SPI transmission address and data is stored.

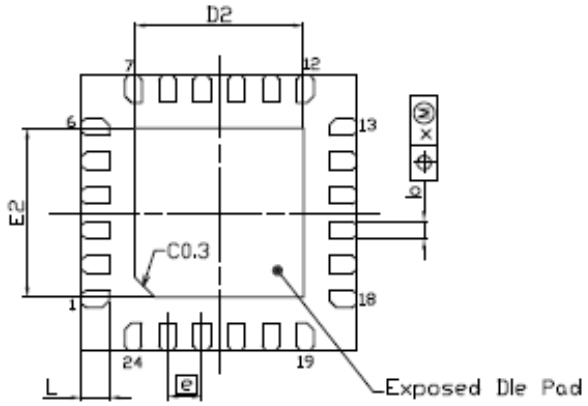
8. Dimensions

Top View





Bottom View



Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	3.90	4.00	4.10
E	3.90	4.00	4.10
A	–	–	1.00
A_1	0.00	–	–
b	0.20	0.25	0.30
e	–	0.50	–
L	0.35	0.40	0.45
D2	2.35	2.45	2.55
E2	2.35	2.45	2.55
x	–	–	0.10
y	–	–	0.08

1 = 1mm

9. Application Note

1. This product incorporates IC, so please handle it with care to avoid static electricity.
2. The output power evaluation results are based on the test circuit constants shown in Figure 5.1, implemented on our evaluation board. Please verify the optimal constants for your application, as optimal circuit constants may vary depending on the wiring pattern of the board on which this product is mounted.
3. The output power may decrease when operating at the maximum output power setting (AM* = 0x3F, P_{out} = about 11 dBm) for extended periods. Please ensure verification on your end if operating under conditions that exceed our reliability test conditions (AM* = 0x28, P_{out} = about 8 dBm).
4. Please use thick wiring for the VDD and VSS lines to maintain low high-frequency impedance. Additionally, we recommend placing a bypass capacitor of approximately 0.1 µF near the product.
5. Avoid power-on from intermediate potential and extremely rapid or slow power voltage ramp-up speeds, as these can cause malfunction.
6. Please verify the characteristics on your end if you intend to obtain wireless standard compliance using this product..

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America

Epson America, Inc.

Headquarter:
3131 Katella Ave.
Los Alamitos, CA 90720, USA
Phone: +1-800-463-7766

San Jose Office:
2860 Zanker Road Suite 204
San Jose, CA 95134, USA
Phone: +1-800-463-7766

Europe

Epson Europe Electronics GmbH
Riesstrasse 15, 80992 Munich,
Germany
Phone: +49-89-14005-0 FAX: +49-89-14005-110

Asia

Epson (China) Co., Ltd.
4th Floor, Tower 1 of China Central Place, 81 Jianguo Road, Chaoyang District, Beijing 100025 China
Phone: +86-10-8522-1199 FAX: +86-10-8522-1120

Shanghai Branch
Room 601-603, Building A One East, No.325 East Longhua Road, Shanghai 200023, China
Phone: +86-21-5330-4888 FAX: +86-21-5423-4677

Shenzhen Branch
Room 804-805, 8 Floor, Tower 2, Ali Center,No.3331 Keyuan South RD(Shenzhen bay), Nanshan District, Shenzhen 518054, China
Phone: +86-755-3299-0588 FAX: +86-755-3299-0560

Epson Taiwan Technology & Trading Ltd.
15F, No.100, Songren Rd, Sinyi Dist, Taipei City 110. Taiwan
Phone: +886-2-8786-6688

Epson Singapore Pte., Ltd.
438B Alexandra Road,
Block B Alexandra TechnoPark, #04-01/04, Singapore 119968
Phone: +65-6586-5500 FAX: +65-6271-7066

Epson Korea Co.,Ltd
10F Posco Tower Yeoksam, Teheranro 134 Gangnam-gu,
Seoul, 06235, Korea
Phone: +82-2-3420-6695

Seiko Epson Corp.
Sales & Marketing Division

MD Sales & Marketing Department
JR Shinjuku Miraina Tower, 4-1-6 Shinjuku,
Shinjuku-ku, Tokyo 160-8801, Japan

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