S1D13C00
S5U13C00M00C100
Adapter Board User Manual

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Rev. 1.0

Evaluation board/kit and Development tool important notice

1. This evaluation board/kit or development tool is designed for use for engineering evaluation, demonstration, or development purposes only. Do not use it for other purposes. It is not intended to meet the requirements of design for finished products.
2. This evaluation board/kit or development tool is intended for use by an electronics engineer and is not a consumer product. The user should use it properly and in a safe manner. Seiko Epson dose not assume any responsibility or liability of any kind of damage and/or fire coursed by the use of it. The user should cease to use it when any abnormal issue occurs even during proper and safe use.
3. The part used for this evaluation board/kit or development tool may be changed without any notice.

NOTICE

Table of Contents

1.   Introduction

The S5U13C00M00C100 is an adapter printed circuit board (PCB) for connecting the S5U13C00P00Cx00 Customer Development Board (which is a Boosterpack board for TI Tiva C Series EK-TM4C1294XL Launchpad board) to an ST Nucleo-144 board such as the NUCLEO-F746ZG.

The PCB is unpopulated and the user is expected to provide and solder headers needed to connect the S5U13C00P00Cx00 board to the Nucleo-144 board.   The J4, J5, J6, and J7 connectors on the top side of the PCB are intended to connect to the bottom side of the S5U13C00P00Cx00 board.   The CN8, CN9, CN10, and CN11 connectors on the bottom side of the PCB are intended to connect to the top side of the Nucleo-144 board.   Figure 1 shows the board stack connection.

S5U13C00P00Cx00 Board

Nucleo-144 Board

Figure 1 – Board Stack Connection

2. Signal Connections Map

The following tables show the signal connections map between the S5U13C00P00Cx00 board and the Nucleo-144 board:

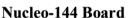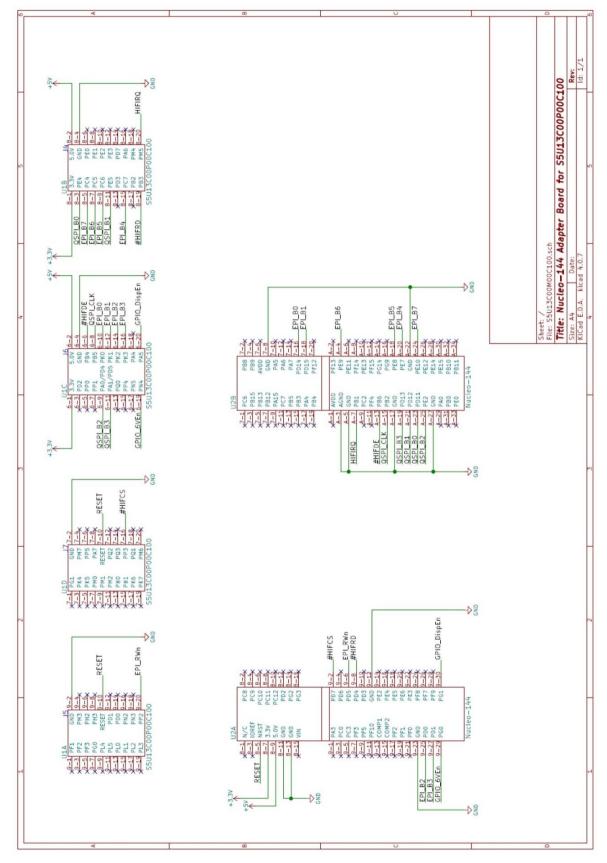| S5U13C00P00Cx00 Board		Nucleo-144		
	Signal	Signal		Description
J4-1	-	-	-	
J4-2	HOST_5V	+5V	CN8-9	5V supply
J4-3	HIFSPID0	PD11	CN10-23	Host SPI/QSPI D0
J4-4	GND	GND	CN7-8	Ground
J4-5	HIFD7	PE10	CN10-24	Host INDIRECT8 D7
J4-6	-	-	-	
J4-7	HIFD6	PE9	CN10-4	Host INDIRECT8 D6
J4-8	-	-	-	
J4-9	HIFD5	PE8	CN10-18	Host INDIRECT8 D5
J4-10	-	-	-	
J4-11	HIFSPID1	PD12	CN10-21	Host SPI/QSPI D1
J4-12	-	-	-	
J4-13	-	-	-	
J4-14	-	-	-	
J4-15	HIFD4	PE7	CN10-20	Host INDIRECT8 D4
J4-16	-	-	-	
J4-17	-	-	-	
J4-18	-	-	-	
J4-19	#HIFRD	PD4	CN9-8	Host INDIRECT8 read signal
J4-20	HIFIRQ	PB1	CN10-7	Interrupt request to host

S5U13C00P00Cx00 Board		Nucleo-144 Board		
	Signal	Signal		Description
J5-1	-	-	-	
J5-2	GND	GND	CN10-22	Ground
J5-3	-	-	-	
J5-4	-	-	-	
J5-5	-	-	-	
J5-6	-	-	-	
J5-7	-	-	-	
J5-8	-	-	-	
J5-9	-	-	-	
J5-10	#RESET	NRST	CN8-5	Reset
J5-11	-	-	-	
J5-12	-	-	-	
J5-13	-	-	-	
J5-14	-	-	-	
J5-15	-	-	-	
J5-16	-	-	-	
J5-17	-	-	-	
J5-18	-	-	-	
J5-19	-	-	-	
J5-20	#HIFWR	PD5	CN9-6	Host INDIRECT8 write signal

Signal Connections Map

S5U13C00P00Cx00 Board		Nucleo-144 Board		
	Signal	**Signal**		**Description**
J6-1	3V3	+3V3	CN8-7	3.3V supply
J6-2	5V	+5V	CN8-9	5V supply
J6-3	-	-	-	
J6-4	GND	GND	CN10-3	Ground
J6-5	-	-	-	
J6-6	#HIFDE	PB6	CN10-13	Host device enable signal
J6-7	-	-	-	
J6-8	HIFSPICLK	PB2	CN10-15	Host SPI/QSPI clock
J6-9	HIFSPID2	PE2	CN10-25	Host SPI/QSPI D2
J6-10	HIFD0	PD14	CN7-16	Host INDIRECT8 D2
J6-11	HIFSPID3	PD13	CN10-19	Host SPI/QSPI D3
J6-12	HIFD1	PD15	CN7-18	Host INDIRECT8 D1
J6-13	-	-	-	
J6-14	HIFD2	PD0	CN9-25	Host INDIRECT8 D2
J6-15	-	-	-	
J6-16	HIFD3	PD1	CN9-27	Host INDIRECT8 D3
J6-17	-	-	-	
J6-18	-	-	-	
J6-19	-	-	-	
J6-20	J3_DISP_EN	PG1	CN9-30	Display enable for SPI panel

S5U13C00P00Cx00 Board		Nucleo-144 Board		
	Signal	**Signal**		**Description**
J7-1	-	-	-	
J7-2	GND	GND	CN10-5	Ground
J7-3	-	-	-	
J7-4	-	-	-	
J7-5	-	-	-	
J7-6	-	-	-	
J7-7	-	-	-	
J7-8	-	-	-	
J7-9	-	-	-	
J7-10	#RESET	NRST	CN8-5	Reset
J7-11	-	-	-	
J7-12	-	-	-	
J7-13	-	-	-	
J7-14	-	-	-	
J7-15	-	-	-	
J7-16	#HIFCS	PD7	CN9-2	Host INDIRECT8 chip-select
J7-17	-	-	-	
J7-18	-	-	-	
J7-19	-	-	-	
J7-20	-	-	-	

3. S5U13C00M00C100 Schematic

Figure 2 - S5U13C00M00C100 Schematic

4.   Revision History

Rev. No.	Date	Page	Category	Contents
1.0	12/09/2018			• Initial release of document

For more information on the S1C13C00 and other Epson Display Controllers, visit the Epson Global website.

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