

S1D13A05 LCD/USB Companion Chip

Power Consumption

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1 S1D13A05 Power Consumption

S1D13A05 power consumption is affected by many system design variables.

- Input clock frequency (CLKI/CLKI2): the CLKI/CLKI2 frequency determines the LCD frame-rate, CPU performance to memory, and other functions – the higher the input clock frequency, the higher the frame-rate, performance and power consumption.
- CPU interface: the S1D13A05 current consumption depends on the BCLK frequency, data width, number of toggling pins, and other factors – the higher the BCLK, the higher the CPU performance and power consumption.
- V_{DD} voltage level: the voltage level affects power consumption – the higher the voltage, the higher the consumption.
- Display mode: the resolution and color depth affect power consumption – the higher the resolution/color depth, the higher the consumption.
- Internal CLK divide: internal registers allow the input clock to be divided before going to the internal logic blocks – the higher the divide, the lower the power consumption.

The S1D13A05 supports a software initiated power save mode. The power consumption in power save mode is affected by various system design variables.

- Clock states during the power save mode: disabling the clocks during power save mode has substantial power savings.

1.1 Conditions

The following table provides examples of typical configurations for some 320x240 panels and their effects on power consumption. The following conditions apply.

- All tests had an appropriate LCD panel connected to the LCD outputs of the S1D13A05.
- All tests were run with a static full color palette display.
- All tests were done using the Generic #1 host bus interface (BCLK = 33MHz).

Table 1-1: S1D13A05 Total Power Consumption for 320x240 panels

Test Conditions <i>COREV_{DD} = 2.0V and IOV_{DD} = 3.3V</i>					Power Consumption (mA)	
					S1D13A05 Active	
Resolution	Panel Type	Frame Rate	Clocks (MHz)	Color Depth	CORE	IO
320x240	Color 8-bit Format 2	94	CLKI = 33.3 = BCLK	4	2.53	2.96
		94	CLKI2 = grounded PCLK = MCLK = BCLK / 4	8	3.05	3.07
		94	USBCLK = 48 USB in Suspend Mode	16	3.44	2.46
	0	CLKI = BCLK = grounded CLKI2 = grounded PCLK = MCLK = BCLK / 4 USBCLK = grounded USB in Suspend Mode Power Save Mode	16	1.50µa	0.25µa	
	Color 4-bit	94	CLKI = 33.3 = BCLK CLKI2 = grounded PCLK = MCLK = BCLK / 4 USBCLK = 48 USB in Suspend Mode	16	3.48	3.64
18-bit TFT	79	CLKI = 33.3 = BCLK CLKI2 = grounded PCLK = MCLK = BCLK / 4 USBCLK = 48 USB in Suspend Mode	16	2.85	2.18	

The following table provides an example of a 320x320 HR-TFT panel and the effects on power consumption for specific environments. The following conditions apply.

- All tests had an appropriate LCD panel connected to the LCD outputs of the S1D13A05.
- All tests were run with a static full color palette display, **except the test where the 2D BitBLT engine was running**.
- All tests were done using the Generic #1 host bus interface (BCLK = 33MHz).

Table 1-2: S1D13A05 Total Power Consumption for 320x320 panels

Test Condition					Power Consumption (mA)	
COREV _{DD} = 2.0V and IOV _{DD} = 3.3V					S1D13A05 Active	
Resolution	Panel Type	Frame Rate	Clocks (MHz)	Color Depth	CORE	IO
320x320	18-bit HR-TFT	64	CLKI = 33.3 = BCLK	4	2.18	2.75
		64	CLKI2 = grounded PCLK = MCLK = BCLK / 4	8	2.65	3.05
		64	USBCLK = 48 USB in Suspend Mode	16	3.02	3.11
		60	CLKI = 33.3 = BCLK MCLK = BCLK / 4 CLKI2 = 7.8 = PCLK USBCLK = 48 USB in Suspend Mode	16	2.93	2.99
		64	CLKI = 33.3 = BCLK CLKI2 = grounded PCLK = MCLK = BCLK / 4 USBCLK = 48 USB Running (loopback) ¹	16	13.99	3.68
		64	CLKI = 33.3 = BCLK CLKI2 = grounded PCLK = MCLK = BCLK / 4 USBCLK = 48 USB in Suspend Mode 2D BitBLT engine running ²	16	6.33	4.78
		0	CLKI = BCLK = grounded CLKI2 = grounded PCLK = MCLK = BCLK / 4 USBCLK = grounded USB in Suspend Mode Power Save Enabled.	16	1.50µa	0.25µa

1. This test has the S1D13A05 USB module running a loop-back test.
2. This test has the 2D BitBLT engine performing a Move BitBLT which requires a high-level of CPU activity and a rapidly updating display.

2 Summary

The system design variables in Section 1, “S1D13A05 Power Consumption” and in the included comparison tables, show that S1D13A05 power consumption depends on the specific implementation. When the S1D13A05 is running power consumption depends on the desired CPU performance and LCD frame-rate. Power save mode consumption depends on the CPU Interface and Input Clock state.

In a typical design environment, the S1D13A05 can be configured to be an extremely power-efficient LCD Controller with high performance and flexibility.

3 Change Record

X40A-G-006-01

Revision 1.1 - Issued: March 28, 2018

- updated Sales and Technical Support Section
- updated some formatting

4 Sales and Technical Support

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