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S1D13A05 LCD/USB Companion Chip

S5U13A05B00C Rev. 1.0 Evaluation Board User Manual

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SEIKO EPSON CORPORATION

Rev. 1.1

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1 Introduction

This manual describes the setup and operation of the S5U13A05B00C Rev. 1.0 Evaluation Board. The board is designed as an evaluation platform for the S1D13A05 LCD/USB Companion Chip.

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2 Features

Following are some features of the S5U13A05B00C Rev. 1.0 Evaluation Board:

- 121-pin PFBGA S1D13A05 Embedded Memory LCD Controller with 256K bytes of embedded SRAM.
- PCI bus operation through onboard PCI bridge.
- CPU/Bus interface header strips for non-PCI bus operation.
- Configuration options.
- On-board adjustable positive LCD bias power supply from +23V to +40V.
- On-board adjustable negative LCD bias power supply from -14V to -24V.
- Software adjustable backlight intensity support using PWMOUT.
- 4/8-bit 3.3V or 5V single monochrome passive LCD panel support.
- 4/8/16-bit 3.3V or 5V single color passive LCD panel support.
- 9/12/18-bit 3.3V or 5V active matrix TFT LCD panel support.
- Direct interface for 18-bit Sharp HR-TFT LCD panel support.
- Direct interface for 18-bit Casio TFT LCD panel support.
- Direct interface for 18-bit TFT Type 2 LCD panel support
- Direct interface for 18-bit TFT Type 3 LCD panel support
- Direct interface for 18-bit TFT Type 4 (Epson ND-TFD) LCD panel support.
- Programmable clock synthesizer to CLKI and CLKI2 for maximum clock flexibility.
- Connector for USB client support.
- Selectable clock source for CLKI and CLKI2.
- External oscillator support for CLKI and CLKI2.

3 Installation and Configuration

The S5U13A05B00C is designed to support as many platforms as possible. The S5U13A05B00C incorporates a DIP switch and five jumpers which allow both the evaluation board and the S1D13A05 LCD controller to be configured for a specified evaluation platform.

3.1 Configuration DIP Switches

The S1D13A05 has seven configuration inputs (CNF[6:0]) which are read on the rising edge of RESET#. In order to configure the S1D13A05 for multiple Host Bus Interfaces an eight-position DIP switch (SW1) is required. The following figure shows the location of DIP switch SW1 on the S5U13A05B00C.

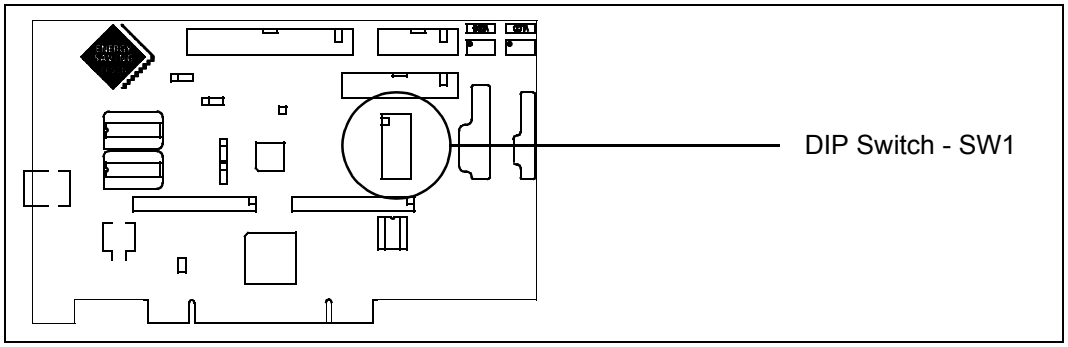

Figure 3-1: Configuration DIP Switch (SW1) Location

All S1D13A05 configuration inputs are fully configurable using the eight position DIP switch as described below.

Table 3-1: Configuration DIP Switch Settings

Switch (SW1)	S1D13A05 Signal	Value on this pin at rising edge of RESET# is used to configure: Closed (On/1)	Open (Off/0)
SW1-5, SW1-[3:1]	CNF4, CNF[2:0]	Select host bus interface as follows: **CNF4 CNF2 CNF1 CNF0 — Host Bus Interface** 1 0 0 0 — SH-4/SH-3 interface, Big Endian 0 0 0 0 — SH-4/SH-3 interface, Little Endian 1 0 0 1 — MC68K #1, Big Endian 0 0 0 1 — Reserved 1 0 1 0 — MC68K #2, Big Endian 0 0 1 0 — Reserved 1 0 1 1 — Generic #1, Big Endian 0 0 1 1 — Generic #1, Little Endian 1 1 0 0 — Reserved 0 1 0 0 — Generic #2, Little Endian 1 1 0 1 — RedCap 2, Big Endian 0 1 0 1 — Reserved 1 1 1 0 — DragonBall, Big Endian 0 1 1 0 — Reserved X 1 1 1 — Reserved	
SW1-4	CNF3	Reserved. Must be set to 1.	
SW1-6	CNF5	WAIT# is active high	WAIT# is active low
SW1-7	CNF6	CLKI to BCLK Divide ratio 2:1	CLKI to BCLK divide ratio 1:1
SW1-8	-	Disable PCI bridge for non-PCI host	Enable PCI bridge for PCI host

= Required settings when using the PCI Bridge FPGA

3.2 Configuration Jumpers

The S5U13A05B00C has five jumper blocks which configure various setting on the board. The jumper positions for each function are shown below.

Table 3-2: Jumper Summary

Jumper	Function	Position 1-2	Position 2-3	No Jumper
JP1	CLKI Source	VCLKOUT from clock synthesizer	External oscillator (U6)	BUSCLK from Header H5
JP2	CLKI2 Source	MCLKOUT from clock synthesizer	External oscillator (U7)	—
JP3	LCD Panel Voltage	+3.3V LCDVCC	+5V LCDVCC	—
JP4	PCI_IRQ Disable	Enable USB IRQ on PCI	—	Disable USB IRQ on PCI
JP5	GP00 Polarity on H3	Normal (Active High)	Inverted (Active Low)	GPO0 not sent to H3

= recommended settings

JP1 - CLKI Source

JP1 selects the source for the CLKI input pin.
When the jumper is at position 1-2, the CLKI source is VCLKOUT from the Cypress clock synthesizer (default setting).
When the jumper is at position 2-3, the CLKI source is the external oscillator at U6.
When no jumper is installed, the CLKI source is the BUSCLK signal from Header H5.

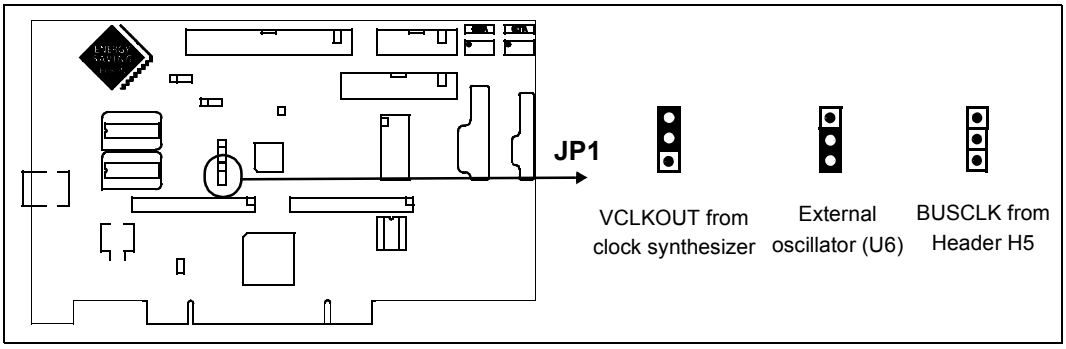

Figure 3-2: Configuration Jumper (JP1) Location

JP2 - CLKI2 Source

JP2 selects the source for the CLKI2 input pin.
When the jumper is at position 1-2, the CLKI2 source is MCLKOUT from the Cypress clock synthesizer (default setting).
When the jumper is at position 2-3, the CLKI2 source is the external oscillator at U7.

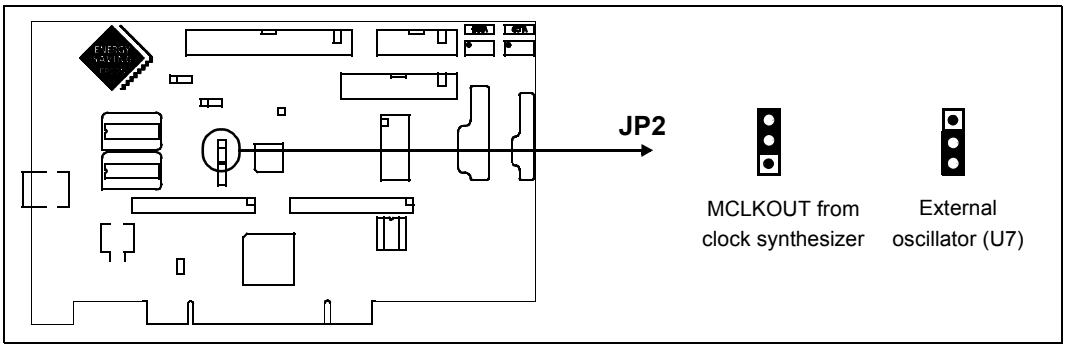

Figure 3-3: Configuration Jumper (JP2) Location

JP3 - LCD Panel Voltage

JP3 selects the voltage level to the LCD panel.
When the jumper is at position 1-2, the voltage level is +3.3V (default setting).
When the jumper is at position 2-3, the voltage level is +5.0V.

Note
When configured for Sharp HR-TFT, JP3 and JP5 must be set to position 1-2.

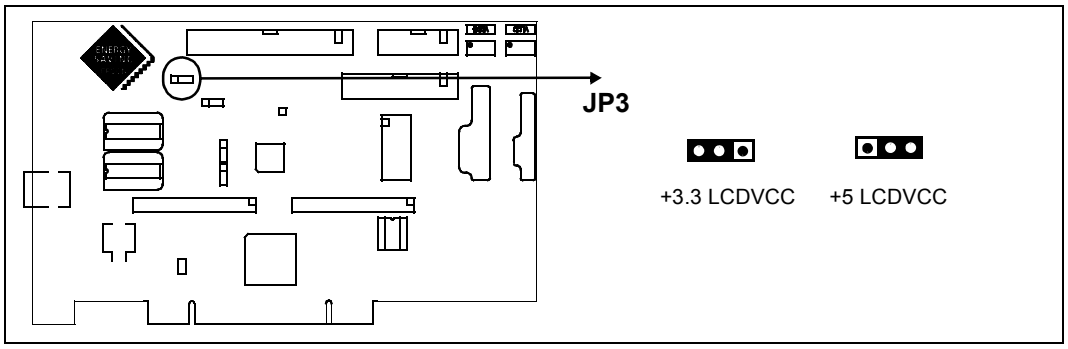

Figure 3-4: Configuration Jumper (JP3) Location

JP4 - PCI_IRQ Enable

JP4 selects whether the USB IRQ on PCI is enabled or disabled.
When the jumper is at position 1-2, the USB IRQ on PCI is enabled (default setting).
When no jumper is installed, the USB IRQ on PCI is disabled.

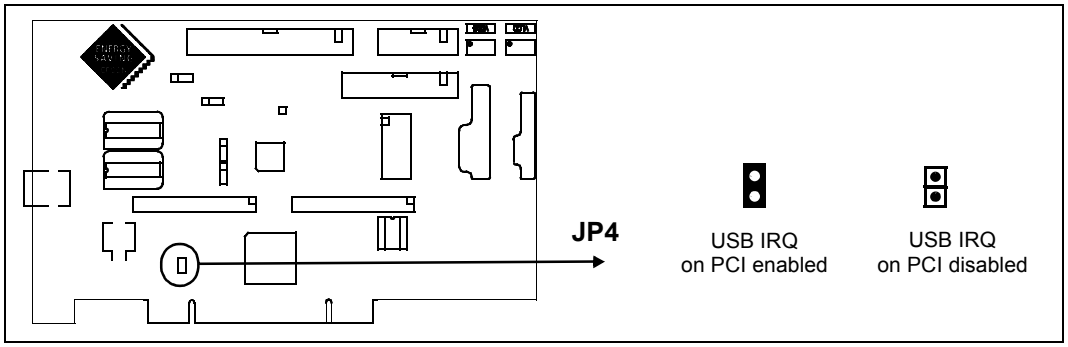

Figure 3-5: Configuration Jumper (JP4) Location

JP5 - GPO0 Polarity on H3

JP5 selects the polarity of the GPO0 signal available on the TFT Type 3 Extended LCD Connector H3.
When the jumper is at position 1-2, the GPO0 signal is sent directly (active high) to H3 (default setting).
When the jumper is at position 2-3, the GPO0 signal is inverted and then sent (active low) to H3.
When no jumper is installed, GPO0 is not sent to H3.

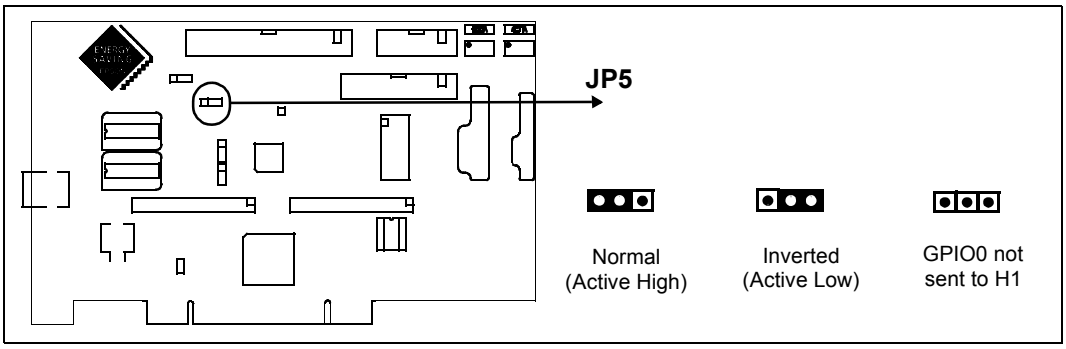

Figure 3-6: Configuration Jumper (JP5) Location

4 CPU Interface

4.1 CPU Interface Pin Mapping

Table 4-1: Host Bus Interface Pin Mapping

S1D13A05 Pin Name	Generic #1	Generic #2	Hitachi SH-3/SH-4	Motorola MC68K #1	Motorola MC68K #2	Motorola REDCAP2	Motorola MC68EZ328/ MC68VZ328 DragonBall
AB[17:1]	A[17:1]	A[17:1]	A[17:1]	A[17:1]	A[17:1]	A[17:1]	A[17:1]
AB0	A0[1]	A0	A0[1]	LDS#	A0	A0[1]	A0[1]
DB[15:0]	D[15:0]	D[15:0]	D[15:0]	D[15:0]	D[15:0][2]	D[15:0]	D[15:0]
CS#	External Decode		CSn#	External Decode		$\overline{CSn}$	$\overline{CSX}$
M/R#	External Decode						
CLKI	BUSCLK	BUSCLK	CKIO	CLK	CLK	CLK	CLKO
BS#	Connected to IOV_{DD}[3]		BS#	AS#	AS#	Connected to IOV_{DD}[3]	
RD/WR#	RD1#	Connected to IOV_{DD}[3]	RD/WR#	R/W#	R/W#	R/$\overline{W}$	Connected to IOV_{DD}[3]
RD#	RD0#	RD#	RD#	Connected to IOV_{DD}[3]	SIZ1	$\overline{OE}$	$\overline{OE}$
WE0#	WE0#	WE#	WE0#	Connected to IOV_{DD}[3]	SIZ0	$\overline{EB1}$	$\overline{LWE}$
WE1#	WE1#	BHE#	WE1#	UDS#	DS#	$\overline{EB0}$	$\overline{UWE}$
WAIT#	WAIT#	WAIT#	WAIT#/ RDY#	DTACK#	DSACK1#	N/A	$\overline{DTACK}$
RESET#	RESET#	RESET#	RESET#	RESET#	RESET#	$\overline{RESET\_OUT}$	$\overline{RESET}$

Note

[1] A0 for these bus interfaces is not used internally by the S1D13A05 and should be connected to V_{SS}.

[2] If the target MC68K bus is 32-bit, then these signals should be connected to D[31:16].

[3] These pins are not used in their corresponding host interface mode. Systems are responsible for externally connecting them to IO V_{DD}.

4.2 CPU Bus Connector Pin Mapping

Table 4-2: CPU Bus Connector (H4) Pinout

Connector Pin No.	Comments
1	Connected to DB0 of the S1D13A05
2	Connected to DB1 of the S1D13A05
3	Connected to DB2 of the S1D13A05
4	Connected to DB3 of the S1D13A05
5	Ground
6	Ground
7	Connected to DB4 of the S1D13A05
8	Connected to DB5 of the S1D13A05
9	Connected to DB6 of the S1D13A05
10	Connected to DB7 of the S1D13A05
11	Ground
12	Ground
13	Connected to DB8 of the S1D13A05
14	Connected to DB9 of the S1D13A05
15	Connected to DB10 of the S1D13A05
16	Connected to DB11 of the S1D13A05
17	Ground
18	Ground
19	Connected to DB12 of the S1D13A05
20	Connected to DB13 of the S1D13A05
21	Connected to DB14 of the S1D13A05
22	Connected to DB15 of the S1D13A05
23	Connected to RESET# of the S1D13A05
24	Ground
25	Ground
26	Ground
27	+12 volt supply
28	+12 volt supply
29	Connected to WE0# of the S1D13A05
30	Connected to WAIT# of the S1D13A05
31	Connected to CS# of the S1D13A05
32	Connected to MR# of the S1D13A05
33	Connected to WE1# of the S1D13A05
34	Connected to +3.3V

Table 4-3: CPU Bus Connector (H5) Pinout

Connector Pin No.	Comments
1	Connected to AB0 of the S1D13A05
2	Connected to AB1 of the S1D13A05
3	Connected to AB2 of the S1D13A05
4	Connected to AB3 of the S1D13A05
5	Connected to AB4 of the S1D13A05
6	Connected to AB5 of the S1D13A05
7	Connected to AB6 of the S1D13A05
8	Connected to AB7 of the S1D13A05
9	Ground
10	Ground
11	Connected to AB8 of the S1D13A05
12	Connected to AB9 of the S1D13A05
13	Connected to AB10 of the S1D13A05
14	Connected to AB11 of the S1D13A05
15	Connected to AB12 of the S1D13A05
16	Connected to AB13 of the S1D13A05
17	Ground
18	Ground
19	Connected to AB14 of the S1D13A05
20	Connected to AB15 of the S1D13A05
21	Connected to AB16 of the S1D13A05
22	Connected to AB17 of the S1D13A05
23	Not connected
24	Not connected
25	Ground
26	Ground
27	+5 volt supply
28	+5 volt supply
29	Connected to RD/WR# of the S1D13A05
30	Connected to BS# of the S1D13A05
31	Connected to BUSCLK of the S1D13A05
32	Connected to RD# of the S1D13A05
33	Not connected
34	Not connected

5 LCD Interface Pin Mapping

Table 5-1: LCD Connector (H1)

Pin Name	H1 Pin No.	Monochrome Passive Panel		Color Passive Panel				Color TFT Panel							
		Single		Single				Others			Sharp HR-TFT	Casio TFT	TFT Type 2	TFT Type 3	TFT Type 4
					Format 1	Format 2									
		4-bit	8-bit	4-bit	8-bit	8-bit	16-Bit	9-bit	12-bit	18-bit	18-bit	18-bit	18-bit	18-bit	18-bit
FPDAT0	1	driven 0	D0	driven 0	D0 (B5)[1]	D0 (G3)[1]	D0 (R6)[1]	R2	R3	R5	R5	R5	R5	R5	R5
FPDAT1	3	driven 0	D1	driven 0	D1 (R5)[1]	D1 (R3)[1]	D1 (G5)[1]	R1	R2	R4	R4	R4	R4	R4	R4
FPDAT2	5	driven 0	D2	driven 0	D2 (G4)[1]	D2 (B2)[1]	D2 (B4)[1]	R0	R1	R3	R3	R3	R3	R3	R3
FPDAT3	7	driven 0	D3	driven 0	D3 (B3)[1]	D3 (G2)[1]	D3 (R4)[1]	G2	G3	G5	G5	G5	G5	G5	G5
FPDAT4	9	D0	D4	D0 (R2)[1]	D4 (R3)[1]	D4 (R2)[1]	D8 (B5)[1]	G1	G2	G4	G4	G4	G4	G4	G4
FPDAT5	11	D1	D5	D1 (B1)[1]	D5 (G2)[1]	D5 (B1)[1]	D9 (R5)[1]	G0	G1	G3	G3	G3	G3	G3	G3
FPDAT6	13	D2	D6	D2 (G1)[1]	D6 (B1)[1]	D6 (G1)[1]	D10 (G4)[1]	B2	B3	B5	B5	B5	B5	B5	B5
FPDAT7	15	D3	D7	D3 (R1)[1]	D7 (R1)[1]	D7 (R1)[1]	D11 (B3)[1]	B1	B2	B4	B4	B4	B4	B4	B4
FPDAT8	17	driven 0	driven 0	driven 0	driven 0	driven 0	D4 (G3)[1]	B0	B1	B3	B3	B3	B3	B3	B3
FPDAT9	19	driven 0	driven 0	driven 0	driven 0	driven 0	D5 (B2)[1]	driven 0	R0	R2	R2	R2	R2	R2	R2
FPDAT10	21	driven 0	driven 0	driven 0	driven 0	driven 0	D6 (R2)[1]	driven 0	driven 0	R1	R1	R1	R1	R1	R1
FPDAT11	23	driven 0	driven 0	driven 0	driven 0	driven 0	D7 (G1)[1]	driven 0	driven 0	R0	R0	R0	R0	R0	R0
FPDAT12	25	driven 0	driven 0	driven 0	driven 0	driven 0	D12 (R3)[1]	driven 0	G0	G2	G2	G2	G2	G2	G2
FPDAT13	27	driven 0	driven 0	driven 0	driven 0	driven 0	D13 (G2)[1]	driven 0	driven 0	G1	G1	G1	G1	G1	G1
FPDAT14	29	driven 0	driven 0	driven 0	driven 0	driven 0	D14 (B1)[1]	driven 0	driven 0	G0	G0	G0	G0	G0	G0
FPDAT15	31	driven 0	driven 0	driven 0	driven 0	driven 0	D15 (R1)[1]	driven 0	B0	B2	B2	B2	B2	B2	B2
FPDAT16	4	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	B1	B1	B1	B1	B1	B1
FPDAT17	6	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	B0	B0	B0	B0	B0	B0
FPSHIFT	33	FPSHIFT									DCLK	CLK	CLK	CPH	FPSHIFT
DRDY	35 & 38	MOD			FPSHIFT2	MOD		DRDY			driven 0	no connect	INV	INV	DRDY
FPLINE	37	FPLINE									LP	GPCK	STB	LP	FPLINE
FPFRAME	39	FPFRAME									SPS	GSRT	STV	STV	FPFRAME
GND	2, 8, 14, 20, 26	GND													
PWMOUT	28	PWMOUT													
VLCD	30	Adjustable -24V to -14V negative LCD bias													
LCDVCC	32	LCDVCC (3.3V or 5V)													
+12V	34	+12V													
VDDH	36	Adjustable +23V to +40V positive LCD bias													
GPO0[2]	40	GPO0 (for controlling on-board LCD bias power supply on/off)													

Note

[1] These pin mappings use signal names commonly used for each panel type, however signal names may differ between panel manufacturers. The values shown in brackets represent the color components as mapped to the corresponding FPDATxx signals at the first valid edge of FPSHIFT. For further FPDATxx to LCD interface mapping, see *S1D13A05 Hardware Functional Specification*, document number X40A-A-001-xx.

[2] GPO0 can be inverted on H1 by setting JP5 to 2-3.

Table 5-2: Extended LCD Connector (H2)

Pin Name	H2 Pin No.	Mono Passive Panels	Color Passive Panels	Color TFT Panel								USB[2]
				Others			Sharp HR-TFT[1]	Casio TFT[1]	TFT Type 2[1]	TFT Type 3[1]	TFT Type 4	
				9-bit	12-bit	18-bit	18-bit	18-bit	18-bit	18-bit	18-bit	
GPIO0	1	GPIO0					PS	POL	VCLK	CPV	GPIO0	GPIO0
GPIO1	3	GPIO1					CLS	GRES	AP	OE	GPIO1	GPIO1
GPIO2	5	GPIO2					REV	FRP	POL	POL	GPIO2	GPIO2
GPIO3	7	GPIO3					SPL	STH	STH	EIO	GPIO3	GPIO3
GPIO4	9	GPIO4										USBPUP
GPIO5	11	GPIO5										USBDETECT
GPIO6	13	GPIO6										USBDM
GPIO7	15	GPIO7										USBDP
GND	2, 4, 6, 8, 10, 12, 14, 16	GND										

Note

[1] If a panel type requiring extra control signals is selected (REG[0Ch] or REG[48h]), GPIO[3:0] are used for the required signals. This leaves GPIO[7:4] available for USB support or as GPIOs.

[2] If USB support is enabled (REG[4000h] bit 7 = 1), GPIO[7:4] are used by the USB interface. GPIO[3:0] remain available for extended panel interface support (HR-TFT, Casio or Type 2/3/4 TFT) or as GPIOs.

Table 5-3: TFT Type 3 Extended LCD Connector (H3)

Pin Name	H3 Pin number	TFT Type 3	All Other LCD Display Modes
GPO0	1	GPO0	GPO0
GPO1	3	VCOM	GPO1
GPO2	5	XOEV	GPO2
GPO3	7	CMD	GPO3
GPO4	9	PCLK1	GPO4
GPO5	11	PCLK2	GPO5
GPO6	13	XRESH	GPO6
GPO7	15	XRESV	GPO7
GPO8	17	XOHV	GPO8
GPO9	19	XSTBY	GPO9
GPO10	21	PMDE	GPO10
NC	23	-	
NC	25	-	
GND	2-26 Even Numbers	GND	

6 Technical Description

6.1 PCI Bus Support

The S1D13A05 **does not** have on-chip PCI bus interface support. The S1D13A05B00C uses the on-board PCI Bridge FPGA to support the PCI bus.

6.2 Direct Host Bus Interface Support

The S5U13A05B00C is specifically designed to work using the PCI Bridge FPGA in a standard PCI bus environment. However, the S1D13A05 directly supports many other host bus interfaces. Connectors H4 and H5 provide the necessary IO pins to interface to these host buses. For further information on the host bus interfaces supported, see "CPU Interface" on page 13.

Note

If a direct host bus interface is used, the PCI Bridge FPGA must be disabled using SW1-8.

6.3 S1D13A05 Embedded Memory

The S1D13A05 has 256K bytes of embedded SRAM. The 256K byte display buffer address space is directly and contiguously available through the 18-bit address bus.

6.4 Adjustable LCD Panel Negative Power Supply

Most monochrome passive LCD panels require a negative power supply to provide between -14V and -24V (I_{out}=45mA). Such a power supply (VLCD) has been provided on the S5U13A05B00C board. VLCD can be adjusted using potentiometer R21 to provide an output voltage from -14V to -24V, and is enabled/disabled using the S1D13A05 general purpose signal, GPO0 (active high).

Note

When manually adjusting the voltage, set the potentiometer according to the panel's specific power requirements **before connecting the panel.**

6.5 Adjustable LCD Panel Positive Power Supply

Most color passive LCD panels and most single monochrome 640x480 passive LCD panels require a positive power supply to provide between +23V and +40V (I_{out}=45mA). Such a power supply (VDDH) has been provided on the S5U13A05B00C board. VDDH can be adjusted using R14 to provide an output voltage from +23V to +40V, and is enabled/disabled using the S1D13A05 general purpose signal, GPO0 (active high).

Note

When manually adjusting the voltage, set the potentiometer according to the panel's specific power requirements **before connecting the panel.**

6.6 Software Adjustable LCD Backlight Intensity Support Using PWM

The S1D13A05 provides Pulse Width Modulation output on PWMOUT. PWMOUT can be used to control LCD panels which support PWM control of the backlight inverter. The PWMOUT signal is provided on LCD Connector H1.

6.7 LCD Panel Support

The S1D13A05 directly supports:

- Single-panel, single drive passive displays.
  - 4/8-bit monochrome interface.
  - 4/8/16-bit color interface.
- Active Matrix TFT interface.
  - 9/12/18-bit interface.
- Direct support for 18-bit Sharp HR-TFT LCD panel.
- Direct support for 18-bit Casio TFT LCD panel.
- Direct support for 18-bit TFT Type 2 LCD panel.
- Direct support for 18-bit TFT Type 3 LCD panel.
- Direct support for 18-bit TFT Type 4 (Epson ND-TFD) LCD panel.

All the necessary signals are provided on the 40-pin LCD Connector H1, 16-pin Extended LCD Connector H2, and the 26-pin TFT Type 3 Extended LCD Connector H3. For detailed connection information, see Section 5, "LCD Interface Pin Mapping" on page 16.

6.7.1 LCD Connector

The LCD Connector H1 provides all LCD panel signals required for Active Matrix TFT and Passive LCD panels. These signals are buffered to either a 3.3V level or a 5.0V level depending on the setting of JP3. See Table 3-2: "Jumper Summary" on page 9.

6.7.2 Extended LCD Connector

The S1D13A05 directly supports several extended panel types such as the Sharp 18-bit HR-TFT, Casio TFT and compatible panels. The Extended LCD Connector H2 provides the extra signals required to support these panels. The signals on this connector are provided directly from the S1D13A05 without any buffering and are 3.3V signals.

6.7.3 TFT Type 3 Extended LCD Connector

The S1D13A05 directly supports 18-bit TFT Type 3 compatible panels. The TFT Type 3 Extended LCD Connector H3 provides the extra signals required to support panels compatible with the specified timings. The signals on this connector are provided directly from the S1D13A05 without any buffering and are 3.3V signals.

6.8 USB Support

The S1D13A05 USB controller provides a Revision 1.1 compliant USB client. The S1D13A05 acts as a USB device and connects to an upstream hub or USB host through connector J1 on the S5U13A05B00C evaluation board. Clamping diodes have been added to protect the USB bus from ESD and shorting.

6.8.1 USB IRQ Support

The S1D13A05 supports interrupts using the output pin, IRQ. In order to support interrupts from the USB client of the S1D13A05, the S5U13A05B00C evaluation board connects IRQ to PCI interrupt INTA# from the PCI slot. The IRQ pin output to the PCI bus can be disabled by removing jumper JP4.

6.9 External oscillator support for CLKI and CLKI2

The S1D13A05 can use CLKI and CLKI2 sources other than the Clock Synthesizer. Two +3.3V supplied 14-pin DIP package sized oscillator slots are present on the board.

6.10 External oscillator support for USBCLK

The S1D13A05 can use a 48MHz oscillator for the USBCLK source, instead of the USB crystal oscillating circuit. A +3.3V supplied 14-pin DIP package sized oscillator slot is present on the board.

Note

The board supports either an external crystal or an external oscillator for USB functionality. Only one can be enabled at a time. If an external crystal is used for the clock source for the USB module, the USBCLK input needs to be disabled by using a pull-

down resistor and removing the oscillator or clock source. If an oscillator or another type of clock external source is used, USBOCSI needs to be disabled by using a pull-down resistor and disabling or removing the crystal oscillator circuitry.

7 Clock Synthesizer and Clock Options

For maximum flexibility, the S5U13A05B00C implements a Cypress ICD2061A Clock Synthesizer. MCLKOUT from the clock synthesizer is connected to CLKI2 of the S1D13A05 and VCLKOUT from the clock synthesizer is connected to CLKI of the S1D13A05. A 14.31818MHz crystal (Y1) is connected to XTALIN and XTALOUT of the clock synthesizer and provides the reference clock to the clock synthesizer.

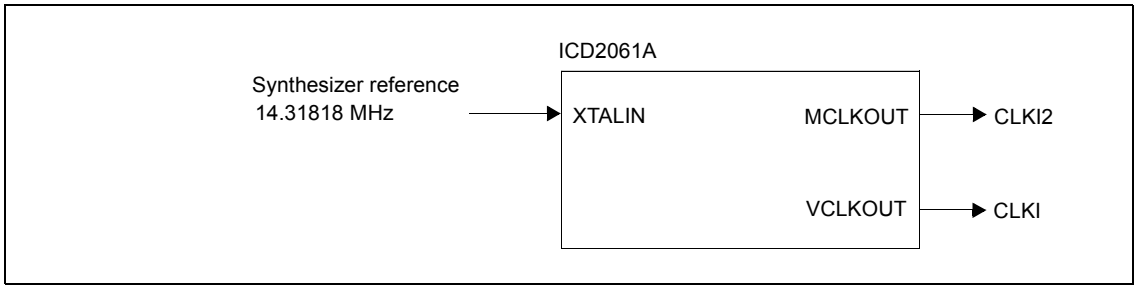

Figure 7-1: Symbolic Clock Synthesizer Connections

At power-on, CLKI2 (MCLKOUT) is configured at 40MHz and CLKI (VCLKOUT) is configured at 25.175MHz.

Note
If a Sharp HR-TFT panel is selected, the clock synthesizer cannot be programmed, and external oscillators must provide the clock signals to CLKI and CLKI2. Jumpers JP1 and JP2 allow selection of external oscillators U7 and U8 as the clock source for both CLKI and CLKI2. For further information, see Table 3-2: "Jumper Summary" on page 9.

7.1 Clock Programming

The S1D13A05 utilities automatically program the clock generator. If manual programming of the clock generator is required, refer to the source code for the S1D13A05 utilities available on the internet at vdc.epson.com.

For further information on programming the clock generator, refer to the *Cypress ICD2061A specification*.

Note
When CLKI and CLKI2 are programmed to multiples of each other (e.g. CLKI = 20MHz, CLKI2 = 40MHz), the clock output signals from the Cypress clock generator may jitter. Refer to the Cypress ICD2061A specification for details.

To avoid this problem, set CLKI and CLKI2 to different frequencies and use the S1D13A05 internal clock divides to obtain the lower frequencies.

8 Parts List

Table 8-1: Parts List

Item	Qty	Designation	Part Value	Description	Manufacturer / Part No. / Assembly Instructions
1	25	C1,C2,C3,C4,C5,C6,C7,C8, C9,C10,C11, C12,C13,C15,C18,C19,C22 ,C24,C28,C31, C33,C35,C36,C37,C38	0.1uF	CAP 0.10UF 16V CERAMIC X7R 0805	KEMET C0805C104K4RACTU or equivalent capacitor
2	1	C14	10uF 10V	Tantalum C-Size, 10uF, 10V, +/-10%	Kemet T491C106K010AS (altern -Panasonic ECST1AC106R (Digikey)
3	2	C17,C16	n/p	1206 Capacitor	Do not purchase. Do not populate.
4	2	C20,C21	6.8pF	6.8PF 50V CERM CHIP CAP SMD 1206	Panasonic ECU-V1H6R8DCM or equivalent capacitor
5	7	C23,C29,C32,C34,C49,C50 ,C51	68uF 10V	Tantalum D-Size, 68uF,10V, +/-10%	Kemet T491D686K010AS (altern -Panasonic ECST1AD686R (Digikey)
6	3	C25,C26,C27	10uF/63V	Electrolytic, Radial Lead 10uF, 63V, +/-20%	NIPPON/UNITED CHEMI-CON KMF63VB10RM5X11LL or equivalent
7	1	C30	56uF/35V	Electrolytic, Radial Lead 56uF, 35V, +/-20%	NIPPON/UNITED CHEMI-CON KMF35VB56RM5X11LL or equivalent
8	9	C39,C40,C41,C42,C43,C44 ,C45,C46,C47	0.22uF	Ceramic Chip 0.22uF, 50V, X7R +/-5%, 1206 pckg	Kemet C1206C224J5RAC or equivalent capacitor
9	2	C48, C52	33uF 20V	Tantalum D-Size, 33uF,20V, +/-10%	Kemet T491D336K020AS (altern -Panasonic ECST1AD686R (Digikey)
10	2	D1, D2	BAV99	Ultra high-speed switching diode	Rohm BAV99
11	1	H1	HEADER 20X2	20x2, .025” sq. shrouded header, keyed	Thomas&Betts P/N:636-4027 or equivalent
12	1	H2	HEADER 8X2	8x2, .025” sq. shrouded header, keyed	Thomas&Betts P/N:636-1627 or equivalent
13	1	H3	HEADER 13X2	SHROUDED HEADER 26 POS STRAIGHT	3M 2526-6002UB or equivalent
14	2	H5, H4	HEADER 17X2	17x2, 0.1” pitch, .025” sq. unshrouded header	Thomas&Betts P/N:609-3407 or equivalent
15	4	JP1,JP2,JP3,JP5	HEADER 3	3x1, 0.1” pitch unshrouded header	
16	2	JP4,JP6	HEADER 2	2x1, 0.1” pitch unshrouded header	Do not purchase or populate JP6.
17	1	J1	USB B Connector	Right Angle, Type B USB Connector	AMP 787780-1

Table 8-1: Parts List

Item	Qty	Designation	Part Value	Description	Manufacturer / Part No. / Assembly Instructions
18	1	L1	1uH	Inductor	RCD MCI-1812 1uH MT or MSI-1812 1uH MT
19	1	L2	Ferrite	Ferrite Bead	Phillips BDS3/3/8.9-4S2
20	1	PCIA1	PCI-A	PCI PCB connector with 2 keyways	Not a part. Layout description.
21	1	PCIB1	PCI-B	PCI PCB connector with 2 keyways	Not a part. Layout description.
22	1	Q1	MMBT3906	PNP signal transistor, SOT23 package	Motorola MMBT3906LT1
23	1	Q2	MMBT2222A	NPN transistor, SOT-23 pckg.	Motorola MMBT2222A or equivalent
24	15	R1,R2,R3,R4,R5,R6,R7,R8, R9,R16,R29, R32,R33,R34,R35	15K 5%	0805 Resistor, 15K, 5%	
25	1	R12	15K 5%	0805 Resistor, 15K, 5%	Do not purchase. Do not populate.
26	1	R10	1M 0805	0805 Resistor, 1M, 1%	
27	1	R11	470R 0805	0805 Resistor, 470R, 1%	
28	1	R13	470K 5%	1206 Resistor, 470K, 5%	
29	1	R14	200K Pot	200K Trim pot	Bourns 3386W-1-204 or equivalent, PTH
30	1	R15	330K 1206	1206 Resistor, 330K, 5%	Do not purchase. Do not populate.
31	5	R17,R18,R30,R31,R36	1K 5%	1206 Resistor, 1K, 5%	
32	3	R19,R20,R28	100K 5%	1206 Resistor, 100K, 5%	
33	1	R21	100K Pot	100K Trim pot	Bourns 3386W-1-104 or equivalent, PTH
34	1	R22	1.5K 1%	1206 Resistor, 1.5K, 1%	
35	1	R23	150K 1%	1206 Resistor, 150K, 1%	
36	2	R27,R24	301K 1%	1206 Resistor, 301K, 1%	
37	2	R26,R25	20 1%	1206 Resistor 20 Ohm, 1%	
38	1	SW1	SW DIP-8	Dip Switch 8-Position	
39	1	SW2	SW DIP-4	Dip Switch 4-Position	Do not populate. Do not purchase.
40	1	TP1	HEADER 1	1x1, 0.1” pitch unshrouded header	Do not populate.
41	1	U1	S1D13A05B00B	121 pin PFBGA 13A05 LCD Controller	Epson S1D13A05B00B. To be supplied by Epson R&D.
42	1	U2	LT1117CST-5	5V fixed voltage regulator, SOT-223	Linear Technology LT1117CST-5
43	1	U3	74AHC04	Inverter, SO-14 package	TI74AHC04, equivalent (Fairchild, 74VHC04SJ)
44	1	U4	ICD2061A	Clock chip generator, wide SO-16 package	Cypress ICD2061A

Table 8-1: Parts List

Item	Qty	Designation	Part Value	Description	Manufacturer / Part No. / Assembly Instructions
45	3	U5,U6,U7	Test Socket	14 pin narrow DIP, screw machine socket	Sockets for oscillator inputs. Do not purchase or populate U5.
46	1	U8	RD-0412	Positive LCD Bias Power Supply	Taiyo Yuden/Xentek Positive Power Supply, RD-0412, PTH
47	1	U9	NC7ST04	TinyLogic HST inverter, SOT23-5 pckg.	Fairchild NC7ST04
48	1	U10	EPN001	Negative LCD Bias Power Supply	Taiyo Yuden/Xentek Negative Power Supply, EPN001, PTH
49	1	U11	RC1117S25T	2.5V fixed voltage regulator, SOT-223	Fairchild Semiconductor RC1117S25T or equiv.
50	1	U12	LT1117CM-3.3	3.3V fixed voltage regulator, 3 Lead Plastic DD	Linear Technology LT1117CM-3.3
51	3	U13,U15,U16	74HCT244	Buffer, SO-20 package	TI74HCT244 or equivalent
52	1	U14	74AHC1G125/ SOT-23		
53	1	U17	EPF6016TC144-2	TQFP 144 pin FLEX 6000 FPGA	Altera EPF6016TC144-2
54	1	(U18)	EPC1441PC8	8-pin DIP package, OTP EPROM (Socketed)	Altera EPC1441PC8, Socketed
55	1	U18	Socket	8-pin narrow DIP, screw machine socket	Socket for U18
56	1	Y1	14.31818MHz	Vertical-mount HC-49	14.31818MHz crystal HC-49 Fox p/n FoxS/143-20 14.31818MHz
57	1	Y2	48MHz	48MHz SMD XTAL	EPSON FA-238 Series 48MHz Fundamental Crystal
58	5	(JP1-JP5)	Shunts	Jumper Shunts	
59	1	Z1	PCI bracket	PCI bracket with slot for USB Type B conn	Hansen Industries PCI bracket (Same bracket used for 13A03B00B board)
60	2	Z2	Pan Head Screw	Screw, pan head, #4-40 x 1/4”	use to assemble PCI bracket onto board

9 Schematics

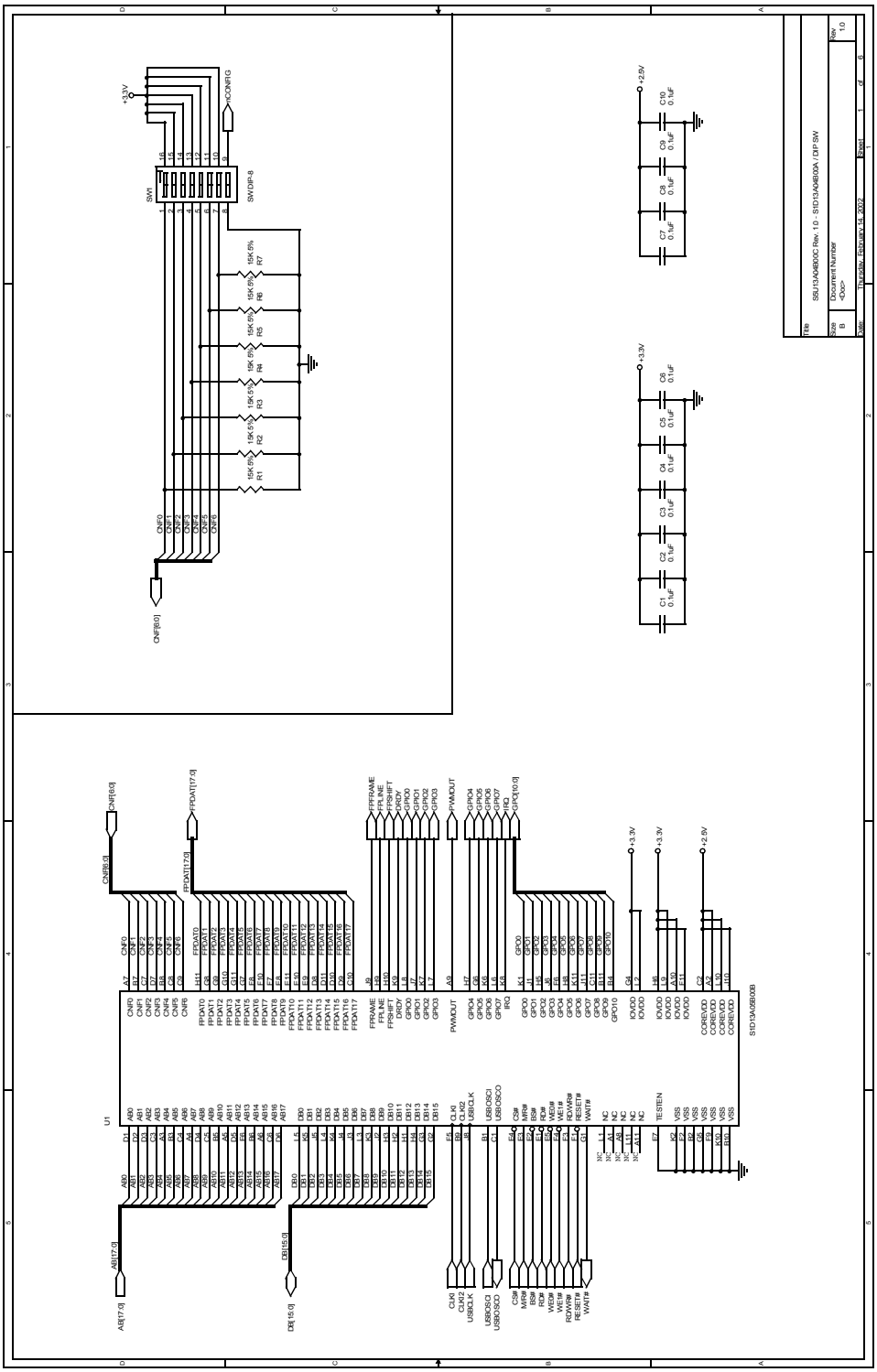

Figure 9-1: S1D13A05B00C Schematics (1 of 6)

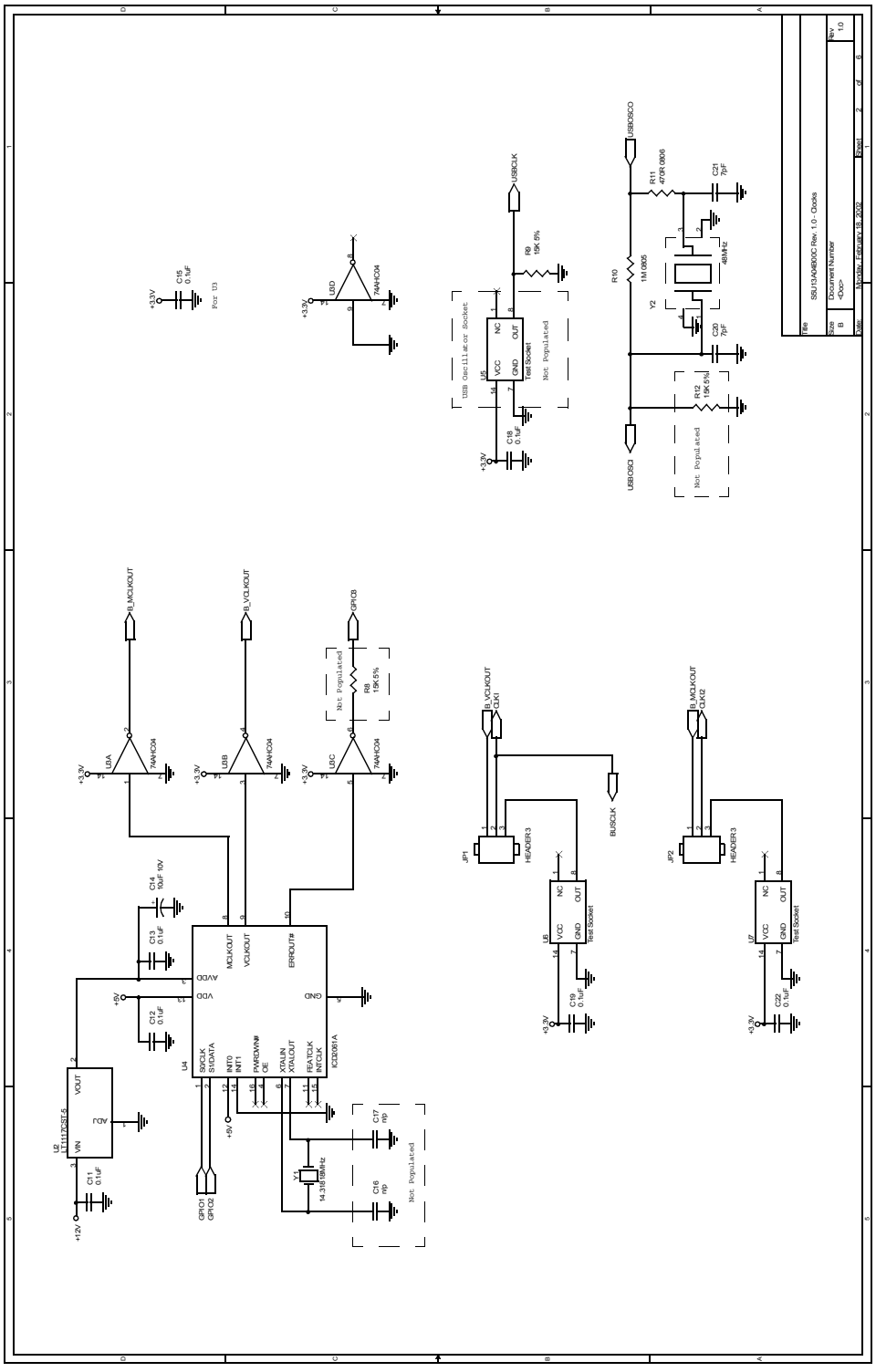

Figure 9-2: S1D13A05B00C Schematics (2 of 6)

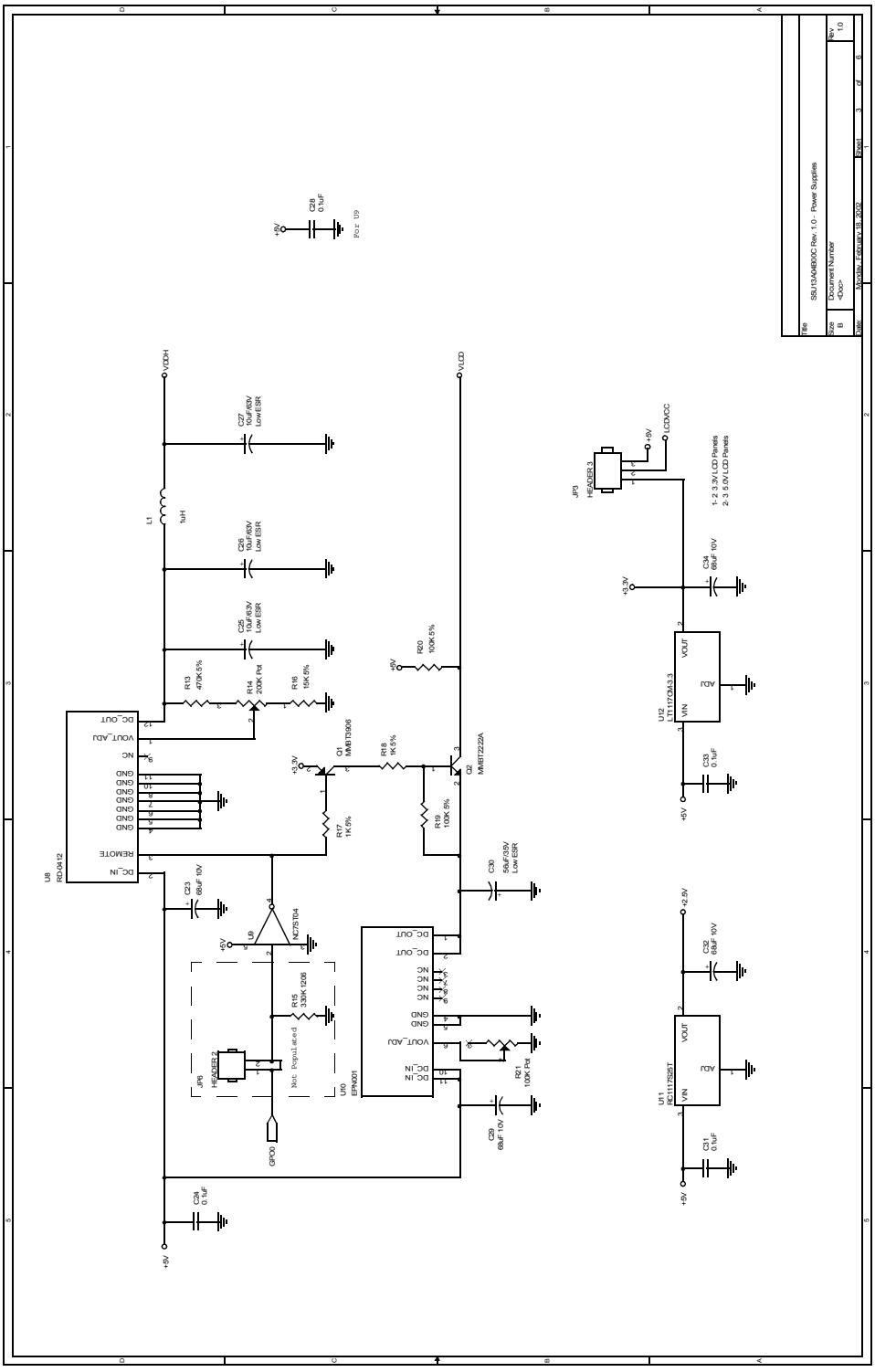

Figure 9-3: S1D13A05B00C Schematics (3 of 6)

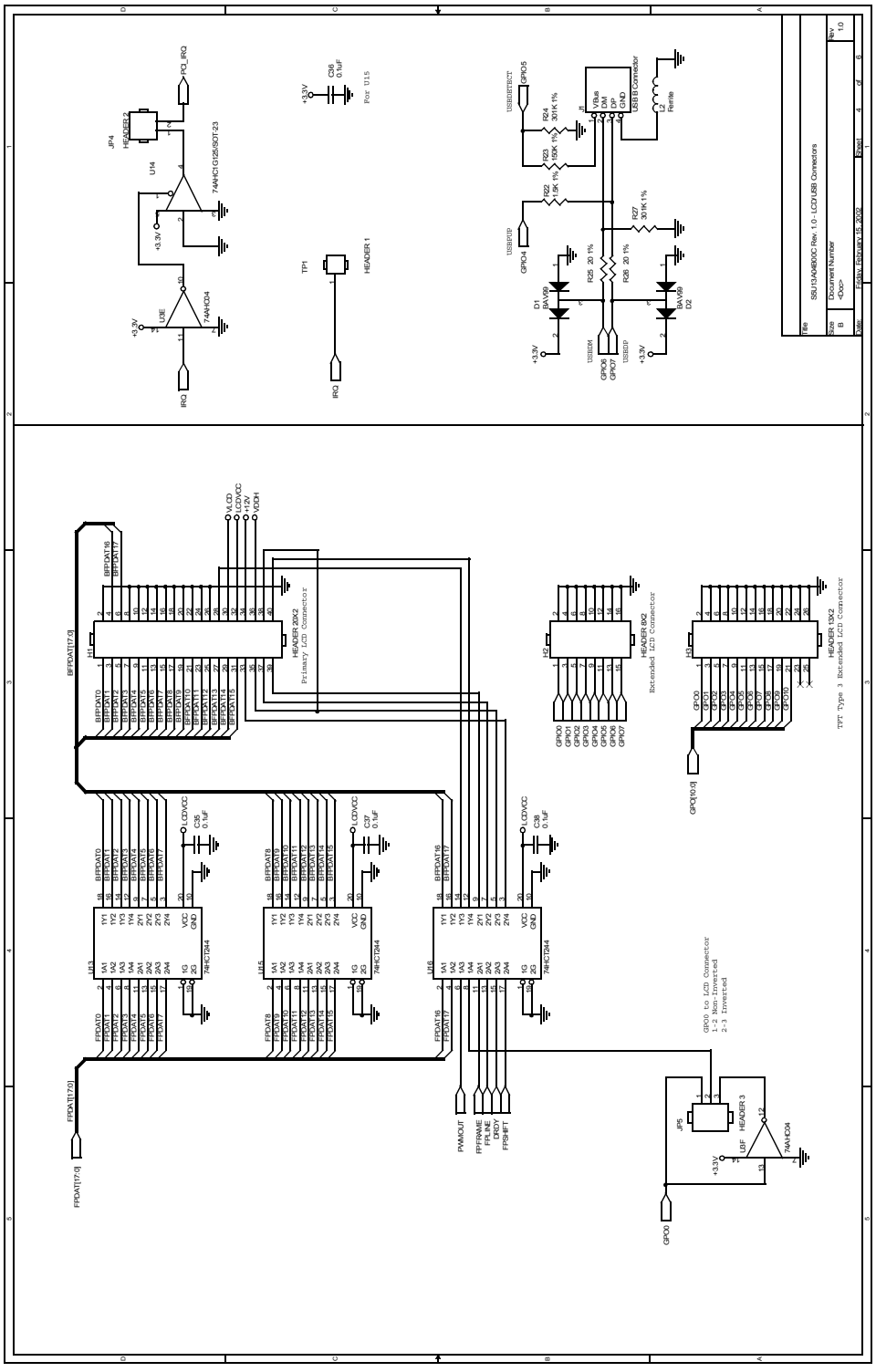

Figure 9-4: S1D13A05B00C Schematics (4 of 6)

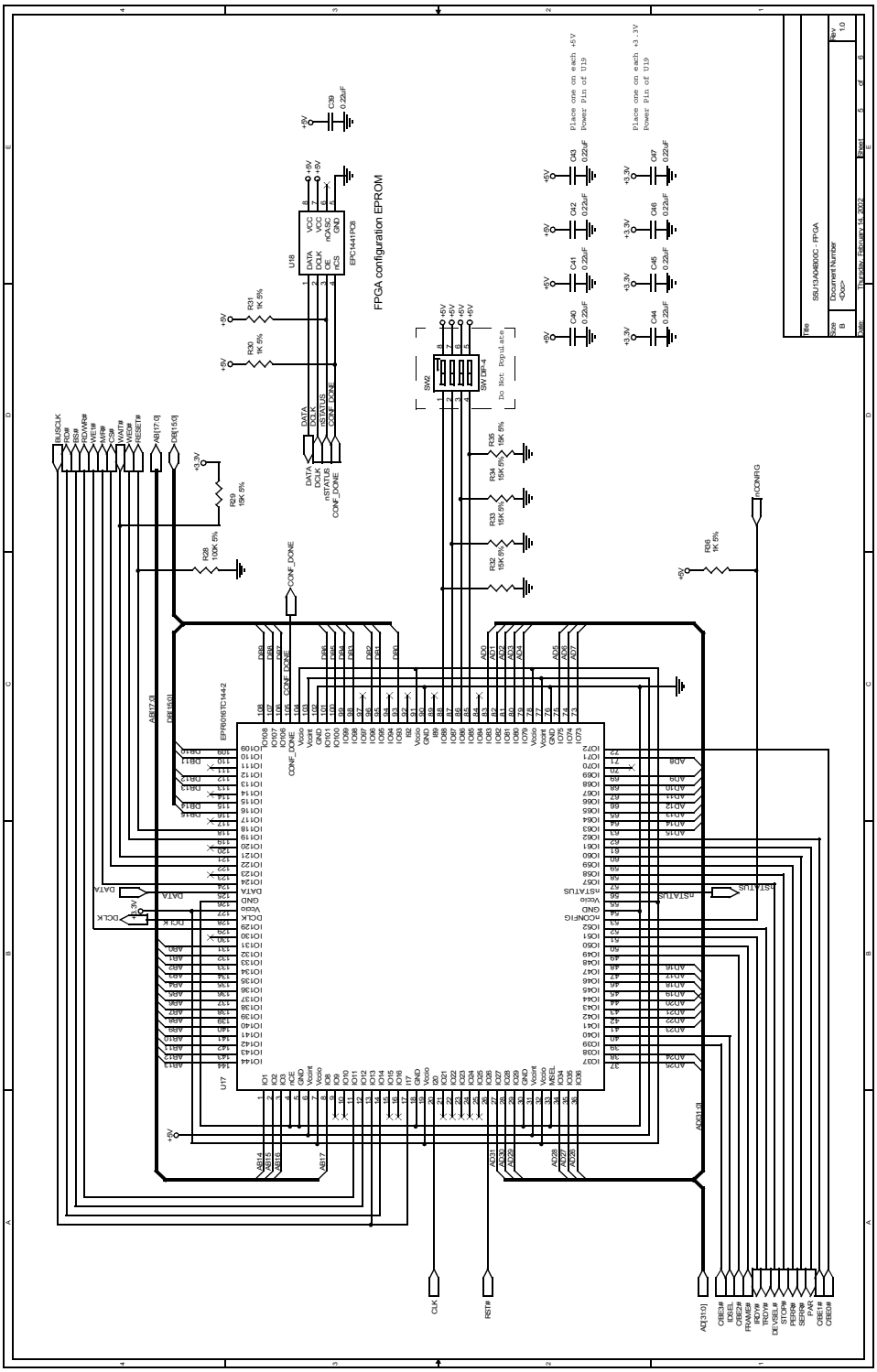

Figure 9-5: S1D13A05B00C Schematics (5 of 6)

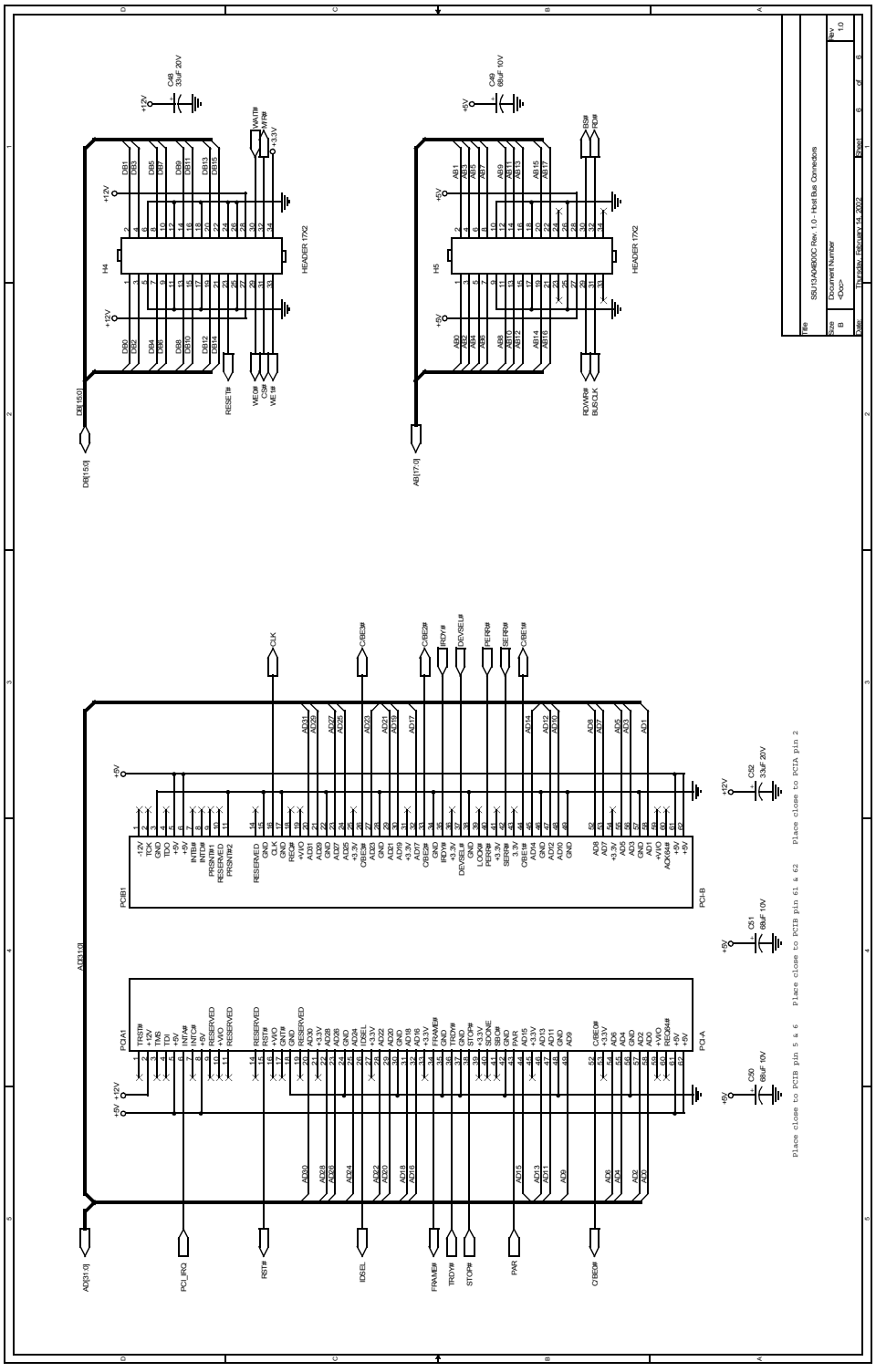

Figure 9-6: S1D13A05B00C Schematics (6 of 6)

10 Board Layout

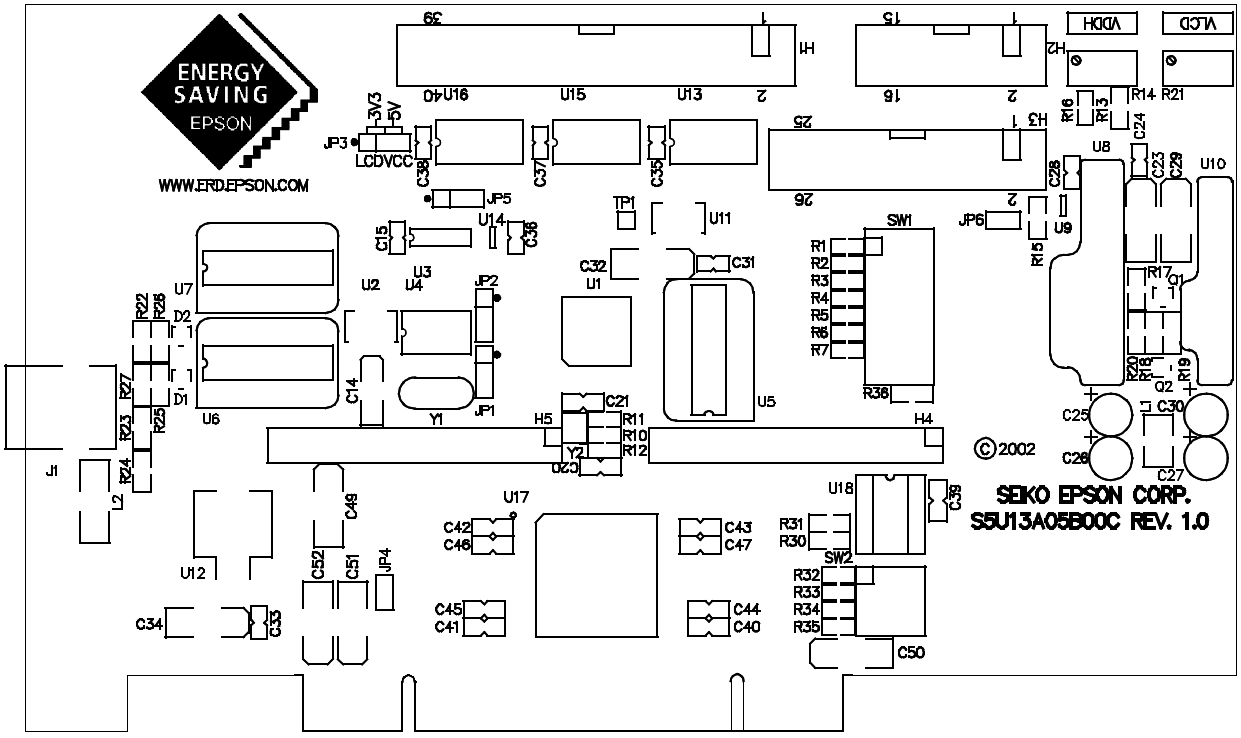

Figure 10-1: S5U13A05B00C Board Layout (Top View)

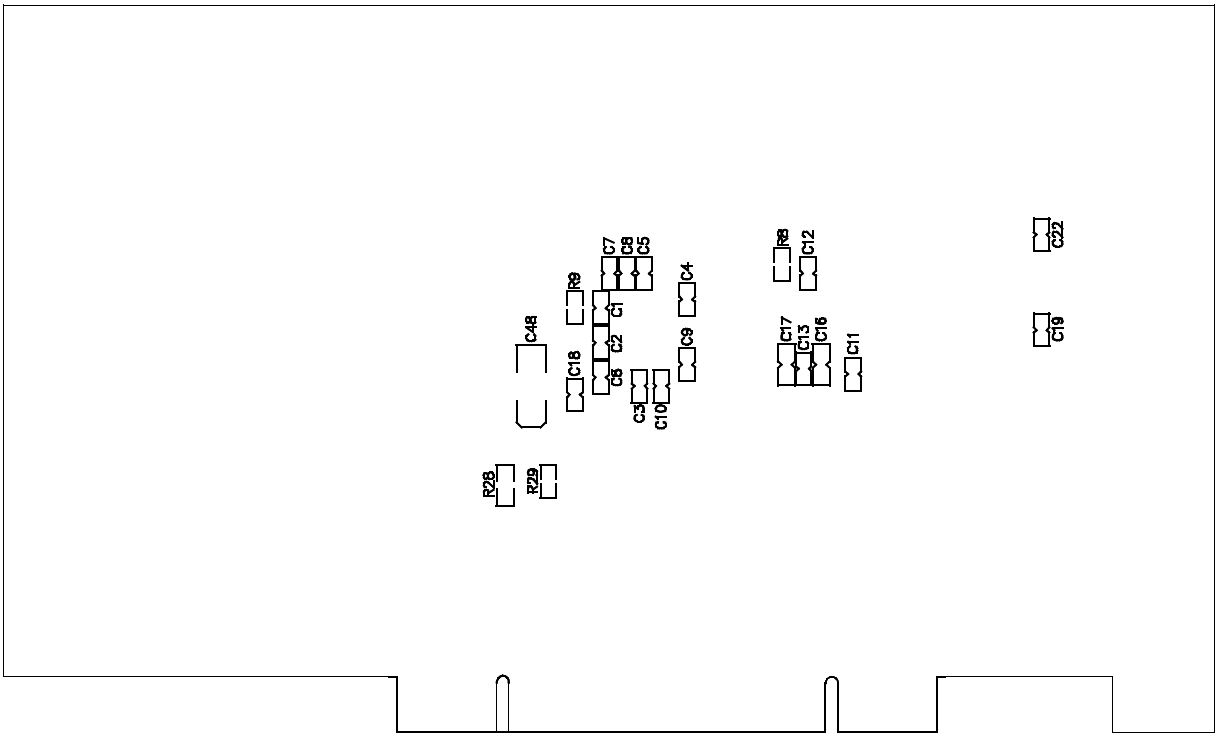

Figure 10-2: S5U13A05B00C Board Layout (Bottom View)

11 Change Record

X40A-G-004-02 Revision 1.1 - Issued: March 28, 2018

- updated Sales and Technical Support Section
- updated some formatting

12 Sales and Technical Support

For more information on Epson Display Controllers, visit the Epson Global website.

https://global.epson.com/products_and_drivers/semicon/products/display_controllers/

For Sales and Technical Support, contact the Epson representative for your region.

https://global.epson.com/products_and_drivers/semicon/information/support.html