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S1D13A04 LCD/USB Companion Chip

Power Consumption

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SEIKO EPSON CORPORATION

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1 S1D13A04 Power Consumption

S1D13A04 power consumption is affected by many system design variables.

- Input clock frequency (CLKI/CLKI2): the CLKI/CLKI2 frequency determines the LCD frame-rate, CPU performance to memory, and other functions – the higher the input clock frequency, the higher the frame-rate, performance and power consumption.
- CPU interface: the S1D13A04 current consumption depends on the BCLK frequency, data width, number of toggling pins, and other factors – the higher the BCLK, the higher the CPU performance and power consumption.
- V_{DD} voltage level: the voltage level affects power consumption – the higher the voltage, the higher the consumption.
- Display mode: the resolution and color depth affect power consumption – the higher the resolution/color depth, the higher the consumption.
- Internal CLK divide: internal registers allow the input clock to be divided before going to the internal logic blocks – the higher the divide, the lower the power consumption.

There is a power save mode in the S1D13A04. The power consumption is affected by various system design variables.

- Clock states during the power save mode: disabling the clocks during power save mode has substantial power savings.

1.1 Conditions

The following table provides an example of some 320x240 panels and the effects on power consumption of specific environments. The following conditions apply.

- All tests had an appropriate LCD panel connected to the LCD outputs of the S1D13A04.
- All tests were run with a static full color palette display.
- All tests were done using the Generic #1 host bus interface (BCLK = 33MHz).

Table 1-1: S1D13A04 Total Power Consumption for 320x240 panels

Test Condition *All $COREV_{DD}$ = 2.0V and IOV_{DD} = 3.3V*					Power Consumption (mA)				
					S1D13A04 Active		Power Save Mode		
Resolution	**Panel Type**	**Frame Rate**	**Clocks (MHz)**	**Color Depth**	**CORE**	**IO**	**CORE[1]**	**IO[1]**	**Clocks Removed[2]**
320x240	Color 8-bit Format 2	67	CLKI = 6 = BCLK = MCLK CLKI2 = 6 = PCLK USBCLK = 48	4	1.7	0.7	0.7	0.1	0.1
		67		8	2.1	0.7	0.7	0.1	0.1
		67		16	2.4	0.6	0.7	0.1	0.1
		67	CLKI = 6 = BCLK CLKI2 = 6 = PCLK USBCLK = grounded	8	1.8	0.6	0.4	0.0	0.1
	Color 4-bit	94	CLKI = 33.3 = MCLK = BCLK CLKI2 = grounded USBCLK = 48, PCLK = MCLK / 4	8	4.3	1.3	2.3	0.2	0.1
		94	CLKI = 33.3 = MCLK = BCLK CLKI2 = grounded USBCLK = grounded, PCLK = MCLK / 4	8	4.0	1.2	2.1	0.1	0.1
	18-bit TFT	79	CLKI = 33.3 = MCLK = BCLK CLKI2 = grounded USBCLK = 48, PCLK = MCLK / 4	8	3.7	2.9	2.3	0.2	0.1
		79	CLKI = 33.3 = MCLK = BCLK CLKI2 = grounded USBCLK = grounded, PCLK = MCLK / 4	8	3.5	2.8	2.1	0.1	0.1

1. The S1D13A04 has Power Save Mode enabled, but the clocks (CLKI, CLKI2 and USBCLK) remain active unless specified otherwise.
2. CLKI, CLKI2, and USBCLK are grounded for the Clocks Removed condition.

The following table provides an example of some 160x160 panels and the effects on power consumption of specific environments. The following conditions apply.

- All tests had an appropriate LCD panel connected to the LCD outputs of the S1D13A04.
- All tests were run with a static full color palette display, **except the test where the 2D BitBLT engine was running**.
- All tests were done using the Generic #1 host bus interface (BCLK = 33MHz).

Table 1-2: S1D13A04 Total Power Consumption for 160x160 panels

Test Condition *All $COREV_{DD}$ = 2.0V and IOV_{DD} = 3.3V*					**Power Consumption (mA)**				
					S1D13A04 Active		**Power Save Mode**		
Resolution	**Panel Type**	**Frame Rate**	**Clocks (MHz)**	**Color Depth**	**CORE**	**IO**	**CORE[1]**	**IO[1]**	**Clocks Removed[2]**
160x160	18-bit HR-TFT	67	CLKI = 33.3 = MCLK = BCLK CLKI2 = 3 = PCLK USBCLK = 48	4	2.5	0.9	2.2	0.2	0.1
		67		8	2.6	1.1	2.2	0.2	0.1
		67		16	2.8	1.1	2.2	0.2	0.1
		67	CLKI = 33.3 = MCLK = BCLK CLKI2 = 3 = PCLK USBCLK = grounded	16	2.6	1.0	4.2	0.1	0.1
	18-bit HR-TFT	67	CLKI = 33.3 = MCLK = BCLK CLKI2 = 3 = PCLK USBCLK = 48, 2D BitBLT engine running[3]	16	12.3	2.4	—[5]	—[5]	0.1
	18-bit HR-TFT	67	CLKI = 33.3 = MCLK = BCLK CLKI2 = 3 = PCLK USBCLK = 48, USB is active/running[4]	16	12.4	1.6	—[5]	—[5]	0.1

1. The S1D13A04 has Power Save Mode enabled, but the clocks (CLKI, CLKI2 and USBCLK) remain active unless specified otherwise.
2. CLKI, CLKI2, and USBCLK are grounded for the Clocks Removed condition.
3. This test has the 2D BitBLT engine performing a Move BitBLT which requires a high-level of CPU activity and a rapidly updating display.
4. This test has the S1D13A04 USB module running a loop-back test.
5. This result is not applicable. See the 16 bpp color depth results for power save mode.

2 Summary

The system design variables in Section 1, “S1D13A04 Power Consumption” and in Table 1-1: “S1D13A04 Total Power Consumption for 320x240 panels” show that S1D13A04 power consumption depends on the specific implementation. Active Mode power consumption depends on the desired CPU performance and LCD frame-rate, whereas power save mode consumption depends on the CPU Interface and Input Clock state.

In a typical design environment, the S1D13A04 can be configured to be an extremely power-efficient LCD Controller with high performance and flexibility.

3 Change Record

X37A-G-006-01 Revision 1.1 - Issued: March 28, 2018

- updated Sales and Technical Support Section
- updated some formatting

4 Sales and Technical Support

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