EPSON
EXCEED YOUR VISION

S1D13A04 LCD/USB Companion Chip

S5U13A04B00C Rev. 1.0 Evaluation Board User Manual

Document Number: X37A-G-004-03.1

SEIKO EPSON CORPORATION

Rev. 3.1

Evaluation Board/Kit and Development Tool Important Notice

1. This evaluation board/kit or development tool is designed for use for engineering evaluation, demonstration, or development purposes only. Do not use it for other purposes. It is not intended to meet the requirements of design for finished products.
2. This evaluation board/kit or development tool is intended for use by an electronics engineer and is not a consumer product. The user should use it properly and in a safe manner. Seiko Epson does not assume any responsibility or liability of any kind of damage and/or fire caused by the use of it. The user should cease to use it when any abnormal issue occurs even during proper and safe use.
3. The part used for this evaluation board/kit or development tool may be changed without any notice.

NOTICE

No part of this material may be reproduced or duplicated in any form or by any means without the written permission of Seiko Epson. Seiko Epson reserves the right to make changes to this material without notice. Seiko Epson does not assume any liability of any kind arising out of any inaccuracies contained in this material or due to its application or use in any product or circuit and, further, there is no representation that this material is applicable to products requiring high level reliability, such as, medical products. Moreover, no license to any intellectual property rights is granted by implication or otherwise, and there is no representation or warranty that anything made in accordance with this material will be free from any patent or copyright infringement of a third party. When exporting the products or technology described in this material, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You are requested not to use, to resell, to export and/or to otherwise dispose of the products (and any technical information furnished, if any) for the development and/or manufacture of weapon of mass destruction or for other military purposes.

All brands or product names mentioned herein are trademarks and/or registered trademarks of their respective companies.

Table of Contents

1 Introduction

This manual describes the setup and operation of the S5U13A04B00C Rev. 1.0 Evaluation Board. The board is designed as an evaluation platform for the S1D13A04 LCD/USB Companion Chip.

This document is updated as appropriate. Please check for the latest revision of this document before beginning any development. The latest revision can be downloaded at vdc.epson.com.

We appreciate your comments on our documentation. Please contact us via email at vdc-documentation@ea.epson.com.

2 Features

Following are some features of the S5U13A04B00C Rev. 1.0 Evaluation Board:

- 121-pin PFBGA S1D13A04 Embedded Memory LCD Controller with 160K bytes of embedded SRAM.
- PCI bus operation through onboard PCI bridge.
- CPU/Bus interface header strips for non-PCI bus operation.
- Configuration options.
- On-board adjustable positive LCD bias power supply from +23V to +40V.
- On-board adjustable negative LCD bias power supply from -14V to -24V.
- Software adjustable backlight intensity support using PWMOUT.
- 4/8-bit 3.3V or 5V single monochrome passive LCD panel support.
- 4/8/16-bit 3.3V or 5V single color passive LCD panel support.
- 9/12/18-bit 3.3V or 5V active matrix TFT LCD panel support.
- Direct interface for 18-bit Epson D-TFD LCD panel support.
- Direct interface for 18-bit Sharp HR-TFT LCD panel support.
- Programmable clock synthesizer to CLKI and CLKI2 for maximum clock flexibility.
- Connector for USB client support.
- Software initiated power save mode.
- Selectable clock source for CLKI and CLKI2.
- External oscillator support for CLKI and CLKI2.

3 Installation and Configuration

The S5U13A04B00C is designed to support as many platforms as possible. The S5U13A04B00C incorporates a DIP switch and five jumpers which allow both the evaluation board and the S1D13A04 LCD controller to be configured for a specified evaluation platform.

3.1 Configuration DIP Switches

The S1D13A04 has configuration inputs (CNF[6:0]) which are read on the rising edge of RESET#. In order to configure the S1D13A04 for multiple Host Bus Interfaces an eight-position DIP switch (SW1) is required. The following figure shows the location of DIP switch SW1 on the S5U13A04B00C.

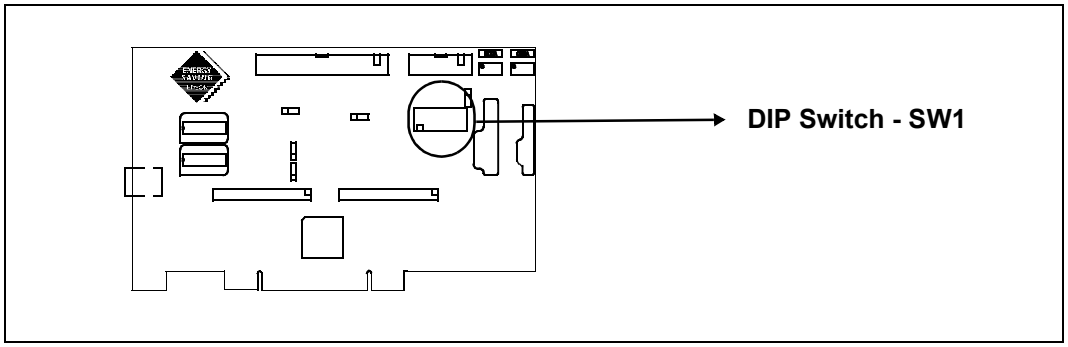

Figure 3-1: Configuration DIP Switch (SW1) Location

The S1D13A04 has seven configuration inputs (CONF[6:0]) which are read on the rising edge of RESET#. All S1D13A04 configuration inputs are fully configurable using an eight position DIP switch as described below.

Table 3-1: Configuration DIP Switch Settings

Switch (SW1)	S1D13A04 Signal	Value on this pin at rising edge of RESET# is used to configure: Closed (On/1)	Open (Off/0)
SW1-5, SW1-[3:1]	CNF4, CNF[2:0]	Select host bus interface as follows: **CNF4 CNF2 CNF1 CNF0 — Host Bus Interface** 1 0 0 0 — SH-4/SH-3 interface, Big Endian 0 0 0 0 — SH-4/SH-3 interface, Little Endian 1 0 0 1 — MC68K #1, Big Endian 0 0 0 1 — Reserved 1 0 1 0 — MC68K #2, Big Endian 0 0 1 0 — Reserved 1 0 1 1 — Generic #1, Big Endian 0 0 1 1 — Generic #1, Little Endian 1 1 0 0 — Reserved 0 1 0 0 — Generic #2, Little Endian 1 1 0 1 — RedCap 2, Big Endian 0 1 0 1 — Reserved 1 1 1 0 — DragonBall, Big Endian 0 1 1 0 — Reserved X 1 1 1 — Reserved	
SW1-4	CNF3	Configure GPIO pins as inputs at power-on	Configure GPIO[7:6] and GPIO[4:0] as outputs and GPIO5 as an input at power-on (for use when USB is selected)
SW1-6	CNF5	WAIT# is active high	WAIT# is active low
SW1-7	CNF6	CLKI to BCLK Divide ratio 2:1	CLKI to BCLK divide ratio 1:1
SW1-8	-	Disable PCI bridge for non-PCI host	Enable PCI bridge for PCI host

= Required settings when used with PCI Bridge FPGA

3.2 Configuration Jumpers

The S5U13A04B00C has five jumper blocks which configure various setting on the board. The jumper positions for each function are shown below.

Table 3-2: Jumper Summary

Jumper	Function	Position 1-2	Position 2-3	No Jumper
JP1	CLKI Source	VCLKOUT from clock synthesizer	External oscillator (U7)	BUSCLK from Header H4
JP2	CLKI2 Source	MCLKOUT from clock synthesizer	External oscillator (U8)	—
JP3	LCD Panel Voltage	+5V LCDVCC	+3.3V LCDVCC	—
JP4	GP0I0 Polarity on H1	Normal (Active High)	Inverted (Active Low)	GPIO0 not sent to H1
JP5	GPIO0 function select	GPIO0	HR-TFT PS signal	—

= recommended settings

JP1 - CLKI Source

JP1 selects the source for the CLKI input pin.
Position 1-2 sets the CLKI source to VCLKOUT from the Cypress clock synthesizer (default setting).
Position 2-3 sets the CLKI source to the external oscillator at U7.

When no jumper is installed, the CLKI source is set to the BUSCLK signal from Header H4.

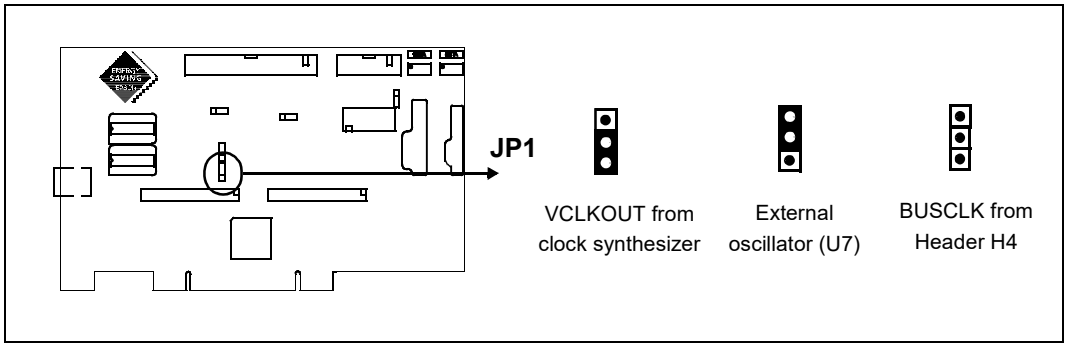

Figure 3-2: Configuration Jumper (JP1) Location

JP2 - CLKI2 Source

JP2 selects the source for the CLKI2 input pin.
Position 1-2 sets the CLKI2 source to MCLKOUT from the Cypress clock synthesizer (default setting).
Position 2-3 sets the CLKI2 source to the external oscillator at U8.

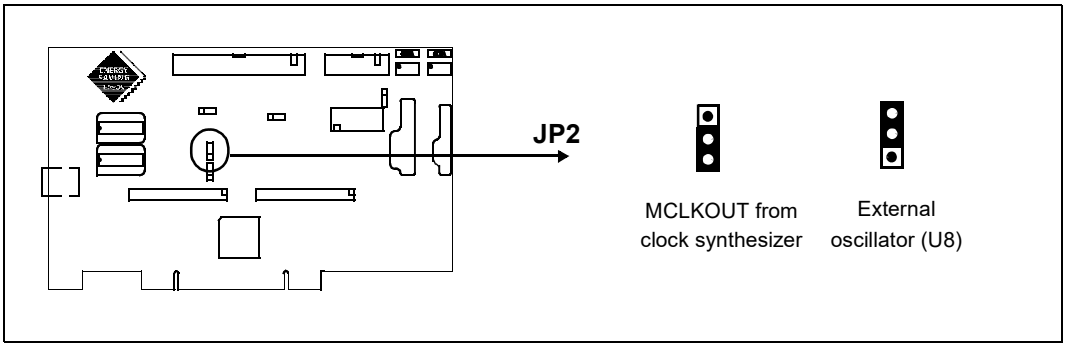

Figure 3-3: Configuration Jumper (JP2) Location

JP3 - LCD Panel Voltage

JP3 selects the voltage level to the LCD panel.
Position 1-2 sets the voltage level to 5.0V (default setting).
Position 2-3 sets the voltage level to 3.3V.

Note
When configured for Sharp HR-TFT or Epson D-TFD panels, JP3 and JP5 must be set to position 2-3.

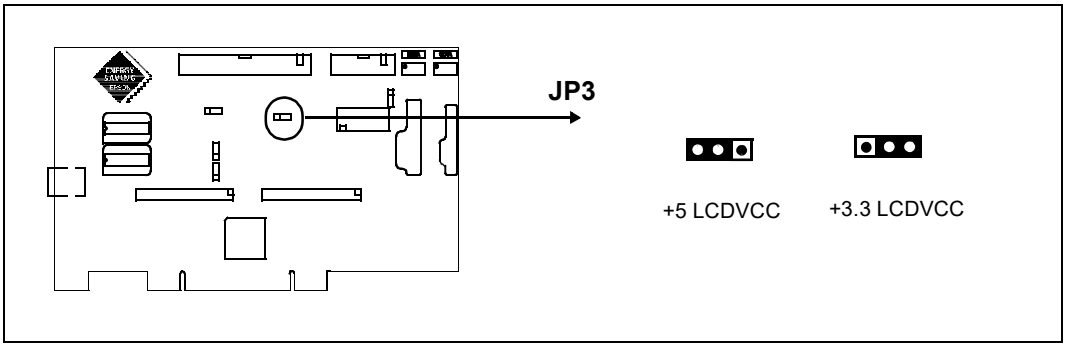

Figure 3-4: Configuration Jumper (JP3) Location

JP4 - GPIO0 Polarity on H1

JP4 selects the polarity of the GPIO0 signal available on the LCD Connector H1.
Position 1-2 sends the GPIO0 signal directly to H1 (default setting).
Position 2-3 inverts the GPIO0 signal before sending it to H1.
When no jumper is installed, GPIO0 is not sent to H1.

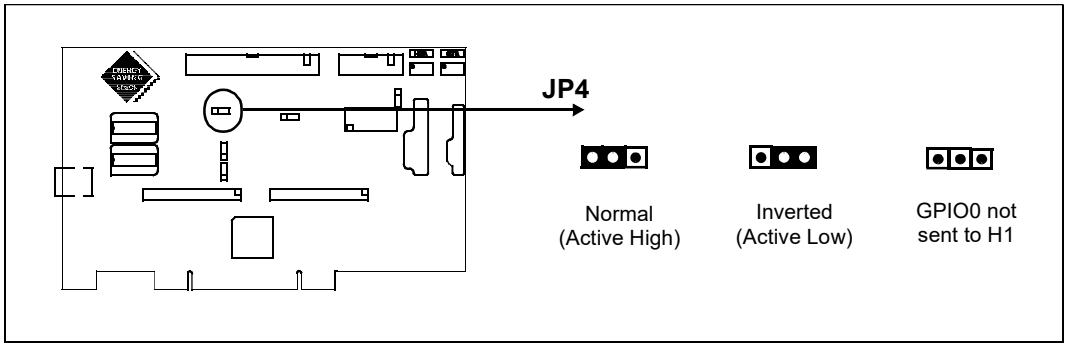

Figure 3-5: Configuration Jumper (JP4) Location

JP5 - GPIO0 Selection

JP5 selects the function of the GPIO0 signal.
Position 1-2 GPIO0 used to control the LCD bias power supplies for STN panels.
Position 2-3 GPIO0 used as the PS signal when the S1D13A04 is configured for HR-TFT panel type.

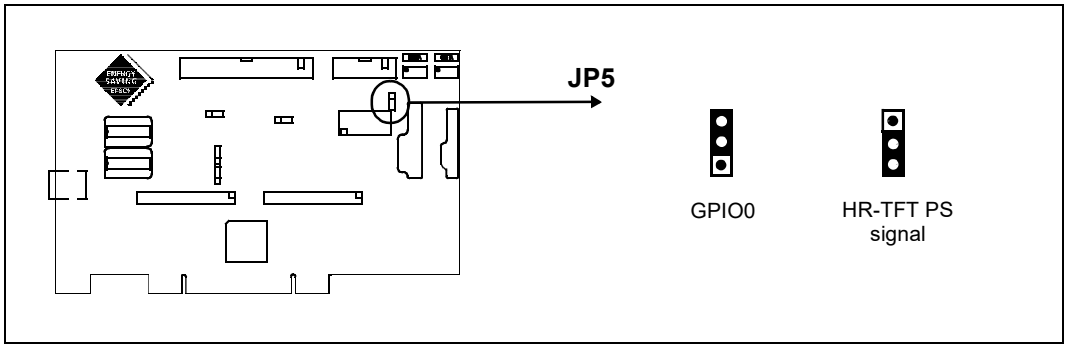

Figure 3-6: Configuration Jumper (JP5) Location

4 CPU Interface

4.1 CPU Interface Pin Mapping

Table 4-1: CPU Interface Pin Mapping

S1D13A04 Pin Name	Generic #1	Generic #2	Hitachi SH-3 /SH-4	Motorola MC68K #1	Motorola MC68K #2	Motorola REDCAP2	Motorola MC68EZ328/ MC68VZ328 DragonBall
AB[17:1]	A[17:1]	A[17:1]	A[17:1]	A[17:1]	A[17:1]	A[17:1]	A[17:1]
AB0	A0[1]	A0	A0[1]	LDS#	A0	A0[1]	A0[1]
DB[15:0]	D[15:0]	D[15:0]	D[15:0]	D[15:0]	D[15:0][2]	D[15:0]	D[15:0]
CS#	External Decode		CSn#	External Decode		$\overline{CSn}$	$\overline{CSX}$
M/R#	External Decode						
CLKI	BUSCLK	BUSCLK	CKIO	CLK	CLK	CLK	CLK
BS#	Connected to $HIOV_{DD}$[3]		BS#	AS#	AS#	Connected to $HIOV_{DD}$[3]	
RD/WR#	RD1#	Connected to $HIOV_{DD}$[3]	RD/WR#	R/W#	R/W#	R/$\overline{W}$	Connected to $HIOV_{DD}$[3]
RD#	RD0#	RD#	RD#	Connected to $HIOV_{DD}$[3]	SIZ1	$\overline{OE}$	$\overline{OE}$
WE0#	WE0#	WE#	WE0#	Connected to $HIOV_{DD}$[3]	SIZ0	$\overline{EB1}$	$\overline{LWE}$
WE1#	WE1#	BHE#	WE1#	UDS#	DS#	$\overline{EB0}$	$\overline{UWE}$
WAIT#	WAIT#	WAIT#	WAIT#/ RDY#	DTACK#	DSACK1#	N/A	$\overline{DTACK}$
RESET#	RESET#	RESET#	RESET#	RESET#	RESET#	$\overline{RESET\_OUT}$	$\overline{RESET}$

Note

[1] A0 for these busses is not used internally by the S1D13A04 and should be connected to V_{SS}.

[2] If the target MC68K bus is 32-bit, then these signals should be connected to D[31:16].

[3] These pins are not used in their corresponding host interface mode. Systems are responsible for externally connecting them to Host Interface IO V_{DD}.

4.2 CPU Bus Connector Pin Mapping

Table 4-2: CPU Bus Connector (H3) Pinout

Connector Pin No.	Comments
1	Connected to DB0 of the S1D13A04
2	Connected to DB1 of the S1D13A04
3	Connected to DB2 of the S1D13A04
4	Connected to DB3 of the S1D13A04
5	Ground
6	Ground
7	Connected to DB4 of the S1D13A04
8	Connected to DB5 of the S1D13A04
9	Connected to DB6 of the S1D13A04
10	Connected to DB7 of the S1D13A04
11	Ground
12	Ground
13	Connected to DB8 of the S1D13A04
14	Connected to DB9 of the S1D13A04
15	Connected to DB10 of the S1D13A04
16	Connected to DB11 of the S1D13A04
17	Ground
18	Ground
19	Connected to DB12 of the S1D13A04
20	Connected to DB13 of the S1D13A04
21	Connected to DB14 of the S1D13A04
22	Connected to DB15 of the S1D13A04
23	Connected to RESET# of the S1D13A04
24	Ground
25	Ground
26	Ground
27	+12 volt supply
28	+12 volt supply
29	Connected to WE0# of the S1D13A04
30	Connected to WAIT# of the S1D13A04
31	Connected to CS# of the S1D13A04
32	Connected to MR# of the S1D13A04
33	Connected to WE1# of the S1D13A04
34	Connected to +3.3V

Table 4-3: CPU Bus Connector (H4) Pinout

Connector Pin No.	Comments
1	Connected to AB0 of the S1D13A04
2	Connected to AB1 of the S1D13A04
3	Connected to AB2 of the S1D13A04
4	Connected to AB3 of the S1D13A04
5	Connected to AB4 of the S1D13A04
6	Connected to AB5 of the S1D13A04
7	Connected to AB6 of the S1D13A04
8	Connected to AB7 of the S1D13A04
9	Ground
10	Ground
11	Connected to AB8 of the S1D13A04
12	Connected to AB9 of the S1D13A04
13	Connected to AB10 of the S1D13A04
14	Connected to AB11 of the S1D13A04
15	Connected to AB12 of the S1D13A04
16	Connected to AB13 of the S1D13A04
17	Ground
18	Ground
19	Connected to AB14 of the S1D13A04
20	Connected to AB15 of the S1D13A04
21	Connected to AB16 of the S1D13A04
22	Connected to AB17 of the S1D13A04
23	Not connected
24	Not connected
25	Ground
26	Ground
27	+5 volt supply
28	+5 volt supply
29	Connected to RD/WR# of the S1D13A04
30	Connected to BS# of the S1D13A04
31	Connected to BUSCLK of the S1D13A04
32	Connected to RD# of the S1D13A04
33	Not connected
34	Not connected

5 LCD Interface Pin Mapping

Table 5-1: LCD Signal Connector (H1)

Pin Name	Connector Pin No.	Monochrome Passive Panel		Color Passive Panel				Color TFT Panel			
		Single		Single				Others			Sharp HR-TFT
					Format 1	Format 2					
		4-bit	8-bit	4-bit	8-bit	8-bit	16-Bit	9-bit	12-bit	18-bit	18-bit
FPDAT0	1	driven 0	D0	driven 0	D0 (B5)[1]	D0 (G3)[1]	D0 (R6)[1]	R2	R3	R5	R5
FPDAT1	3	driven 0	D1	driven 0	D1 (R5)[1]	D1 (R3)[1]	D1 (G5)[1]	R1	R2	R4	R4
FPDAT2	5	driven 0	D2	driven 0	D2 (G4)[1]	D2 (B2)[1]	D2 (B4)[1]	R0	R1	R3	R3
FPDAT3	7	driven 0	D3	driven 0	D3 (B3)[1]	D3 (G2)[1]	D3 (R4)[1]	G2	G3	G5	G5
FPDAT4	9	D0	D4	D0 (R2)[1]	D4 (R3)[1]	D4 (R2)[1]	D8 (B5)[1]	G1	G2	G4	G4
FPDAT5	11	D1	D5	D1 (B1)[1]	D5 (G2)[1]	D5 (B1)[1]	D9 (R5)[1]	G0	G1	G3	G3
FPDAT6	13	D2	D6	D2 (G1)[1]	D6 (B1)[1]	D6 (G1)[1]	D10 (G4)[1]	B2	B3	B5	B5
FPDAT7	15	D3	D7	D3 (R1)[1]	D7 (R1)[1]	D7 (R1)[1]	D11 (B3)[1]	B1	B2	B4	B4
FPDAT8	17	driven 0	driven 0	driven 0	driven 0	driven 0	D4 (G3)[1]	B0	B1	B3	B3
FPDAT9	19	driven 0	driven 0	driven 0	driven 0	driven 0	D5 (B2)[1]	driven 0	R0	R2	R2
FPDAT10	21	driven 0	driven 0	driven 0	driven 0	driven 0	D6 (R2)[1]	driven 0	driven 0	R1	R1
FPDAT11	23	driven 0	driven 0	driven 0	driven 0	driven 0	D7 (G1)[1]	driven 0	driven 0	R0	R0
FPDAT12	25	driven 0	driven 0	driven 0	driven 0	driven 0	D12 (R3)[1]	driven 0	G0	G2	G2
FPDAT13	27	driven 0	driven 0	driven 0	driven 0	driven 0	D13 (G2)[1]	driven 0	driven 0	G1	G1
FPDAT14	29	driven 0	driven 0	driven 0	driven 0	driven 0	D14 (B1)[1]	driven 0	driven 0	G0	G0
FPDAT15	31	driven 0	driven 0	driven 0	driven 0	driven 0	D15 (R1)[1]	driven 0	B0	B2	B2
FPDAT16	4	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	B1	B1
FPDAT17	6	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	B0	B0
FPSHIFT	33	FPSHIFT									CLK
DRDY	35 & 38	MOD			FPSHIFT2	MOD		DRDY			GPO[3]
FPLINE	37	FPLINE									LP
FPFRAME	39	FPFRAME									SPS
GND	2, 8, 14, 20, 26	GND									
PWMOUT	28	PWMOUT									
VLCD	30	Adjustable -24V to -14V negative LCD bias									
VCC	32	LCDVCC (3.3V or 5V)									
+12V	34	+12V									
VDDH	36	Adjustable +23V to +40V positive LCD bias									
DISPLAY[2]	40	GPIO0 (for controlling on-board LCD bias power supply on/off)									PS

Note

[1] These pin mappings use signal names commonly used for each panel type, however signal names may differ between panel manufacturers. The values shown in brackets represent the color components as mapped to the corresponding FPDATxx signals at the first valid edge of FPSHIFT. For further FPDATxx to LCD interface mapping, see *S1D13A04 Hardware Functional Specification*, document number X37A-A-001-xx.

[2] DISPLAY can be disconnected from GPIO0 using JP5 (2-3 position) and can be inverted on H1 setting JP4 to 2-3.

[3] When the 'Direct' HR-TFT interface is selected, DRDY becomes a general purpose output (GPO) controllable using the 'Direct' HR-TFT LCD Interface GPO Control bit

(REG[14h] bit 0). This GPO can be used to control the HR-TFT MOD signal if required. For further information, see the *S1D13A04 Hardware Functional Specification*, document number X37A-A-001-xx.

Table 5-2: Extended LCD Signal Connector (H2)

Pin Name	Connector Pin No.	Monochrome Passive Panel		Color Passive Panel				Color TFT Panel				USB[3]
		Single		Single				Others			HR-TFT[2]	
					Format 1	Format 2						
		4-bit	8-bit	4-bit	8-bit	8-bit	16-Bit	9-bit	12-bit	18-bit	18-bit	
GPIO0[1]	1	GPIO0									PS	GPIO0
GPIO1[1]	3	GPIO1									CLS	GPIO1
GPIO2[1]	5	GPIO2									REV	GPIO2
GPIO3[1]	7	GPIO3									SPL	GPIO3
GPIO4[1]	9	GPIO4										USBPUP
GPIO5[1]	11	GPIO5										USBDETECT
GPIO6[1]	13	GPIO6										USBDM
GPIO7[1]	15	GPIO7										USBDP
GND	2, 4, 6, 8, 10, 12, 14, 16	GND										

Note

[1] When Switch SW1-4 is open (CNF3 = 0 at RESET#), GPIO[7:6] and GPIO[4:0] are set as outputs at 0 (low state) and GPIO5 is set as an input at power-on/RESET# (for use when USB is selected). If SW1-4 is closed then GPIO[7:0] are set as inputs upon power-on/RESET#.

[2] If the 'Direct' HR-TFT interface is selected (REG[0Ch] bits 1:0 = 10), GPIO[3:0] are used for the 'Direct' HR-TFT interface. GPIO[7:4] remain available for USB support or as GPIOs.

[3] If USB support is enabled (REG[4000h] bit 7 = 1), GPIO[7:4] are used by the USB interface. GPIO[3:0] remain available for 'Direct' HR-TFT interface support or as GPIOs.

6 Technical Description

6.1 PCI Bus Support

The S1D13A04 **does not** have on-chip PCI bus interface support. The S1D13A04B00C uses the PCI Bridge FPGA to support the PCI bus.

6.2 Direct Host Bus Interface Support

The S5U13A04B00C is specifically designed to work using the PCI Bridge FPGA in a standard PCI bus environment. However, the S1D13A04 directly supports many other host bus interfaces. Connectors H3 and H4 provide the necessary IO pins to interface to these host buses. For further information on the host bus interfaces supported, see "CPU Interface" on page 12.

Note

The PCI Bridge FPGA must be disabled using SW1-8 in order for direct host bus interface to operate properly.

6.3 S1D13A04 Embedded Memory

The S1D13A04 has 160K bytes of embedded SRAM. The 160K byte display buffer address space is directly and contiguously available through the 18-bit address bus.

6.4 Adjustable LCD Panel Negative Power Supply

Most monochrome passive LCD panels require a negative power supply to provide between -14V and -24V (I_{out}=45mA). Such a power supply (VLCD) has been provided on the S5U13A04B00C board. VLCD can be adjusted using potentiometer R39 to provide an output voltage from -14V to -24V, and is enabled/disabled using the S1D13A04 general purpose signal, GPIO0 (active high).

Note

When manually adjusting the voltage, set the potentiometer according to the panel's specific power requirements **before connecting the panel.**

6.5 Adjustable LCD Panel Positive Power Supply

Most color passive LCD panels and most single monochrome 640x480 passive LCD panels require a positive power supply to provide between +23V and +40V (I_{out}=45mA). Such a power supply (VDDH) has been provided on the S5U13A04B00C board. VDDH can be adjusted using R22 to provide an output voltage from +23V to +40V, and is enabled/disabled using the S1D13A04 general purpose signal, GPIO0 (active high).

Note

When manually adjusting the voltage, set the potentiometer according to the panel's specific power requirements **before connecting the panel.**

6.6 Software Adjustable LCD Backlight Intensity Support Using PWM

The S1D13A04 provides Pulse Width Modulation output on PWMOUT. PWMOUT can be used to control LCD panels which support PWM control of the backlight inverter. The PWMOUT signal is provided on the LCD connector, H1.

6.7 LCD Panel Support

The S1D13A04 directly supports:

- Single-panel, single drive passive displays.
  - 4/8-bit monochrome interface.
  - 4/8/16-bit color interface.
- Active Matrix TFT interface.
  - 9/12/18-bit interface.
- 'Direct' support for 18-bit Sharp HR-TFT LCD or compatible interface.

All the necessary signals are provided on the 40-pin LCD connector H1 and the 16-pin LCD connector H2. For connection information, refer to Table 5-1: "LCD Signal Connector (H1)" on page 15 and Table 5-2: "Extended LCD Signal Connector (H2)" on page 17.

6.7.1 Direct LCD Connector

The direct LCD Connector (H1) provides all LCD panel signals required for Active Matrix TFT and Passive LCD panels. These signals are buffered to either a 3.3V level or a 5.0V level depending on the setting of JP3. See Table 3-2: "Jumper Summary" on page 9.

6.7.2 Extended LCD Connector

The S1D13A04 directly supports Sharp 18-bit HR-TFT and compatible panels. The extended LCD connector (H2) provides the extra signals required to support these panels. The signals on this connector are provided directly from the S1D13A04 without any buffering and are 3.3V signals.

6.8 USB Support

The S1D13A04 USB controller provides a Revision 1.1 compliant USB client. The S1D13A04 acts as a USB device and connects to an upstream hub or USB host through connector J1 on the S5U13A04B00C evaluation board. Clamping diodes have been added to protect the USB bus from ESD and shorting.

6.8.1 USB IRQ Support

The S1D13A04 supports interrupts through output pin, IRQ. This interrupt can be used to support interrupts from the USB client of the S1D13A04. The S5U13A04B00C evaluation board supports this capability by connecting IRQ to the PCI interrupt INTA# of the PCI slot that the S5U13A04B00C evaluation board is connected to.

7 Clock Synthesizer and Clock Options

For maximum flexibility, the S5U13A04B00C implements a Cypress ICD2061A Clock Synthesizer. MCLKOUT from the clock synthesizer is connected to CLKI2 of the S1D13A04 and VCLKOUT from the clock synthesizer is connected to CLKI of the S1D13A04. A 14.31818MHz crystal (Y1) is connected to XTALIN and XTALOUT of the clock synthesizer and provides the reference clock to the clock synthesizer.

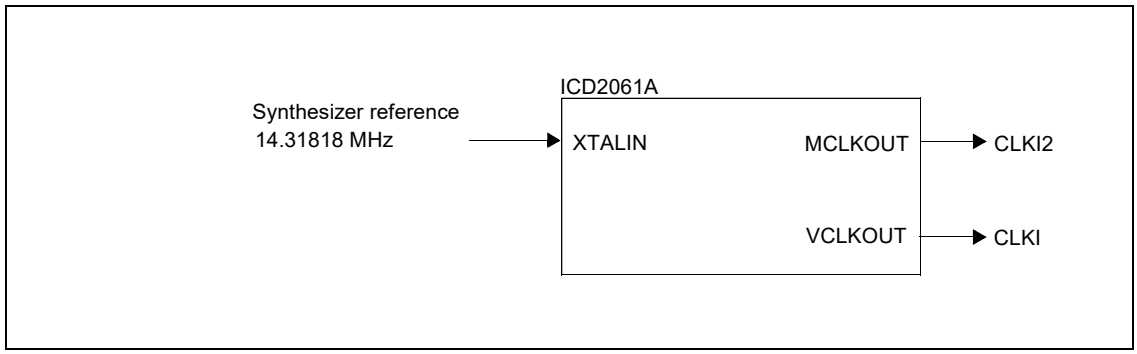

Figure 7-1: Symbolic Clock Synthesizer Connections

At power-on, CLKI2 (MCLKOUT) is configured to be 40MHz and CLKI (VCLKOUT) is configured at 25.175MHz.

Note

If a Sharp HR-TFT panel is selected, the clock synthesizer cannot be programmed, and external oscillators must provide the clock signals to CLKI and CLKI2. Jumpers JP1 and JP2 allow selection of external oscillators U7 and U8 as the clock source for both CLKI and CLKI2. For further information, see Table 3-2: “Jumper Summary” on page 9.

7.1 Clock Programming

The S1D13A04 utilities automatically program the clock generator. If manual programming of the clock generator is required, refer to the source code for the S1D13A04 utilities available on the internet at vdc.epson.com.

For further information on programming the clock generator, refer to the *Cypress ICD2061A specification*.

Note

When CLKI and CLKI2 are programmed to multiples of each other (e.g. CLKI = 20MHz, CLKI2 = 40MHz), the clock output signals from the Cypress clock generator may jitter. Refer to the Cypress ICD2061A specification for details.

To avoid this problem, set CLKI and CLKI2 to different frequencies and use the S1D13A04 internal clock divides to obtain the lower frequencies.

8 Parts List

Table 8-1: Parts List

Item	Qty	Designation	Part Value	Description	Manufacturer / Part No. / Assembly Instructions
1	25	C1-C11,C15-C21,C28,C30,C32-C35,C48	0.1u	Ceramic Chip, 50V X7R +/-5%, 1206 pckg.	Kemet C1206C104J5RAC
2	1	C12	10u,10V	Tantalum C-Size, +/-10%	Kemet T491C106K010AS
3	2	C13,C14	n/p	1206 pckg.	Do not populate
4	7	C22,C2,C29,C31,C45,C46, C49	68u, 10V	Tantalum D-Size, +/-10%	Kemet T491D86K010AS
5	3	C23-C25	10uF, 63V	Electrolytic, Radial Lead, +/-20%	NIPPON/UNITED CHEMI-CON KMF63VB10RM5X11LL
6	1	C27	56uF, 35V	Electrolytic, Radial Lead, +/-20%	NIPPON/UNITED CHEMI-CON KMF35VB56RM5X11LL
7	9	C36-C44	0.22uF	Ceramic Chip, 50V X7R +/-5%, 1206 pckg.	Kemet C1206C224J5RAC
8	2	C47,C50	33u, 20V	Tantalum D-Size, +/-10%	Kemet T491D33K020AS
9	2	D1,D2	BAV99	Ultra high-speed switching diode	Rohm BAV99
10	1	H1	HEADER 20X2	20x2, .025" sq. shrouded header, keyed	Thomas&Betts P/N:636-4027 or equivalent
11	1	H2	HEADER 8X2	8x2, .025" sq. shrouded header, keyed	Thomas&Betts P/N:636-1627 or equivalent
12	2	H3,H4	HEADER 17X2	17x2, .025" sq. unshrouded header, right angle	Thomas&Betts P/N:609-3407 or equivalent
13	5	JP1-JP5	HEADER 3	3x1 .1" pitch unshrouded header	
14	1	J1	USB Type B	Right Angle, Type B USB Connector	AMP787780-1
15	1	L1	1uH	Inductor	RCD MCI-1812 1uH MT
16	1	L2	Ferrite	Ferrite Bead	Phillips BDS3/3/8.9-4S2
17	1	Q1	MMBT3906	PNP signal transistor, SOT23 package	Motorola MMBT3906LT1
18	1	Q2	MMBT2222A	NPN transistor, SOT-23 pckg.	Motorola MMBT2222A
19	13	R1-R7,R23,R31,R34-R37	15K, 5%	1206 Resistor	
20	8	R8-R14,R16	330K, 5%	1206 Resistor	
21	6	R15,R17,R18,R32,R33,R38	1K, 5%	1206 Resistor	
22	3	R19,R20,R30	100K, 5%	1206 Resistor	
23	1	R21	470 Ohm, 5%	1206 Resistor	
24	1	R22	200K Pot	200K Trim Pot	Bourns 3386W-1-204
25	2	R24,R25	20 Ohm, 1%	1206 Resistor	
26	2	R26,R29	301K, 1%	1206 Resistor	
27	1	R27	1.5K, 1%	1206 Resistor	

Table 8-1: Parts List

Item	Qty	Designation	Part Value	Description	Manufacturer / Part No. / Assembly Instructions
28	1	R28	150K, 1%	1206 Resistor	
29	1	R39	100K Pot	100K Trim Pot	Bourns 3386W-1-104
30	1	SW1	SW DIP-8	Dip Switch, 8-Position	
31	1	SW2	SW DIP-4	DIP switch, 4-position	Do Not Populate
32	1	U1	S1D13A04F0A	121-pin PFBGA 13A04 LCDC	Supplied by Epson R&D
33	1	U2	LT1117CST-5	5V fixed voltage regulator, SOT-223	Linear Technology LT1117CST-5
34	1	U3	ICD2061A	Clock Chip, Wide SO-16 pckg	Cypress ICD2061A
35	1	U4	74AHC04	Inverter, SO-14 package	TI74AHC04
36	2	U5,U6	NC7SZ04	TinyLogic UHS inverter, SOT23-5 package	Fairchild NC7SZ04
37	2	U7,U8	Test Socket	14 pin narrow DIP, screw machine socket	Sockets for oscillator input
38	1	U9	RD-0412	Positive LCD Bias Power Supply	Taiyo Yuden/Xentek Positive Power Supply, RD-0412
39	1	U10	EPN001	Negative LCD Bias Power Supply	Taiyo Yuden/Xentek Negative Power Supply, EPN001
40	1	U11	NC7ST04	TinyLogic HST inverter, SOT23-5 package	Fairchild NC7ST04
41	1	U12	LT1118CST-2.5	2.5V fixed volt reg / SOT-223	Linear Technology LT1118CST-2.5
42	1	U13	LT1117CM-3.3	3.3V fixed volt reg / 3 Lead PlasticDD	Linear Technology LT1117CM-3.3
43	3	U14-U16	74HCT244	Buffer, SO-20 package	TI74HCT244
44	1	U17	EPF6016TC144-2	144-pin TQFP FLEX6000 FPGA	Altera EPF6016TC144-2
45	1	U18	EPC1441PC8	8-pin DIP pckg, OTP EPROM	Altera EPC1441PC8, socketed
46	1	U19	74HCT125	Buffer, SO-14 package	TI74HCT125
47	1	Y1	14.31818MHz	14.31818MHz crystal, Fox HC-49	FOX FoxS/143-20 14.31818MHz
48	1	Y2	48MHz Osc	SMD 48MHz oscillator	Epson SG-615PH-48.000MHz
49	1	U18	Socket	4-pin narrow DIP, screw machine socket	Socket for U18
50	5	(JP1-JP5)	Shunts	Jumper Shunts	
51	1	Z1	PCI Bracket	PCI bracket with slot for USB Type B connector	Hansen Industries
52	2	Z2	Screw	Screw, pan head, #4-40 x 1/4"	Use to Assemble PCI bracket onto PCB board

9 Schematics

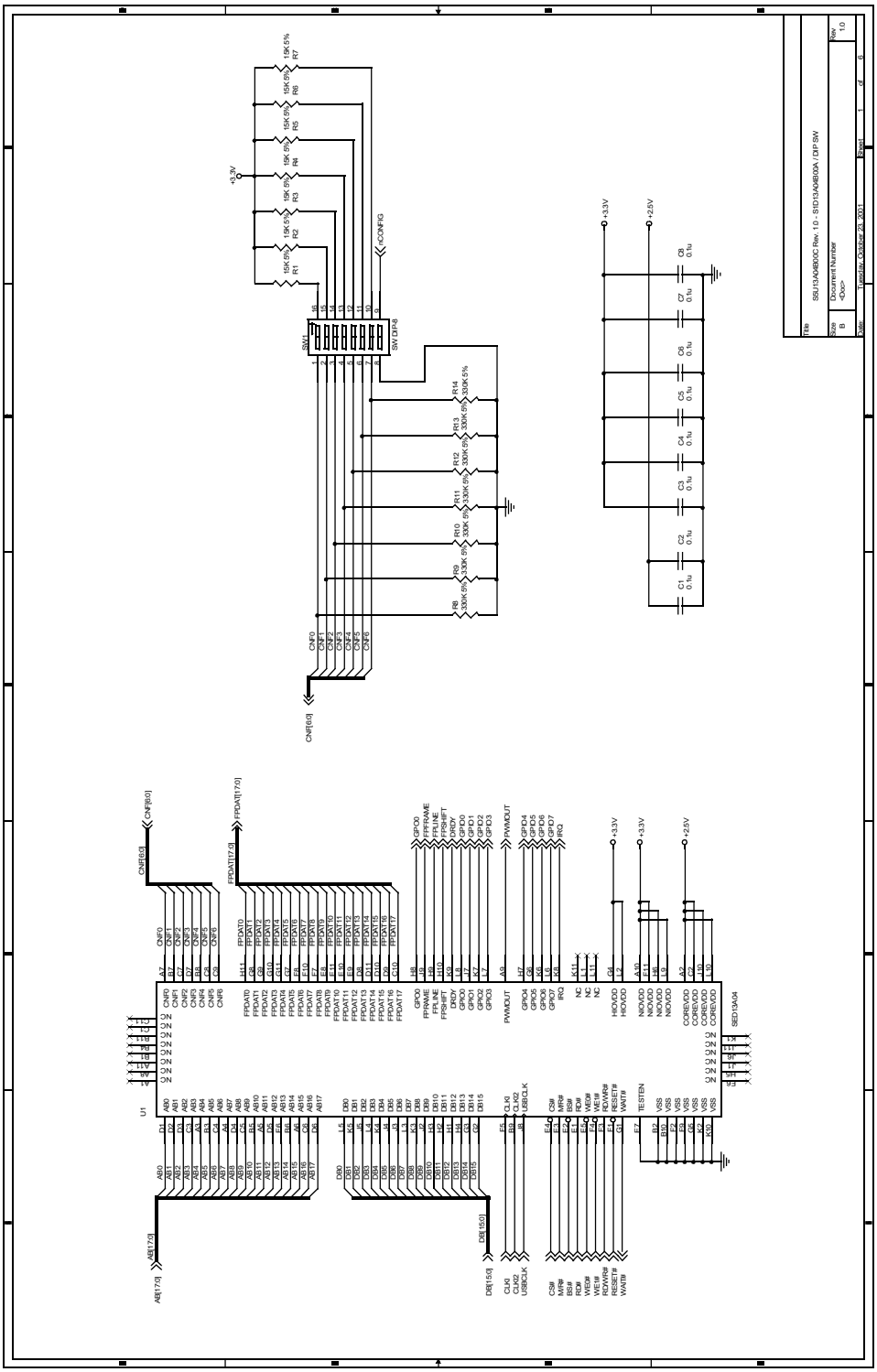

Figure 9-1: S1D13A04B00C Schematics (1 of 6)

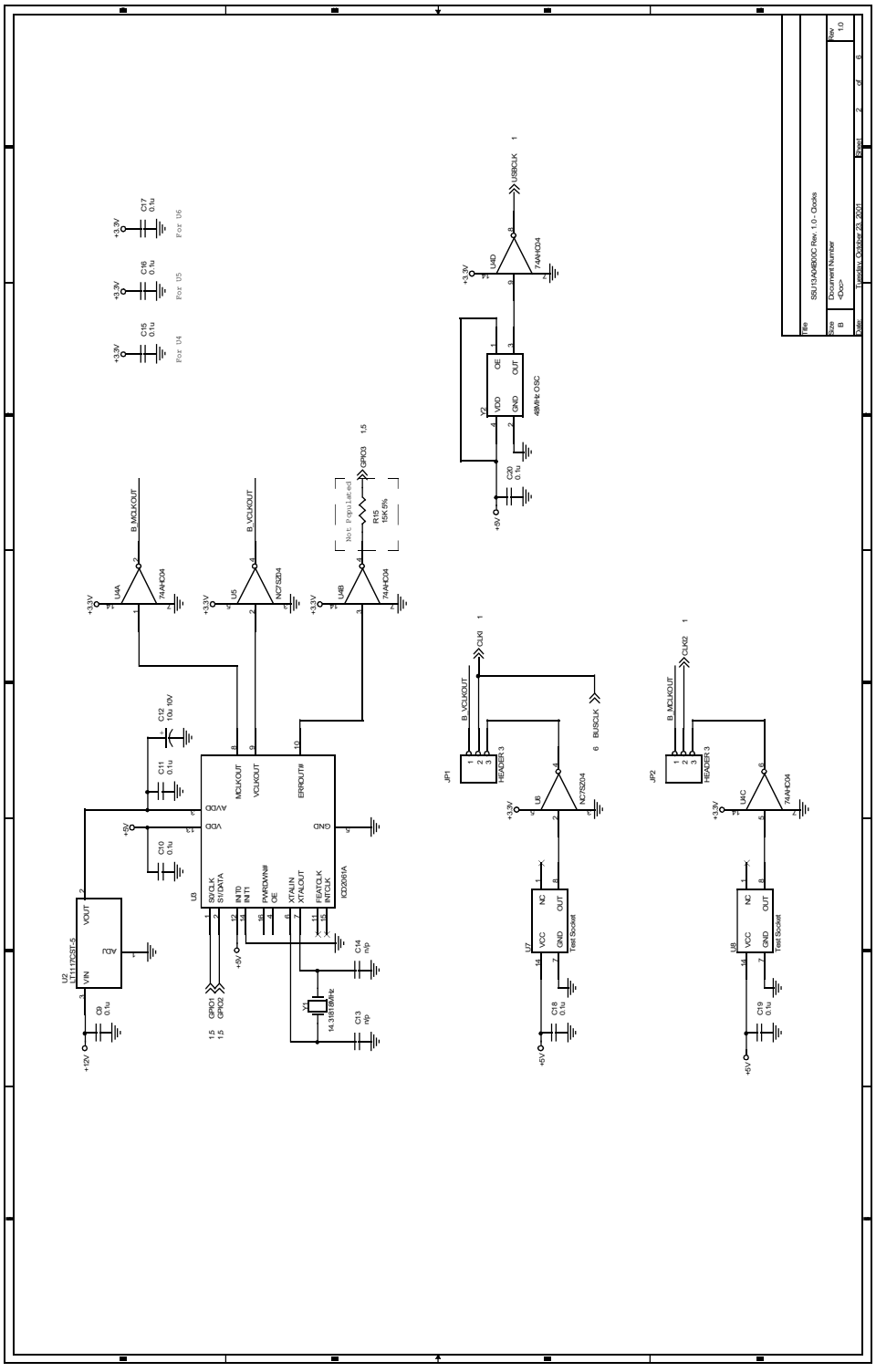

Figure 9-2: S1D13A04B00C Schematics (2 of 6)

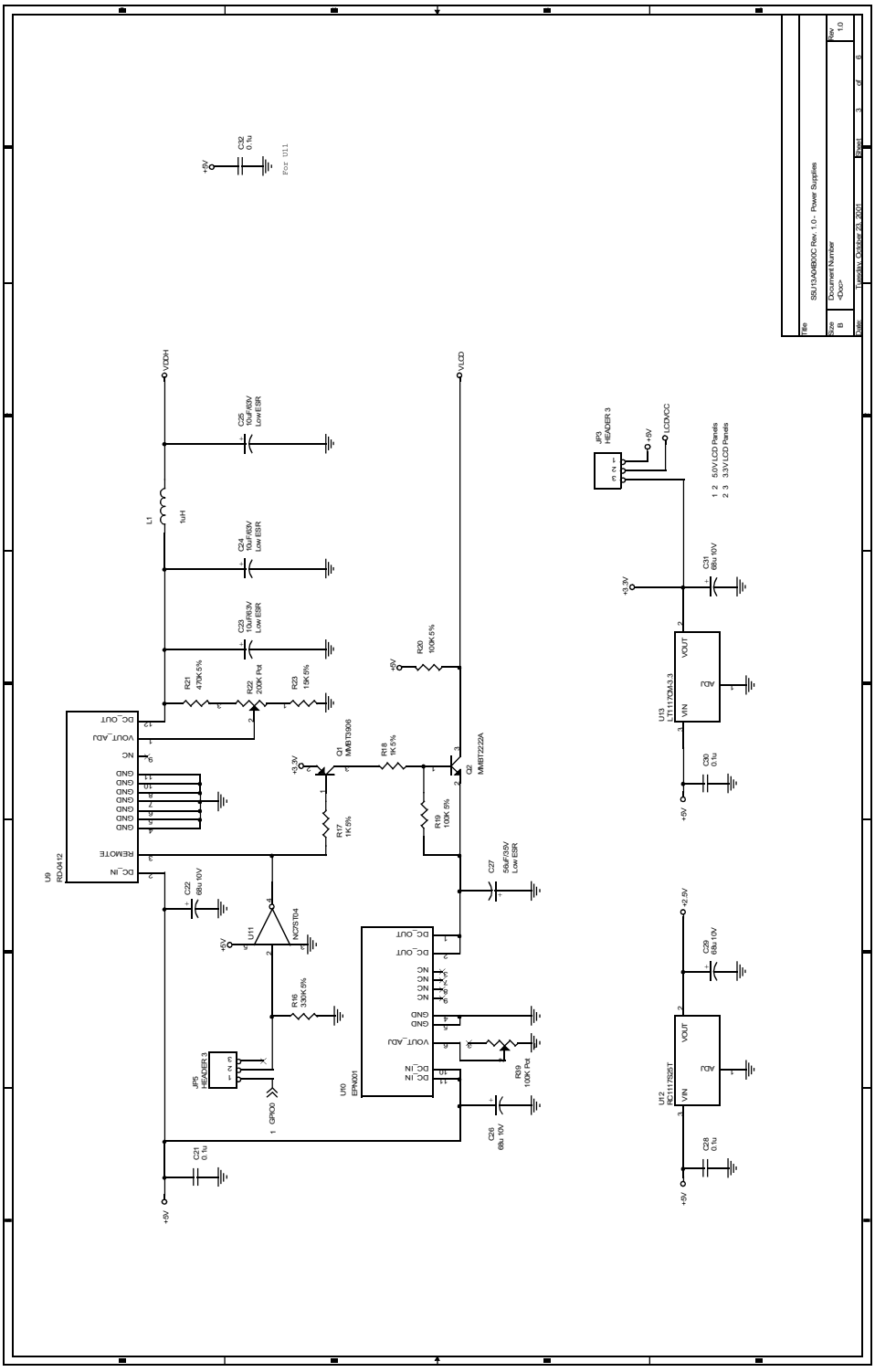

Figure 9-3: S1D13A04B00C Schematics (3 of 6)

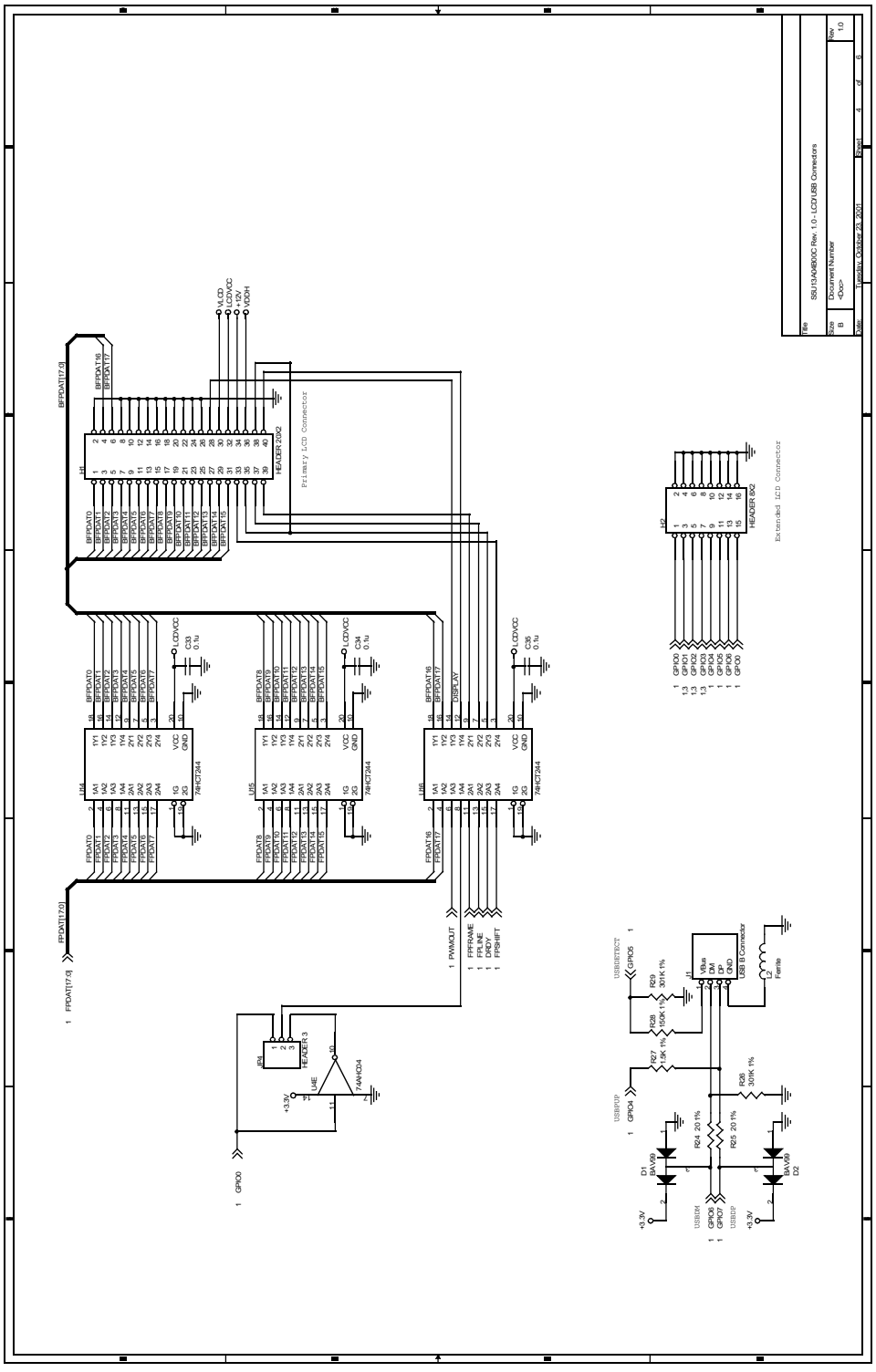

Figure 9-4: S1D13A04B00C Schematics (4 of 6)

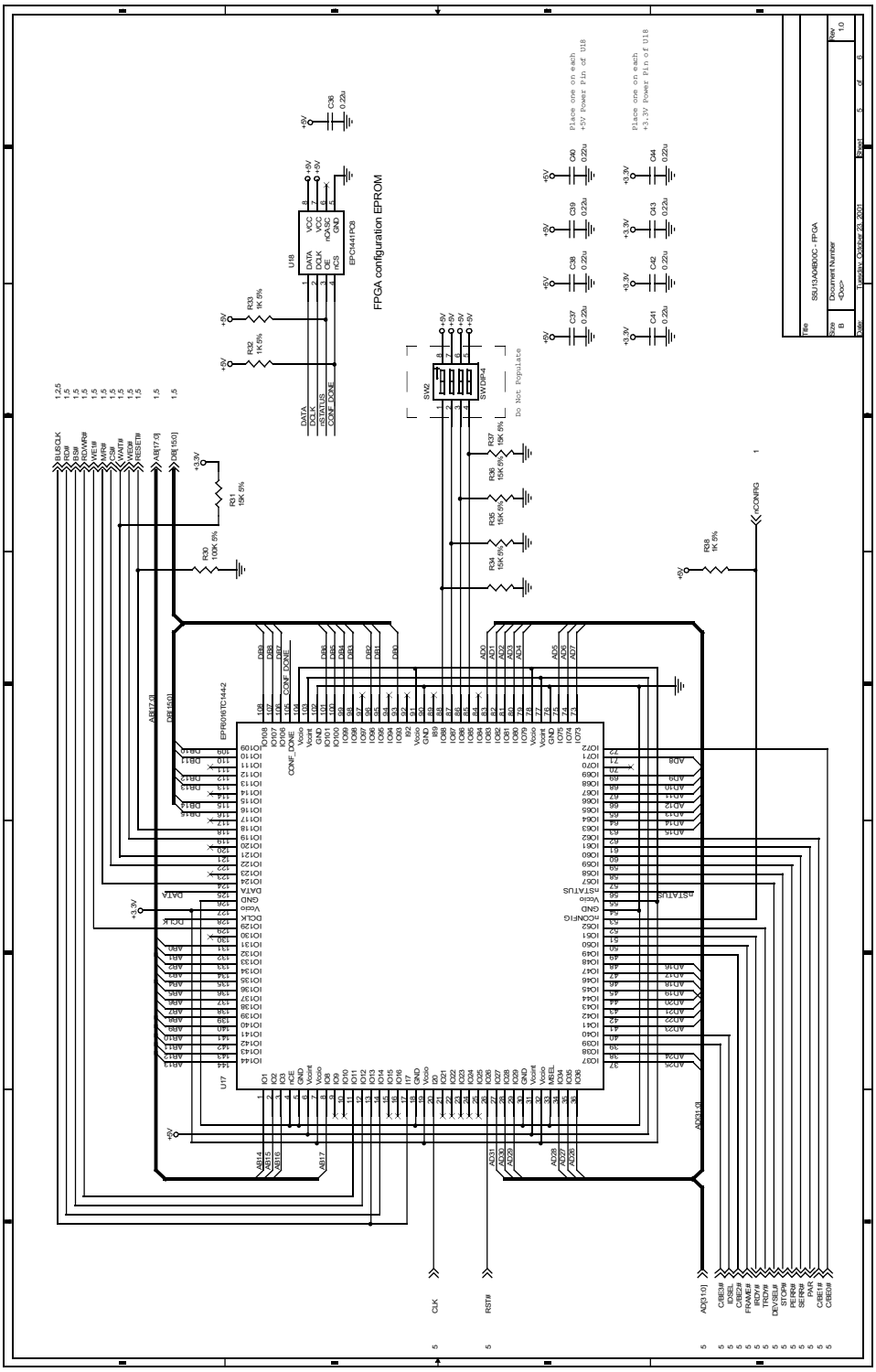

Figure 9-5: S1D13A04B00C Schematics (5 of 6)

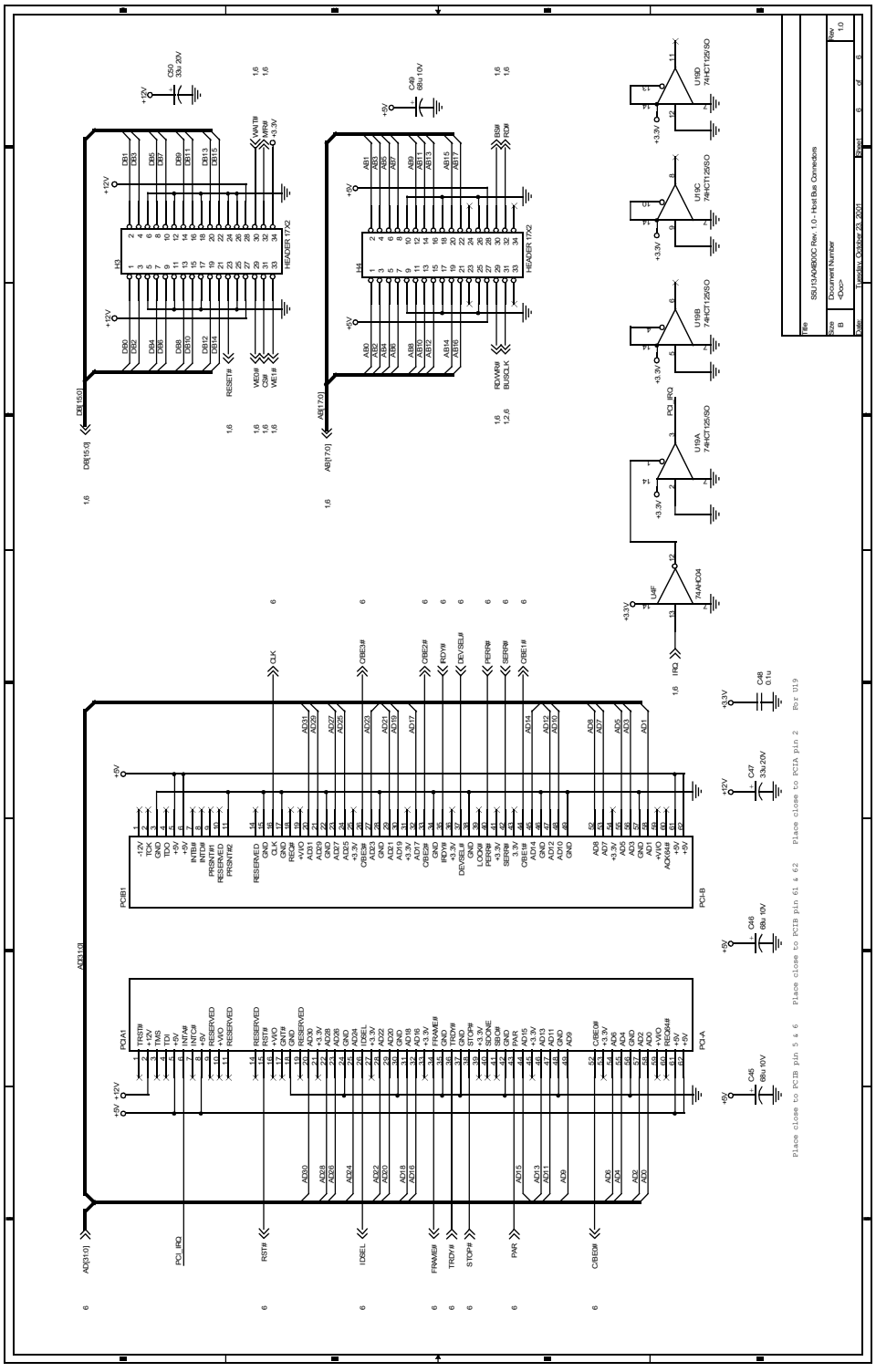

Figure 9-6: S1D13A04B00C Schematics (6 of 6)

10 Board Layout

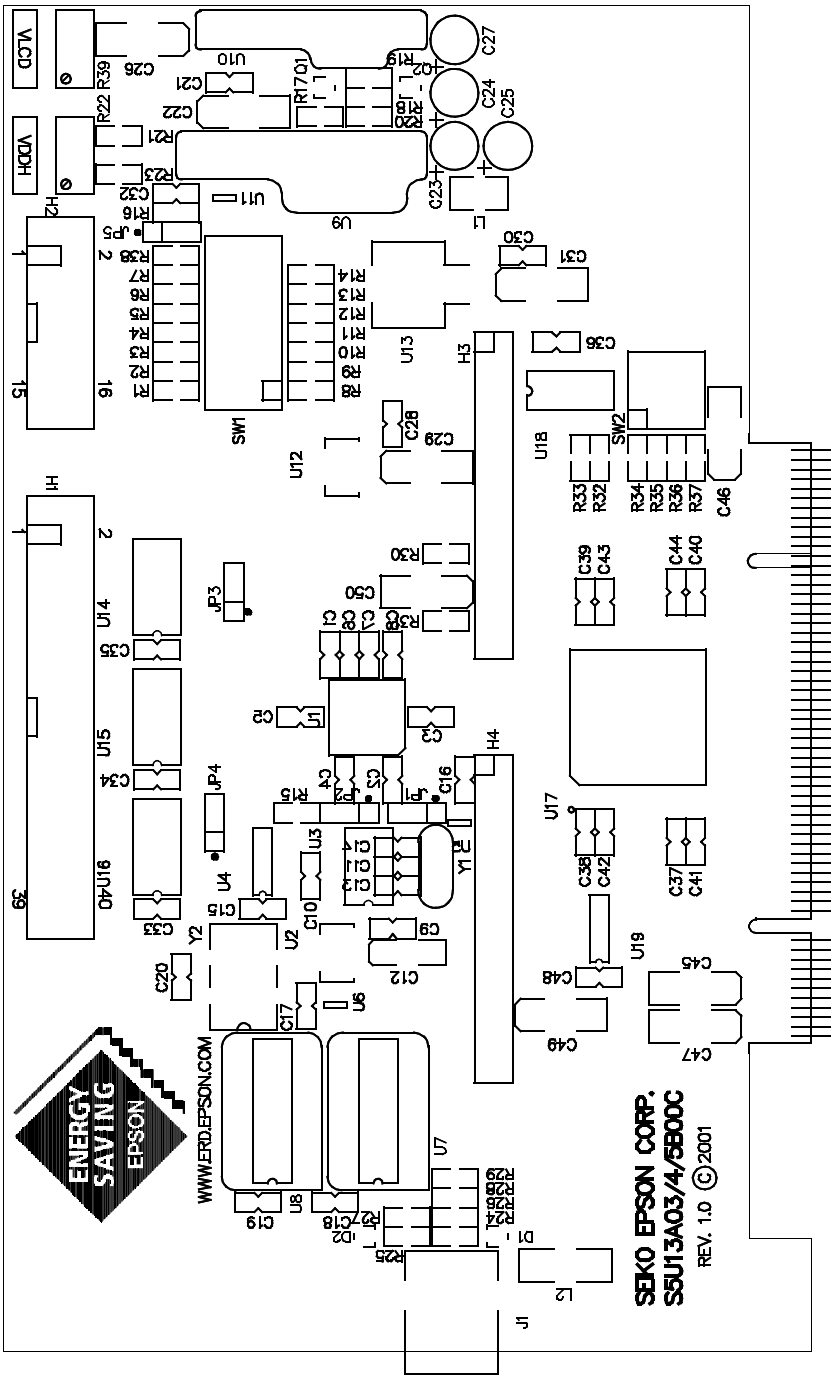

Figure 10-1: S5U13A04B00C Board Layout

11 Change Record

X37A-G-004-01 Revision 3.1 - Issued: March 28, 2018

- updated Sales and Technical Support Section
- updated some formatting

12 Sales and Technical Support

For more information on Epson Display Controllers, visit the Epson Global website.

https://global.epson.com/products_and_drivers/semicon/products/display_controllers/

For Sales and Technical Support, contact the Epson representative for your region.

https://global.epson.com/products_and_drivers/semicon/information/support.html