Errata No. X00Z-P-001-01

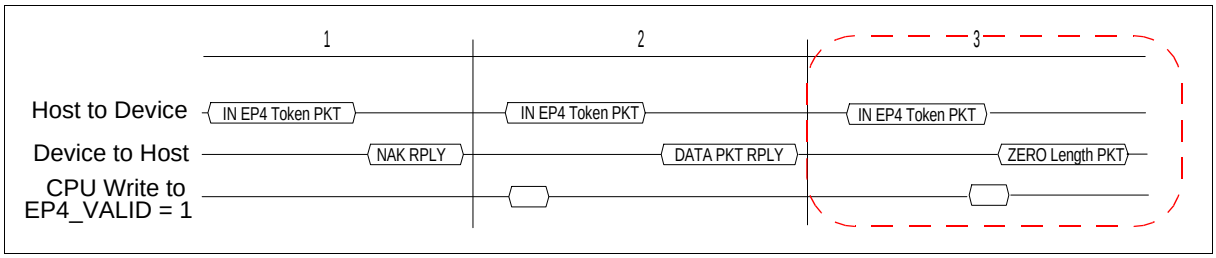
Device: S1D13A03, S1D13A04, S1D13A05.

Description: Setting EP4 FIFO Valid bit while NAKing an IN token.

Bit 5 of REG[402Ch] indicates to the S1D13A0x controller when data in the endpoint 4 FIFO is ready to be transferred to the host computer. Changing the state of this bit at certain times may generate an error.

When the S1D13A0x USB controller receives an endpoint 4 IN request and endpoint 4 is not ready to transmit data (REG[402Ch] bit 5 = 0), the response is a NAK packet. If endpoint 4 is toggled to a ready to transmit state just before a NAK response packet is sent, the controller may erroneously send a zero length packet instead. When this happens, the data toggle state will be incorrectly set for the next endpoint 4 data transmit.

The following timing diagram shows the error occurring in section 3.



This unexpected occurrence of a zero length packet may cause file system handling errors for some operating systems.

Corrective Action:

There are two software solutions for this occurrence.

Disable USB Receiver before setting the EP4 FIFO Valid bit

The first solution involves disabling the USB receiver to avoid responding to an EP4 IN packet. During the time the USB receiver is disabled the EP4 FIFO Valid bit is set.

When the local CPU is ready to send data on endpoint 4 the steps to follow are:

1. Disable the USB differential input receiver (REG[4040h] bit 6 = 0)
2. Wait a minimum of 1µs. If needed, delays may be added
3. Enable the EP4 FIFO Valid bit (REG[402Ch] bit 5 = 1)
4. Clear the EP4 Interrupt status bit (REG[4004h] bit 4 = 1)
5. Enable the USB differential input receiver (REG[4040h] bit 6 = 1)

Note
Steps 1 through 5 are time critical and must be performed in less than 6 µs.

Note
To comply with "EP4 NAK Status not set correctly in USB Status register", steps 3 and 4 must be completed within 5 µs of each other. For further information on "EP4 NAK Status not set correctly in USB Status register", see the S1D13A0x Programming Notes and Examples, document numbers X36A-G-003-xx, X37A-G-003-xx, and X40A-G-003-xx.

EP4 FIFO Valid bit set after NAK and before the next IN token.

The second solution is to wait until immediately after the USB has responded to an IN request with a NAK packet before setting the transmit FIFO valid bit. This solution is recommended only for fast processors.

When the local CPU is ready to send data on endpoint 4, it must first detect that a NAK packet has been sent. This is done by reading the EP4 Interrupt Status bit (REG[4004h] bit 4). If the EP4 FIFO Valid bit was not set, the EP4 Interrupt Status bit is set only if a NAK packet has been sent. When the local CPU detects the NAK it must immediately set the EP4 FIFO Valid bit (before responding to the next IN token).

After filling the EP4 FIFO the steps to follow before setting the EP4 FIFO Valid bit are:

1. Clear the EP4 Interrupt Status bit (REG[4004h] bit 4)
2. Read the EP4 Interrupt Status bit (REG[4004h] bit 4) until it is set
3. Set the EP4 FIFO Valid bit (REG[402Ch] bit 5 = 1)

Note
The setting of the EP4 FIFO Valid bit is time critical. The EP4 FIFO Valid bit must be set within 3 µs after the EP4 Interrupt Status has been set internally by the S1D13A0x.