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S1D13743 Mobile Graphics Engine

Interfacing the Sharp LQ043xxx 480x272 TFT Panel

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SEIKO EPSON CORPORATION

Rev. 1.1

NOTICE

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Chapter 1 Interfacing the Sharp LQ043xxx 480x272 TFT Panel

This document describes the hardware and software environment required to interface the S1D13743 Mobile Graphics Engine and Sharp LQ043xxxx 480x272 TFT Panel.

The designs described in this document are presented only as examples of how such interfaces might be implemented.

1.1 Overview

The S1D13743 directly supports the Sharp LQ043xxx and requires no additional hardware and minimal programming. The S1D13743 register settings and electrical interface is described below.

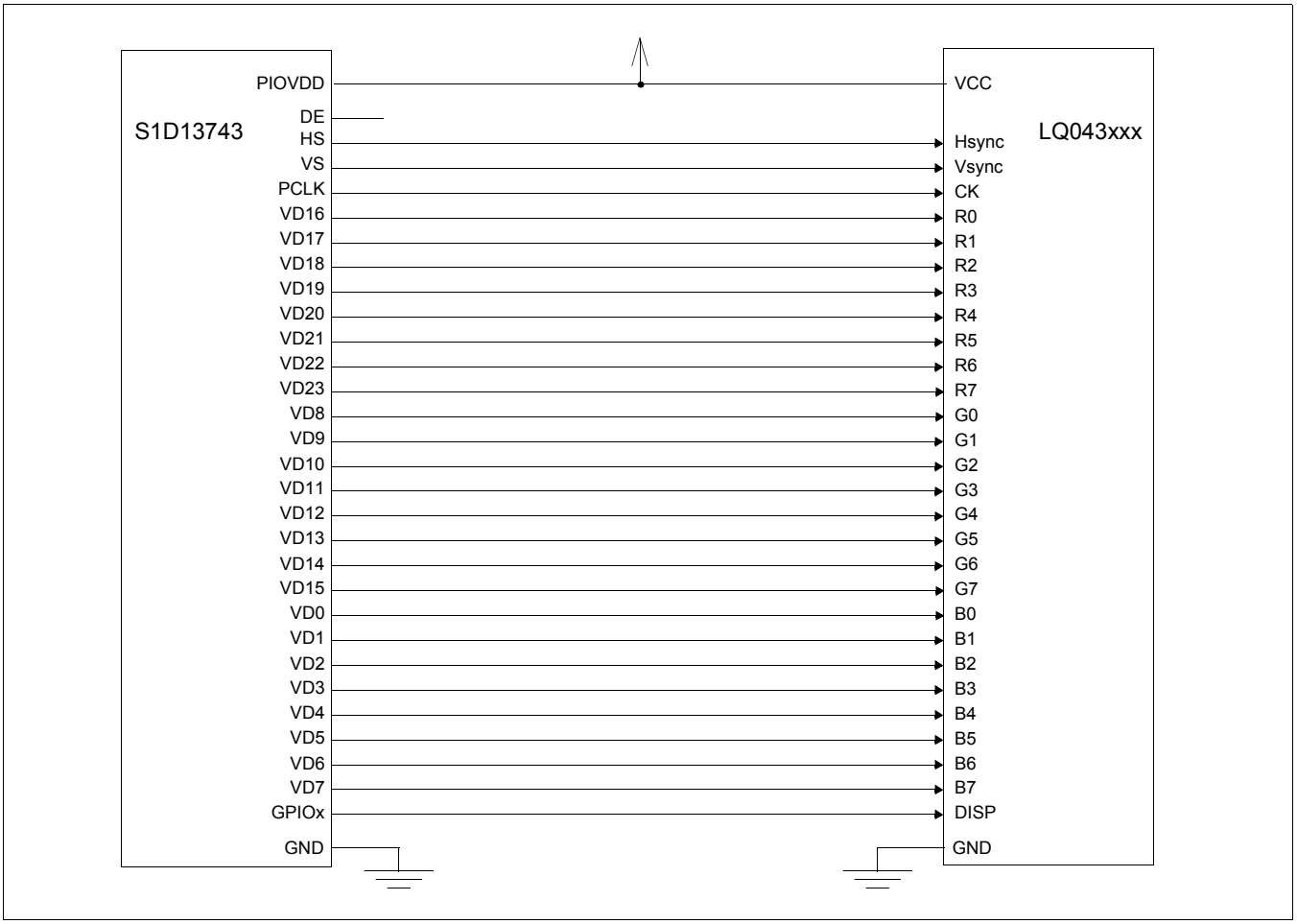

Figure 1-1: S1D13743 to Sharp LQ043xxx Connection Diagram

1.1.1 Electrical Interface

Table 1-1: Pin Mapping

S1D13743 Pin Name	LQ043xxxx Pin Name
HS	Hsync
VS	Vsync
PCLK	CK
DE	-
VD16	R0
VD17	R1
VD18	R2
VD19	R3
VD20	R4
VD21	R5
VD22	R6
VD23	R7
VD8	G0
VD9	G1
VD10	G2
VD11	G3
VD12	G4
VD13	G5
VD14	G6
VD15	G7
VD0	B0
VD1	B1
VD2	B2
VD3	B3
VD4	B4
VD5	B5
VD6	B6
VD7	B7
GPIOx (any of GPIO[7:0] pins)	DISP

The same power must be connected to PIOVDD pins of S1D13743 and to VCC pins of Sharp LQ043xxx panel.

Display ON/OFF signal is provided by one of S1D13743 GPIO pins and it is under application software control. The Vertical Non-Display Period status bit or TE pin, can be used to comply with the Sharp LQ043xxx requirement that DISP signal does not change while Vsync is low.

1.1.2 S1D13743 Register Settings for Sharp LQ043xxx, 480x272 TFT Panel

The registers listed below are only those associated with panel specific timing issues. All other registers are not shown here.

When a window is setup for YUV data, the data must always alternate between odd and even lines, starting with an odd line.

Table 1-2: Example Register Settings for Sharp LQ043xxx 480x272 TFT Panel

Register	Value	Comment
All	default	Come out of reset - all registers set to default values
REG[56h]	02h	enter sleep mode (or use PWRSVE pin)
REG[04h]	03h	set PLL M-Divider. CLKI = 4MHz, PLL input clock = CLKI/4 = 1MHz.
REG[06h]	F8h	
REG[08h]	80h	
REG[0Ah]	28h	
REG[0Ch]	00h	
REG[0Eh]	3Eh	LL = 63, resulting SYSCLK = LL x PLL input clock = 63MHz
REG[12h]	31h	set PCLK divide, PCLK = 9MHz set SYSCLK source = PLL
REG[14h]	01h	no panel data swap, 24-bit panel
REG[16h]	3Ch	HDP = 480 pixels
REG[18h]	2Dh	HNDP = 45 pixels
REG[1Ah]	10h	VDP = 272 lines
REG[1Ch]	01h	
REG[1Eh]	0Eh	VNDP = 14 lines
REG[20h]	29h	HS Pulse Width = 41 pixels
REG[22h]	02h	HS Start Position = 2 pixels
REG[24h]	0Ah	VS Width = 10 lines
REG[26h]	02h	VS Start Position (VFP) = 2 line
REG[28h]	00h	PCLK Polarity: data output on rising edge
REG[2Ah]	03h	set input data mode to RGB 8:8:8 mode 1
REG[56h]	00h	disable sleep mode
REG[04h] bit 7	—	wait for PLL to lock - poll REG[04h] bit 7
REG[38h]	00h	Window X Start Position = 0
REG[3Ah]	00h	
REG[3Ch]	00h	Window Y Start Position = 0
REG[3Eh]	00h	
REG[40h]	DFh	Window X End Position = 479
REG[42h]	01h	
REG[44h]	0Fh	Window Y End Position = 271
REG[46h]	01h	
REG[48h]	Write the image data to the Memory Data Port, REG[48h] and REG[49h]. The image will immediately begin to appear on the LCD.	
REG[49h]		

The above values are intended as examples. This example assumes that CLKI = 4MHz and that the PLL is used to generate SYSCLK. Actual settings can vary and still remain within the LCD panel timing requirements.

Chapter 2 Change Record

X63A-A-001-01 Revision 1.1 - Issued: March 28, 2018

- updated Sales and Technical Support Section
- updated some formatting

X63A-A-001-01 Revision 1.0 - Issued: June 11, 2008

- all changes from the last revision are highlighted in Red
- initial release

Chapter 3 Sales and Technical Support

For more information on Epson Display Controllers, visit the Epson Global website.

https://global.epson.com/products_and_drivers/semicon/products/display_controllers/

For Sales and Technical Support, contact the Epson representative for your region.

https://global.epson.com/products_and_drivers/semicon/information/support.html