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S1D13709 Embedded Memory Graphics LCD Controller

S5U13709P00C100 Evaluation Board User Manual Rev.1.0

Document Number: XA8A-G-001-01.1

SEIKO EPSON CORPORATION

Rev.1.1

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1. This evaluation board/kit or development tool is designed for use for engineering evaluation, demonstration, or development purposes only. Do not use it for other purposes. It is not intended to meet the requirements of design for finished products.
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NOTICE

Table of Contents

1. Introduction

This manual describes the setup and operation of the S5U13709P00C100 Rev.1.0 Evaluation Board. This evaluation board is designed as an evaluation platform for the S1D13709 Embedded Memory Graphics LCD Controller.

The S5U13709P00C100 Evaluation Board can be used with the USB Interface Board (S5U13U00P00C100), thus providing an easy connection to Personal Computer with a USB interface.

This document is updated as appropriate. Please check for the latest revision of this document before beginning any development. The latest revision can be downloaded at vdc.epson.com.

We appreciate your comments on our documentation. Please contact us via email at vdc-documentation@ea.epson.com

2. Features

The S5U13709P00C100 Evaluation Board includes the following features:

- 80-pin TQFP14 S1D13709 Embedded Memory Graphics LCD Controller
- 2.0mm pitch 40pin connector (x2) for USB Interface Board. (S5U13U00P00C100)
- 2.54mm pitch 34pin connector (x2) for connecting other host interface.
- 2.54mm pitch 40pin connector (x2) for panel interface.
- Clock source can be selected from two types.
  Use on-board 24MHz crystal oscillator or set crystal in the 14pin socket.
- SW1, SW2 are switches to change the configuration for the S1D13709.
- On-board voltage regulator (LM1117MPX-3.3) with 3.3V output for HIOVDD/NIOVDD.
- On-board white LED driver (TPS61161A) for the panel backlight power supply.

3. Installation and Configuration

3.1 3.1 Switches

The S5U13709P00C100 Evaluation Board incorporates DIP switches (SW1, SW2), which allow configuration of the board. For switch locations on the evaluation board, see Figure 3-1: “Configuration DIP Switches Location”.

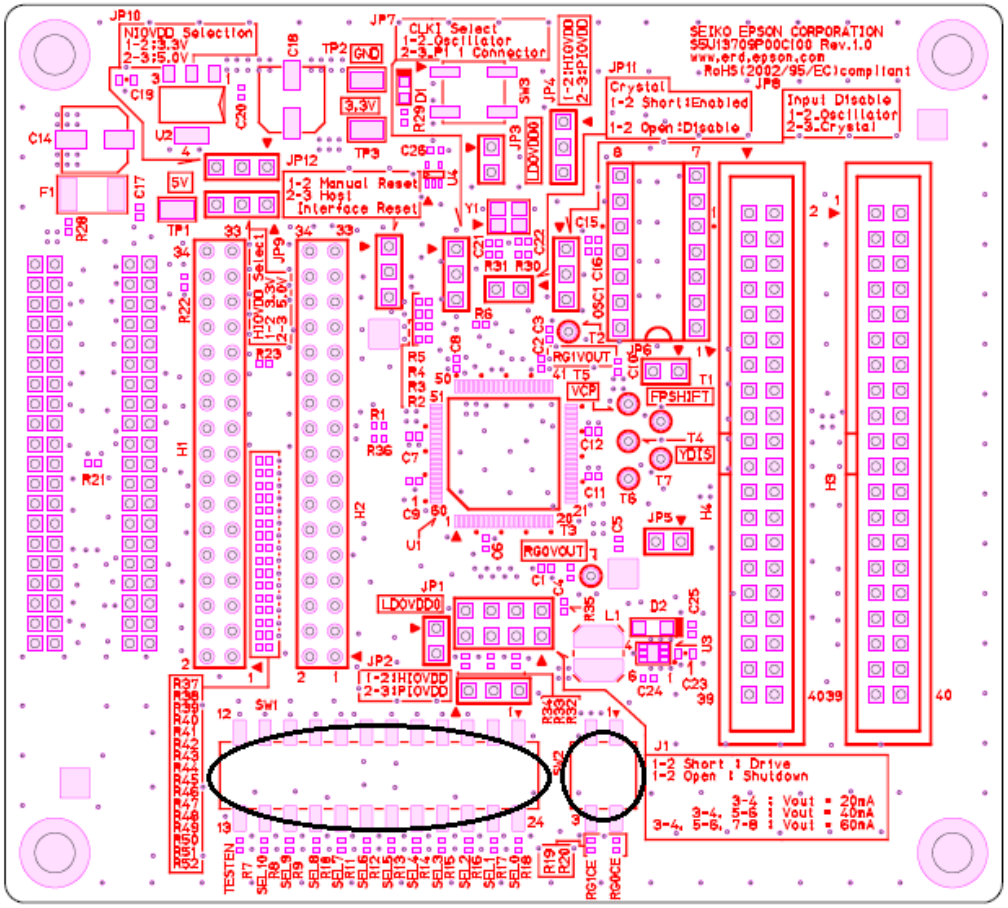

Figure 3.1 Configuration DIP Switches (SW1), (SW2) Location

The 12-position DIP switch (SW1) is used to configure the S1D13709 for different host bus interfaces and for TFT panel or STN panel for TFT-LCD Automatic Setting Mode.

Table 3.1 Summary of Configuration Options

S5U13709P00C100 SW1-[12:1] Configuration	S1D13709 Pin	Configuration State	
		1 (ON)	0 (OFF)
SW1-[12]	TESTEN	Not use	Normal use "GND"
SW1-[11]	CNF10	CLKI (XCG1) frequency is 24MHz This setting is available only when the TFT-LCD Automatic Setting Mode is enabled (CNF[7:5] = 001,010, 011 or 100)	CLKI (XCG1) frequency is 20MHz
SW1-[10]	CNF9	TFT Interface Output Drive is 6mA@3.3V (8mA@5V) This setting is available only when the TFT-LCD Automatic Setting Mode is enabled (CNF[7:5] = 001,010, 011 or 100)	TFT Interface Output Drive is 2mA@3.3V (3mA@5V)
SW1-[9]	CNF8	All output video signals change at rising edge of FPSHIFT This setting is available only when the TFT-LCD Automatic Setting Mode is enabled (CNF[7:5] = 001,010, 011 or 100)	All output video signals change at the falling edge of FPSHIFT
SW1-[8:6]	CNF[7:5]	**CNF7 CNF6 CNF5 TFT-LCD Automatic Setting Mode** 0 0 0 Disable (Manual setting) 0 0 1 S1D13700 S/W: QVGA → TFT: QVGA 0 1 0 S1D13700 S/W: QVGA → TFT: WQVGA 0 1 1 S1D13700 S/W: QVGA → TFT: VGA 1 0 0 S1D13700 S/W: QVGA → TFT: WVGA 1 0 1 Reserved 1 1 0 Reserved 1 1 1 Reserved When the STN interface is used (REG[34h] bit0 = 0), CNF[7:5] should be 000.	TFT interface is used. (TFT-LCD Automatic Setting Mode Disable) Or STN interface is used. (REG[34h] bit0 = 0)
SW1-[5]	CNF4	Indirect Addressing Mode: 1-bit address bus, 8-bit data bus 9pin are used	Direct Addressing Mode: 16bit address bus, 8-bit data bus 24pin are used.
SW1-[4:3]	CNF[3:2]	Select the host bus interface as follows: **CNF3 CNF2 Host Bus** 0 0 Generic Bus 0 1 Reserved 1 0 M6800 Family Bus Interface 1 1 MC68K Family Bus Interface	Select the host bus interface as "Generic Bus".
SW1-[2:1]	CNF[1:0]	Select the XSCL cycle time (XSCL:CLOCK Input) as follows: For 1bpp mode (REG[20h] bit 1-0 = 00) **CNF1 CNF0 XSCL Cycle Time** 0 0 4:1 0 1 8:1 1 0 16:1 1 1 Reserved For 2bpp mode (REG[20h] bit 1-0 = 01) **CNF1 CNF0 XSCL Cycle Time** 0 0 8:1 0 1 16:1 1 0 32:1 1 1 Reserved For 4bpp mode (REG[20h] bit 1-0 = 10) **CNF1 CNF0 XSCL Cycle Time** 0 0 16:1 0 1 32:1 1 0 64:1 1 1 Reserved When the TFT Interface is used (REG[34h] bit0 = 1), CNF[1:0] should be 00.	For 1bpp mode (REG[20h] bit 1-0 = 00) **CNF1 CNF0 XSCL Cycle Time** 0 0 4:1 For 2bpp mode (REG[20h] bit 1-0 = 01) **CNF1 CNF0 XSCL Cycle Time** 0 0 8:1 For 4bpp mode (REG[20h] bit 1-0 = 10) **CNF1 CNF0 XSCL Cycle Time** 0 0 16:1

= default setting

The 2-position DIP switch (SW2) is used to configure for production test only. For normal use this switch state should be set to "ON".

Table 3.2 Summary of Configuration Options

S5U13709P00C100 SW2-[2:1] Configuration	S1D13709 Pin	Configuration State	
		1 (ON)	0 (OFF)
SW2-[1]	CORECE	Normal use	Not use
SW2-[2]	PLLCE	Normal use	Not use

= default setting

3.2 3.2 Configuration Jumpers

The S5U13709P00C100 Evaluation Board includes the following 2-pin, 3-pin and 8-pin jumper blocks which are used to control function and for power consumption measurement. For jumper locations on the evaluation board, see Figure 3-2: “Configuration Jumper Location”

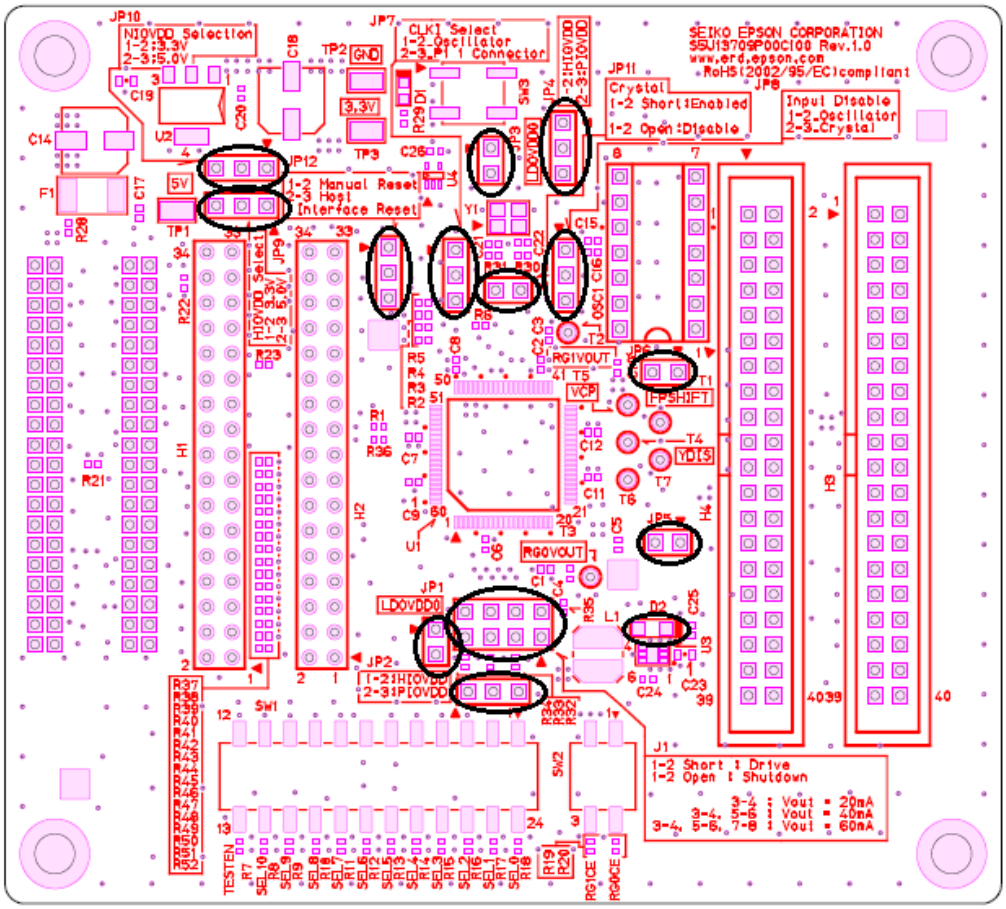

Figure 3.2 Configuration Jumper Location

Table 3.3 2-Pin Jumper Settings

Jumper	Position1-2	No Jumper
JP1	COREVDD power supply	COREVDD no power Connect a current meter for power measurement
JP3	PLLVDD power supply	PLLVDD no power Connect a current meter for power measurement
JP5	HIOVDD power supply	HIPVDD no power Connect a current meter for power measurement
JP6	NIOVDD power supply	NIOVDD no power Connect a current meter for power measurement
JP11	Use OSC clock source	Disable OSC clock source

= default setting

Table 3.4 3-Pin Jumper Settings

Jumper	Position1-2	Position2-3
JP2	Select power supply HIOVDD	Select power supply NIOVDD
JP4	Select power supply HIOVDD	Select power supply NIOVDD
JP7	Select clock source OSC1	Select clock source P1-4pin (S5U13U00P00C100)
JP8	Select clock input OSCI	Select clock input MCLK
JP9	Select HIOVDD Voltage 3.3V	Select HIOVDD Voltage 5.0V
JP10	Select NIOVDD Voltage 3.3V	Select NIOVDD Voltage 5.0V
JP12	Reset# pulse supply from SW3	Reset# pulse supply from P1-21pin, H1-30pin

= default setting

Table 3.5 8-Pin Jumper Settings

Jumper	Position		Function
J1	Position1-2	No Jumper	TPS61161A Enable
	Position3-4	No Jumper	Vout = 20mA
	Position5-6	No Jumper	Vout = 40mA (and Position3-4)
	Position7-8	No Jumper	Vout = 60mA (And position3-4/5-6)

= default setting

3.3 Power Requirement

3.3.1 HIOVDD, NIOVDD, COREVDD, PLLVDD

The S5U13709P00C100 Evaluation Board is designed to generate HIOVDD, NIOVDD, COREVDD and PLLVDD from 5V via the S5U13U00P00C100 USB Interface Board. 5V must be supplied from the S5U13U00P00C100. JP1 on the S5U13U00P00C100 USB Interface Board should be set to position 2-3. 3.3V power supply is generated by one voltage regulator (U3) and fixed output. HIOVDD and NIOVDD can be selected 3.3V or 5V using jumper JP9 and JP10. COREVDD is possible to select HIOVDD, NIOVDD or LDOVDD0. PLLVDD are possible to select HIOVDD, NIOVDD or LDOVDD1. If use the LDOVDD0 and LDOVDD1, it is external input from JP1 and JP3. Refer to Table 3-2a and 3-2b on page 9.

3.3.2 Backlight Power Supply for LCD Panel

The S5U13709P00C100 Evaluation Board has an incorporated White LDE Driver Controller (TPS61161A) for the panel backlight. White LED Driver Controller drives the panel at a constant current. The S5U13709P00C100 Evaluation Board is possible to change the output current (20mA, 40mA, 60mA / Max 38V). Please set J1 with the specifications of the panel. Refer to Table 3-2c on page 9.

4. Connectors

The S5U13709P00C100 Evaluation Board has host interface connectors and panel interface connectors (P1, P2, H1, H2, H3 and H4). For connector locations on the evaluation board, see Figure 4-1: “Evaluation board Connector Location”

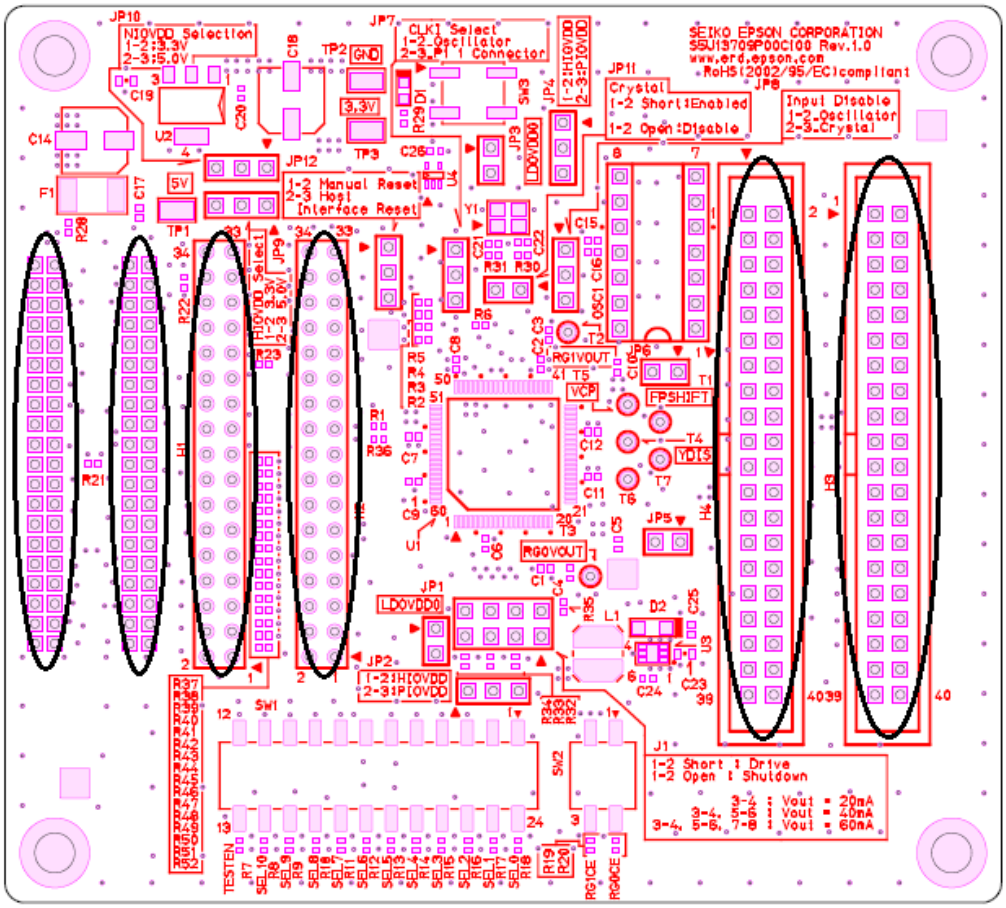

Figure 4.1 Evaluation board Connector Location

4.1 P1, P2 Host Interface Connector

The S5U13709P00C100 Evaluation Board is designed to connect to a S5U13U00P00C100 USB Interface Board. The USB Interface Board provides a simple connection to any computer via USB 2.0 connection. The S5U13709P00C100 directly connects to the USB Interface Board through connectors P1 and P2.

When the S5U13709P00C100 is connected to the S5U13U00P00C100, there is a LED on the S5U13U00P00C100 which provide a quick visual status of the power supply (5V). And S5U13709P00C100 has a LED too. This LED indicates that the 3.3V power is supplied. P1 and P2 connectors are 2mm pitch, dual row, and 40-pin female headers (20x2).

Note:
A windows driver must be installed on the PC when the S5U13709P00C100 is used with the S5U13U00P00C100 USB Interface Board. The S1D13xxxUSB driver is available at vdc.epson.com.

4.2 H1, H2 Host Interface Connector

When the S5U13709P00C100 Evaluation Board connects with the S5U13U00P00C100 USB Interface Board, H1 and H2 connectors can be used as monitor terminals.

The S5U13709P00C100 is designed to connect to a S5U13U00P00C100. But H1 and H2 connectors allow a variety of development platforms to be used with the S5U13709P00C100. When not used with the S5U13U00P00C100, please supply the 5V power to TP1 terminal.

4.3 H3, H4 Panel Interface Connector

The LCD interface uses the FPFRAME, FPSHIFT, FPDRDY, FPLINE and FPDAT [3:0] pins. All signals on these pins are available on connectors H3 and H4. Connectors H3 and H4 are 2.54mm pitch, dual row, and 40-pin female headers (20x2).

5. Technical Descriptions

5.1 Current Measurement

Current measurement can be performed individually for each power supplies: HIOVDD, NIOVDD, COREVDD and PLLVDD. For details on which jumper block is used for each power supply, refer to Table 3-2a: “2-Pin Jumper Settings,” on page 9.

To measure current for a particular power supply, remove the corresponding jumper shunt and place an ammeter on the jumper terminals to measure the current draw. Use the lowest possible range for the measurement to minimize loading from the ammeter.

Note:
Attaching an ammeter while doing other tests can cause a voltage drop across the ammeter and may produce invalid test results.

5.2 Clock source select

The S5U13709P00C100 Evaluation Board has an on-board 24MHz oscillator (Y1) which drives the input with the internal oscillator circuit (XCG1). When not using the internal oscillator circuit, this board allows the usage of a variety of crystal oscillators with osc1 connectors (CLKI). The XCG1 source selection is determined with jumper on 1-2pin of JP8 and 1-2pin of JP11. The CLKI source selection is determined with jumper on 1-2pin of JP7 and 2-3pin of JP8. For details on configuring the clock source, refer to Table 3-2a and Table 3-2b on page 9.

5.3 Hardware Reset

The S5U13709C00100 Evaluation Board has an on-board reset IC which drives the RESET# input pin on the panel. This occurs when push button SW3 is pressed.

6. Parts List

Table 6.1 S5U13531B02C100 Parts List

Item	Qty	Reference	Part	Description	Manufacture Part No. / Comments
1	5	C1, C2, C3, C4, C25	Capacitance	1uF	
2	2	C5, C10	Capacitance	4.7uF	
3	11	C6, C7, C8, C9, C11, C12, C15, C17, C20, C24, C26	Capacitance	0.1uF	
4	1	C14	Capacitance	100uF / 16V	
5	1	C16	Capacitance	0.01uF	
6	1	C18	Capacitance	100uF / 10V	
7	1	C19	Capacitance	10uF /16V	
8	2	C21, C22	Capacitance	10pF	
9	1	C23	Capacitance	0.22uF	
10	1	D1	LED	BG1111C	STANLEY
11	1	D2	Diode	CRS04	TOSHIBA
12	1	F1	Inductance	MINISMDC110F-2	TE
13	2	H1, H2	Connector	A1-34PA-2.54DSA	HIROSE
14	2	H3, H4	Connector	HIF3FC-40PA-2.54DSA	HIROSE
15	5	JP1, JP3, JP5, JP6, JP11	Header Pin	A2-2PA-2.54DSA	HIROSE
16	7	JP2, JP4, JP7, JP8, JP9, JP10, JP12	Header Pin	A2-3PA-2.54DSA-	HIROSE
17	1	J1	Header Pin	A1-8PA-2.54DSA	HIROSE
18	1	L1	Inductance	VLCF5020T-220MR75-1	TDK
19	1	OSC1	SOCKET	4-1571552-2	TE
20	2	P1, P2	Connector	PRPN202PAEN	SULLINS
21	1	R1	Resister	1KΩ	
22	7	R2, R3, R4, R5, R6 R28, R31	Resister	0Ω	
23	32	R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52	Resister	10KΩ	
24	1	R21	Resister	22KΩ	
25	1	R22	Resister	10KΩ	
26	1	R23	Resister	0Ω	
27	1	R29	Resister	240	
28	1	R30	Resister	10MΩ	
29	3	R32, R33, R34	Resister	10Ω	
30	16	SH1, SH2, SH3, SH4, SH5, SH6, SH7, SH8, SH9, SH10, SH11, SH12, SH13, SH14, SH15, SH16	Short socket	XJ8A-0211	OMRON
31	1	SW1	DIP switch	219-12MST	CTS
32	1	SW2	DIP switch	219-2MST	CTS
33	1	SW3	Switch	KSC241J	C&K

Table 6.2 S5U13531B02C100 Parts List (continued)

Item	Qty	Reference	Part	Description	Manufacture Part No. / Comments
34	3	TP1, TP2, TP3	Monitor pin	HK-2-S	MAC8
35	7	T1, T2, T3, T4, T5, T6, T7	Monitor TH	TH	
36	1	U1	IC	S1D13709	EPSON
37	1	U2	Regulator	LM1117MPX-3.3	NS
38	1	U3	LDE Driver	TPS61161A	TI
39	3	U4	Power Supply	TPS3801K33DCKR	TI
40	1	Y1	Crystal	FA-238 (24MHz)	EPSON TOYOCOM

7. Schematic Diagrams

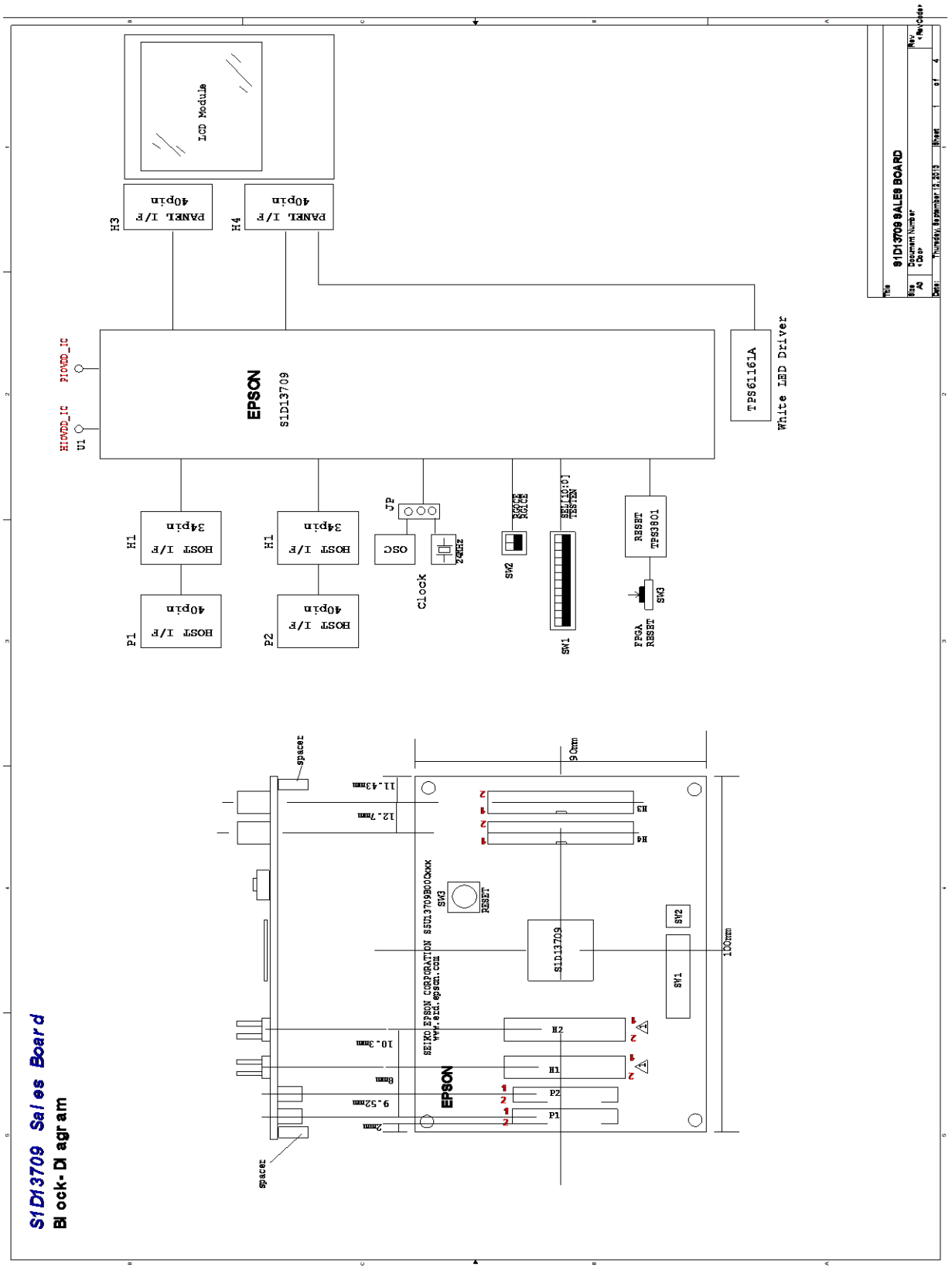

Figure 7.1 S5U13709P00C100 Schematics (1 of 4)

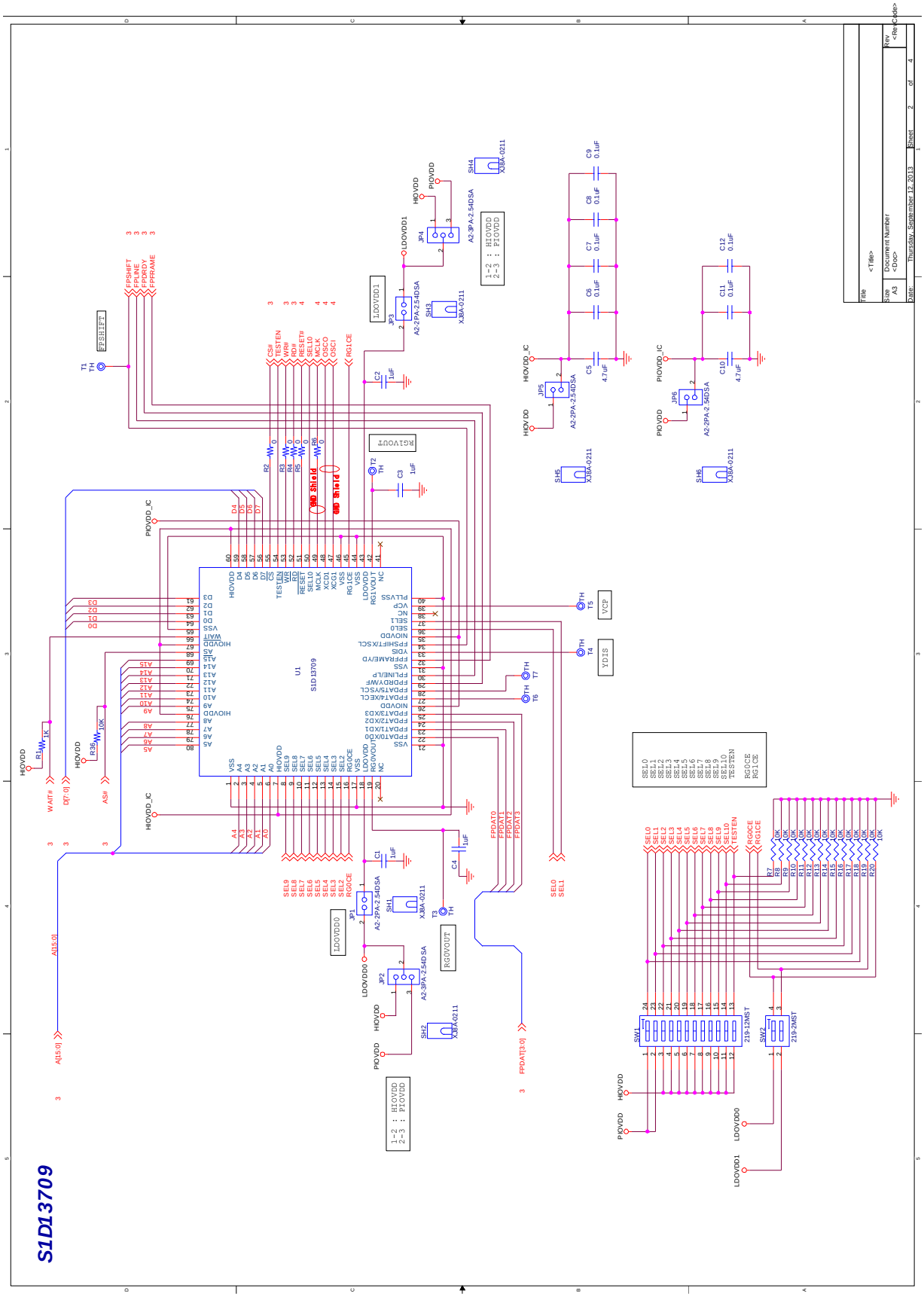

Figure 7.2 S5U13709P00C100 Schematics (2of 4)

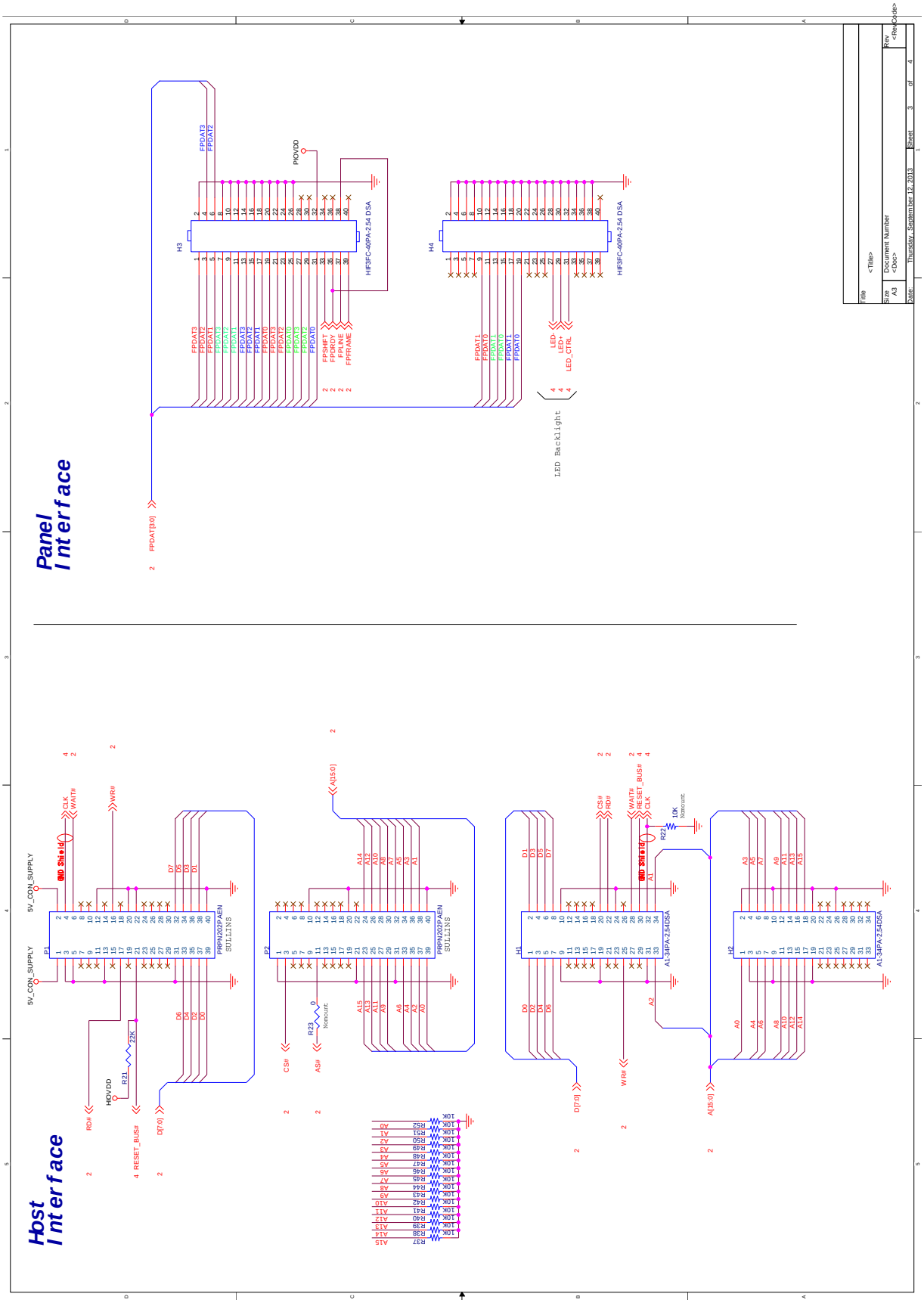

Figure 7.3 S5U13709P00C100 Schematics (3of 4)

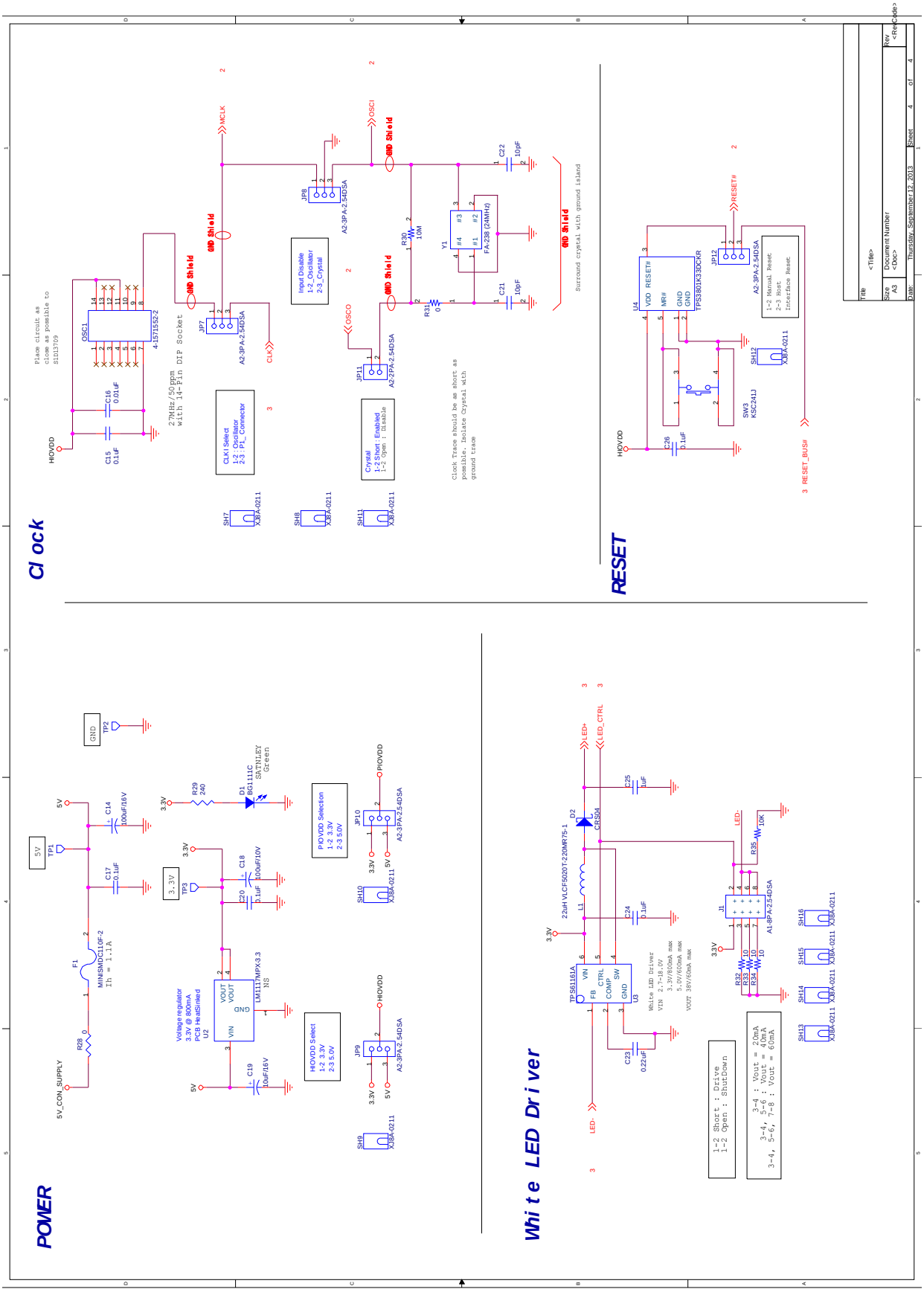

Figure 7.4 S5U13709P00C100 Schematics (4of 4)

8. S5U13709P00C100 Board Layout

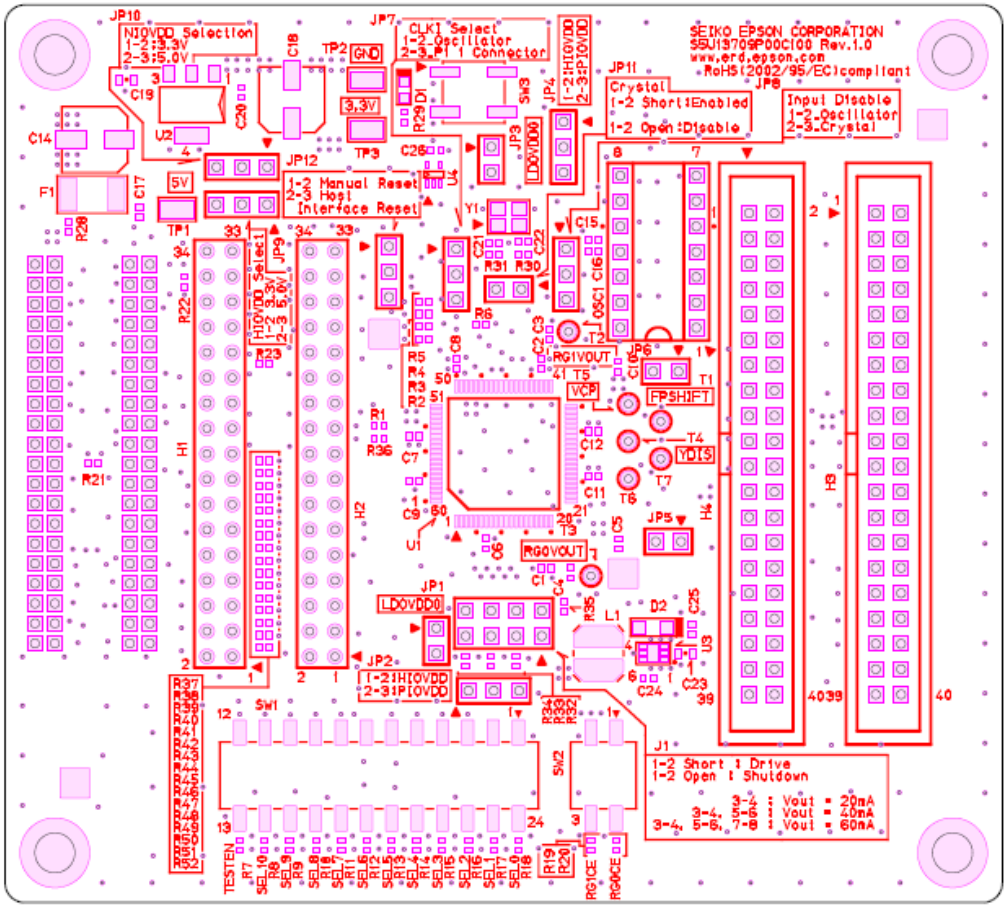

Figure 8.1 S5U13709P00C100 Board Layout – Parts Side

9. Installation Guide for the S5U13U00P00C100

9.1 Installation and connecting

The following instructions are for connecting the S5U13709P00C100 Evaluation Board to the S5U13U00P00C100 USB Interface Board. The S5U13U00P00C100 is not included with the S5U13709P00C100 kit.

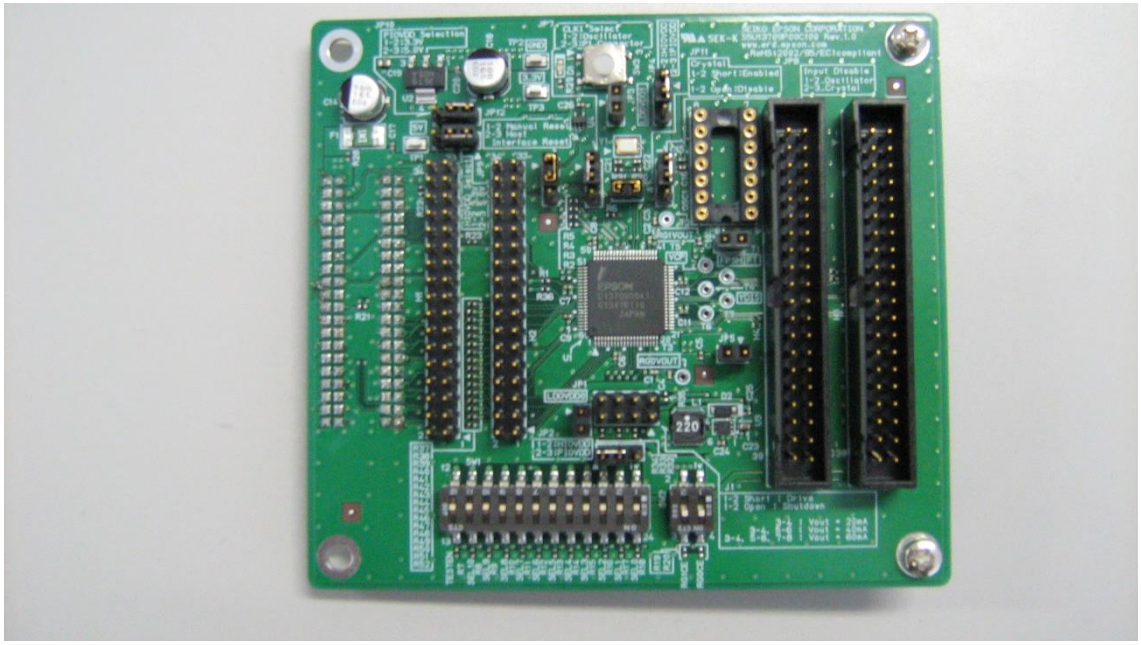

Figure 9.1 S5U13709P00C100 Evaluation Board

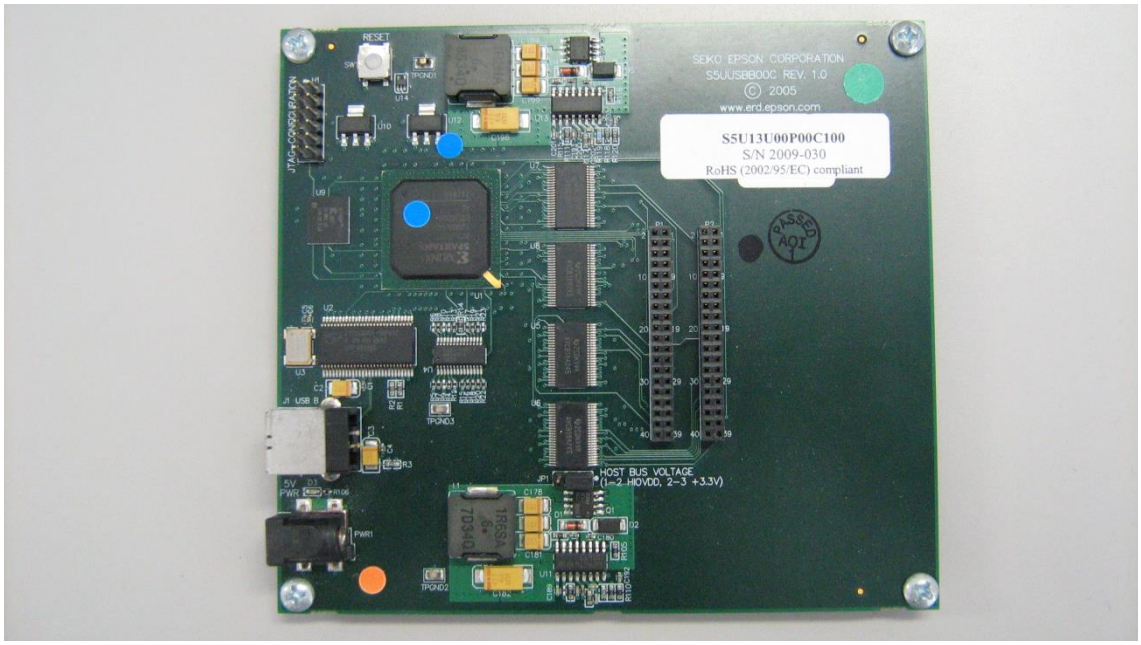

Figure 9.2 S5U13U00P00C100 USB Interface Board

1. Download the S5U13U00P00C100 driver “S1d13xxx USB Evaluation Board Driver For Windows (2012-01-20)” from vdc.epson.com.
2. Install the driver onto your PC.
3. Connect P1 on the S5U13709P00C100 with P1 on the S5U13U00P00C100, and P2 on the S5U13709P00C100 with P2 on the S5U13U00P00C100. And connect to your panel with H3 and H4.

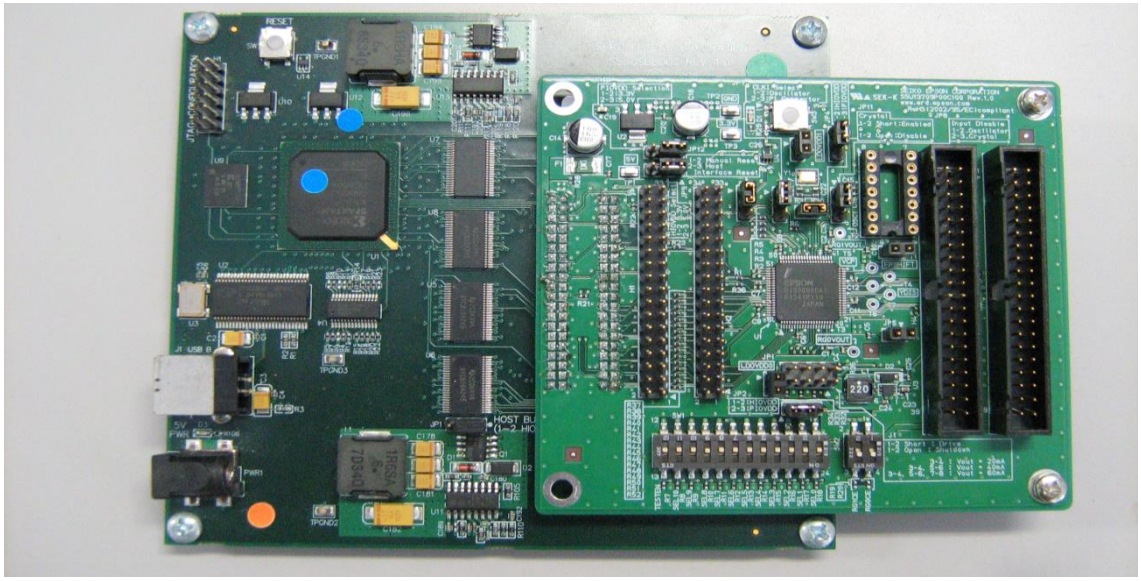

Figure 9.3 Connecting S5U13U00P00C100 Board and S5U13U00P00C100 Board

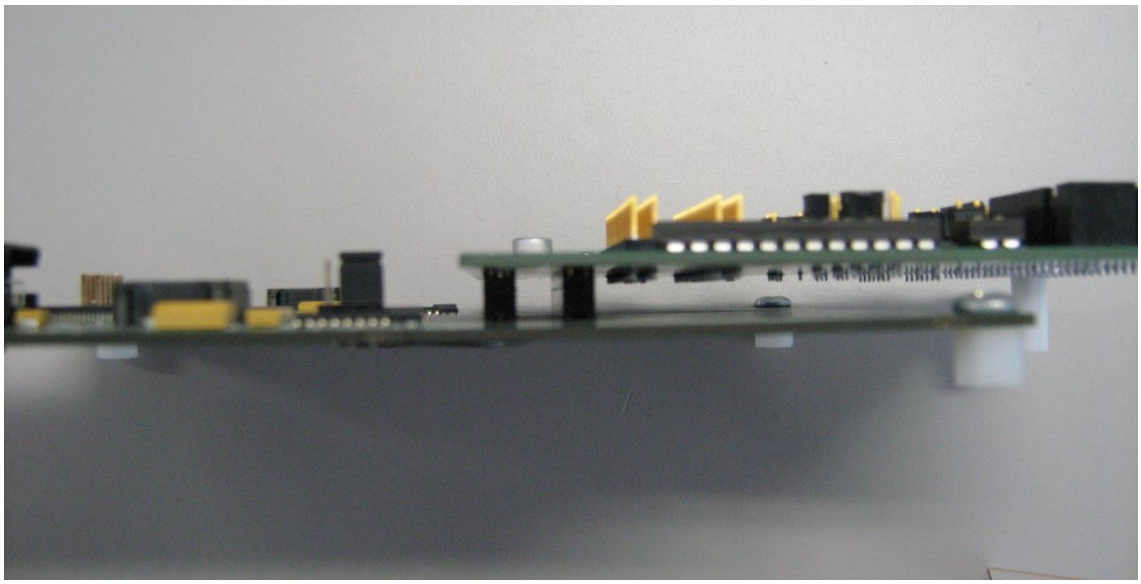

Figure 9.4 Connecting S5U13U00P00C100 Board and S5U13U00P00C100 Board

4. Connect the 5V power supply adapter to the S5U13U00P00C100 and connect to the PC via USB.

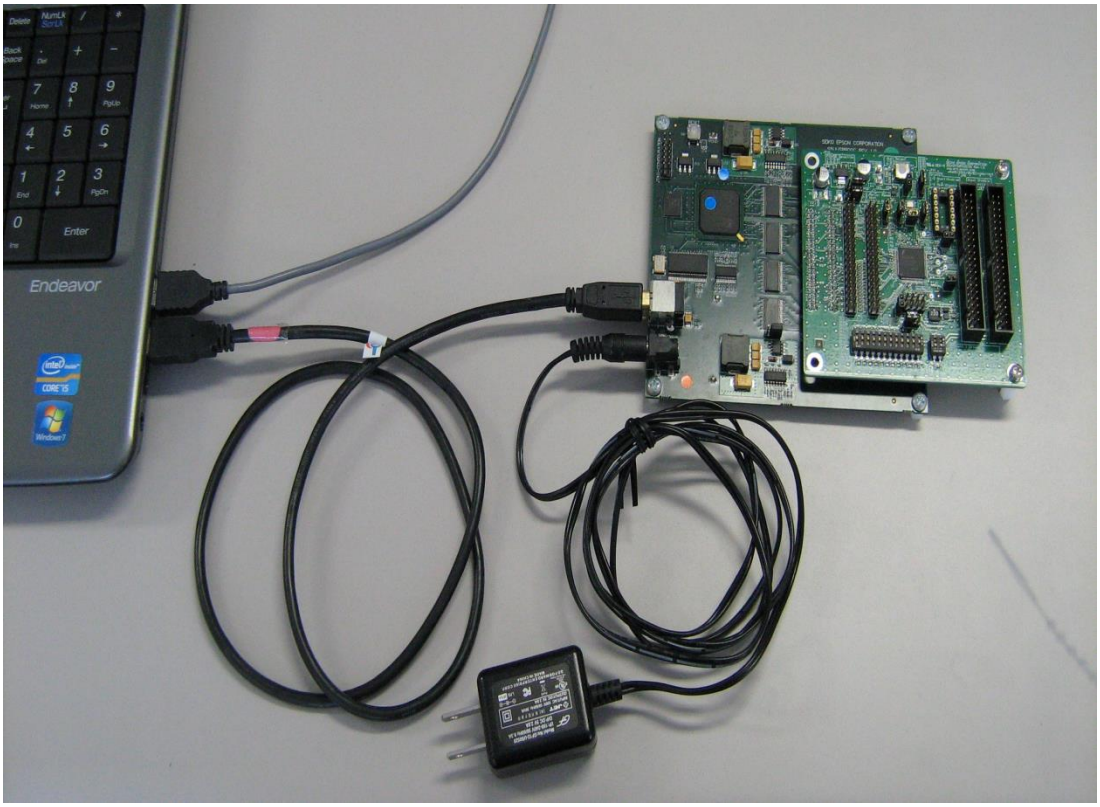

Figure 9.5 Connecting S5U13U00P00C100 Board, USB cable and 5V power adapter

10. Using the panel I/F board

10.1 Connecting the panel I/F board

Panel I/F board for easier connection to your TFT panel is prepared in the 5U13709P00C100 Evaluation Board kit. The available panel verified for this panel I/F board are as follows.

NHD-4.3-480272EF-ATXL# (WQVGA) from Newhaven Display International, Inc.

TCG043WQLBAANN-GN00 (WQVGA) from Kyocera.

TX11D06VM2APA (WQVGA) from KOE.

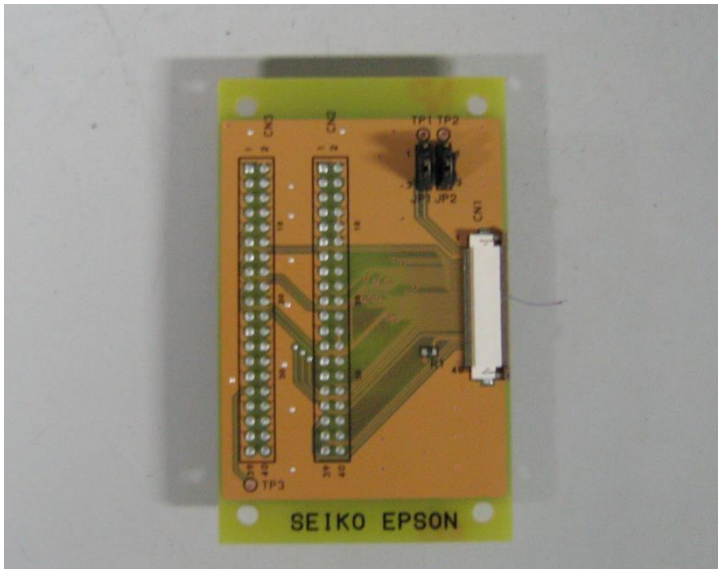

Figure 10.1 Panel I/F board

Connect with the H3, H4 header of S5U13709 Evaluation Board and Panel I/F board.

Please refer to Figure 10.2 Panel I/F board and S5U13709 board. Connect H3 header of S5U13709 board and CN2 connecter of panel I/F board. Connect H4 header of S5U13709 board and CN3 connecter of panel I/F board.

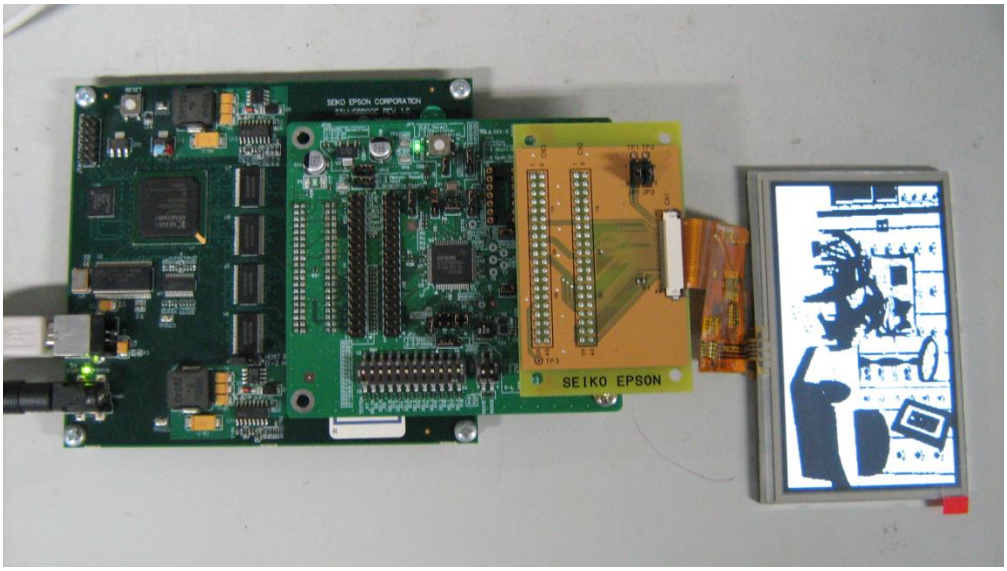

Figure 10.2 Panel I/F board and S5U13709 board

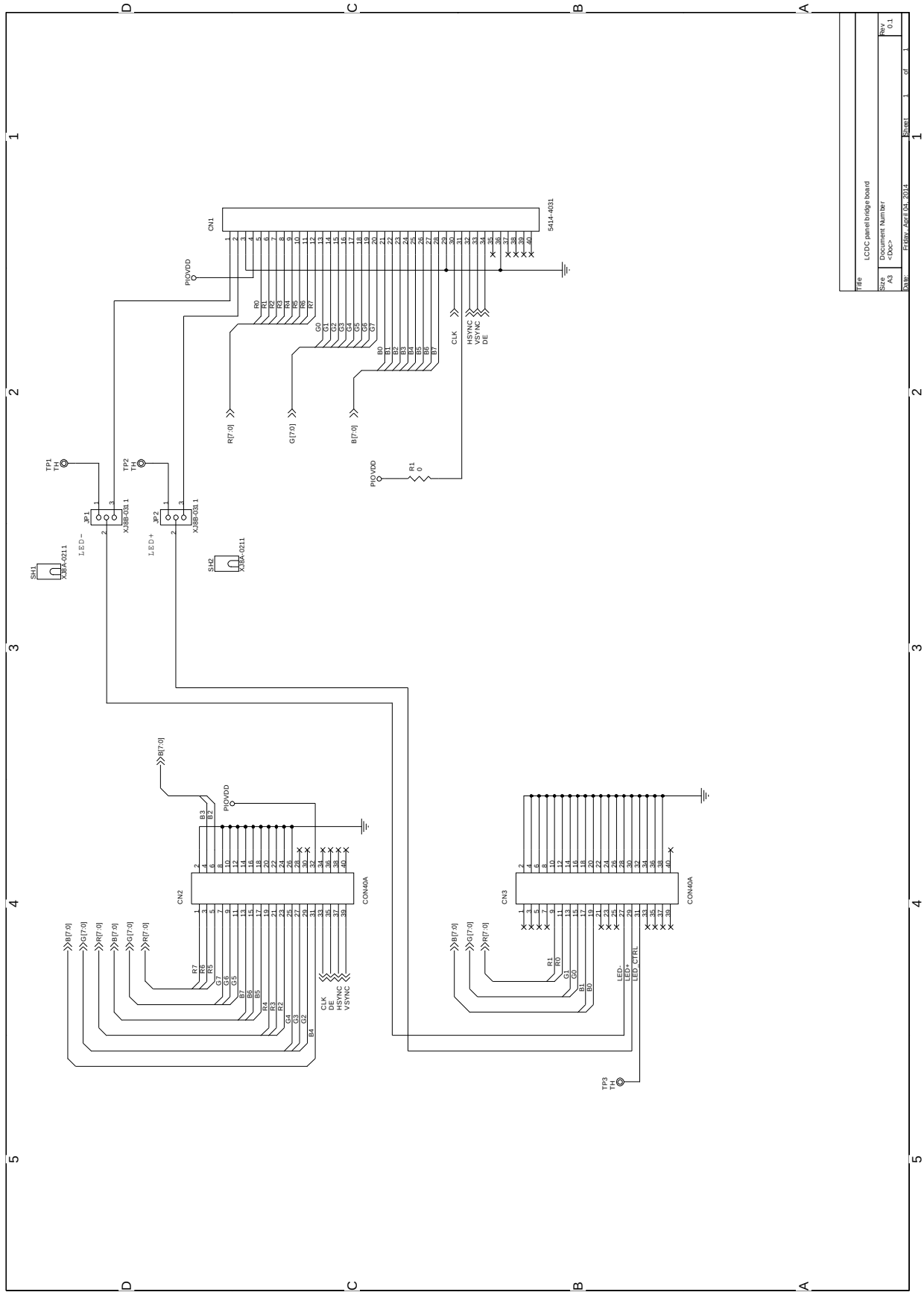

Figure 10.3 Panel I/F board schematic

11. Change Record

XA8A-G-001-01 Revision 1.1 - Issued: April 09, 2018

- Reformat entire document
- Updated address/contact page
- Updated Epson web page and email address

XA8A-G-001-01 Revision 1.0 - Issued: July 31, 2014

- Initial Release

12. Sales and Technical Support

For more information on Epson Display Controllers, visit the Epson Global website.

https://global.epson.com/products_and_drivers/semicon/products/display_controllers/

For Sales and Technical Support, contact the Epson representative for your region.

https://global.epson.com/products_and_drivers/semicon/information/support.html