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S1D13706 Embedded Memory LCD Controller

Power Consumption

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SEIKO EPSON CORPORATION

Rev. 2.1

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1 S1D13706 Power Consumption

S1D13706 power consumption is affected by many system design variables.

- Input clock frequency (CLKI/CLKI2): the CLKI/CLKI2 frequency determines the LCD frame-rate, CPU performance to memory, and other functions – the higher the input clock frequency, the higher the frame-rate, performance and power consumption.
- CPU interface: the S1D13706 current consumption depends on the BCLK frequency, data width, number of toggling pins, and other factors – the higher the BCLK, the higher the CPU performance and power consumption.
- V_{DD} voltage level: the voltage level affects power consumption – the higher the voltage, the higher the consumption.
- Display mode: the resolution and color depth affect power consumption – the higher the resolution/color depth, the higher the consumption.
- Internal CLK divide: internal registers allow the input clock to be divided before going to the internal logic blocks – the higher the divide, the lower the power consumption.

There is a power save mode in the S1D13706. The power consumption is affected by various system design variables.

- Clock states during the power save mode: disabling the clocks during power save mode has substantial power savings.

1.1 Conditions

The following table gives an example of a specific environment and its effects on power consumption.

Table 1-1: S1D13706 Total Power Consumption in mW

Test Condition *All V_{DD} = 3.3V*	MCLK/ PCLK Ratio	Color Depth	S1D13706 Active (mW)	Power Save Mode	
				Clocks Active (mW)	Clocks Removed (mW) [1]
LCD Panel = 60Hz 320x240 8-bit Single Color Format 2 CLKI = 6 MHz, CLKI2 = 6 MHz	1/16	1 bpp	6.58	3.02	0.00
	1/8	2 bpp	7.76	3.02	0.00
	1/4	4 bpp	8.80	3.02	0.00
	1/2	8 bpp	10.61	3.02	0.00
LCD Panel = 60Hz 320x240 4-bit Single Color CLKI = 6 MHz, CLKI2 = 6 MHz	1/2	8 bpp	11.16	3.02	0.00
LCD Panel = 60Hz 320x240 4-bit Single Monochrome CLKI = 6 MHz, CLKI2 = 6 MHz	1/2	8 bpp	9.43	3.02	0.00
LCD Panel = 60Hz 320x240 18-bit TFT CLKI = 6 MHz, CLKI2 = 6 MHz	1/2	8 bpp	8.84	3.02	0.00
LCD Panel = 60Hz 320x240 18-bit HR-TFT CLKI = 6 MHz, CLKI2 = 6 MHz	1/2	8 bpp	9.26	3.02	0.00
LCD Panel = 60Hz 320x240 18-bit D-TFD CLKI = 6 MHz, CLKI2 = 6 MHz	1/2	8 bpp	9.78	3.02	0.00
LCD Panel = 60Hz 160x240 18-bit D-TFD CLKI = 6 MHz, CLKI2 = 6 MHz	1/2	8 bpp	6.45	3.02	0.00
	1/1	16 bpp	8.12	3.02	0.00

Note

[1] CLKI and CLKI2 are stopped for this condition.

2 Summary

The system design variables in Section 1, “S1D13706 Power Consumption” and in Table 1-1: “S1D13706 Total Power Consumption in mW” show that S1D13706 power consumption depends on the specific implementation. Active Mode power consumption depends on the desired CPU performance and LCD frame-rate, whereas power save mode consumption depends on the CPU Interface and Input Clock state.

In a typical design environment, the S1D13706 can be configured to be an extremely power-efficient LCD Controller with high performance and flexibility.

3 Change Record

X31B-G-006-02 Revision 2.1 - Issued: March 26, 2018

- updated Sales and Technical Support Section
- updated some formatting

4 Sales and Technical Support

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