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S1D13705 Embedded Memory LCD Controller

S5U13705B00C Rev. 2.0 Evaluation Board User Manual

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SEIKO EPSON CORPORATION

Rev. 3.1

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1 Introduction

This manual describes the setup and operation of the S5U13705B00C Rev. 2.0 Evaluation Board. The board is designed as an evaluation platform for the S1D13705 Embedded Memory LCD Controller.

This document is updated as appropriate. Please check for the latest revision of this document before beginning any development. The latest revision can be downloaded at vdc.epson.com.

We appreciate your comments on our documentation. Please contact us via email at vdc-documentation@ea.epson.com.

2 Features

Following are some features of the S5U13705B00C Rev. 2.0 Evaluation Board:

- 80-pin TQFP S1D13705F00A Embedded Memory LCD Controller with 80K bytes of embedded SRAM.
- Headers for connecting to various Host Bus Interfaces.
- Configuration options.
- Adjustable positive LCD bias power supply from +23V to +40V.
- Adjustable negative LCD bias power supply from -23V to -14V.
- 4/8-bit 3.3V or 5V single monochrome or color passive LCD panel support.
- 9/12-bit 3.3V or 5V active matrix TFT LCD panel support.
- Software and hardware initiated power save mode.
- Selectable clock source for bus clock and CLKI.
- External oscillator for CLKI (up to 50MHz with internal clock divider or 25MHz with no internal clock divider) and BUSCLK.

3 Installation and Configuration

The S5U13705B00C is designed to support as many platforms as possible. The S5U13705B00C incorporates a DIP switch and seven jumpers which allow both evaluation board and S1D13705 LCD controller to be configured for a specified evaluation platform.

3.1 Configuration DIP Switches

The S1D13705 has configuration inputs (CNF[3:0]) and BS# input, which are read on the rising edge of RESET#. In order to configure the S1D13705 for multiple Host Bus Interfaces a six-position DIP switch (SW1) is required. The following figure shows the location of DIP switch SW1 on the S5U13705B00C.

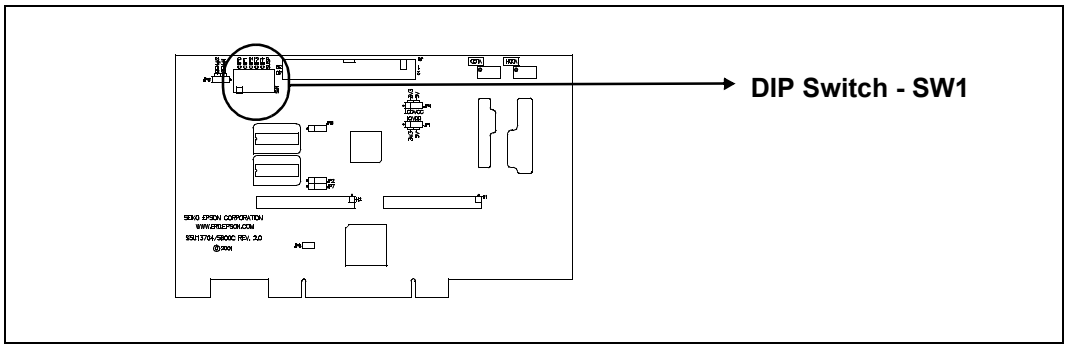


Figure 3-1: Configuration DIP Switch (SW1) Location

The S1D13705 has 4 configuration inputs (CONF[3:0]) and BS# input, which are read on the rising edge of RESET#. All S1D13705 configuration inputs and BS# input are fully configurable using a six position DIP switch as described below and a jumper for BS#.

Table 3-1: Configuration DIP Switch Settings

Switch	S1D13705 Signal	Value on this pin at rising edge of RESET# is used to configure: Open (Off/1)	Closed (On/0)
SW1-[3:1]	CNF[2:0]	Select host bus interface as follows: **CNF2 CNF1 CNF0 — Host Bus Interface** 0 0 0 — SH-4 0 0 1 — SH-3 0 1 0 — Reserved 0 1 1 — MC68K #1 1 0 0 — Reserved 1 0 1 — MC68K #2 1 1 0 — Reserved 1 1 1 — Generic #1/Generic #2[1] Note: The host bus interface is 16-bit.	
SW1-4	CNF3	Big Endian bus interface	Little Endian bus interface
SW1-5	Not Used	Not Used	
SW1-6	GPIO0	Hardware Suspend Enable	Hardware Suspend Disable

= Required settings when used with PCI Bridge FPGA

Note

[1] The selection between Generic #1 and Generic #2 is made with JP3.

3.2 Configuration Jumpers

The S5U13705B00C has six jumper blocks which configure various setting on the board. The jumper positions for each function are shown below.

Table 3-2: Jumper Summary

Jumper	Function	Position 1-2	Position 2-3	No Jumper
JP1	IOVDD Selection	+3.3V IOVDD	+5.0V IOVDD	n/a
JP2	Bus Clock Selection	External Oscillator (U7)	From Host CPU	n/a
JP3	BS# Signal Selection	Pulled Down to GND (for Generic #1 Interface)	Pulled High to IOVDD (for Generic #2 Interface)	For SH-3, SH-4, MC68k #1 and MC68K #2 bus
JP4	LCD Panel Voltage Selection	+3.3V LCDVCC	+5.0V LCDVCC	n/a
JP5	PCI Bridge FPGA	Disabled for non-PCI host	n/a	Enabled for PCI host
JP6	LCDPWR Polarity	Active Low	Active High	n/a
JP7	CLKI Selection	External Oscillator (U2)	BCLK	n/a

= Required settings when used with PCI Bridge FPGA

JP1 - IOVDD Selection

JP1 selects the IOVDD voltage for S1D13705.
When the jumper is in position 1-2, IOVDD is 3.3V. This settings must be used for a 3.3V host CPU system.
When the jumper is in position 2-3, IOVDD is 5.0V. This setting must be used for a 5.0V host CPU system.

Note
For PCI host, JP1 can be set in either position.

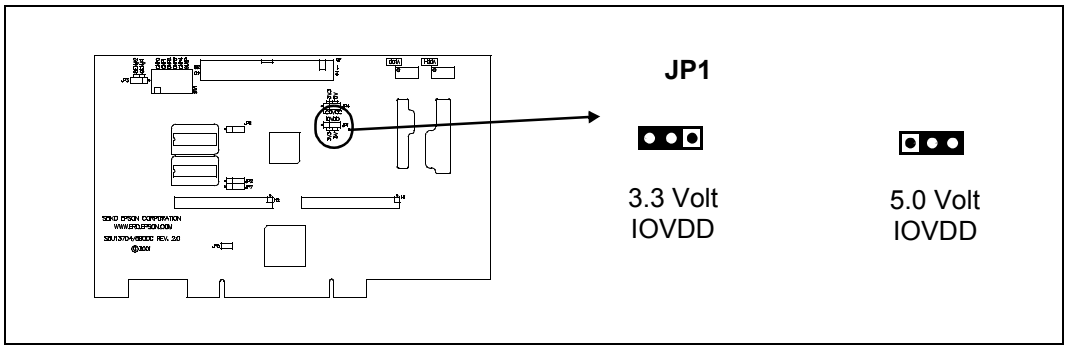


Figure 3-2: Configuration Jumper (JP1) Location

JP2 - Bus Clock Selection

JP2 selects the source for BCLK input on S1D13705.
When the jumper is in position 1-2, the BCLK source is the external oscillator U7. This position must be used for PCI-host.
When the jumper is in position 2-3, the BCLK must be provided by the host CPU. This setting may be used for non-PCI host.

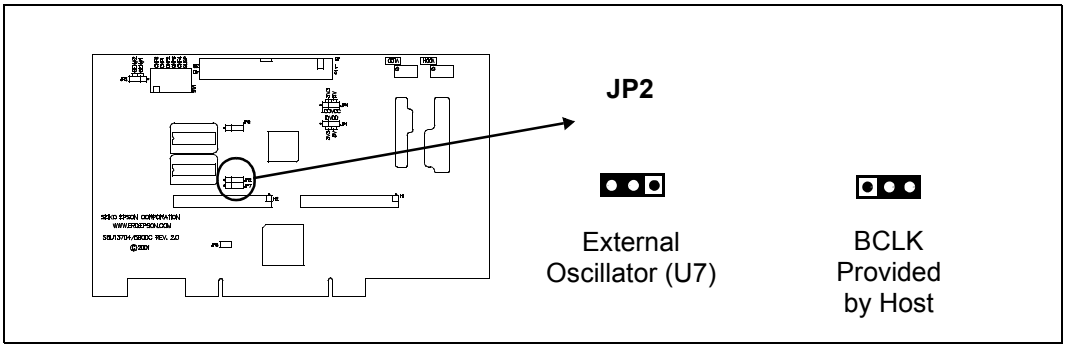


Figure 3-3: Configuration Jumper (JP2) Location

JP3 - BS# Signal Selection

JP3 is used to pull up or down BS# input of S1D13705 for selection of Generic #1 or Generic #2 interface.
When the jumper is in position 1-2, BS# is pulled down to select Generic #1 interface.
When the jumper is in position 2-3, BS# is pulled high to IOVDD, to select Generic #2 interface.

For SH-3, SH-4, MC68K #1 and MC68K #2 buses, which use BS# line, the jumper should not be installed.

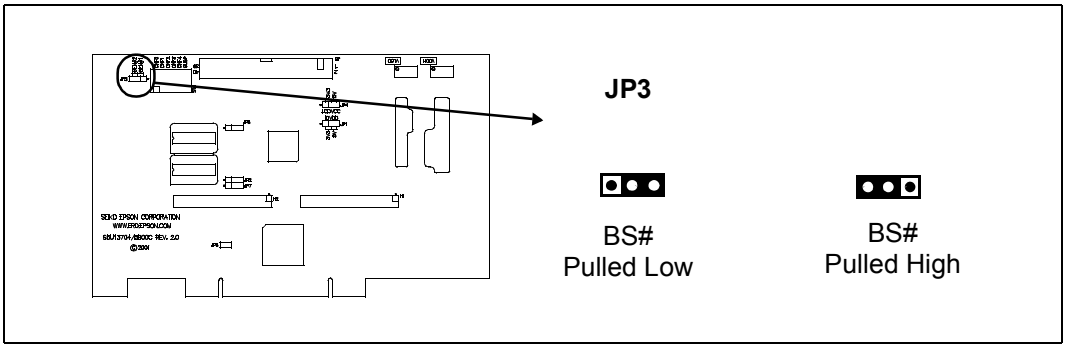


Figure 3-4: Configuration Jumper (JP3) Location

JP4 - LCD Panel Voltage Selection

JP4 selects voltage level to the LCD panel.
When the jumper is in position 1-2, the voltage level is set to 3.3V.
When the jumper is in position 2-3, the voltage level is set to 5.0V.

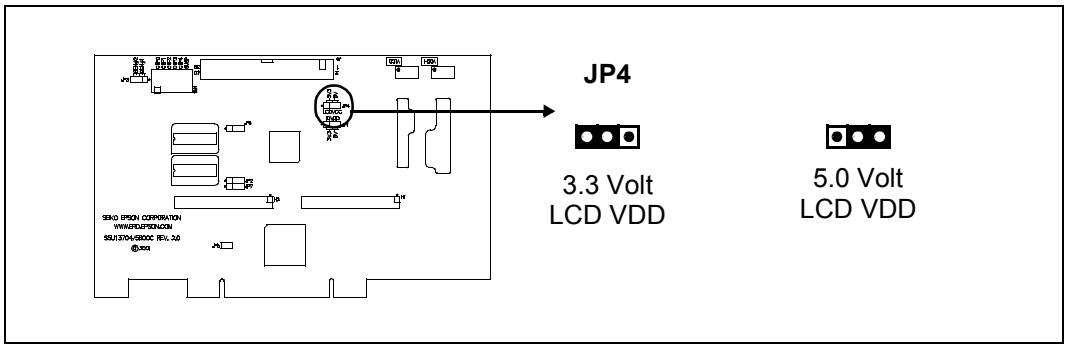


Figure 3-5: Configuration Jumper (JP4) Location

JP5 - PCI Bridge FPGA

JP5 is used to enable or disable the PCI bridge FPGA.
When the jumper is in position 1-2, the PCI bridge FPGA is disabled. This position must be used for non-PCI host.
When the jumper is off, the PCI bridge FPGA is enabled. The jumper must not be present for PCI host.

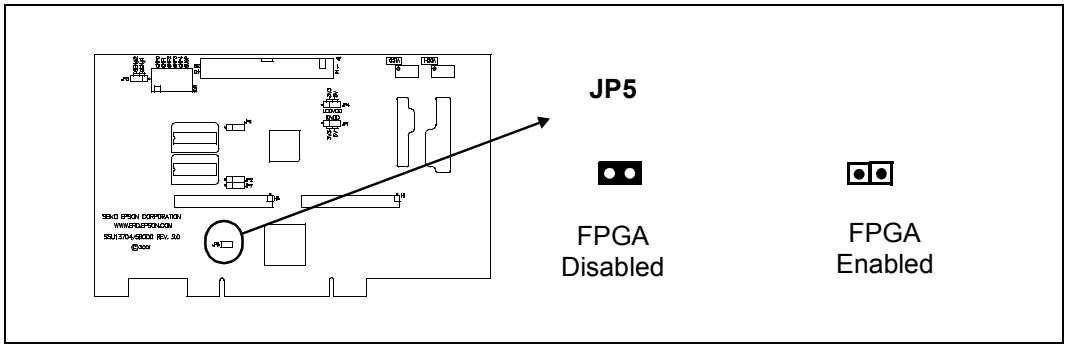


Figure 3-6: Configuration Jumper (JP5) Location

JP6 - LCDPWR Polarity

LCDPWR output from S1D13705 is only active high but some panels may require an active low signal. To provide both active high and active low signals, the output from S1D13705 is inverted and the selection is made by the setting of JP6
When the jumper is in position 1-2, LCDPWR signal to the panel is active low
When the jumper is in position 2-3, LCDPWR signal to the panel is active high

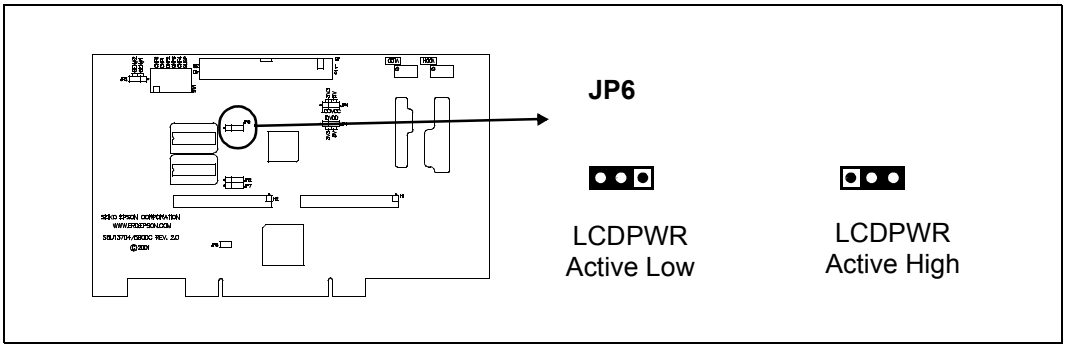


Figure 3-7: Configuration Jumper (JP6) Location

JP7 - CLKI Selection

JP7 selects the source for CLKI input on S1D13705.
When the jumper is in position 1-2, CLKI signal is provided by external oscillator U2
When the jumper is in position 2-3, CLKI signal is the same as BCLK signal

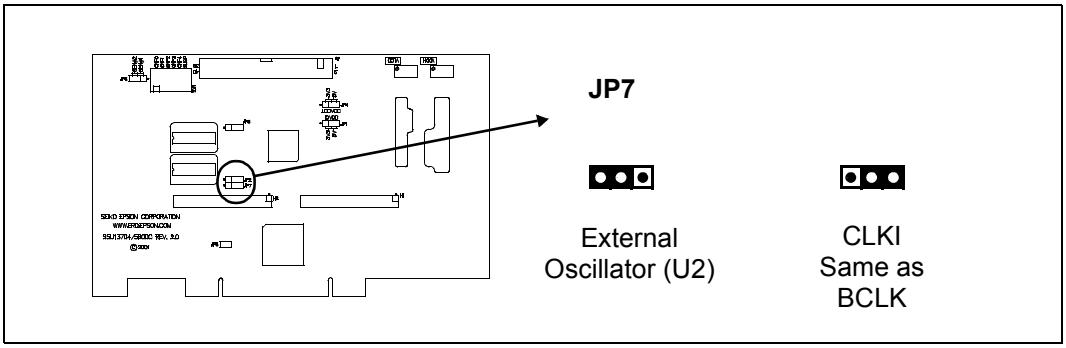


Figure 3-8: Configuration Jumper (JP7) Location

4 CPU Interface

4.1 CPU Interface Pin Mapping

Table 4-1: CPU Interface Pin Mapping

S1D13705 Pin Name	Generic #1	Generic #2	Hitachi SH-3	Hitachi SH-4	Motorola MC68K #1	Motorola MC68K #2
AB[16:1]	A[16:1]	A[16:1]	A[16:1]	A[16:1]	A[16:1]	A[16:1]
AB0	A0	A0	A0	A0	LDS#	A0
DB[15:0]	D[15:0]	D[15:0]	D[15:0]	D[15:0]	D[15:0]	D[15:0][1]
CS#	External Decode		CSn#	CSn#	External Decode	
BCLK	BCLK	BCLK	CKIO	CKIO	CLK	CLK
BS#	Connect to VSS	Connect to IOVDD	BS#	BS#	AS#	AS#
RD/WR#	RD1#	Connect to IOVDD	RD/WR#	RD/WR#	R/W#	R/W#
RD#	RD0#	RD#	RD#	RD#	Connect to IOVDD	SIZ1
WE0#	WE0#	WE#	WE0#	WE0#	Connect to IOVDD	SIZ0
WE1#	WE1#	BHE#	WE1#	WE1#	UDS#	DS#
WAIT#	WAIT#	WAIT#	WAIT#	RDY#	DTACK#	DSACK1#
RESET#	RESET#	RESET#	RESET#	RESET#	RESET#	RESET#

Note

[1] If the target MC68K bus is 32-bit, then these signals should be connected to D[31:16].

4.2 CPU Bus Connector Pin Mapping

Table 4-2: CPU Bus Connector (H1) Pinout

Connector Pin No.	Comments
1	Connected to DB0 of the S1D13705
2	Connected to DB1 of the S1D13705
3	Connected to DB2 of the S1D13705
4	Connected to DB3 of the S1D13705
5	Ground
6	Ground
7	Connected to DB4 of the S1D13705
8	Connected to DB5 of the S1D13705
9	Connected to DB6 of the S1D13705
10	Connected to DB7 of the S1D13705
11	Ground
12	Ground
13	Connected to DB8 of the S1D13705
14	Connected to DB9 of the S1D13705
15	Connected to DB10 of the S1D13705
16	Connected to DB11 of the S1D13705
17	Ground
18	Ground
19	Connected to DB12 of the S1D13705
20	Connected to DB13 of the S1D13705
21	Connected to DB14 of the S1D13705
22	Connected to DB15 of the S1D13705
23	Connected to RESET# of the S1D13705
24	Ground
25	Ground
26	Ground
27	+12 volt supply
28	+12 volt supply
29	Connected to WE0# of the S1D13705
30	Connected to WAIT# of the S1D13705
31	Connected to CS# of the S1D13705
32	Not connected
33	Connected to WE1# of the S1D13705
34	Connected to IOVDD

Table 4-3: CPU Bus Connector (H2) Pinout

Connector Pin No.	Comments
1	Connected to AB0 of the S1D13705
2	Connected to AB1 of the S1D13705
3	Connected to AB2 of the S1D13705
4	Connected to AB3 of the S1D13705
5	Connected to AB4 of the S1D13705
6	Connected to AB5 of the S1D13705
7	Connected to AB6 of the S1D13705
8	Connected to AB7 of the S1D13705
9	Ground
10	Ground
11	Connected to AB8 of the S1D13705
12	Connected to AB9 of the S1D13705
13	Connected to AB10 of the S1D13705
14	Connected to AB11 of the S1D13705
15	Connected to AB12 of the S1D13705
16	Connected to AB13 of the S1D13705
17	Ground
18	Ground
19	Connected to AB14 of the S1D13705
20	Connected to AB15 of the S1D13705
21	Connected to AB16 of the S1D13705
22	Not connected
23	Not connected
24	Not connected
25	Ground
26	Ground
27	+5 volt supply
28	+5 volt supply
29	Connected to RD/WR# of the S1D13705
30	Connected to BS# of the S1D13705
31	Connected to BCLK of the S1D13705
32	Connected to RD# of the S1D13705
33	Not connected
34	Not connected

5 LCD Interface Pin Mapping

Table 5-1: LCD Signal Connector (J5)

Pin Name	Connector Pin No.	Monochrome Passive			Color Passive Panel				Color TFT Panel	
		Single		Dual	Single			Dual		
						Format 1	Format 2			
		4-bit	8-bit	8-bit	4-bit	8-bit	8-bit	8-Bit	9-bit	12-bit
BFPDAT0	1	driven 0	D0	LD0	driven 0	D0 (B5)[1]	D0 (G3)[1]	LD0 (IR2)[1]	R2	R3
BFPDAT1	3	driven 0	D1	LD1	driven 0	D1 (R5)[1]	D1 (R3)[1]	LD1 (lB1)[1]	R1	R2
BFPDAT2	5	driven 0	D2	LD2	driven 0	D2 (G4)[1]	D2 (B2)[1]	LD2 (lG1)[1]	R0	R1
BFPDAT3	7	driven 0	D3	LD3	driven 0	D3 (B3)[1]	D3 (G2)[1]	LD3 (lR1)[1]	G2	G3
BFPDAT4	9	D0	D4	UD0	D0 (R2)[1]	D4 (R3)[1]	D4 (R2)[1]	UD0 (uR2)[1]	G1	G2
BFPDAT5	11	D1	D5	UD1	D1 (B1)[1]	D5 (G2)[1]	D5 (B1)[1]	UD1 (uB1)[1]	G0	G1
BFPDAT6	13	D2	D6	UD2	D2 (G1)[1]	D6 (B1)[1]	D6 (G1)[1]	UD2 (uG1)[1]	B2	B3
BFPDAT7	15	D3	D7	UD3	D3 (R1)[1]	D7 (R1)[1]	D7 (R1)[1]	UD3 (uR1)[1]	B1	B2
BFPDAT8	17	GPIO1							B0	B1
BFPDAT9	19	GPIO2								R0
BFPDAT10	21	GPIO3								G0
BFPDAT11	23	GPIO4								B0
BFPSHIFT	33	FPSHIFT								
BDRDY	35 & 38	MOD				FPSHIFT2	MOD		DRDY	
BFPLINE	37	FPLINE								
BFPFRAME	39	FPFRAME								
GND	2-26 (Even Pins)	GND								
VLCD	30	Adjustable -24V to -14V negative LCD bias								
LCDVCC	32	LCDVCC (3.3V / 5.0V)								
+12V	34	+12V								
VDDH	36	Adjustable +23V to +40V positive LCD bias								
BLCDPWR	40	LCDPWR[2] (for controlling on-board LCD bias power supply on/off)								

Note

[1]These pin mappings use signal names commonly used for each panel type, however signal names may differ between panel manufacturers. The values shown in brackets represent the color components as mapped to the corresponding FPDATxx signals at the first valid edge of FPSHIFT. For further FPDATxx to LCD interface mapping, see *S1D13705 Hardware Functional Specification*, document number ***X27A-A-001-xx.***

[2]LCDPWR on J5 can be inverted by setting JP6 to 1-2.

6 Technical Description

6.1 PCI Bus Support

The S1D13705 **does not** have on-chip PCI bus interface support. The S1D13705B00C uses the PCI Bridge FPGA to support the PCI bus. When using the PCI Bridge FPGA, a Windows device driver is required, see Section 7, "Software" on page 20 for further information on available software and drivers.

6.2 Direct Host Bus Interface Support

The S5U13705B00C is specifically designed to work using the PCI Bridge FPGA in a standard PCI bus environment. However, the S1D13705 directly supports many other host bus interfaces. Connectors H1 and H2 provide the necessary IO pins to interface to these host buses. For further information on the host bus interfaces supported, see "CPU Interface" on page 13.

Note

The PCI Bridge FPGA must be disabled using JP5 in order for direct host bus interface to operate properly.

6.3 S1D13705 Embedded Memory

The S1D13705 has 80K bytes of embedded SRAM. The 80K byte display buffer address space is directly and contiguously available through the 17-bit address bus.

The S1D13705 registers are located in the upper 32 bytes of the 128K byte address range of S1D13705.

6.4 Adjustable LCD Panel Positive Power Supply (VDDH)

For those LCD panels requiring a positive power supply to provide between +23V and +40V (Iout = 45mA) a power supply has been provided as an integral part of this design. The VDDH power supply can be adjusted by R15 to provide an output voltage from +23V to +40V and is enabled and disabled by the active high LCDPWR control signal of S1D13705 and inverted externally.

Determine the panel's specific power requirements and set the potentiometer accordingly before connecting the panel.

6.5 Adjustable LCD Panel Negative Power Supply (VLCD)

For those LCD panels requiring a negative power supply to provide between -23V and -14V (Iout = 25mA) a power supply has been provided as an integral part of this design. The VLCD power supply can be adjusted by R21 to give an output voltage from -23V to -14V and is enabled and disabled by the active high LCDPWR control signal of S1D13705 and inverted externally.

Determine the panel's specific power requirements and set the potentiometer accordingly before connecting the panel.

6.6 Passive/Active LCD Panel Support

The S1D13705 directly supports:

- 4/8-bit, single and dual, monochrome passive panels.
- 4/8-bit, single and dual, color passive panels.
- 9/12-bit, TFT active matrix panels.

All the necessary signals are provided on the 40-pin LCD connector J5. For connection information, refer to ***Table 5-1: "LCD Signal Connector (J5)"*** on page 16.

The buffered LCD connector (J5) provides the same LCD panel signals as those directly from S1D13705, but with voltage-adapting buffers selectable to 3.3V or 5.0V. Pin 32 on this connector provides a voltage level of 3.3V or 5.0V to the LCD panel logic (see "JP6 - LCDPWR Polarity" on page 12 for information on setting the panel voltage).

6.7 Power Save Modes

The S1D13705 supports one hardware and one software power save mode. The hardware power save mode needs to be enabled by setting REG[02h] bit1 to 1 and then can be activated by DIP switch SW1-6. See ***Table 3-1: "Configuration DIP Switch Settings"*** on page 8**.**

6.8 Clock Options

The input clock (CLKI) frequency can be up to 50MHz for the S1D13705 if the internal divide-by-2 mode is set. If the clock divider is not used, the maximum CLKI frequency is 25MHz. There is no minimum input clock frequency.

A 6.0MHz oscillator (U2, socketed) is provided as the input clock source. However, depending on the LCD resolution, desired frame rate and power consumption budget, another clock frequency may be required.

A jumper, JP7 is provided to allow CLKI input to be the same as BCLK input, for systems in which is desired to use only one clock signal for both BCLK and CLKI.

The bus clock (BCLK) is selectable and can be provided by a 50MHz oscillator (U7, socketed) or the host CPU (for non-PCI host).

7 Software

This evaluation board, when used with the PCI Bridge FPGA adapter, requires drivers to work in the 32-bit Windows environment. See the *S1D13XXX 32-Bit Windows Device Driver Installation Guide*, document number X00A-E-003-xx for more information.

Test utilities and display drivers are also available for the S1D13705. Full source code is available for both the test utilities and the drivers.

The test utilities are configurable for different panel types using a program called 13705CFG, or by directly modifying the source. The display drivers can be customized by the OEM for different panel types, resolutions and color depths only by modifying the source.

The S1D13705 test utilities and drivers are available from your sales support contact or on the internet at vdc.epson.com.

8 Parts List

Item	Quantity	Reference	Part	Description
1	15	C1-C11, C16, C17, C24, C25	0.1uF, 20%, 50V	1206 pckg., ceramic capacitor
2	1	C12	10uF, 10%, 25V	Tantalum capacitor size D
3	2	C22,C18	47uF, 10%, 16V	Tantalum capacitor size D
4	3	C19,C20,C21	4.7uF, 10%, 50V	Tantalum capacitor size D
5	1	C23	56uF, 20%, 35V, Low ESR	Electrolytic, radial, low ESR
6	2	C36,C33	33uF, 10%, 20V	Tantalum capacitor size D
7	3	C34,C35,C37	68uF, 10%, 10V	Tantalum capacitor size D
8	9	C38-C46	0.22uF, 5%, 50V	X7R, 1206 pckg
9	2	H2,H1	HEADER 17X2	0.1", 17x2, unshrouded header
10	6	JP1,JP2,JP3,JP4,JP6,JP7	HEADER 3	0.1", 3x1, unshrouded header
11	1	JP5	HEADER 2	0.1", 2x1, unshrouded header
12	1	J5	CON40A	0.1", 20x2, 0.025" sq. shrouded header, center key, t/h
13	1	L1	1uH	RCD MCI-1812 inductor 1uH MT or MSI-1812 1uH MT
14	3	L2,L3,L4	Ferrite Bead	Philips BDS3/3/8.9-4S2
15	1	Q1	MMBT3906	Generic MMBT3906
16	1	Q2	MMBT3904	Generic MMBT3904
17	13	R1-R6, R10, R11, R33, R36-R39	15K, 5%	1206 resistor
18	1	R8	0R	1206 resistor, 0 ohms
19	1	R14	475K, 1%	1206 resistor
20	1	R15	200K Pot.	200K Trim POT Spectrol 63S204T607 or equiv.
21	1	R16	14K, 1%	1206 resistor
22	2	R18, R17	10K, 5%	1206 resistor
23	3	R19, R20, R32	100K, 5%	1206 resistor
24	1	R21	100K Pot.	100K Trim POT Spectrol 63S104T607 or equiv.
25	3	R34, R35, R40	1K, 5%	1206 resistor
26	1	SW1	SW DIP-6	6 position DIP switch
27	1	U1	S1D13705	
28	1	U2	14-pin DIP socket	Machined socket, 14-pin
29	1	U2	6MHz	Fox 6.0MHz oscillator or equiv., 14-pin DIP pckg, socketed
30	3	U3,U4,U5	74AHC244	SO-22, TI74AHC244 or equivalent
31	1	U6	LT1117CM-3.3	Linear Technology 5V to 3.3V regulator, 800mA or equiv.

Item	Quantity	Reference	Part	Description
32	1	U7	14-pin DIP socket	Machined socket, 14-pin
33	1	U7	50MHz	Fox 50.0MHz oscillator or equiv., 14-pin DIP pckg, socketed
34	1	U8	74AHC04/SO	SO-14, 74AHC04
35	1	U9	74HCT86/SO	SO-14, 74HCT86
36	1	U10	RD-0412	Xentek RD-0412, positive power supply
37	1	U11	EPN001	Xentek EPN001, negative power supply
38	1	U14	EPF6016TC144-2	Altera EPF6016TC144-2
39	1	U15	8-pin DIP socket	Machined socket, 8-pin
40	1	U15	EPC1441PC8	Altera EPC1441PC8, socketed
41	6	JP1,JP2,JP3,JP4,JP6,JP7	Jumper shunt for 0.1" header	
42	1		Bracket	Computer Bracket, Blank - PCI, Keystone - Cat. No. 9203
43	2		Scew	Pan Head, #4-40 x 1/4"

9 Schematics

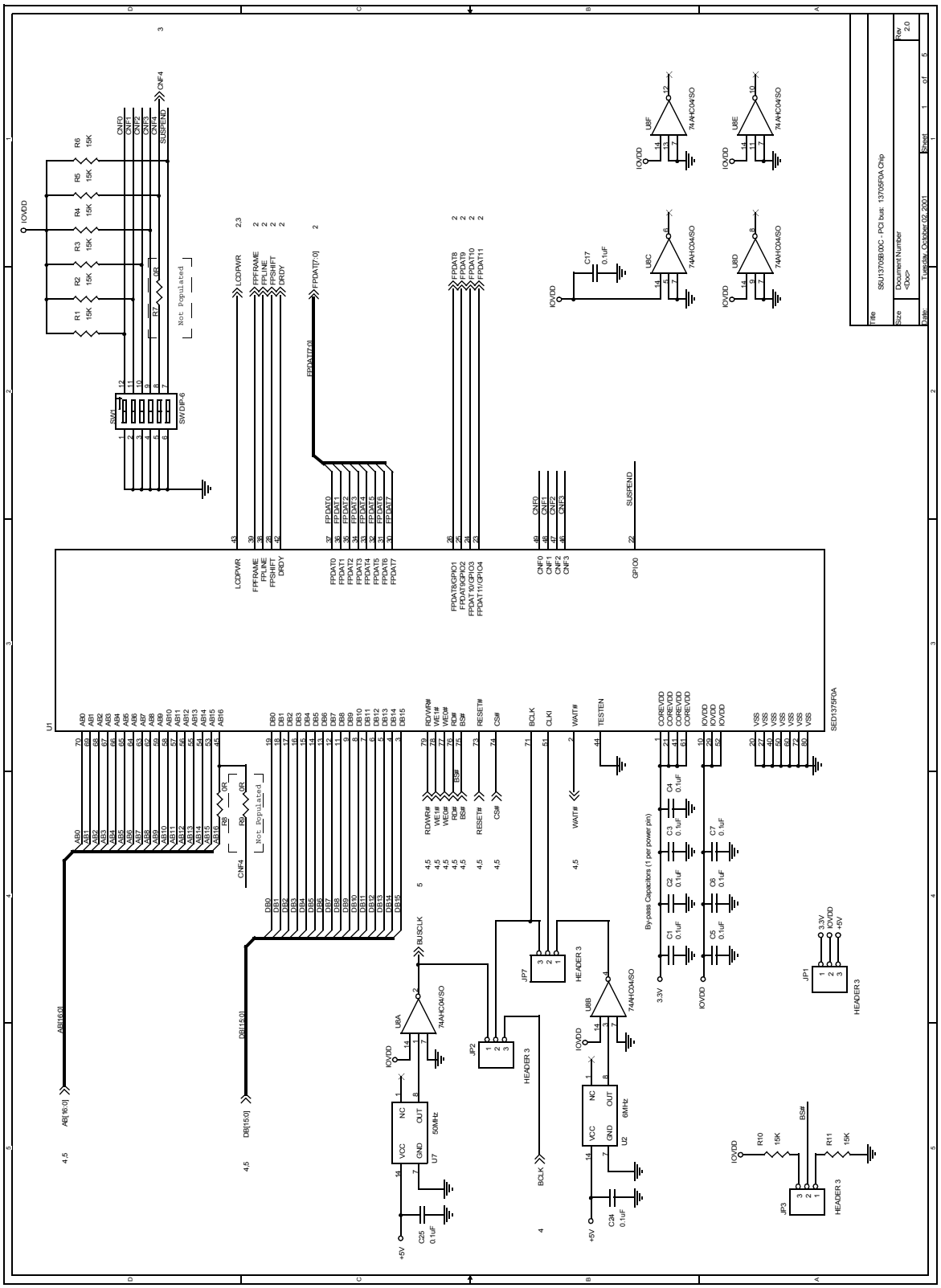


Figure 9-1: S1D13705B00C Schematics (1 of 5)

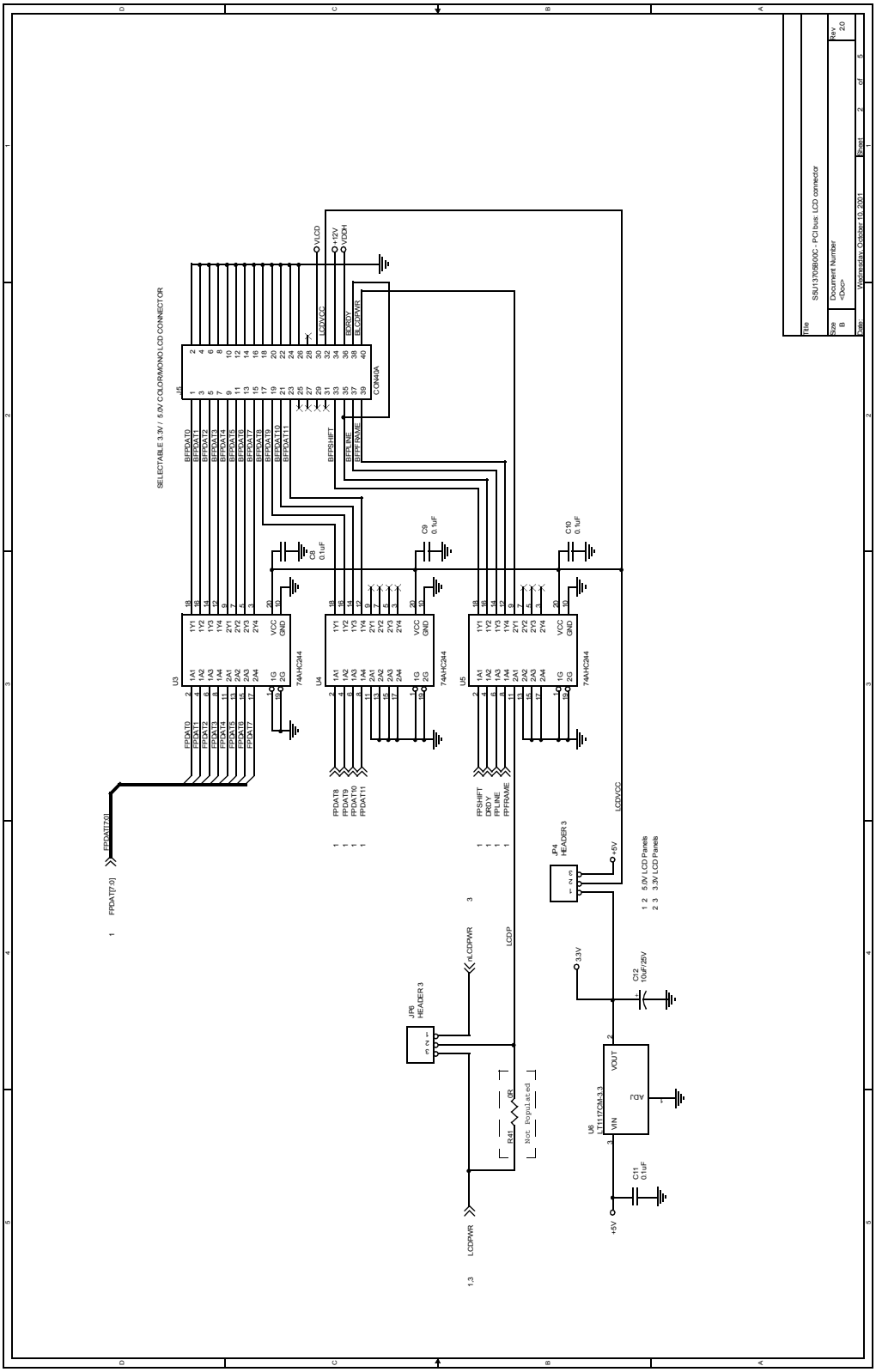


Figure 9-2: S1D13705B00C Schematics (2 of 5)

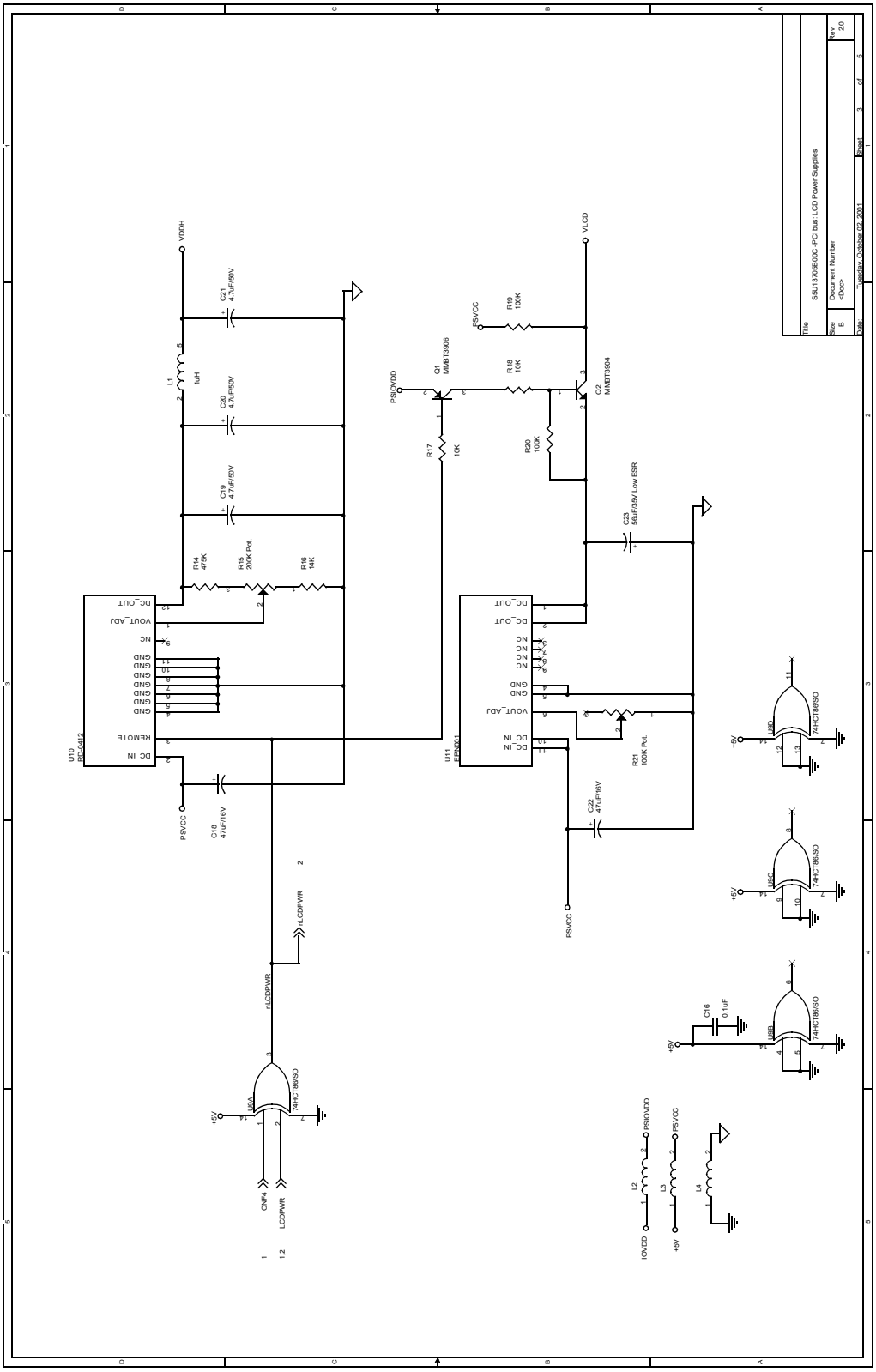


Figure 9-3: S1D13705B00C Schematics (3 of 5)

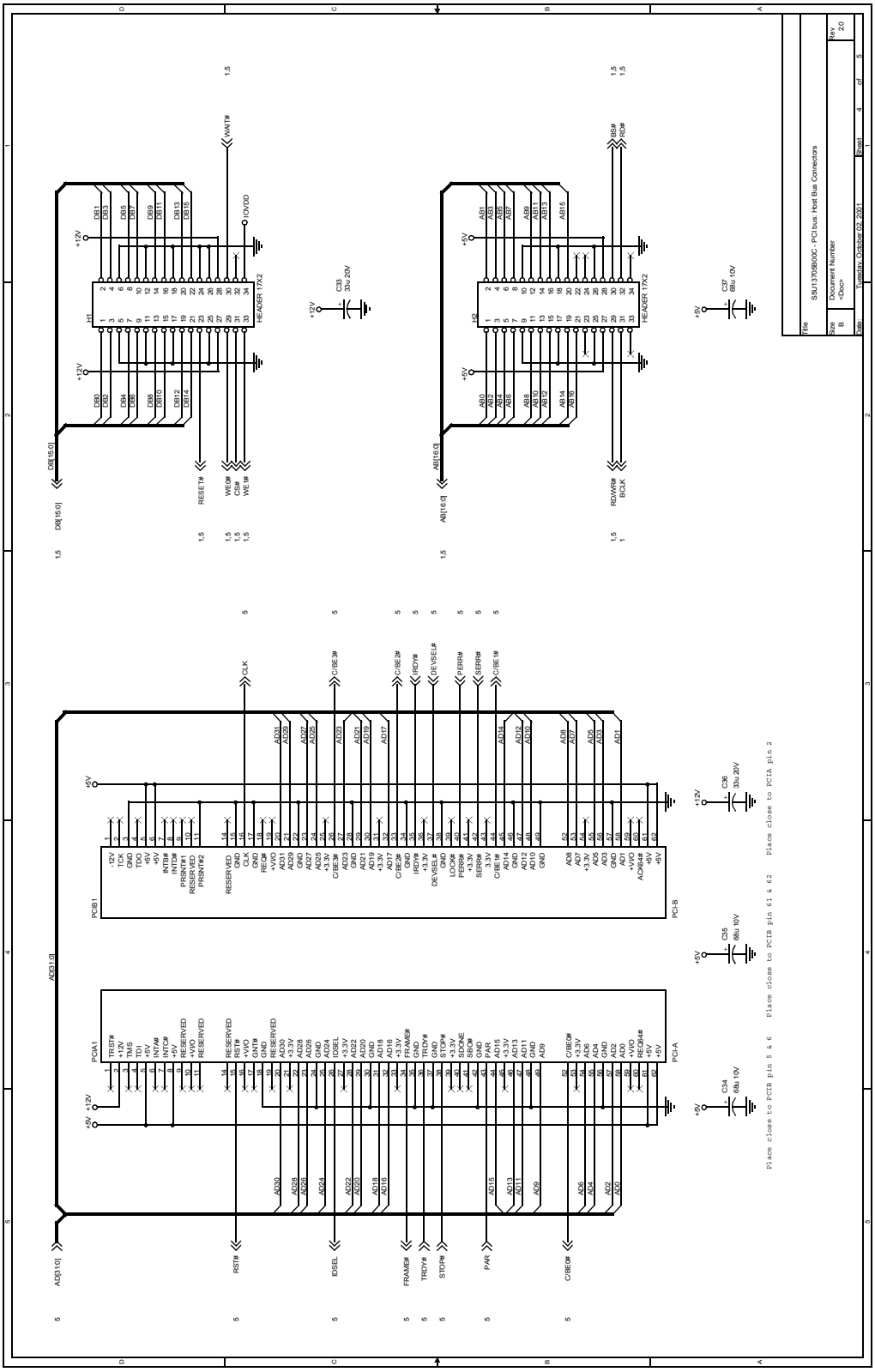


Figure 9-4: S1D13705B00C Schematics (4 of 5)

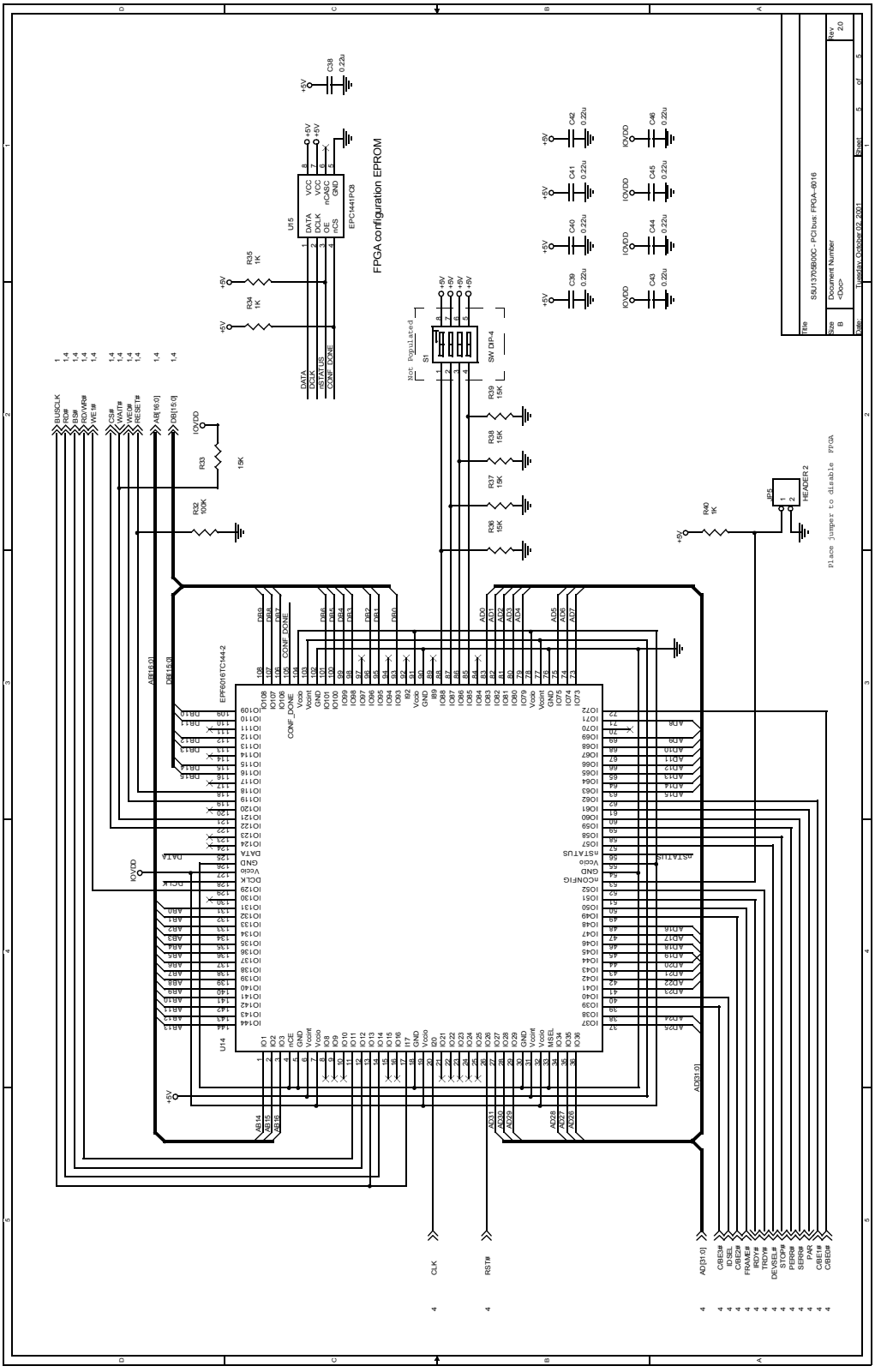
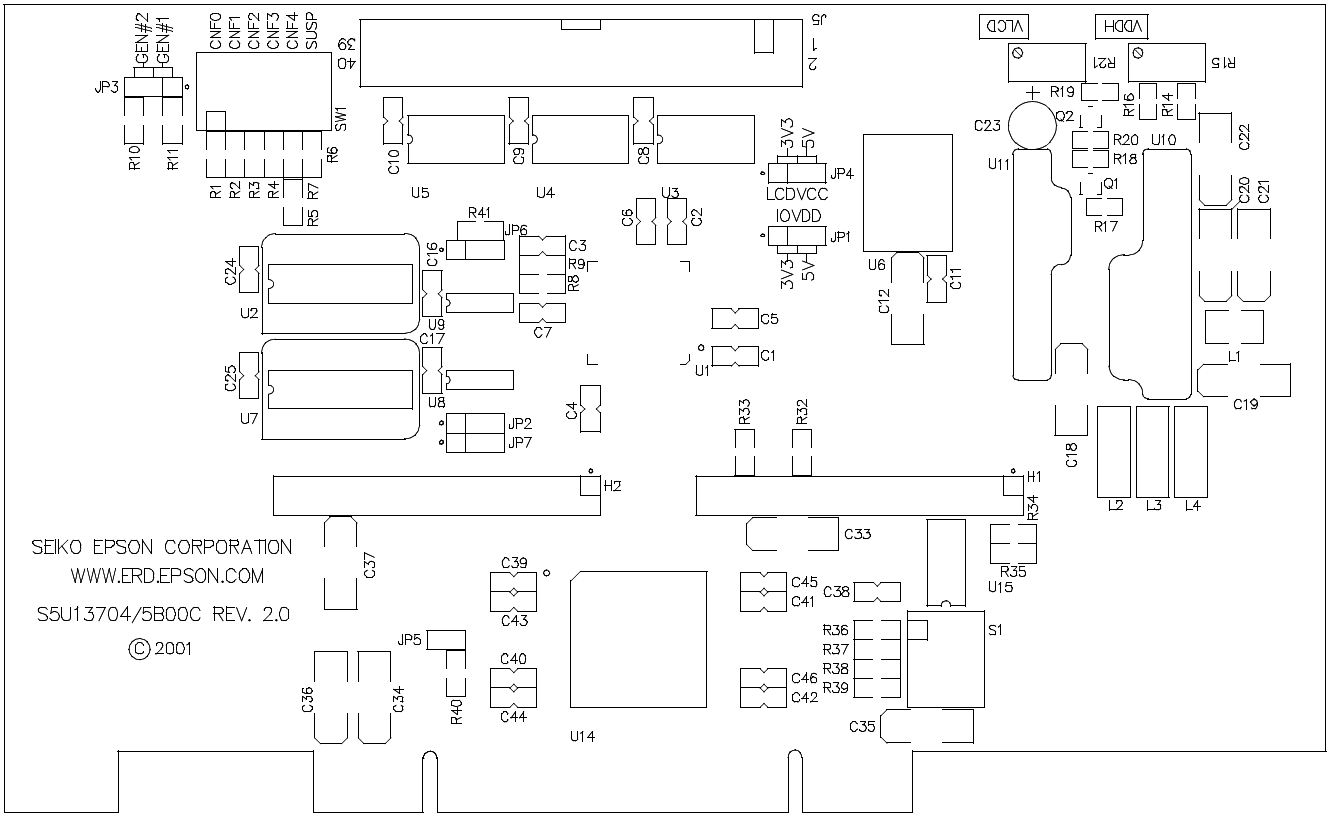


Figure 9-5: S1D13705B00C Schematics (5 of 5)

10 Board Layout



11 Change Record

X27A-G-014-03 Revision 3.1 - Issued: March 26, 2018

- updated Sales and Technical Support Section
- updated some formatting

12 Sales and Technical Support

For more information on Epson Display Controllers, visit the Epson Global website.

https://global.epson.com/products_and_drivers/semicon/products/display_controllers/

For Sales and Technical Support, contact the Epson representative for your region.

https://global.epson.com/products_and_drivers/semicon/information/support.html