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S1D13705 Embedded Memory LCD Controller

S5U13705B00C Rev. 1.0 ISA Bus Evaluation Board User Manual

Document Number: X27A-G-005-03.1

SEIKO EPSON CORPORATION

Rev. 3.1

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NOTICE

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1 Introduction

This manual describes the setup and operation of the S5U13705B00C Rev. 1.0 Evaluation Board. Implemented using the S1D13705 Embedded Memory Color LCD Controller, the S5U13705B00C board is designed for the 16-bit ISA bus environment. To accommodate other bus architectures, the S5U13705B00C board also provides CPU/Bus interface connectors.

For more information regarding the S1D13705, refer to the S1D13705 Hardware Functional Specification, document number X27A-A-001-xx.

This document is updated as appropriate. Please check for the latest revision of this document before beginning any development. The latest revision can be downloaded at vdc.epson.com.

We appreciate your comments on our documentation. Please contact us via email at vdc-documentation@ea.epson.com.

1.1 Features

- 80-pin QFP14 package.
- SMT technology for all appropriate devices.
- 4/8-bit monochrome and color passive LCD panel support.
- 9/12-bit LCD TFT/D-TFD panel support.
- Selectable 3.3V or 5V LCD panel support.
- Oscillator support for CLKI (up to 50MHz with internal clock divider or 25MHz with no internal clock divider).
- Embedded 80K byte SRAM display buffer for 1/2/4 bit-per-pixel (bpp), 2/4/16-level gray shade display and 1/2/4/8 bpp, 2/4/16/256 level color display.
- Support for software and hardware power save modes.
- On-board adjustable LCD bias positive power supply (+23V to +40V).
- On-board adjustable LCD bias negative power supply (-23V to -14V).
- 16-bit ISA bus support.
- CPU/Bus interface header strips for non-ISA bus support.

2 Installation and Configuration

The S1D13705 has four configuration inputs, CNF[3:0], which are read on the rising edge of RESET# and are fully configurable on this evaluation board. One six-position DIP switch is provided on the board to configure the four configuration inputs, select the S5U13705B00C memory/register start address, and enable/disable hardware power save mode.

The following settings are recommended when using the S5U13705B00C with the ISA bus.

Table 2-1: Configuration DIP Switch Settings

Switch	Signal	Closed (0 or low)	Open (1 or high)
S1-1	CNF0	See “Host Bus Selection” table below	See “Host Bus Selection” table below
S1-2	CNF1		
S1-3	CNF2		
S1-4	CNF3	Little Endian	Big Endian
S1-5	ADDR	Memory/Register Start Address = C0000h	Memory/Register Start Address = F00000h
S1-6	GPIO0	Hardware Suspend Disable	Hardware Suspend Enable

= recommended settings (configured for ISA bus support)

Table 2-2: Host Bus Selection

S1-3	S1-2	S1-1	BS#	Host Bus Interface
0	0	0	X	SH-4 bus interface
0	0	1	X	SH-3 bus interface
0	1	0	X	reserved
0	1	1	X	MC68K bus interface #1, 16-bit
1	0	0	X	reserved
1	0	1	X	MC68K bus interface #2, 16-bit
1	1	0	0	reserved
1	1	0	1	reserved
1	1	1	0	Generic #1, 16-bit
1	1	1	1	Generic #2, 16-bit

= recommended settings (configured for ISA bus support)

Table 2-3: Jumper Settings

	Description	1-2	2-3
JP1	IOVDD Selection	5.0V IOVDD	3.3V IOVDD
JP2	RD/WR# Signal Selection	Pulled up to IOVDD	No Connection
JP3	BS# Signal Selection	Pulled up to IOVDD	No Connection
JP4	LCD Panel Voltage Selection	5V LCD Panel	3.3V LCD Panel
JP6	LCDPWR polarity	Active low ('LCDPWR#')	Active high ('LCDPWR')

= recommended settings (JP1 through JP3 configured for ISA bus support)

3 LCD Interface Pin Mapping

Table 3-1: LCD Signal Connector (J5) Pinout

Connector		Single Passive Panel					Dual Passive Panel		Color TFT/D-TFD	
		Color			Mono		Color	Mono		
Pin Name	Pin #	4-bit	8-bit	8-bit Alternate Format	4-bit	8-bit	8-bit	8-bit	9-bit	12-bit
BFPDAT0	1	driven 0	D0	LD0	driven 0	D0	D0	LD0	R2	R3
BFPDAT1	3	driven 0	D1	LD1	driven 0	D1	D1	LD1	R1	R2
BFPDAT2	5	driven 0	D2	LD2	driven 0	D2	D2	LD2	R0	R1
BFPDAT3	7	driven 0	D3	LD3	driven 0	D3	D3	LD3	G2	G3
BFPDAT4	9	D0	D4	UD0	D0	D4	D4	UD0	G1	G2
BFPDAT5	11	D1	D5	UD1	D1	D5	D5	UD1	G0	G1
BFPDAT6	13	D2	D6	UD2	D2	D6	D6	UD2	B2	B3
BFPDAT7	15	D3	D7	UD3	D3	D7	D7	UD3	B1	B2
BFPDAT8	17	GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	B0	B1
BFPDAT9	19	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	R0
BFPDAT10	21	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	G0
BFPDAT11	23	GPIO4/ Inverse Video	GPIO4/ Inverse Video	GPIO4/ Inverse Video	GPIO4/ Inverse Video	GPIO4/ Inverse Video	GPIO4/ Inverse Video	GPIO4/ Inverse Video	GPIO4	B0
BFPSHIFT	33	FPSHIFT	FPSHIFT	FPSHIFT	FPSHIFT	FPSHIFT	FPSHIFT	FPSHIFT	FPSHIFT	FPSHIFT
BFPSHIFT2	35		FPSHIFT2							
BFPLINE	37	FPLINE	FPLINE	FPLINE	FPLINE	FPLINE	FPLINE	FPLINE	FPLINE	FPLINE
BFPFRAME	39	FPFRAME	FPFRAME	FPFRAME	FPFRAME	FPFRAME	FPFRAME	FPFRAME	FPFRAME	FPFRAME
GND	2-26 (Even Pins)	GND	GND	GND	GND	GND	GND	GND	GND	GND
N / C	28									
VLCD	30	LCD panel negative bias voltage (-24V to -14V)								
LCDVCC	32	+3.3V or +5V (selectable with JP4)								
+12V	34	+12V	+12V	+12V	+12V	+12V	+12V	+12V	+12V	+12V
VDDH	36	LCD panel positive bias voltage (+23V to +40V)								
BDRDY	38	MOD		MOD	MOD	MOD	MOD	MOD	DRDY	DRDY
BLCDPWR	40	LCDPWR	LCDPWR	LCDPWR	LCDPWR	LCDPWR	LCDPWR	LCDPWR	LCDPWR	LCDPWR

Note

1. Un-used GPIO pins must be connected to IO V_{DD}.
2. Inverse Video is enabled on FPDAT11 by REG[02h] bit 1.

4 CPU/Bus Interface Connector Pinouts

Table 4-1: CPU/BUS Connector (H1) Pinout

Connector Pin No.	CPU/BUS Pin Name	Comments
1	SD0	Connected to DB0 of the S1D13705
2	SD1	Connected to DB1 of the S1D13705
3	SD2	Connected to DB2 of the S1D13705
4	SD3	Connected to DB3 of the S1D13705
5	GND	Ground
6	GND	Ground
7	SD4	Connected to DB4 of the S1D13705
8	SD5	Connected to DB5 of the S1D13705
9	SD6	Connected to DB6 of the S1D13705
10	SD7	Connected to DB7 of the S1D13705
11	GND	Ground
12	GND	Ground
13	SD8	Connected to DB8 of the S1D13705
14	SD9	Connected to DB9 of the S1D13705
15	SD10	Connected to DB10 of the S1D13705
16	SD11	Connected to DB11 of the S1D13705
17	GND	Ground
18	GND	Ground
19	SD12	Connected to DB12 of the S1D13705
20	SD13	Connected to DB13 of the S1D13705
21	SD14	Connected to DB14 of the S1D13705
22	SD15	Connected to DB15 of the S1D13705
23	RESET#	Connected to the RESET# signal of the S1D13705
24	GND	Ground
25	GND	Ground
26	GND	Ground
27	+12V	12 volt supply
28	+12V	12 volt supply
29	WE0#	Connected to the WE0# signal of the S1D13705
30	WAIT#	Connected to the WAIT# signal of the S1D13705
31	CS#	Connected to the CS# signal of the S1D13705
32	NC	Not connected
33	WE1#	Connected to the WE1# signal of the S1D13705
34	IOVDD	Connected to the IOVDD supply of the S1D13705

Table 4-2: CPU/BUS Connector (H2) Pinout

Connector Pin No.	CPU/BUS Pin Name	Comments
1	SA0	Connected to AB0 of the S1D13705
2	SA1	Connected to AB1 of the S1D13705
3	SA2	Connected to AB2 of the S1D13705
4	SA3	Connected to AB3 of the S1D13705
5	SA4	Connected to AB4 of the S1D13705
6	SA5	Connected to AB5 of the S1D13705
7	SA6	Connected to AB6 of the S1D13705
8	SA7	Connected to AB7 of the S1D13705
9	GND	Ground
10	GND	Ground
11	SA8	Connected to AB8 of the S1D13705
12	SA9	Connected to AB9 of the S1D13705
13	SA10	Connected to AB10 of the S1D13705
14	SA11	Connected to AB11 of the S1D13705
15	SA12	Connected to AB12 of the S1D13705
16	SA13	Connected to AB13 of the S1D13705
17	GND	Ground
18	GND	Ground
19	SA14	Connected to AB14 of the S1D13705
20	SA15	Connected to AB14 of the S1D13705
21	SA16	Connected to AB16 of the S1D13705
22	SA17	Connected to SA17 of the ISA bus connector
23	SA18	Connected to SA18 of the ISA bus connector
24	SA19	Connected to SA19 of the ISA bus connector
25	GND	Ground
26	GND	Ground
27	VCC	5 volt supply
28	VCC	5 volt supply
29	RD/WR#	Connected to the R/W# signal of the S1D13705
30	BS#	Connected to the BS# signal of the S1D13705
31	BUSCLK	Connected to the BCLK signal of the S1D13705
32	RD#	Connected to the RD# signal of the S1D13705
33	NC	Not connected
34	CLKI	Connected to the CLKI signal of the S1D13705

5 Host Bus Interface Pin Mapping

Table 5-1: Host Bus Interface Pin Mapping

S1D13705 Pin Names	SH-3	SH-4	MC68K #1	MC68K #2	Generic Bus #1	Generic Bus #2
AB[16:1]	A[16:1]	A[16:1]	A[16:1]	A[16:1]	A[16:1]	A[16:1]
AB0	A0	A0	LDS#	A0	A0	A0
DB[15:0]	D[15:0]	D[15:0]	D[15:0]	D[15:0]	D[15:0]	D[15:0]
WE1#	WE1#	WE1#	UDS#	DS#	WE1#	BHE#
CS#	CSn#	CSn#	External Decode	External Decode	External Decode	External Decode
BCLK	CKIO	CKIO	BCLK	BCLK	BCLK	BCLK
BS#	BS#	BS#	AS#	AS#	Connect to V_{SS}	Connect to IO V_{DD}
RD/WR#	RD/WR#	RD/WR#	R/W#	R/W#	RD1#	Connect to IO V_{DD}
RD#	RD#	RD#	Connect to IO V_{DD}	SIZ1	RD0#	RD#
WE0#	WE0#	WE0#	Connect to IO V_{DD}	SIZ0	WE0#	WE#
WAIT#	WAIT#	RDY#	DTACK#	DSACK1#	WAIT#	WAIT#
RESET#	RESET#	RESET#	RESET#	RESET#	RESET#	RESET#

6 Technical Description

6.1 Embedded Memory Support

The S1D13705 contains 80K bytes of embedded, 16-bit, SRAM used for the display buffer and a 32 byte internal register set.

Since the S1D13705 does not distinguish between memory and register accesses, both the 80K byte display buffer and the 32 byte register set must be memory mapped into the host's memory space.

When using the S5U13705B00C board on an ISA bus system, the board can be configured to map the S1D13705 to one of two memory blocks.

The SRAM start address is determined by a DIP switch setting. See Table 2-1: "Configuration DIP Switch Settings," on page 6.

1. When switch S1-5 is in the closed position, the S1D13705 is mapped into segments 0C0000h and 0D0000h.

   This memory space is in the first 1M byte of ISA bus memory and should be used if these segments are not taken up by other devices such as network adapters, SCSI cards, or other peripherals.

Note
Since VGA and VGA compatible video adapters use address 0C8000, these cards cannot be used while using the S5U13705B00C board at this memory address. A monochrome display adapter, a terminal, or a non-VGA compatible display adapter must be used.

2. When switch S1-5 is in the open position, the S1D13705 is mapped into the upper megabyte of ISA bus memory, starting address of F00000h. To use this memory on an ISA bus system, the system BIOS has to be configured to set a memory 'hole' starting at this address. Some systems allow the user to configure the size of this hole and the starting address of where it begins while others just allow a 1M byte hole at the top of the 16M byte memory space. This memory hole is configured by entering the system CMOS Setup Utility. This memory space should be used if segments 0Dh and 0Eh are being used by other devices or if a VGA display adapter is needed.

Starting at the SRAM start address, the board design decodes a 128K byte segment accommodating both the 80K byte display buffer and the S1D13705 internal register set. The S1D13705 registers are mapped into the upper 32 bytes of the 128K byte segment (1FFE0h to 1FFFFh).

When using the S5U13705B00C board on a non-ISA bus system, system or external decode logic must map the S1D13705 into an appropriate memory space.

6.2 ISA Bus Support

The S5U13705B00C board has been designed to directly support the 16-bit ISA bus environment and can be used in conjunction with either a VGA or a monochrome display adapter card.

There are 4 configuration inputs associated with the Host Interface (CNF[2:0] and BS#). Refer to Table 2-3: "Jumper Settings," on page 7 and Table 5-1: "Host Bus Interface Pin Mapping," on page 11 for complete details.

6.2.1 Display Adapter Card Support

When using the S5U13705B00C in conjunction with another primary Display Adapter (VGA or Monochrome) the following applies:

VGA Display Adapter

All VGA display adapters can be used with the S5U13705B00C board if the S1D13705 is mapped to the upper 1M Byte of ISA bus memory, address F00000-F1FFFF. If the S1D13705 is mapped to the address range 0C0000-0D0000, then no VGA or VGA compatible display adapters can be used with the S5U13705B00C board. See Embedded Memory Support on page 12.

Monochrome Display Adapter

The S5U13705B00C board can be used with monochrome display adapters at both memory addresses.

6.2.2 Expanded Memory Manager Support

If a memory manager is being used for system memory, the address range selected for the SRAM start address must be excluded from use or memory conflicts will arise.

6.3 Non-ISA Bus Support

The S5U13705B00C board is specifically designed to support the standard 16-bit ISA bus. However, the S1D13705 directly supports many other host bus interfaces. Header strips H1 and H2 are provided and contain all the necessary IO pins to interface to these host buses. See CPU/Bus Interface Connector Pinouts on page 9; Table 2-1: "Configuration DIP Switch Settings," on page 6; and Table 2-3: "Jumper Settings," on page 7 for details.

When using the header strips to provide the bus interface observe the following:

- All signals on the ISA bus card edge must be isolated from the ISA bus (do not plug the card into a computer). Power must be provided through the headers.
- U7, a PLD of type 22V10-15, is used to provide the S1D13705 CS# (pin 74) and other decoding logic signals for ISA bus mode. For non-ISA applications, this functionality must be provided externally. Remove the PAL from its socket to eliminate conflicts driving S1D13705 control signals. Refer to Table 5-1: "Host Bus Interface Pin Mapping" for connection details.

Note
When using a 3.3V host bus interface, IO V_{DD} must be set to 3.3V by setting jumper (JP1) to the 2-3 position. Refer to Table 2-3: "Jumper Settings," on page 7.

6.4 Decoding Logic

All the required decode logic is provided through a PLD of type 22V10-15 (U7, socketed). This PAL contains the following equations.

```
!CS      = (Address >= ^hC0000) & (Address <= ^hDFFFF) & !ADDR & REFRESH & ENAB
         # (Address1 >= ^hF00000) & (Address1 <= ^hF1FFFF) & ADDR & REFRESH & ENAB;

!MEMCS16 = (Address1 >= ^h0C0000) & (Address1 <= ^h0DFFFF) & !ADDR & !CS
         # (Address1 >= ^hF00000) & (Address1 <= ^hF1FFFF) & ADDR & !CS;

!WE0     = (!CS & !ADDR & !SMEMW) # (!CS & ADDR & !MEMW);

!RD      = (!CS & !ADDR & !SMEMR) # (!CS & ADDR & !MEMR);
```

Note
ADDR = Switch S1-5 (see Table 2-1:, "Configuration DIP Switch Settings," on page 6).

6.5 Clock Input Support

The input clock (CLKI) frequency can be up to 50MHz for the S1D13705 if the internal clock divide-by-2 mode is set. If the clock divider is not used, the maximum CLKI frequency is 25MHz. There is no minimum input clock frequency.

A 25.0MHz oscillator (U2, socketed) is provided as the input clock source. However, depending on the LCD resolution , desired frame rate, and power consumtion budget, a lower frequency clock may be required.

6.6 LCD Panel Voltage Setting

The S5U13705B00C board supports both 3.3V and 5V LCD panels through the LCD connector J5. The voltage level is selected by setting jumper J4 to the appropriate position. Refer to Table 2-3: "Jumper Settings," on page 7 for setting this jumper.

Although not necessary for signal buffering, buffers have been implemented in the board design to provide flexibility in handling 3 and 5 volt panels.

6.7 Monochrome LCD Panel Support

The S1D13705 directly supports 4 and 8-bit, dual and single, monochrome passive LCD panels. All necessary signals are provided on the 40-pin ribbon cable header J5. The interface signals on the cable are alternated with grounds to reduce crosstalk and noise.

Refer to Table 3-1: "LCD Signal Connector (J5) Pinout," on page 8 for specific connection information.

6.8 Color Passive LCD Panel Support

The S1D13705 directly supports 4 and 8-bit, dual and single, color passive LCD panels. All the necessary signals are provided on the 40-pin ribbon cable header J5. The interface signals on the cable are alternated with grounds to reduce crosstalk and noise.

Refer to Table 3-1: "LCD Signal Connector (J5) Pinout," on page 8 for specific connection information.

6.9 Color TFT/D-TFD LCD Panel Support

The S1D13705 directly supports 9 and 12-bit active matrix color TFT/D-TFD panels. All the necessary signals can also be found on the 40-pin LCD connector J5. The interface signals on the cable are alternated with grounds to reduce crosstalk and noise.

Refer to Table 3-1: "LCD Signal Connector (J5) Pinout," on page 8 for connection information.

6.10 Power Save Modes

The S1D13705 supports hardware and software power save modes. These modes are controlled by the utility 13705PWR. The hardware power save mode needs to be enabled by 13705PWR and then activated by DIP switch S1-6. See Table 2-1: "Configuration DIP Switch Settings," on page 6 for details on setting this switch.

6.11 Adjustable LCD Panel Negative Power Supply

For those LCD panels requiring a negative power supply to provide between -23V and -14V (I_{out}=25mA) a power supply has been provided as an integral part of this design. The VLCD power supply can be adjusted by R21 to give an output voltage from -23V to -14V, and is enabled and disabled by the active high S1D13705 control signal LCDPWR, inverted externally.

Determine the panel's specific power requirements and set the potentiometer accordingly before connecting the panel.

6.12 Adjustable LCD Panel Positive Power Supply

For those LCD panels requiring a positive power supply to provide between +23V and +40V (I_{out}=45mA) a power supply has been provided as an integral part of this design. The VDDH power supply can be adjusted by R15 to provide an output voltage from +23V to +40V and is enabled and disabled by the active high S1D13705 control signal LCDPWR, inverted externally.

Determine the panel's specific power requirements and set the potentiometer accordingly before connecting the panel.

6.13 CPU/Bus Interface Header Strips

All of the CPU/Bus interface pins of the S1D13705 are connected to the header strips H1 and H2 for easy interface to a CPU/Bus other than ISA.

Refer to Table 4-1: "CPU/BUS Connector (H1) Pinout," on page 9 and Table 4-2: "CPU/BUS Connector (H2) Pinout," on page 10 for specific settings.

Note

These headers only provide the CPU/bus interface signals from the S1D13705. When another host bus interface is selected by CNF[3:0] and BS#, appropriate external decoding logic MUST be used to access the S1D13705. Refer to Table 5-1: "Host Bus Interface Pin Mapping," on page 11 for connection details.

7 Parts List

Item #	Qty/board	Designation	Part Value	Description
1	15	C1-C11, C15-17,C24	0.1uF, 20%, 50V	0805 ceramic capacitor
2	3	C12-14	10uF, 10%, 25V	Tantalum capacitor size D
3	2	C18, C22	47uF, 10%, 16V	Tantalum capacitor size D
4	3	C19-C21	4.7uF, 10%, 50V	Tantalum capacitor size D
5	1	C23	56uF, 20%, 63V	Electrolytic, radial, low ESR
6	2	H1,H2	CON34A Header	0.1” 17x2 header, PTH
7	5	JP1-JP4, JP6	HEADER 3	0.1” 1x3 header, PTH
8	1	J1	AT CON-A	ISA Bus gold fingers
9	1	J2	AT CON-B	ISA Bus gold fingers
10	1	J3	AT CON-C	ISA Bus gold fingers
11	1	J4	AT CON-D	ISA Bus gold fingers
12	1	J5	CON40A	Shrouded header 2x20, PTH, center key
13	1	L1	1µH	MCI-1812 inductor
14	2	L3, L4	Ferrite bead	Philips BDS3/3/8.9-4S2
15	1	Q1	2N3906	PNP signal transistor, SOT23
16	1	Q2	2N3904	NPN signal transistor, SOT23
17	6	R1-R6	15K, 5%	0805 resistor
18	9	R7-R13, R17, R18	10K, 5%	0805 resistor
19	1	R14	475K, 1%	0805 resistor
20	1	R15	200K Pot.	200K Trim POT Spectrol 63S204T607 (or equivalent)
21	1	R16	14K, 1%	0805 resistor
22	3	R19, R20, R22	100K, 5%	0805 resistor
23	1	R21	100K Pot.	100K Trim POT Spectrol 63S104T607 (or equivalent)
24	1	S1	SW DIP-6	6 position DIP switch
25	1	U1	S1D13705F00A	QFP14-80, 80 pin, SMT
26	1	U2	25.0 MHz oscillator	FOX 25MHz oscillator or equiv., 14 pin DIP socketed
27	3	U3-U5	74AHC244	SO-22, TI74AHC244
28	1	U6	LT1117CM-3.3	Linear Technology 5V to 3.3V regulator, 800mA
29	1	U7	PLD22V10-15	PLD type 22V10-15, 20 Pin DIP, socketed
30	1	U8	74ALS125	SO-14, 74ALS125
31	1	U9	74HCT04	SO-14, 74HCT04
32	1	U10	RD-0412	Xentek RD-0412, positive PS
33	1	U11	EPN001	Xentek EPN001 negative PS

8 Schematic Diagrams

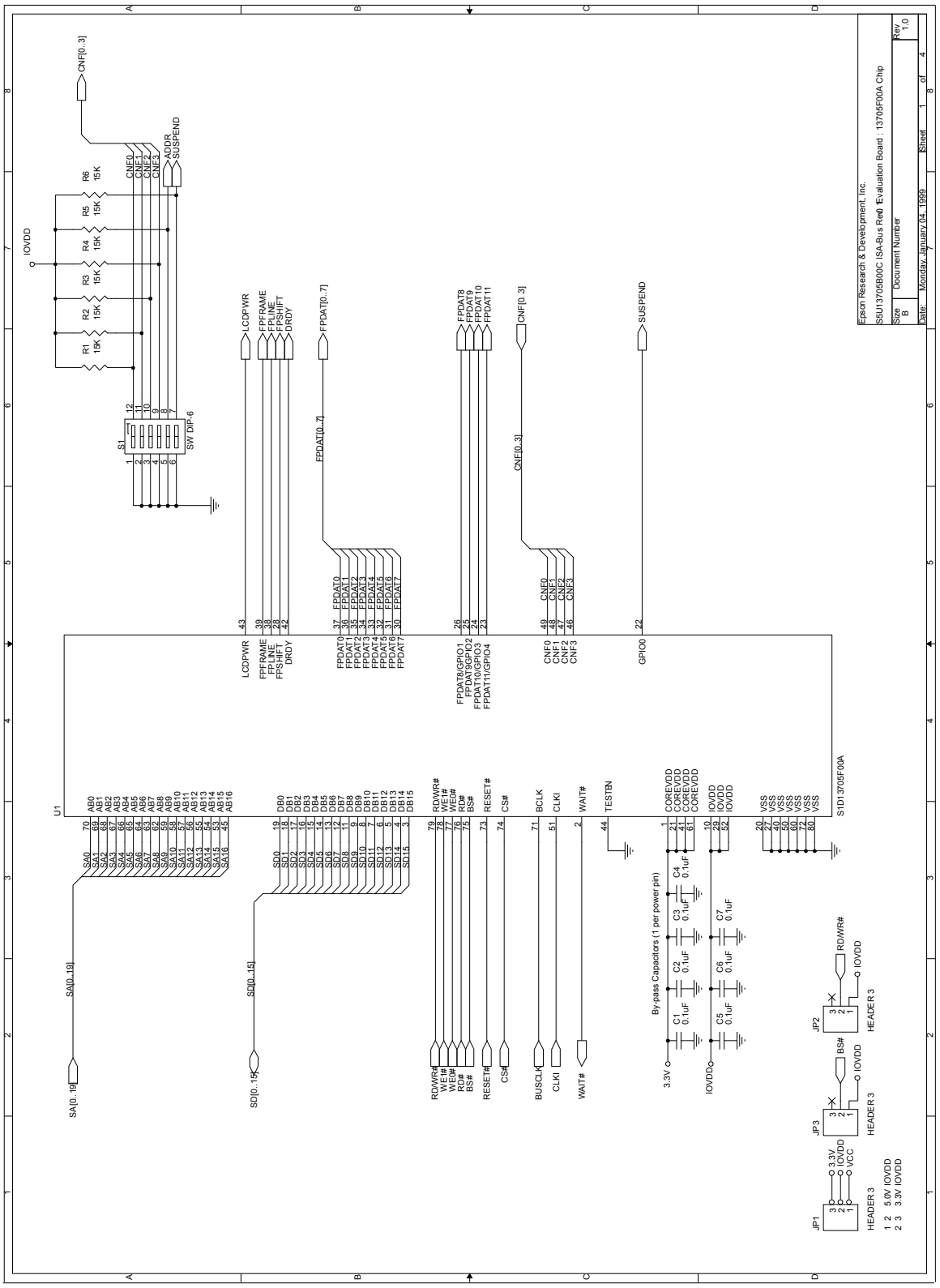

Figure 8-1: S1D13705B00C Schematic Diagram (1 of 4)

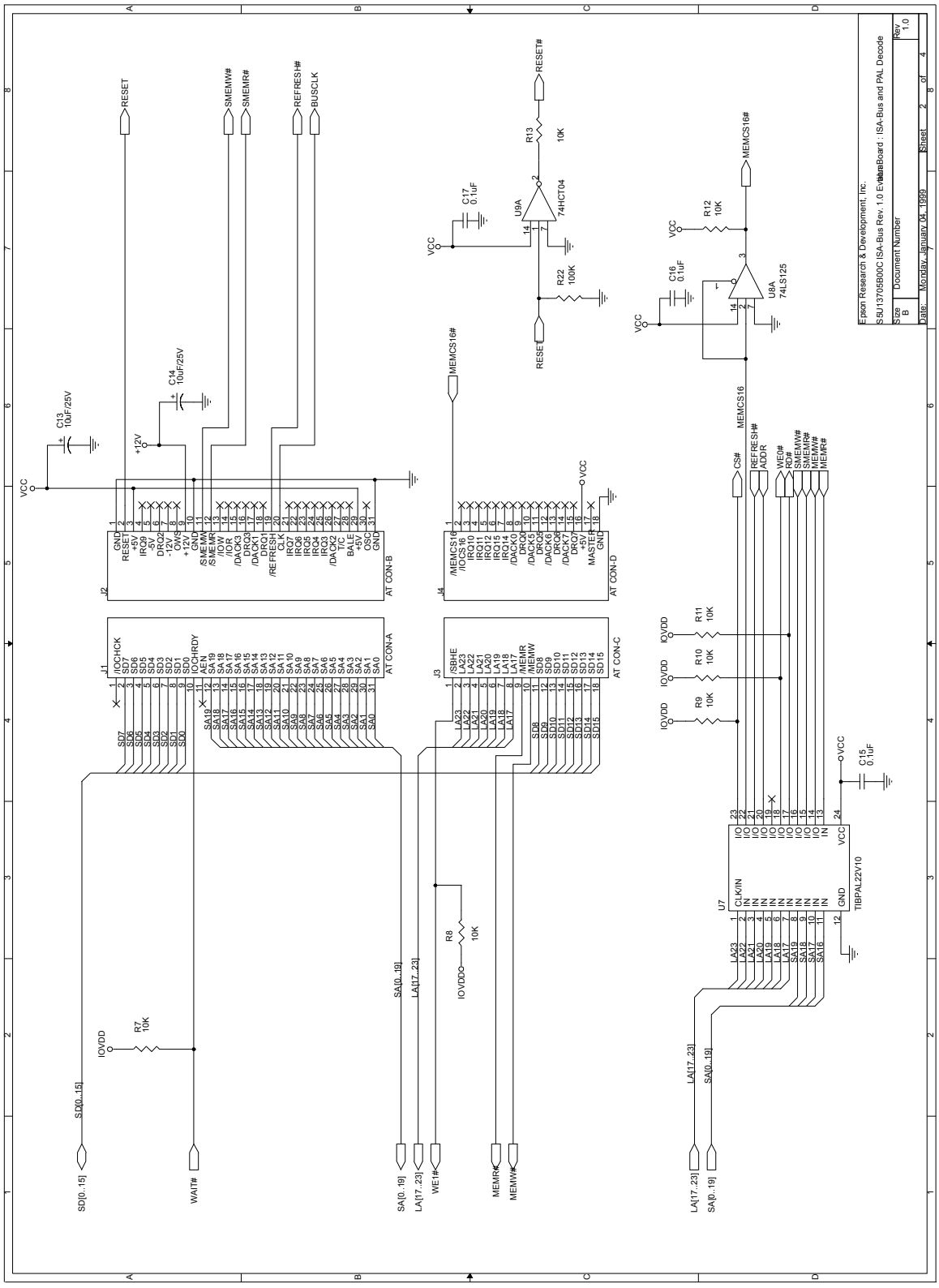

Figure 8-2: S1D13705B00C Schematic Diagram (2 of 4)

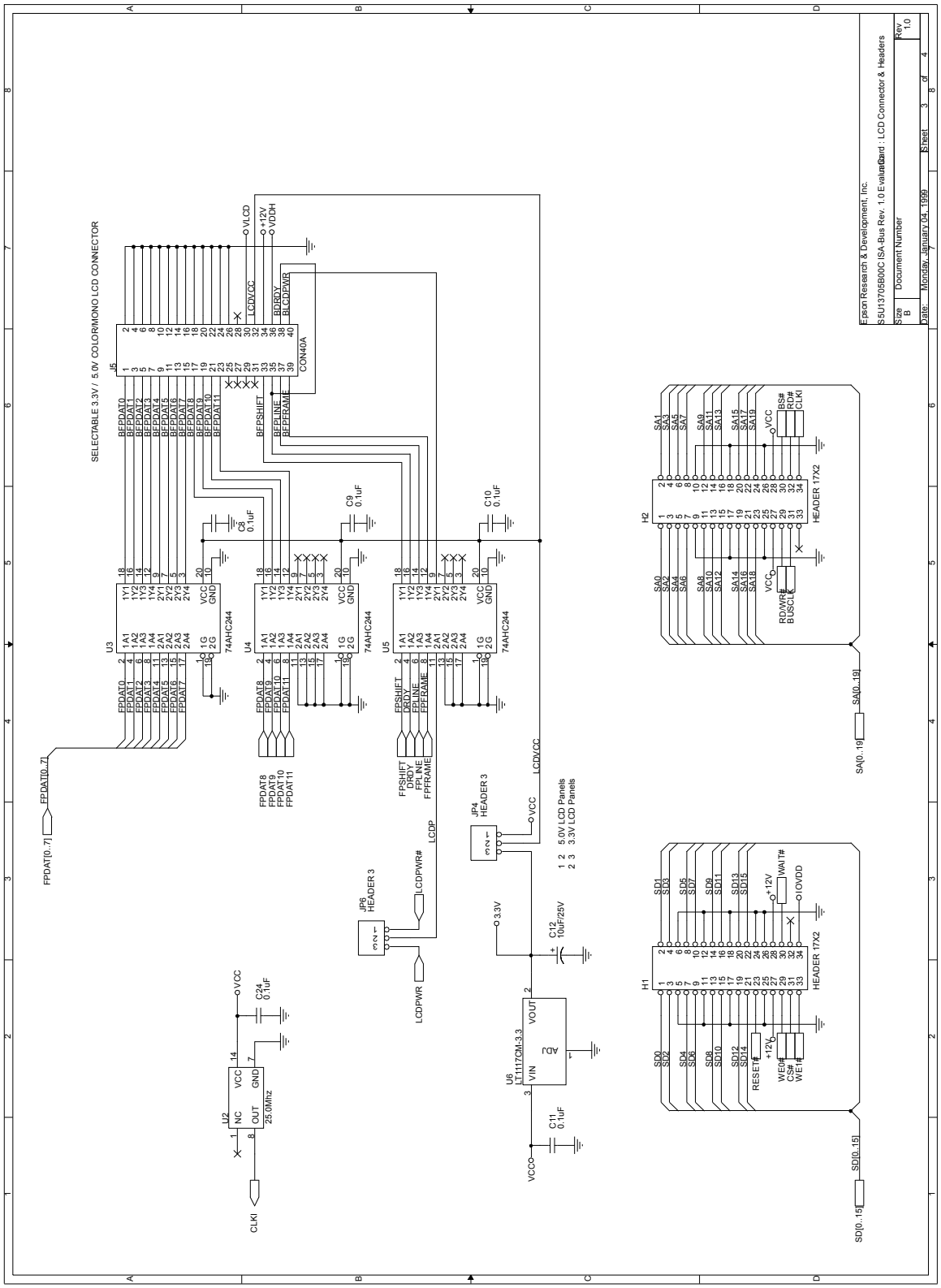

Figure 8-3: S1D13705B00C Schematic Diagram (3 of 4)

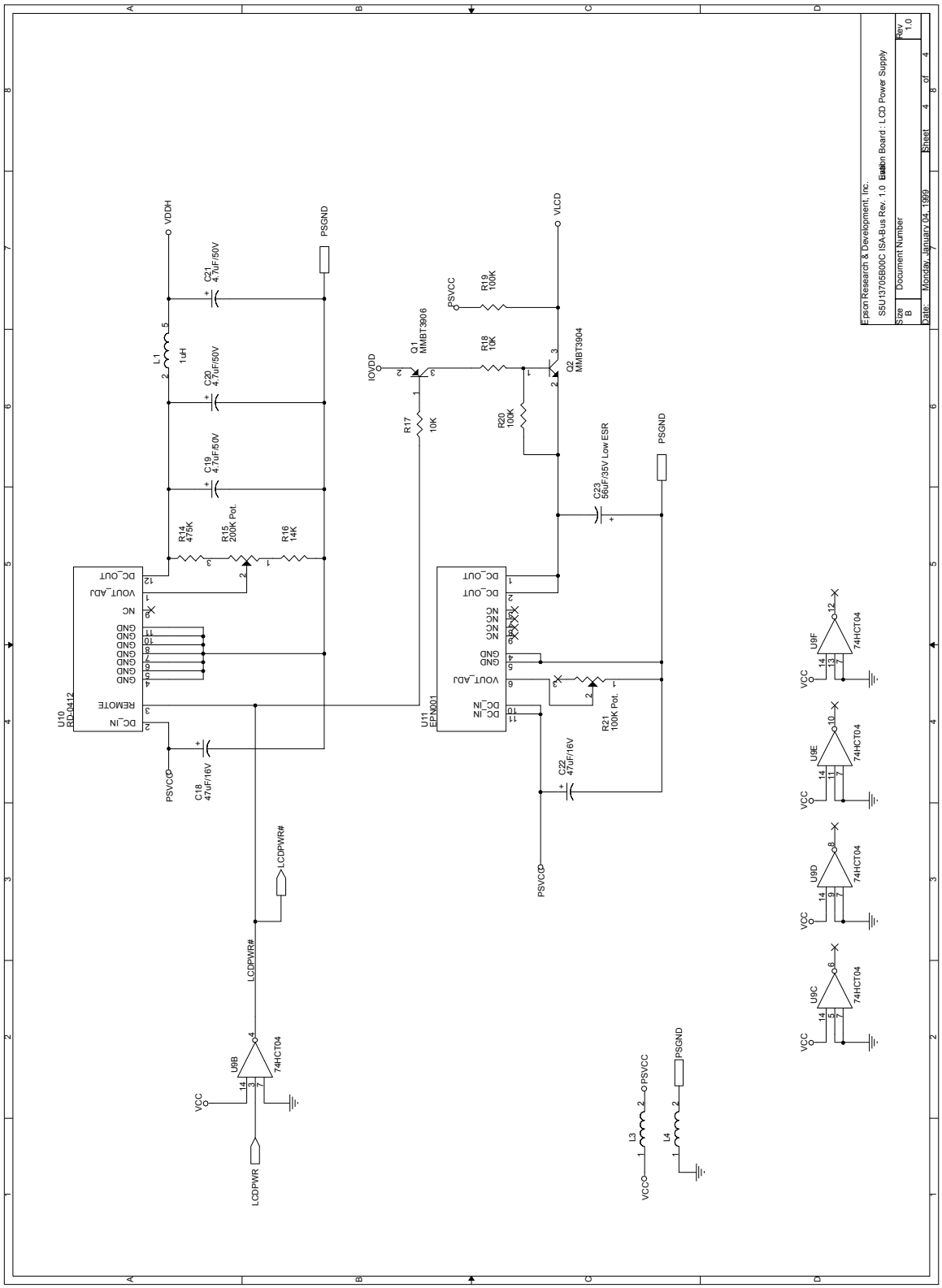

Figure 8-4: S1D13705B00C Schematic Diagram (4 of 4)

9 Change Record

X27A-G-005-03 Revision 3.1 - Issued: March 26, 2018

- updated Sales and Technical Support Section
- updated some formatting

10 Sales and Technical Support

For more information on Epson Display Controllers, visit the Epson Global website.

https://global.epson.com/products_and_drivers/semicon/products/display_controllers/

For Sales and Technical Support, contact the Epson representative for your region.

https://global.epson.com/products_and_drivers/semicon/information/support.html