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S1D13705 Embedded Memory LCD Controller

Hardware Functional Specification

Document Number: X27A-A-001-10.3

SEIKO EPSON CORPORATION

Rev. 10.3

NOTICE

Table of Contents

1 Introduction

1.1 Scope

This is the Hardware Functional Specification for the S1D13705 Embedded Memory LCD Controller Chip. Included in this document are timing diagrams, AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Video Subsystem Designers and Software Developers.

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1.2 Overview Description

The S1D13705 is a color / monochrome LCD graphics controller with an embedded 80K byte SRAM display buffer. The high integration of the S1D13705 provides a low cost, low power, single chip solution to meet the requirements of embedded markets such as Office Automation equipment, Mobile Communications devices, and Hand-Held PCs where board size and battery life are major concerns.

Products requiring a “Portrait” display can take advantage of the SwivelView™ Mode feature of the S1D13705. Virtual and Split Screen are just some of the display modes supported. The above features, combined with the Operating System independence of the S1D13705, make it the ideal solution for a wide variety of applications.

2 Features

2.1 Integrated Frame Buffer

- Embedded 80K byte SRAM display buffer.

2.2 CPU Interface

- Direct support of the following interfaces:
  Hitachi SH-3.
  Hitachi SH-4.
  Motorola M68K.
  MPU bus interface using WAIT# signal.
- Direct memory mapping of internal registers.
- Single level CPU write buffer.
- Registers are mapped into upper 32 bytes of 128K byte address space.
- The complete 80K byte display buffer is directly and contiguously available through the 17-bit address bus.

2.3 Display Support

- 4/8-bit monochrome LCD interface.
- 4/8-bit color LCD interface.
- Single-panel, single-drive passive displays.
- Dual-panel, dual-drive passive displays.
- Active Matrix TFT / D-TFD interface
- Register level support for EL panels.
- Example resolutions:
  640x480 at a color depth of 2 bpp
  640x240 at a color depth of 4 bpp
  320x240 at a color depth of 8 bpp

2.4 Display Modes

- SwivelView™: direct 90° hardware rotation of display image for portrait mode display
- 1/2/4 bit-per-pixel (bpp), 2/4/16-level grayscale display.
- 1/2/4/8 bit-per-pixel, 2/4/16/256-level color display.
- Up to 16 shades of gray by FRM on monochrome passive LCD panels; a 256x4 Look-Up Table is used to map 1/2/4 bpp modes into these shades.
- 256 simultaneous of 4096 colors on color passive and active matrix LCD panels; three 256x4 Look-Up Tables are used to map 1/2/4/8 bpp modes into these colors.
- Split screen display for all landscape panel modes allows two different images to be simultaneously displayed.
- Virtual display support (displays images larger than the panel size through the use of panning).

2.5 Clock Source

- Maximum operating clock (CLK) frequency of 25MHz.
- Operating clock (CLK) is derived from CLKI input.
  CLK = CLKI
  or
  CLK = CLKI/2
- Pixel Clock (PCLK) and Memory Clock (MCLK) are derived from CLK.

2.6 Miscellaneous

- Hardware/Software Video Invert.
- Software Power Save mode.
- Hardware Power Save mode.
- LCD power-down sequencing.
- 5 General Purpose Input/Output pins are available.
  - GPIO0 is available if Hardware Power Save is not required.
  - GPIO[4:1] are available if upper LCD data pins (FPDAT[11:8]) are not required for TFT/D-TFD support or hardware inverse video.
- Core operates from 2.7 volts to 3.6 volts.
- IO Operates from the core voltage up to 5.5 volts.

2.7 Package

- 80 pin QFP14 package.

3 Typical System Implementation Diagrams

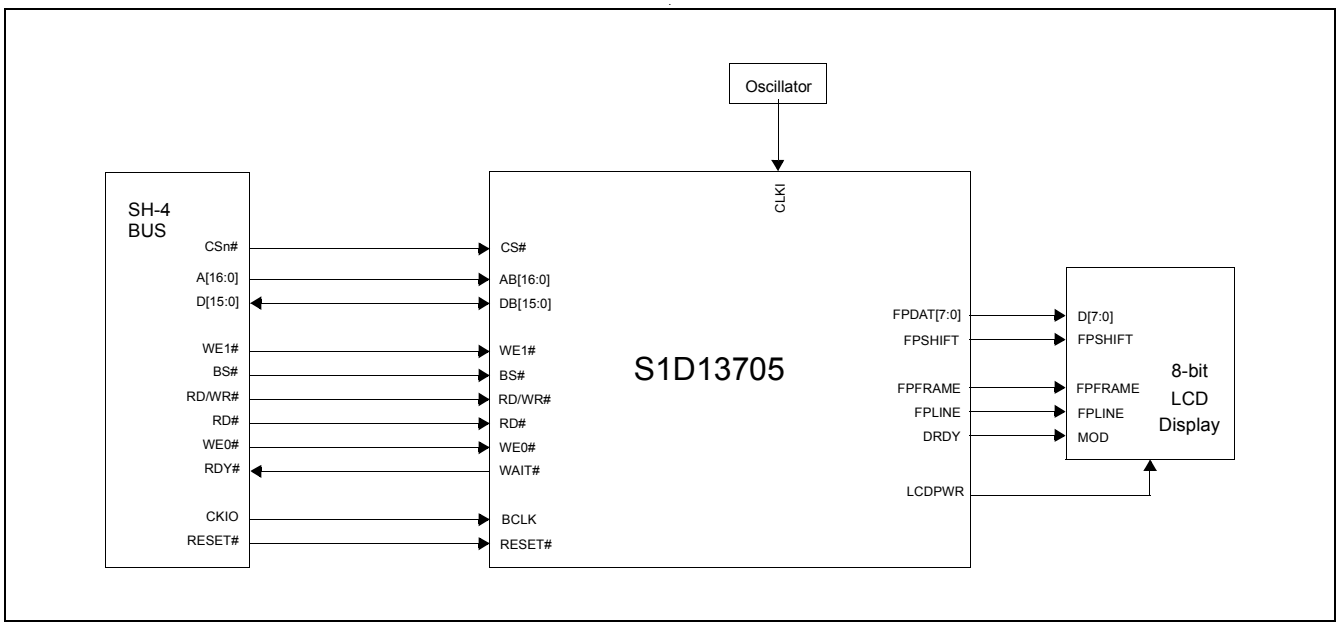


Figure 3-1: Typical System Diagram (SH-4 Bus)

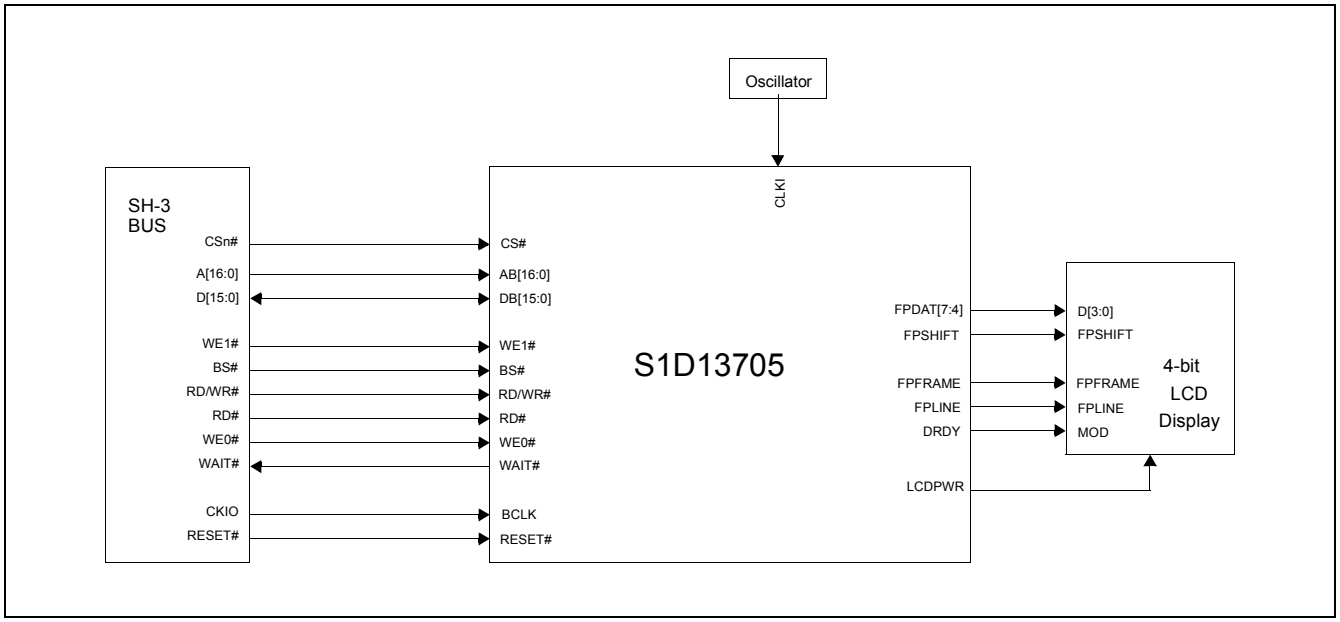


Figure 3-2: Typical System Diagram (SH-3 Bus)

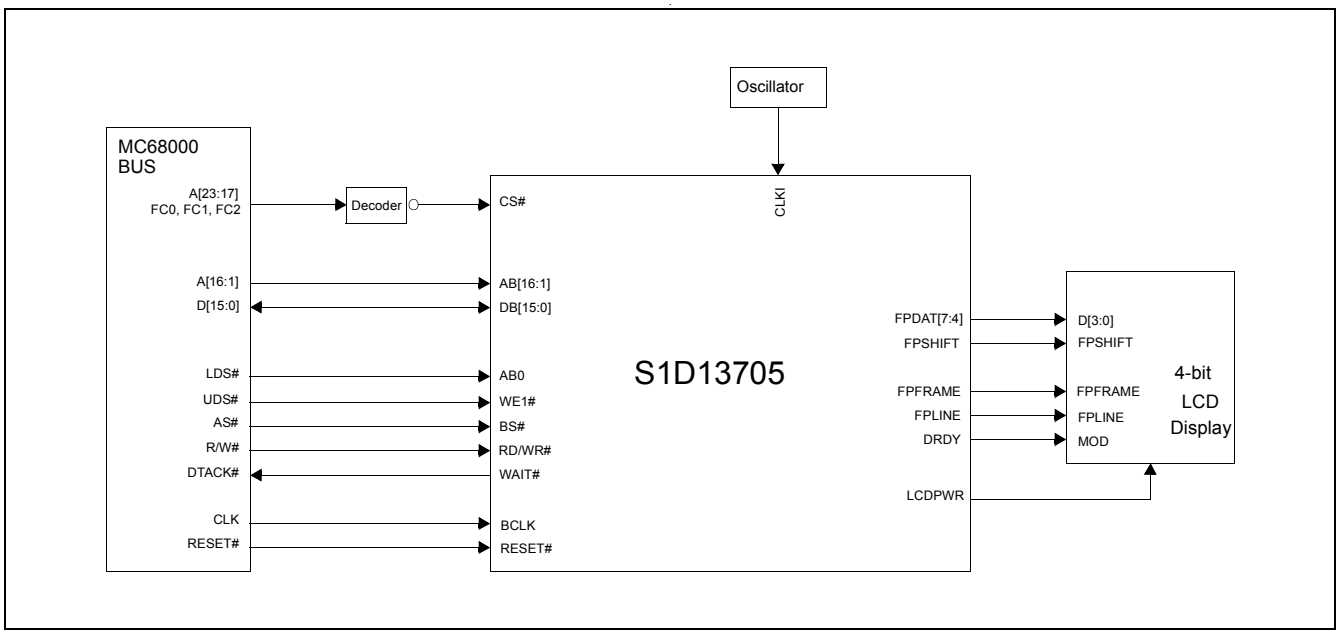


Figure 3-3: Typical System Diagram (M68K #1 Bus)

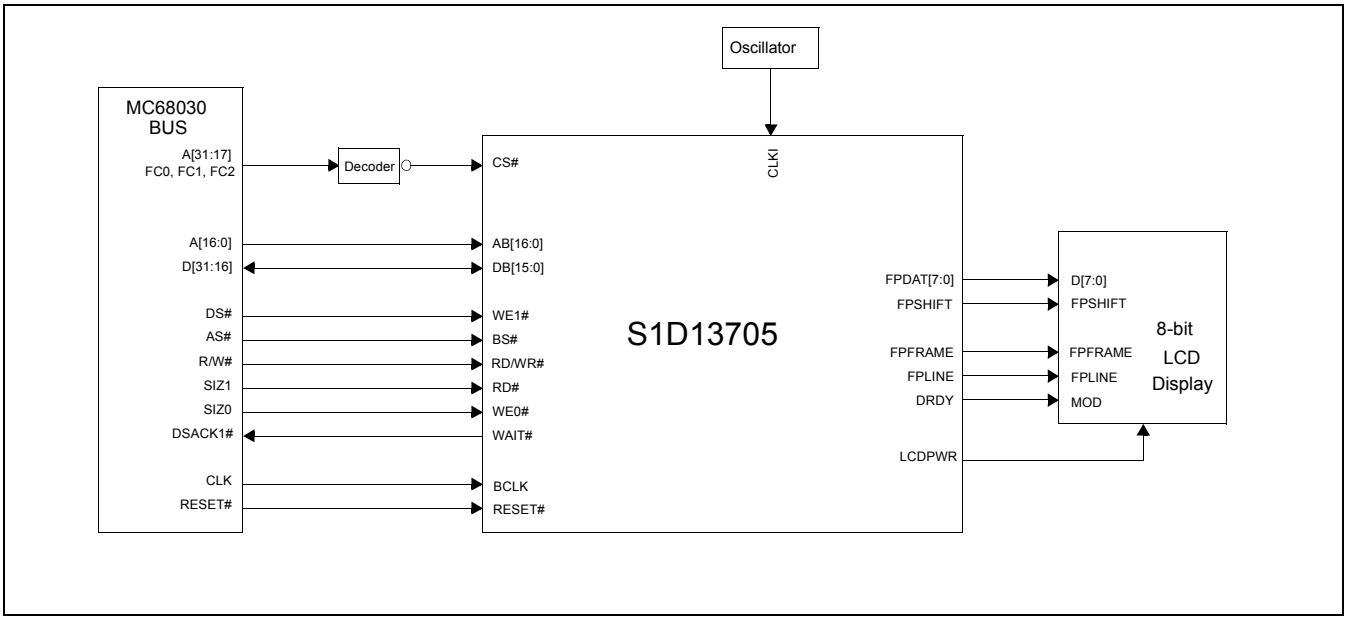


Figure 3-4: Typical System Diagram (M68K #2 Bus)

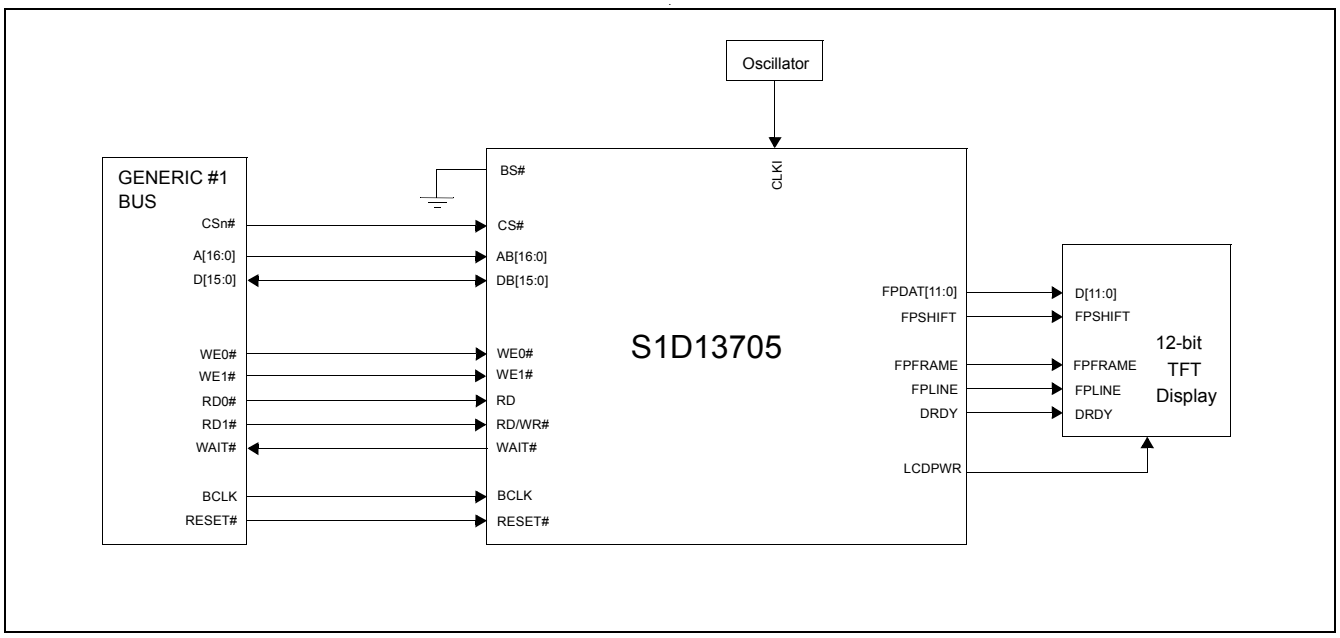


Figure 3-5: Typical System Diagram (Generic #1 Bus)

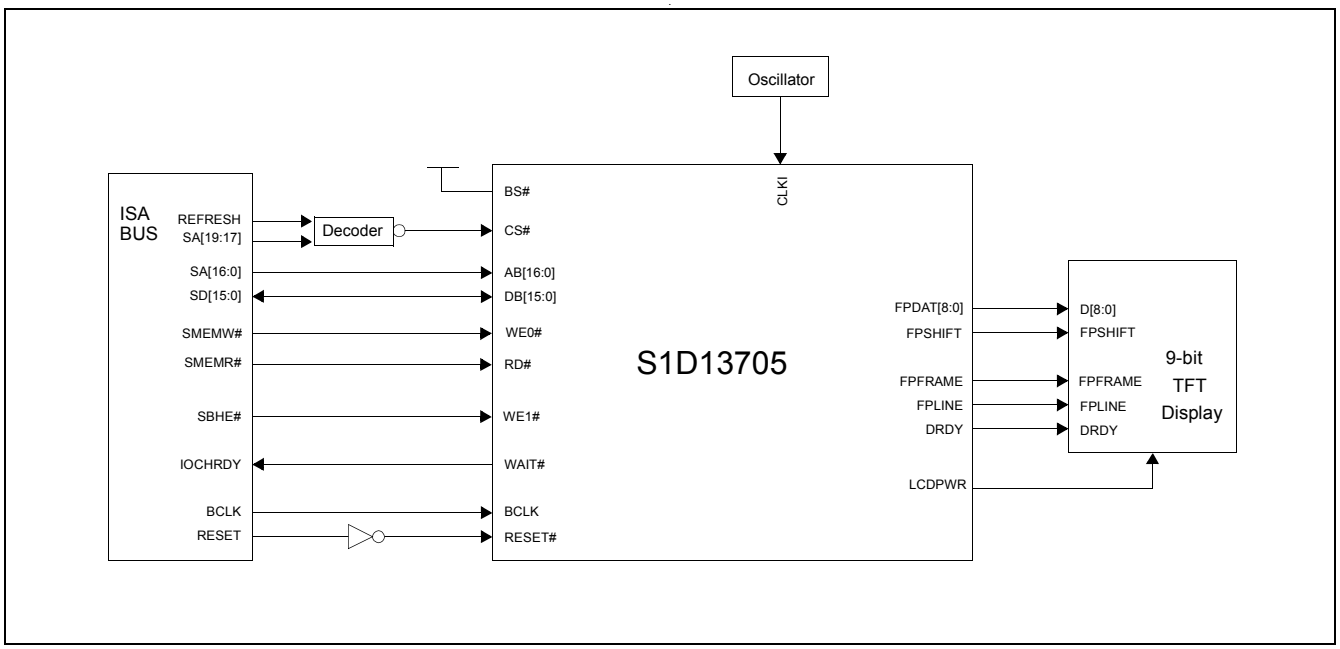


Figure 3-6: Typical System Diagram (Generic #2 Bus - e.g. ISA Bus)

4 Functional Block Diagram

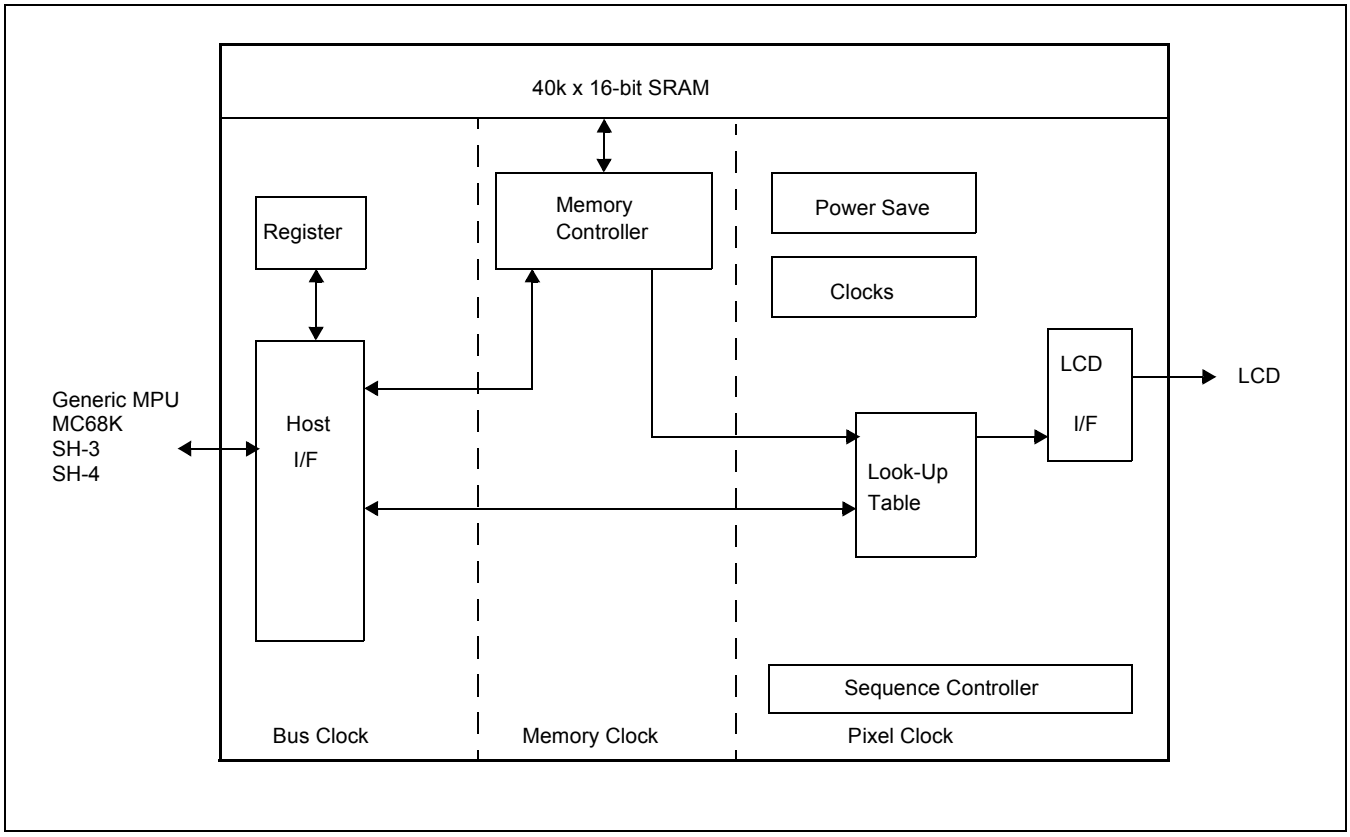


Figure 4-1: System Block Diagram Showing Data Paths

4.1 Functional Block Descriptions

4.1.1 Host Interface

The Host Interface provides the means for the CPU/MPU to communicate with the display buffer and internal registers.

4.1.2 Memory Controller

The Memory Controller arbitrates between CPU accesses and display refresh accesses. It also generates the necessary signals to control the SRAM frame buffer.

4.1.3 Sequence Controller

The Sequence Controller controls data flow from the Memory Controller through the Look-Up Table and to the LCD Interface. It also generates memory addresses for display refresh accesses.

4.1.4 Look-Up Table

The Look-Up Table contains three 256x4 Look-Up Tables or palettes, one for each primary color. In monochrome mode only the green Look-Up Table is used.

4.1.5 LCD Interface

The LCD Interface performs frame rate modulation for passive LCD panels. It also generates the correct data format and timing control signals for various LCD and TFT/D-TFD panels.

4.1.6 Power Save

Power Save contains the power save mode circuitry.

5 Pins

5.1 Pinout Diagram

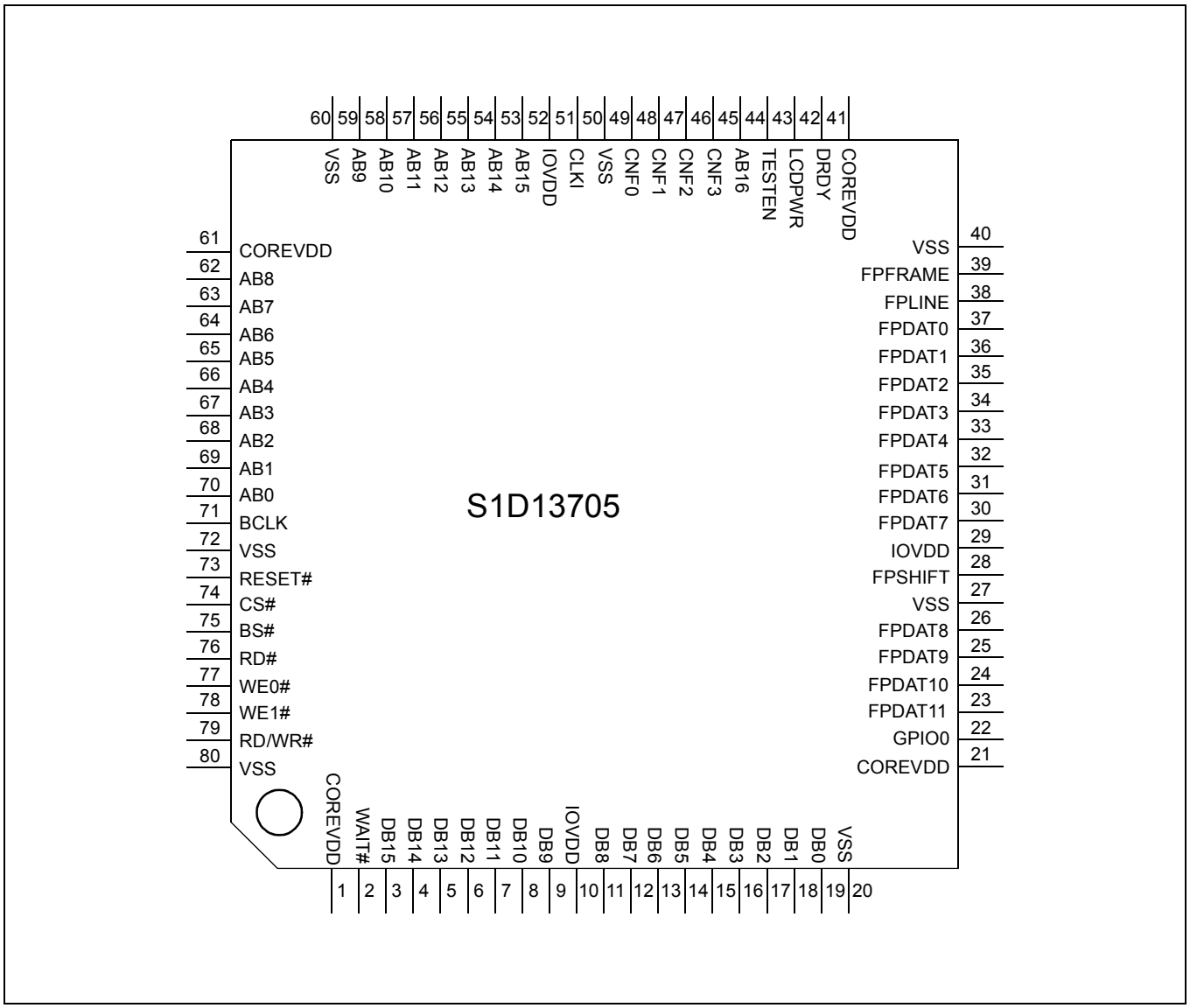


Figure 5-1: Pinout Diagram

Note

Package type: 80 pin surface mount QFP14

5.2 Pin Description

Key:

I	=	Input
O	=	Output
IO	=	Bi-Directional (Input/Output)
P	=	Power pin
C	=	CMOS level input
CS	=	CMOS level Schmitt input
COx	=	CMOS output driver, x denotes driver type (see I_{OL}/I_{OH} in Table 6-4: "Output Specifications," on page 23)
TSx	=	Tri-state CMOS output driver, x denotes driver type (see I_{OL}/I_{OH} in Table 6-4: "Output Specifications," on page 23)
CNx	=	CMOS low-noise output driver, x denotes driver type (see I_{OL}/I_{OH} in Table 6-4: "Output Specifications," on page 23)
TEST	=	CMOS level test input with pull down resistor

5.2.1 Host Interface

Pin Names	Type	Pin #	Cell	RESET# State	Description
AB0	I	70	CS	Input	This pin has multiple functions. • For SH-3/SH-4 mode, this pin inputs system address bit 0 (A0). • For MC68K #1, this pin inputs the lower data strobe (LDS#). • For MC68K #2, this pin inputs system address bit 0 (A0). • For Generic #1, this pin inputs system address bit 0 (A0). • For Generic #2, this pin inputs system address bit 0 (A0). See Table 5-2: "Host Bus Interface Pin Mapping," on page 20 for summary.
AB[16:1]	I	45, 53, 54, 55, 56, 57, 58, 59, 62, 63, 64, 65, 66, 67, 68, 69	C	Input	These pins input the system address bits 16 through 1 (A[16:1]).
DB[15:0]	IO	3, 4, 5, 6, 7, 8, 9, 11, 12, 13, 14, 15, 16, 17, 18, 19	C/TS2	Hi-Z	These pins have multiple functions. • For SH-3/SH-4 mode, these pins are connected to [D15:0]. • For MC68K #1, these pins are connected to D[15:0]. • For MC68K #2, these pins are connected to D[31:16] for a 32-bit device (e.g. MC68030) or D[15:0] for a 16-bit device (e.g. MC68340). • For Generic #1, these pins are connected to D[15:0]. • For Generic #2, these pins are connected to D[15:0]. See Table 5-2: "Host Bus Interface Pin Mapping," on page 20 for summary.

Pin Names	Type	Pin #	Cell	RESET# State	Description
WE0#	I	77	CS	Input	This pin has multiple functions. • For SH-3/SH-4 mode, this pin inputs the write enable signal for the lower data byte (WE0#). • For MC68K #1, this pin must be tied to IO V_{DD} • For MC68K #2, this pin inputs the bus size bit 0 (SIZ0). • For Generic #1, this pin inputs the write enable signal for the lower data byte (WE0#). • For Generic #2, this pin inputs the write enable signal (WE#) See Table 5-2: “Host Bus Interface Pin Mapping,” on page 20 for summary.
WE1#	I	78	CS	Input	This pin has multiple functions. • For SH-3/SH-4 mode, this pin inputs the write enable signal for the upper data byte (WE1#). • For MC68K #1, this pin inputs the upper data strobe (UDS#). • For MC68K #2, this pin inputs the data strobe (DS#). • For Generic #1, this pin inputs the write enable signal for the upper data byte (WE1#). • For Generic #2, this pin inputs the byte enable signal for the high data byte (BHE#). See Table 5-2: “Host Bus Interface Pin Mapping,” on page 20 for summary.
CS#	I	74	C	Input	This pin inputs the chip select signal.
BCLK	I	71	C	Input	This pin inputs the system bus clock.
BS#	I	75	CS	Input	This pin has multiple functions. • For SH-3/SH-4 mode, this pin inputs the bus start signal (BS#). • For MC68K #1, this pin inputs the address strobe (AS#). • For MC68K #2, this pin inputs the address strobe (AS#). • For Generic #1, this pin must be tied to V_{SS}. • For Generic #2, this pin must be tied to IO V_{DD}. See Table 5-2: “Host Bus Interface Pin Mapping,” on page 20 for summary.
RD/WR#	I	79	CS	Input	This pin has multiple functions. • For SH-3/SH-4 mode, this pin inputs the RD/WR# signal. The S1D13705 needs this signal for early decode of the bus cycle. • For MC68K #1, this pin inputs the R/W# signal. • For MC68K #2, this pin inputs the R/W# signal. • For Generic #1, this pin inputs the read command for the upper data byte (RD1#). • For Generic #2, this pin must be tied to IO V_{DD}. See Table 5-2: “Host Bus Interface Pin Mapping,” on page 20 for summary.

Pin Names	Type	Pin #	Cell	RESET# State	Description
RD#	I	76	CS	Input	This pin has multiple functions. • For SH-3/SH-4 mode, this pin inputs the read signal (RD#). • For MC68K #1, this pin must be tied to IO V_{DD}. • For MC68K #2, this pin inputs the bus size bit 1 (SIZ1). • For Generic #1, this pin inputs the read command for the lower data byte (RD0#). • For Generic #2, this pin inputs the read command (RD#). See Table 5-2: “Host Bus Interface Pin Mapping,” on page 20 for summary.
WAIT#	O	2	TS2	Hi-Z	This pin has multiple functions. • For SH-3 mode, this pin outputs the wait request signal (WAIT#). • For SH-4 mode, this pin outputs the device ready signal (RDY#). • For MC68K #1, this pin outputs the data transfer acknowledge signal (DTACK#). • For MC68K #2, this pin outputs the data transfer and size acknowledge bit 1 (DSACK1#). • For Generic #1, this pin outputs the wait signal (WAIT#). • For Generic #2, this pin outputs the wait signal (WAIT#). See Table 5-2: “Host Bus Interface Pin Mapping,” on page 20 for summary.
RESET#	I	73	CS	0	Active low input to set all internal registers to the default state and to force all signals to their inactive states.

5.2.2 LCD Interface

Pin Name	Type	Pin #	Cell	RESET# State	Description
FPDAT[7:0]	O	30, 31, 32, 33, 34, 35, 36, 37	CN3	0	Panel Data
FPDAT[10:8]	O, IO	24, 25, 26	CN3	Input	These pins have multiple functions. • Panel Data bits [10:8] for TFT/D-TFD panels. • General Purpose Input/Output pins GPIO[3:1]. These pins should be connected to IO V_{DD} when unused. See Table 5-3: “LCD Interface Pin Mapping,” on page 21 for summary.
FPDAT11	O, IO	23	CN3	Input	This pin has multiple functions. • Panel Data bit 11 for TFT/D-TFD panels. • General Purpose Input/Output pin GPIO4. • Inverse Video select pin. This pin should be connected to IO V_{DD} when unused. See Table 5-3: “LCD Interface Pin Mapping,” on page 21 for summary.
FPFRAME	O	39	CN3	0	Frame Pulse
FPLINE	O	38	CN3	0	Line Pulse
FPSHIFT	O	28	CN3	0	Shift Clock
LCDPWR	O	43	CO1	0	Active high LCD Power Control
DRDY	O	42	CN3	0	This pin has multiple functions. • TFT/D-TFD Display Enable (DRDY). • LCD Backplane Bias (MOD). • Second Shift Clock (FPSHIFT2). See Table 5-3: “LCD Interface Pin Mapping,” on page 21 for summary.

5.2.3 Clock Input

Pin Name	Type	Pin #	Driver	Description
CLKI	I	51	C	Input Clock

5.2.4 Miscellaneous

Pin Name	Type	Pin #	Cell	RESET# State	Description
CNF[3:0]	I	46, 47, 48, 49	C	As set by hardware	These inputs are used to configure the S1D13705 - see Table 5-1: “Summary of Power On/Reset Options,” on page 19. Must be connected directly to IO V_{DD} or V_{SS}.
GPIO0	IO, I	22	CS/ TS1	Input	This pin has multiple functions - see REG[03h] bit 2. • General Purpose Input/Output pin. • Hardware Power Save.
TESTEN	I	44	TEST	pulled low	Test Enable input. This input must be connected to V_{SS}.

5.2.5 Power Supply

Pin Name	Type	Pin #	Driver	Description
COREVDD	P	1, 21, 41, 61	P	Core V_{DD}
IOVDD	P	10, 29, 52	P	IO V_{DD}
VSS	P	20, 27, 40, 50, 60, 72, 80	P	Common V_{SS}

5.3 Summary of Configuration Options

Table 5-1: Summary of Power On/Reset Options

Configuration Pin	Power On/Reset State					
CNF[3:0]	Select host bus interface as follows:					
	CNF3	**CNF2**	**CNF1**	**CNF0**	**BS#**	**Host Bus**
	1	0	0	0	X	SH-4 interface Big Endian
	0	0	0	0	X	SH-4 interface Little Endian
	1	0	0	1	X	SH-3 interface Big Endian
	0	0	0	1	X	SH-3 interface Little Endian
	X	0	1	0	X	reserved
	1	0	1	1	X	MC68K #1, 16-bit Big Endian
	0	0	1	1	X	reserved
	X	1	0	0	X	reserved
	1	1	0	1	X	MC68K #2, 16-bit Big Endian
	0	1	0	1	X	reserved
	X	1	1	0	0	reserved
	X	1	1	0	1	reserved
	1	1	1	1	0	Generic #1, 16-bit Big Endian
	0	1	1	1	0	Generic #1, 16-bit Little Endian
	1	1	1	1	1	reserved
	0	1	1	1	1	Generic #2, 16-bit Little Endian

5.4 Host Bus Interface Pin Mapping

Table 5-2: Host Bus Interface Pin Mapping

S1D13705 Pin Names	SH-3	SH-4	MC68K #1	MC68K #2	Generic #1	Generic #2
AB[16:1]	A[16:1]	A[16:1]	A[16:1]	A[16:1]	A[16:1]	A[16:1]
AB0	A0	A0	LDS#	A0	A0	A0
DB[15:0]	D[15:0]	D[15:0]	D[15:0]	D[31:16]	D[15:0]	D[15:0]
WE1#	WE1#	WE1#	UDS#	DS#	WE1#	BHE#
CS#	CSn#	CSn#	External Decode	External Decode	External Decode	External Decode
BCLK	CKIO	CKIO	CLK	CLK	BCLK	BCLK
BS#	BS#	BS#	AS#	AS#	connect to V_{SS}	connect to IO V_{DD}
RD/WR#	RD/WR#	RD/WR#	R/W#	R/W#	RD1#	connect to IO V_{DD}
RD#	RD#	RD#	connect to IO V_{DD}	SIZ1	RD0#	RD#
WE0#	WE0#	WE0#	connect to IO V_{DD}	SIZ0	WE0#	WE#
WAIT#	WAIT#	RDY#	DTACK#	DSACK1#	WAIT#	WAIT#
RESET#	RESET#	RESET#	RESET#	RESET#	RESET#	RESET#

5.5 LCD Interface Pin Mapping

Table 5-3: LCD Interface Pin Mapping

S1D13705 Pin Name	Monochrome Passive Panel			Color Passive Panel				Color TFT/D-TFD	
	4-bit Single	8-bit Single	8-bit Dual	4-bit Single	8-bit Single Format 1	8-bit Single Format 2	8-bit Dual	9-bit	12-bit
FPFRAME	FPFRAME								
FPLINE	FPLINE								
FPSHIFT	FPSHIFT								
DRDY	MOD	MOD	MOD	MOD	FPSHIFT2	MOD	MOD	DRDY	
FPDAT0	driven 0	D0	LD0	driven 0	D0	D0	LD0	R2	R3
FPDAT1	driven 0	D1	LD1	driven 0	D1	D1	LD1	R1	R2
FPDAT2	driven 0	D2	LD2	driven 0	D2	D2	LD2	R0	R1
FPDAT3	driven 0	D3	LD3	driven 0	D3	D3	LD3	G2	G3
FPDAT4	D0	D4	UD0	D0	D4	D4	UD0	G1	G2
FPDAT5	D1	D5	UD1	D1	D5	D5	UD1	G0	G1
FPDAT6	D2	D6	UD2	D2	D6	D6	UD2	B2	B3
FPDAT7	D3	D7	UD3	D3	D7	D7	UD3	B1	B2
FPDAT8	GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	B0	B1
FPDAT9	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	R0
FPDAT10	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	G0
FPDAT11	GPIO4/ Hardware Video Invert	GPIO4/ Hardware Video Invert	GPIO4/ Hardware Video Invert	GPIO4/ Hardware Video Invert	GPIO4/ Hardware Video Invert	GPIO4/ Hardware Video Invert	GPIO4/ Hardware Video Invert	GPIO4	B0

Note

1. Unused GPIO pins must be connected to IO V_{DD}.
2. Hardware Video Invert is enabled on FPDAT11 by REG[02h] bit 1.

6 D.C. Characteristics

Table 6-1: Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
Core V_{DD}	Supply Voltage	V_{SS} - 0.3 to 4.0	V
IO V_{DD}	Supply Voltage	Core V_{DD} to 7.0	V
V_{IN}	Input Voltage	V_{SS} - 0.3 to IO V_{DD} + 0.5	V
V_{OUT}	Output Voltage	V_{SS} - 0.3 to IO V_{DD} + 0.5	V
T_{STG}	Storage Temperature	-65 to 150	° C
T_{SOL}	Solder Temperature/Time	260 for 10 sec. max at lead	° C

Table 6-2: Recommended Operating Conditions for Core VDD = 3.3V ± 10%

Symbol	Parameter	Condition	Min	Typ	Max	Units
Core V_{DD}	Supply Voltage	V_{SS} = 0 V	2.7	3.0/3.3	3.6	V
IO V_{DD}	Supply Voltage	V_{SS} = 0 V, IO $V_{DD} \geq$ Core V_{DD}	2.7	3.0/3.3/5.0	5.5	V
V_{IN}	Input Voltage		V_{SS}		IO V_{DD}	V
T_{OPR}	Operating Temperature		-40	25	85	° C

Table 6-3: Input Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Low Level Input Voltage CMOS inputs	IO V_{DD} = 3.0 3.3 5.0			0.8 0.8 1.0	V
V_{IH}	High Level Input Voltage CMOS inputs	IO V_{DD} = 3.0 3.3 5.0	1.9 2.0 3.5			V
V_{T+}	Positive-going Threshold CMOS Schmitt inputs	IO V_{DD} = 3.0 3.3 5.0	1.0 1.1 2.0		2.3 2.4 4.0	V
V_{T-}	Negative-going Threshold CMOS Schmitt inputs	IO V_{DD} = 3.0 3.3 5.0	0.5 0.6 0.8		1.7 1.8 3.1	V
I_{IZ}	Input Leakage Current	V_{DD} = Max V_{IH} = V_{DD} V_{IL} = V_{SS}	-1		1	µA
C_{IN}	Input Pin Capacitance				10	pF

Table 6-4: Output Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{OL} (3.0V)	Low Level Output Current	IO V_{DD} = 3.0V V_O = 0.4V, Type = 1 2 3		1.8 5 10		mA
I_{OL} (3.3V)	Low Level Output Current	IO V_{DD} = 3.3V V_O = 0.4V, Type = 1 2 3		2 6 12		mA
I_{OL} (5.0V)	Low Level Output Current	IO V_{DD} = 5.0V V_O = 0.4V, Type = 1 2 3		3 8 12		mA
I_{OH} (3.0V)	High Level Output Current	IO V_{DD} = 3.0V V_O = IO V_{DD}-0.4V, Type = 1 2 3		-1.8 -5 -10		mA
I_{OH} (3.3V)	High Level Output Current	IO V_{DD} = 3.3V V_O = IO V_{DD}-0.4V, Type = 1 2 3		-2 -6 -12		mA
I_{OH} (5.0V)	High Level Output Current	IO V_{DD} = 5.0V V_O = IO V_{DD}-0.4V, Type = 1 2 3		-3 -8 -12		mA
V_{OL}	Low Level Output Voltage	I = I_{OL}			0.4	V
V_{OH}	High Level Output Voltage	I = I_{OH}	IO V_{DD} - 0.4			V
I_{OZ}	Output Leakage Current	V_{DD} = MAX V_{OH} = V_{DD} V_{OL} = V_{SS}	-1		1	µA
C_{OUT}	Output Pin Capacitance				10	pF
C_{BID}	Bidirectional Pin Capacitance				10	pF

7 A.C. Characteristics

Conditions: IO V_{DD} = 2.7 V to 5.0 V
T_A = -40° C to 85° C
T_{rise} and T_{fall} for all inputs must be ≤ 5 nsec (10% ~ 90%)
C_L = 60pF (Bus/MPU Interface)
C_L = 60pF (LCD Panel Interface)

7.1 Bus Interface Timing

7.1.1 SH-4 Interface Timing

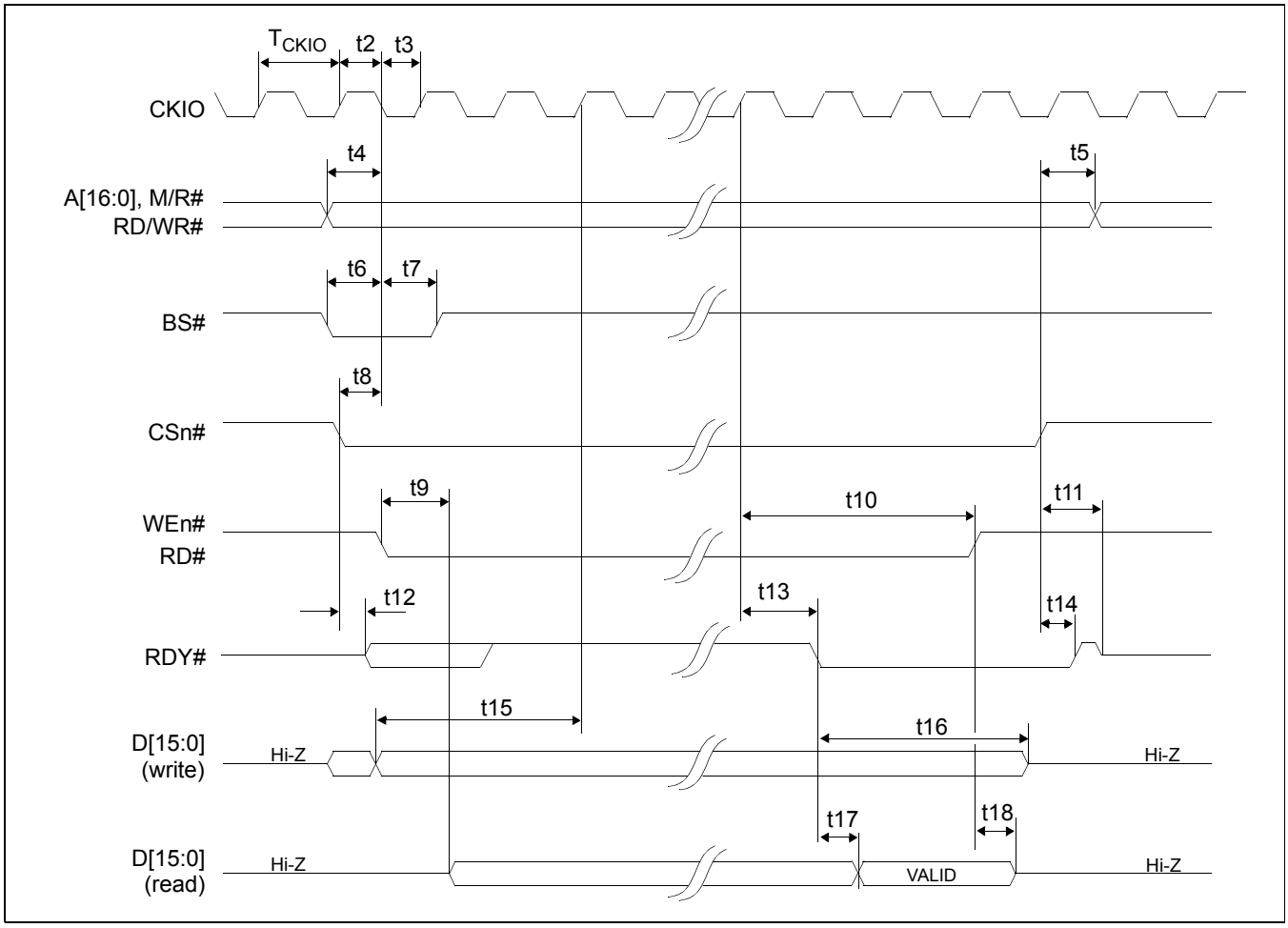


Figure 7-1: SH-4 Timing

Note

The SH-4 Wait State Control Register for the area in which the S1D13705 resides must be set to a non-zero value. The SH-4 read-to-write cycle transition must be set to a non-zero value (with reference to BUSCLK).

Table 7-1: SH-4 Timing

Symbol	Parameter	Min	Max	Units
f_{CKIO}	Bus Clock frequency		50	MHz
T_{CKIO}	Bus Clock period	$1/f_{CKIO}$		
t2	Bus Clock pulse width low	8		ns
t3	Bus Clock pulse width high	8		ns
t4	A[16:0], RD/WR# setup to CKIO	0		ns
t5	A[16:0], RD/WR# hold from CS#	0		ns
t6	BS# setup	5		ns
t7	BS# hold	5		ns
t8	CSn# setup	0		ns
t9	Falling edge RD# to DB[15:0] driven		25	ns
t10	CKIO to WE#, RD# high	$1.5T_{CKIO}$		
t11	Rising edge CSn# to RDY# high impedance		T_{CKIO}	
t12	Falling edge CSn# to RDY# driven		20	ns
t13	CKIO to RDY# low		20	ns
t14	Rising edge CSn# to RDY# high		16	ns
t15	DB[15:0] setup to 2nd CKIO after BS# (write cycle)	0		ns
t16	DB[15:0] hold (write cycle)	0		ns
t17	RDY# falling edge to DB[15:0] valid (read cycle)		7	ns
t18	Rising edge RD# to DB[15:0] high impedance (read cycle)		10	ns

Note

CKIO may be turned off (held low) between accesses - see Section 13.5, “Turning Off BCLK Between Accesses” on page 84

7.1.2 SH-3 Interface Timing

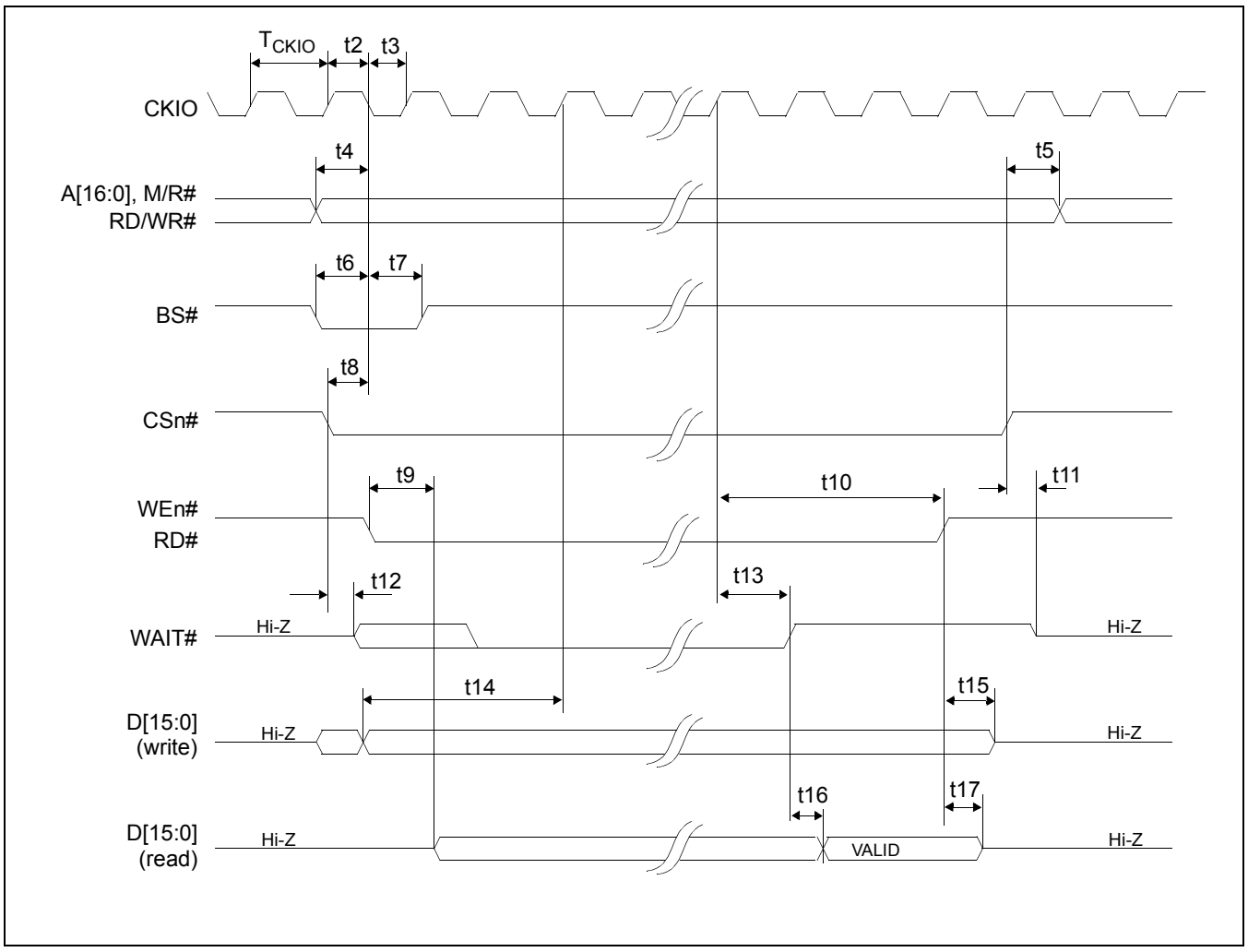


Figure 7-2: SH-3 Bus Timing

Note

The SH-3 Wait State Control Register for the area in which the S1D13705 resides must be set to a non-zero value.

Table 7-2: SH-3 Bus Timing

Symbol	Parameter	Min	Max[a]	Units
f_{CKIO}	Bus Clock frequency		50	MHz
T_{CKIO}	Bus Clock period	$1/f_{CKIO}$		
t2	Bus Clock pulse width low	8		ns
t3	Bus Clock pulse width high	8		ns
t4	A[16:0], RD/WR# setup to CKIO	0		ns
t5	A[16:0], RD/WR# hold from CS#	0		ns
t6	BS# setup	5		ns
t7	BS# hold	5		ns
t8	CSn# setup	0		ns
t9	Falling edge RD# to DB[15:0] driven		25	ns
t10	CKIO to WEn#, RD# high	$1.5T_{CKIO}$		
t11	Rising edge CSn# to WAIT# high impedance		10	ns
t12	Falling edge CSn# to WAIT# driven		15	ns
t13	CKIO to WAIT# delay		20	ns
t14	DB[15:0] setup to 2nd CKIO after BS# (write cycle)	0		ns
t15	DB[15:0] hold from rising edge of WEn# (write cycle)	0		ns
t16	WAIT# rising edge to DB[15:0] valid (read cycle)		6	ns
t17	Rising edge RD# to DB[15:0] high impedance (read cycle)		10	ns

[a] One Software WAIT State Required

Note

CKIO may be turned off (held low) between accesses - see Section 13.5, “Turning Off BCLK Between Accesses” on page 84

7.1.3 Motorola MC68K #1 Interface Timing

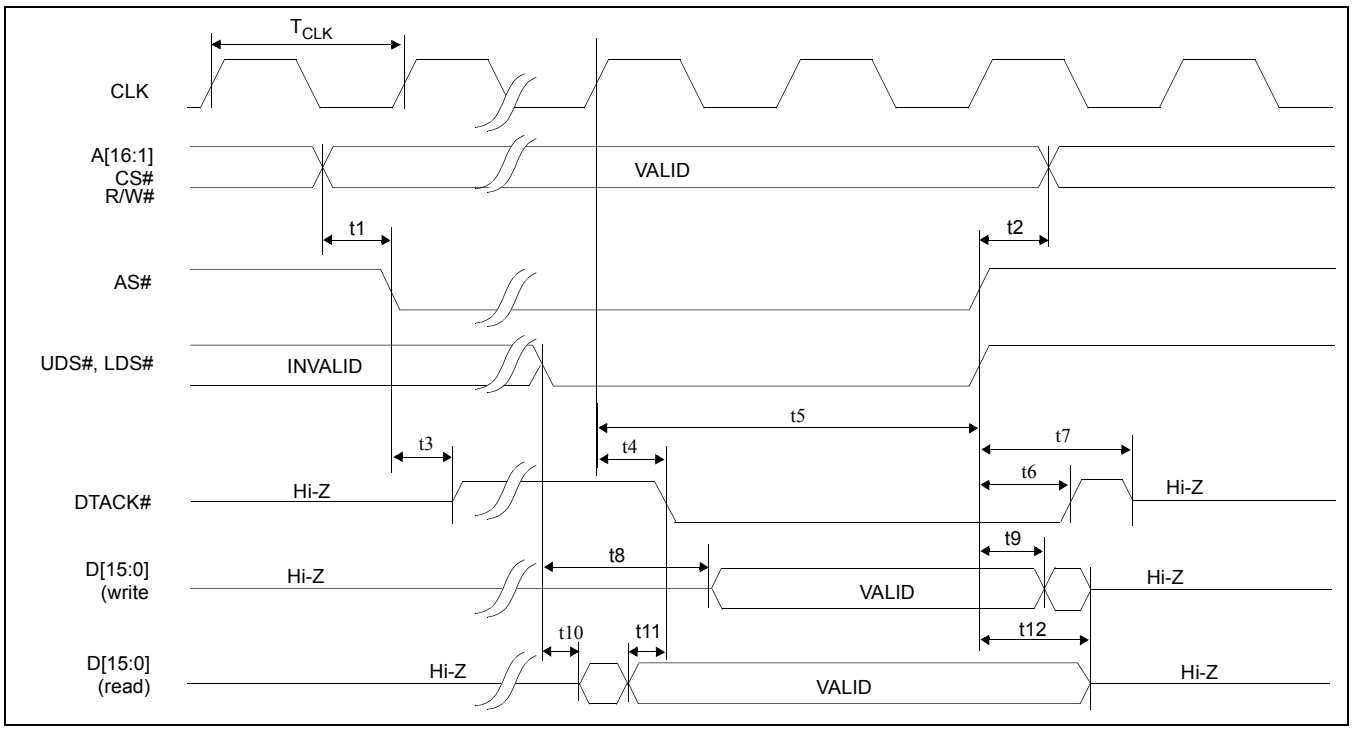


Figure 7-3: MC68K #1 Bus Timing (MC68000)

Table 7-3: MC68K #1 Bus Timing (MC68000)

Symbol	Parameter	Min	Max	Units
f_{CLK}	Bus Clock Frequency		33	MHz
T_{CLK}	Bus Clock period	$1/f_{CLK}$		
t1	A[16:1], CS# valid before AS# falling edge	0		ns
t2	A[16:1], CS# hold from AS# rising edge	0		ns
t3	AS# low to DTACK# driven high		16	ns
t4	CLK to DTACK# low		15	ns
t5	CLK to AS#, UDS#, LDS# high	$1T_{CLK}$		
t6	AS# high to DTACK# high		20	ns
t7	AS# high to DTACK# high impedance		T_{CLK}	
t8	UDS#, LDS# falling edge to D[15:0] valid (write cycle)		T_{CLK}	
t9	D[15:0] hold from AS# rising edge (write cycle)	0		ns
t10	UDS#, LDS# falling edge to D[15:0] driven (read cycle)		15	ns
t11	D[15:0] valid to DTACK# falling edge (read cycle)	0		ns
t12	UDS#, LDS# rising edge to D[15:0] high impedance		10	ns

Note

CLK may be turned off (held low) between accesses - see Section 13.5, “Turning Off BCLK Between Accesses” on page 84

7.1.4 Motorola MC68K #2 Interface Timing

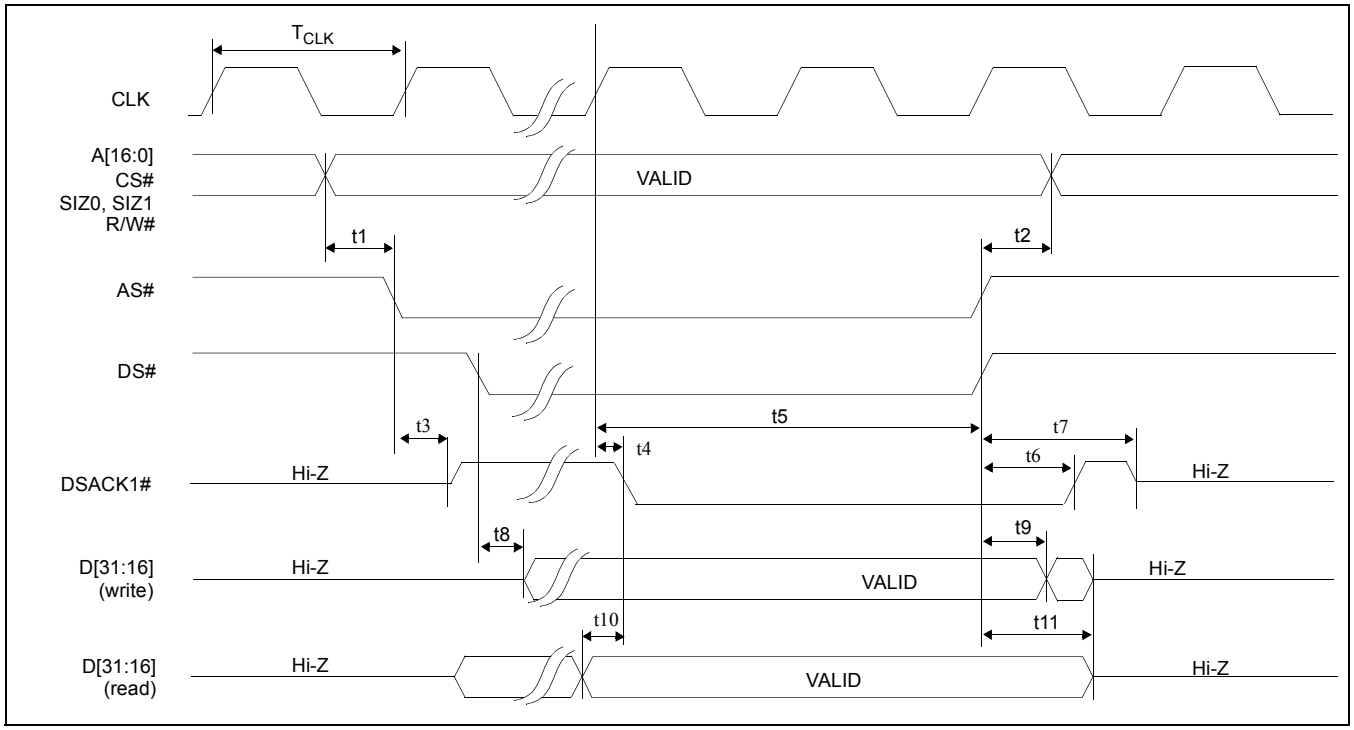


Figure 7-4: MC68K #2 Timing (MC68030)

Table 7-4: MC68K #2 Timing (MC68030)

Symbol	Parameter	Min	Max	Units
f_{CLK}	Bus Clock frequency		33	MHz
T_{CLK}	Bus Clock period	$1/f_{CLK}$		
t1	A[16:0], CS#, SIZ0, SIZ1 valid before AS# falling edge	0		ns
t2	A[16:0], CS#, SIZ0, SIZ1 hold from AS#, DS# rising edge	0		ns
t3	AS# low to DSACK1# driven high		22	ns
t4	CLK to DSACK1# low		18	ns
t5	CLK to AS#, DS# high	$1T_{CLK}$		ns
t6	AS# high to DSACK1# high		20	ns
t7	AS# high to DSACK1# high impedance		T_{CLK}	
t8	DS# falling edge to D[31:16] valid (write cycle)		$T_{CLK}/2$	
t9	AS#, DS# rising edge to D[31:16] invalid (write cycle)	0		ns
t10	D[31:16] valid to DSACK1# low (read cycle)	0		ns
t11	AS#, DS# rising edge to D[31:16] high impedance		20	ns

Note

CLK may be turned off (held low) between accesses - see Section 13.5, “Turning Off BCLK Between Accesses” on page 84

7.1.5 Generic #1 Interface Timing

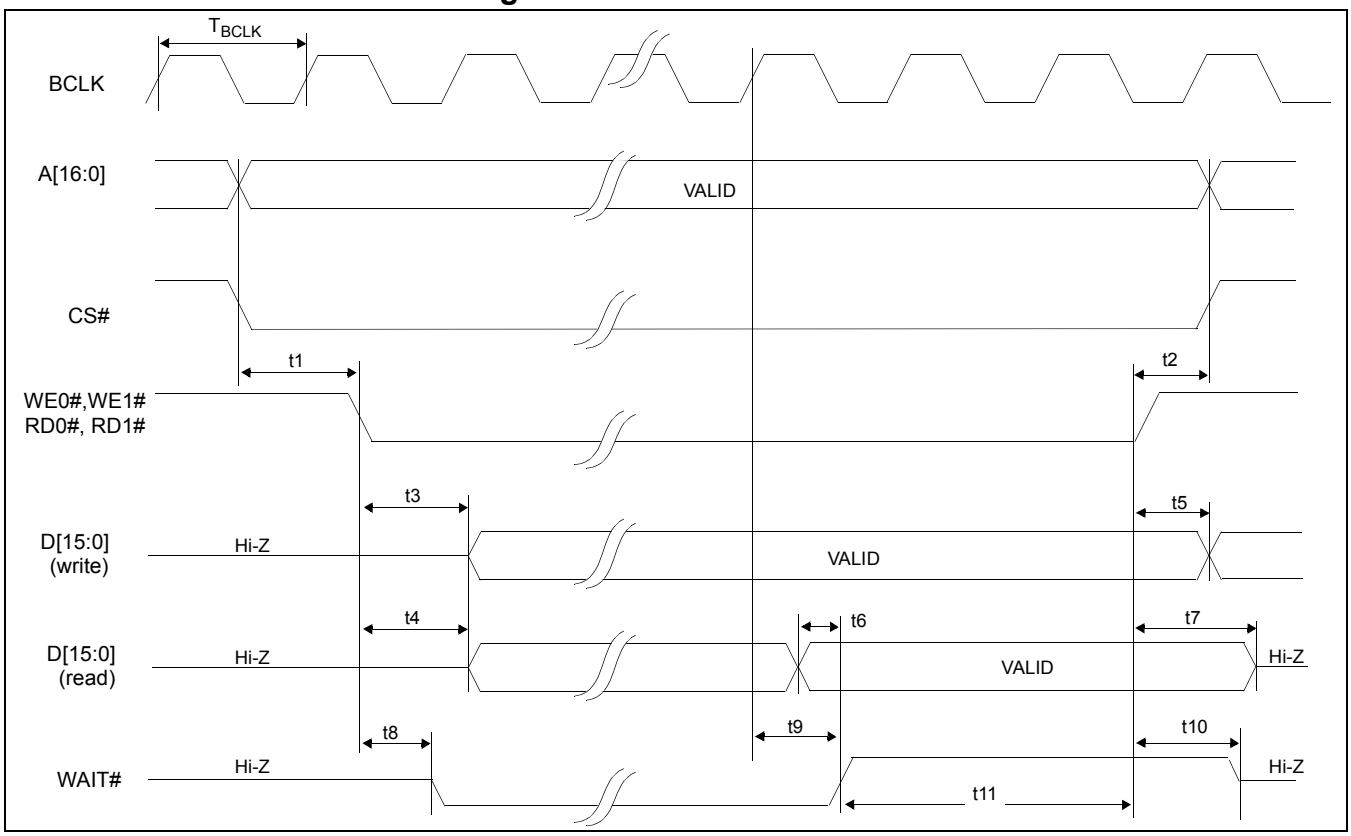


Figure 7-5: Generic #1 Timing

Table 7-5: Generic #1 Timing

Symbol	Parameter	Min	Max	Units
f_{BCLK}	Bus Clock frequency		50	MHz
T_{BCLK}	Bus Clock period	$1/f_{BCLK}$		MHz
t1	A[16:0], CS# valid to WE0#, WE1# low (write cycle) or RD0#, RD1# low (read cycle)	0		ns
t2	WE0#, WE1# high (write cycle) or RD0#, RD1# high (read cycle) to A[16:0], CS# invalid	0		ns
t3	WE0#, WE1# low to D[15:0] valid (write cycle)		T_{BCLK}	
t4	RD0#, RD1# low to D[15:0] driven (read cycle)		17	ns
t5	WE0#, WE1# high to D[15:0] invalid (write cycle)	0		ns
t6	D[15:0] valid to WAIT# high (read cycle)	0		ns
t7	RD0#, RD1# high to D[15:0] high impedance (read cycle)		10	ns
t8	WE0#, WE1# low (write cycle) or RD0#, RD1# low (read cycle) to WAIT# driven low		16	ns
t9	BCLK to WAIT# high		16	ns
t10	WE0#, WE1# high (write cycle) or RD0#, RD1# high (read cycle) to WAIT# high impedance		16	ns
t11	WAIT# high to WE0#, WE1#, RD0#, RD1# high	$1T_{BCLK}$		

Note

BCLK may be turned off (held low) between accesses - see Section 13.5, “Turning Off BCLK Between Accesses” on page 84

7.1.6 Generic #2 Interface Timing

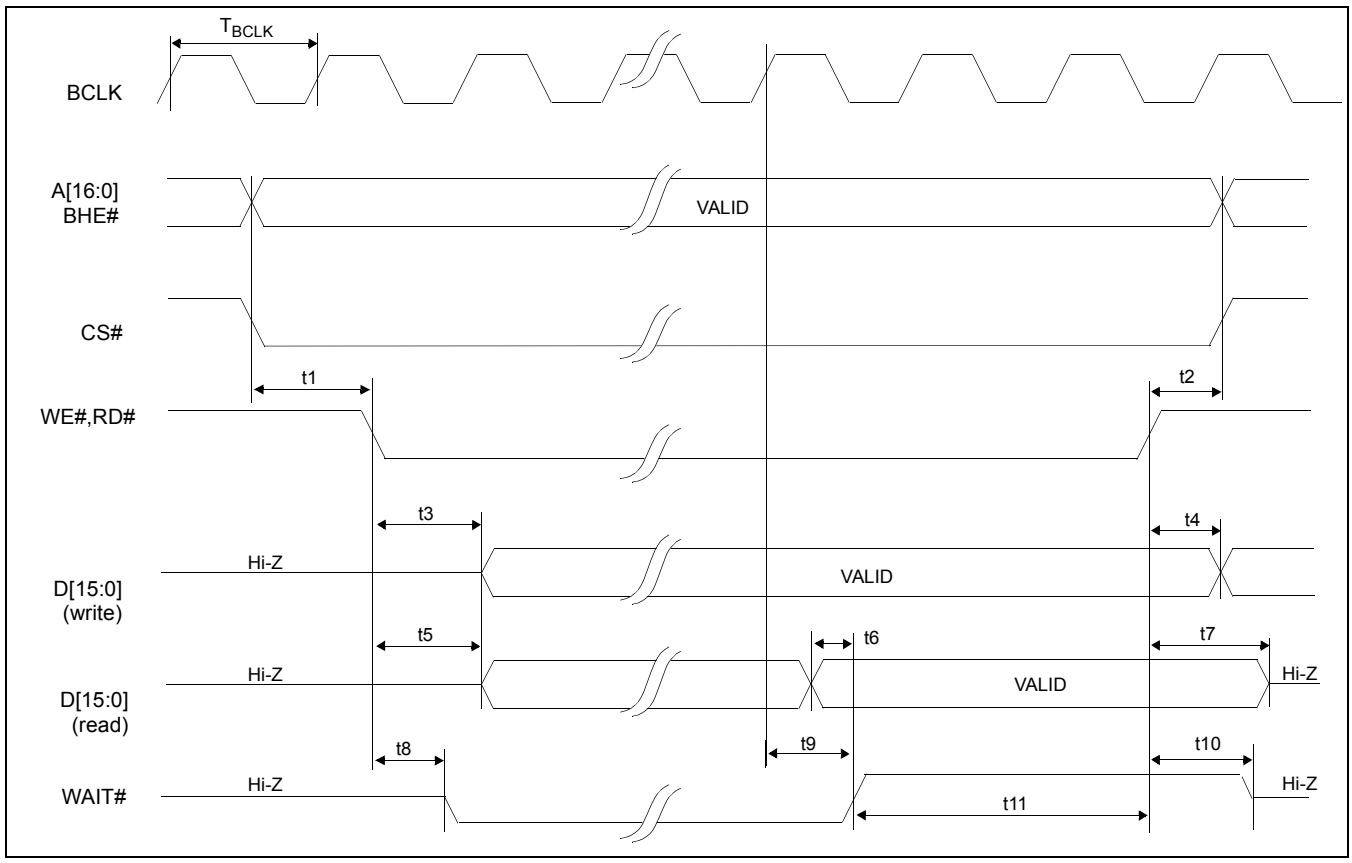


Figure 7-6: Generic #2 Timing

Table 7-6: Generic #2 Timing

Symbol	Parameter	Min	Max	Units
f_{BCLK}	Bus Clock frequency		50	MHz
T_{BCLK}	Bus Clock period	$1/f_{BCLK}$		
t1	A[16:0], BHE#, CS# valid to WE#, RD# low	0		ns
t2	WE#, RD# high to A[16:0], BHE#, CS# invalid	0		ns
t3	WE# low to D[15:0] valid (write cycle)		T_{BCLK}	
t4	WE# high to D[15:0] invalid (write cycle)	0		ns
t5	RD# low to D[15:0] driven (read cycle)		16	ns
t6	D[15:0] valid to WAIT# high (read cycle)	0		ns
t7	RD# high to D[15:0] high impedance (read cycle)		10	ns
t8	WE#, RD# low to WAIT# driven low		14	ns
t9	BCLK to WAIT# high		10	ns
t10	WE#, RD# high to WAIT# high impedance		11	ns
t11	WAIT# high to WE#, RD# high	$1T_{BCLK}$		

Note

BCLK may be turned off (held low) between accesses - see Section 13.5, “Turning Off BCLK Between Accesses” on page 84

7.2 Clock Input Requirements

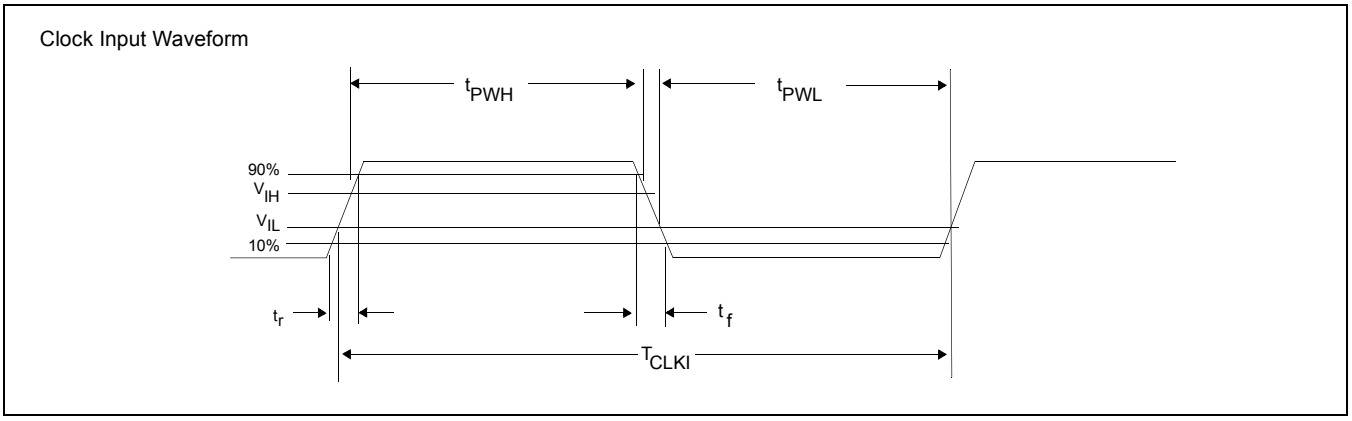


Figure 7-7: Clock Input Requirements for CLKI

Table 7-7: Clock Input Requirements for CLKI

Symbol	Parameter	Min	Max	Units
f_{CLKI}	Input Clock Frequency (CLKI)		50	MHz
T_{CLKI}	Input Clock period (CLKI)	$1/f_{CLKI}$		ns
t_{PWH}	Input Clock Pulse Width High (CLKI)	8		ns
t_{PWL}	Input Clock Pulse Width Low (CLKI)	8		ns
t_f	Input Clock Fall Time (10% - 90%)		5	ns
t_r	Input Clock Rise Time (10% - 90%)		5	ns

Note

When CLKI is > 25MHz the Input Clock Divide bit (REG[02h] bit 4) must be set to 1.

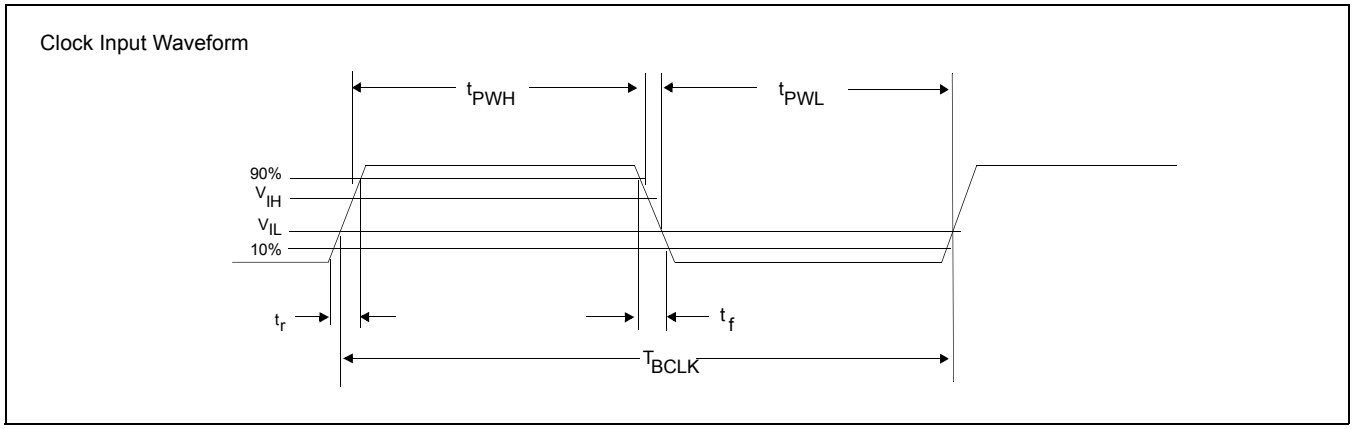


Figure 7-8: Clock Input Requirements for BCLK

Table 7-8: Clock Input Requirements for BCLK

Symbol	Parameter	Min	Max	Units
f_{BCLK}	Input Clock Frequency (BCLK)		50	MHz
T_{BCLK}	Input Clock period (BCLK)	$1/f_{CLKI}$		
t_{PWH}	Input Clock Pulse Width High (BCLK)	8		ns
t_{PWL}	Input Clock Pulse Width Low (BCLK)	8		ns
t_f	Input Clock Fall Time (10% - 90%)		5	ns
t_r	Input Clock Rise Time (10% - 90%)		5	ns

7.3 Display Interface

7.3.1 Power On/Reset Timing

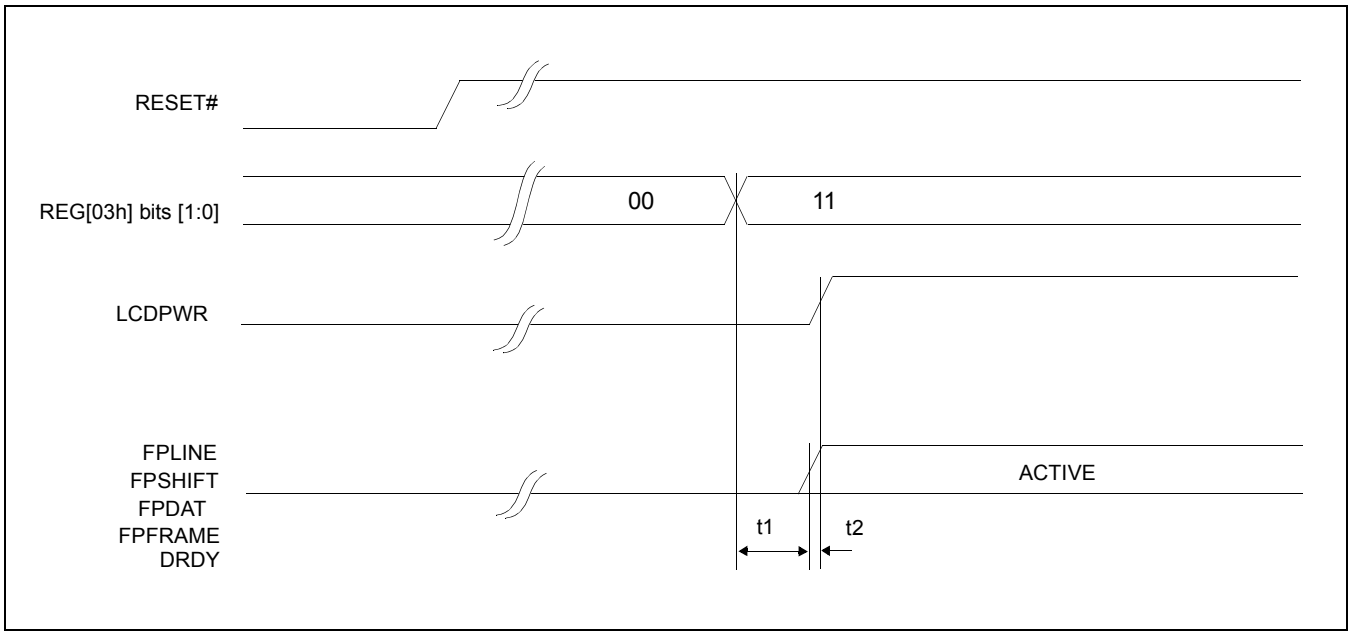


Figure 7-9: LCD Panel Power On/Reset Timing

Table 7-9: LCD Panel Power On/Reset Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	REG[03h] to FPLINE, FPFRAME, FPSHIFT, FPDAT, DRDY active			$T_{FPFRAME}$	ns
t2	FPLINE, FPFRAME, FPSHIFT, FPDAT, DRDY active to LCDPWR		0		Frames

Note

Where $T_{FPFRAME}$ is the period of FPFRAME and T_{PCLK} is the period of the pixel clock.

7.3.2 Power Down/Up Timing

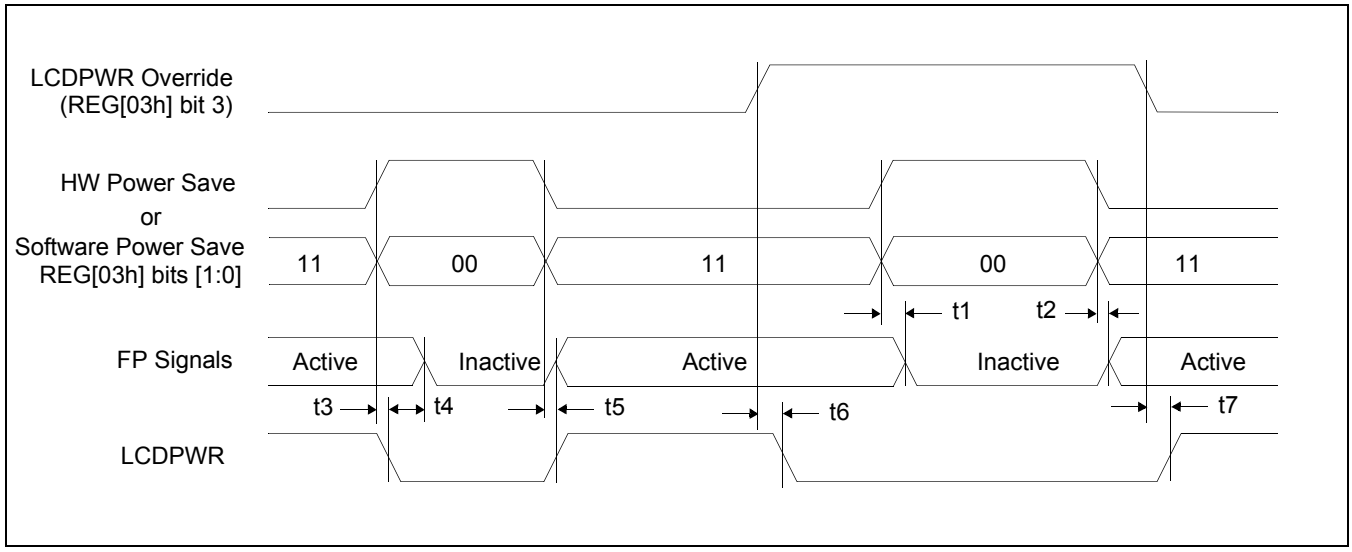
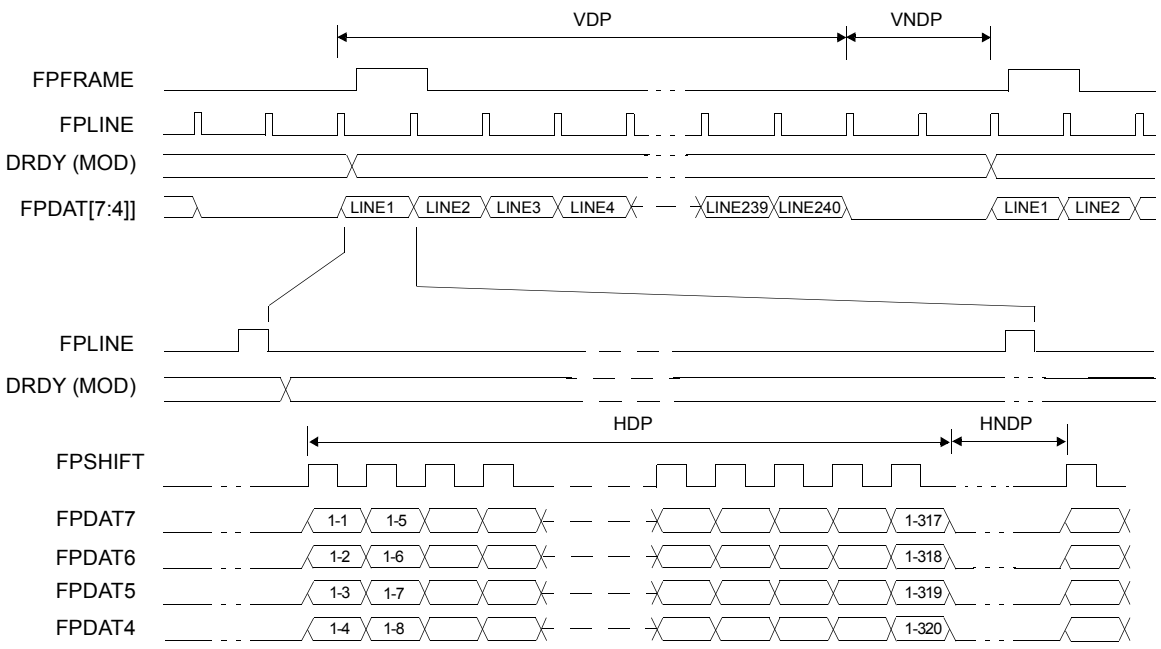


Figure 7-10: Power Down/Up Timing

Table 7-10: Power Down/Up Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	HW Power Save active to FPLINE, FPFRAME, FPSHIFT, FPDAT, DRDY inactive - LCDPWR Override = 1			1	Frame
t2	HW Power Save inactive to FPLINE, FPFRAME, FPSHIFT, FPDAT, DRDY active - LCDPWR Override = 1			1	Frame
t3	HW Power Save active to FPLINE, FPFRAME, FPSHIFT, FPDAT, DRDY inactive - LCDPWR Override = 0			1	Frame
t4	LCDPWR low to FPLINE, FPFRAME, FPSHIFT, FPDAT, DRDY inactive - LCDPWR Override = 0		127		Frame
t5	HW Power Save inactive to FPLINE, FPFRAME, FPSHIFT, FPDAT, DRDY, LCDPWR active - LCDPWR Override = 0		0		Frame
t6	LCDPWR Override active (1) to LCDPWR inactive			1	Frame
t7	LCDPWR Override inactive (1) to LCDPWR active			1	Frame

7.3.3 Single Monochrome 4-Bit Panel Timing



* Diagram drawn with 2 FPLINE vertical blank period
Example timing for a 320x240 panel
For this timing diagram Mask FPSHIFT, REG[01h] bit 3, is set to 1

Figure 7-11: Single Monochrome 4-Bit Panel Timing

VDP =	Vertical Display Period	= (REG[06h] bits 1-0, REG[05h] bits 7-0) + 1 Lines
VNDP =	Vertical Non-Display Period	= REG[0Ah] bits 5-0 Lines
HDP =	Horizontal Display Period	= ((REG[04h] bits 6-0) + 1) x 8Ts
HNDP =	Horizontal Non-Display Period	= (REG[08h] + 4) x 8Ts

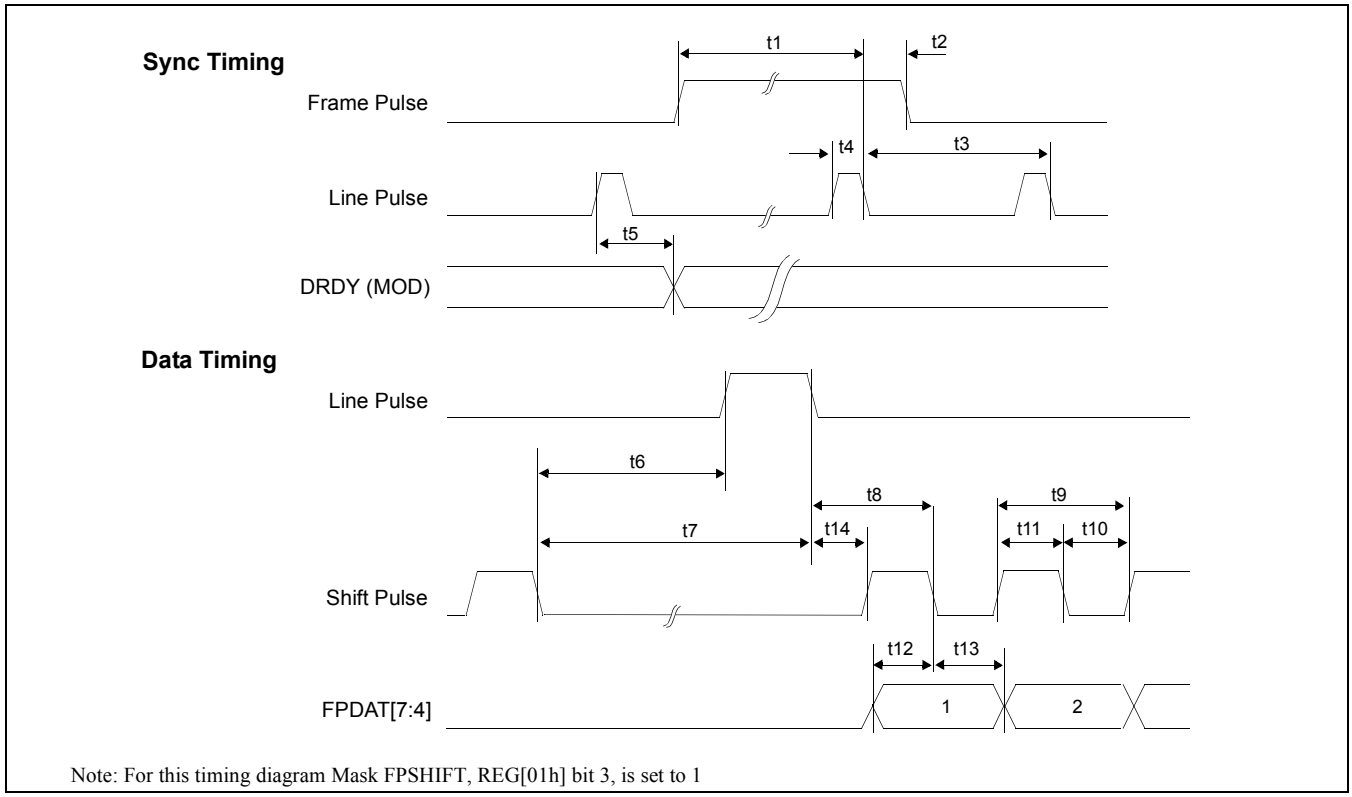


Figure 7-12: Single Monochrome 4-Bit Panel A.C. Timing

Table 7-11: Single Monochrome 4-Bit Panel A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Frame Pulse setup to Line Pulse falling edge	note 2			(note 1)
t2	Frame Pulse hold from Line Pulse falling edge	9			Ts
t3	Line Pulse period	note 3			
t4	Line Pulse pulse width	9			Ts
t5	MOD delay from Line Pulse rising edge	1			Ts
t6	Shift Pulse falling edge to Line Pulse rising edge	note 4			
t7	Shift Pulse falling edge to Line Pulse falling edge	note 5			
t8	Line Pulse falling edge to Shift Pulse falling edge	t14 + 2			Ts
t9	Shift Pulse period	4			Ts
t10	Shift Pulse pulse width low	2			Ts
t11	Shift Pulse pulse width high	2			Ts
t12	FPDAT[7:4] setup to Shift Pulse falling edge	2			Ts
t13	FPDAT[7:4] hold to Shift Pulse falling edge	2			Ts
t14	Line Pulse falling edge to Shift Pulse rising edge	23			Ts

1. Ts = pixel clock period
2. $t1_{min}$ = $t3_{min}$ - 9Ts
3. $t3_{min}$ = [((REG[04h] bits 6-0)+1) x 8 + ((REG[08h] bits 4-0) + 4) x 8]Ts
4. $t6_{min}$ = [(REG[08h] bits 4-0) x 8 + 2]Ts
5. $t7_{min}$ = [(REG[08h] bits 4-0) x 8 + 11]Ts

7.3.4 Single Monochrome 8-Bit Panel Timing

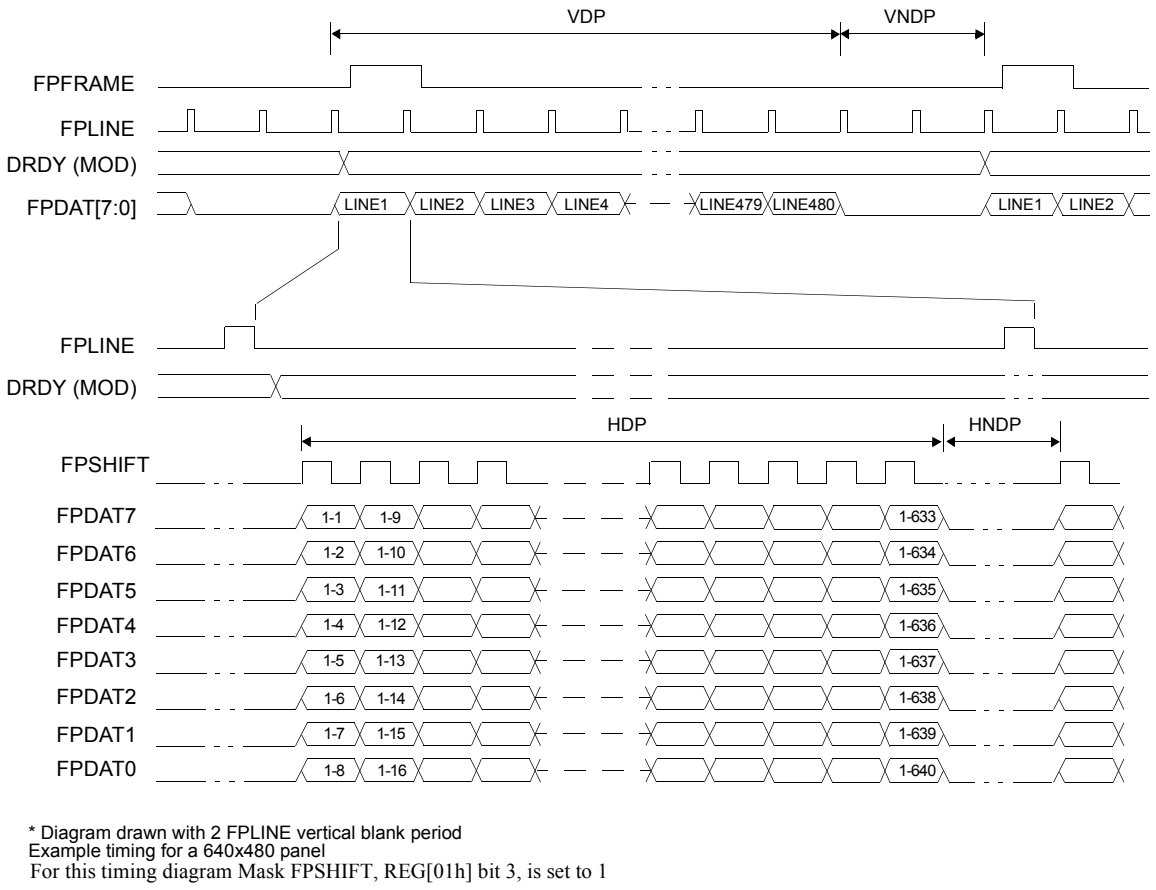


Figure 7-13: Single Monochrome 8-Bit Panel Timing

VDP =	Vertical Display Period	= (REG[06h] bits 1-0, REG[05h] bits 7-0) + 1 Lines
VNDP =	Vertical Non-Display Period	= REG[0Ah] bits 5-0 Lines
HDP =	Horizontal Display Period	= ((REG[04h] bits 6-0) + 1) x 8Ts
HNDP =	Horizontal Non-Display Period	= (REG[08h] + 4) x 8Ts

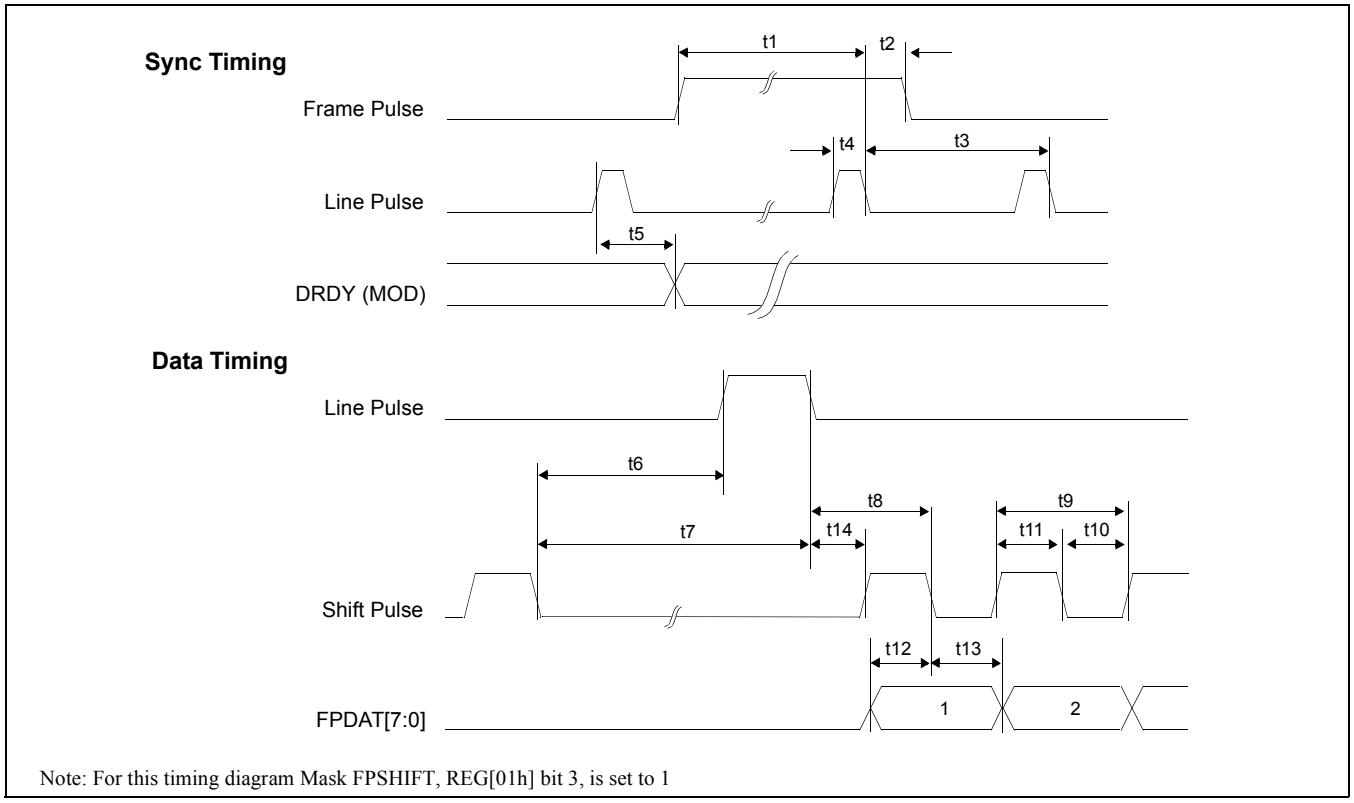


Figure 7-14: Single Monochrome 8-Bit Panel A.C. Timing

Table 7-12: Single Monochrome 8-Bit Panel A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Frame Pulse setup to Line Pulse falling edge	note 2			(note 1)
t2	Frame Pulse hold from Line Pulse falling edge	9			Ts
t3	Line Pulse period	note 3			
t4	Line Pulse pulse width	9			Ts
t5	MOD delay from Line Pulse rising edge	1			Ts
t6	Shift Pulse falling edge to Line Pulse rising edge	note 4			
t7	Shift Pulse falling edge to Line Pulse falling edge	note 5			
t8	Line Pulse falling edge to Shift Pulse falling edge	t14 + 4			Ts
t9	Shift Pulse period	8			Ts
t10	Shift Pulse pulse width low	4			Ts
t11	Shift Pulse pulse width high	4			Ts
t12	FPDAT[7:0] setup to Shift Pulse falling edge	4			Ts
t13	FPDAT[7:0] hold to Shift Pulse falling edge	4			Ts
t14	Line Pulse falling edge to Shift Pulse rising edge	23			Ts

1. Ts = pixel clock period
2. $t1_{min}$ = $t3_{min}$ - 9Ts
3. $t3_{min}$ = [((REG[04h] bits 6-0)+1) x 8 + ((REG[08h] bits 4-0) + 4) x 8]Ts
4. $t6_{min}$ = [(REG[08h] bits 4-0) x 8 + 4]Ts
5. $t7_{min}$ =[(REG[08h] bits 4-0) x 8 + 13]Ts

7.3.5 Single Color 4-Bit Panel Timing

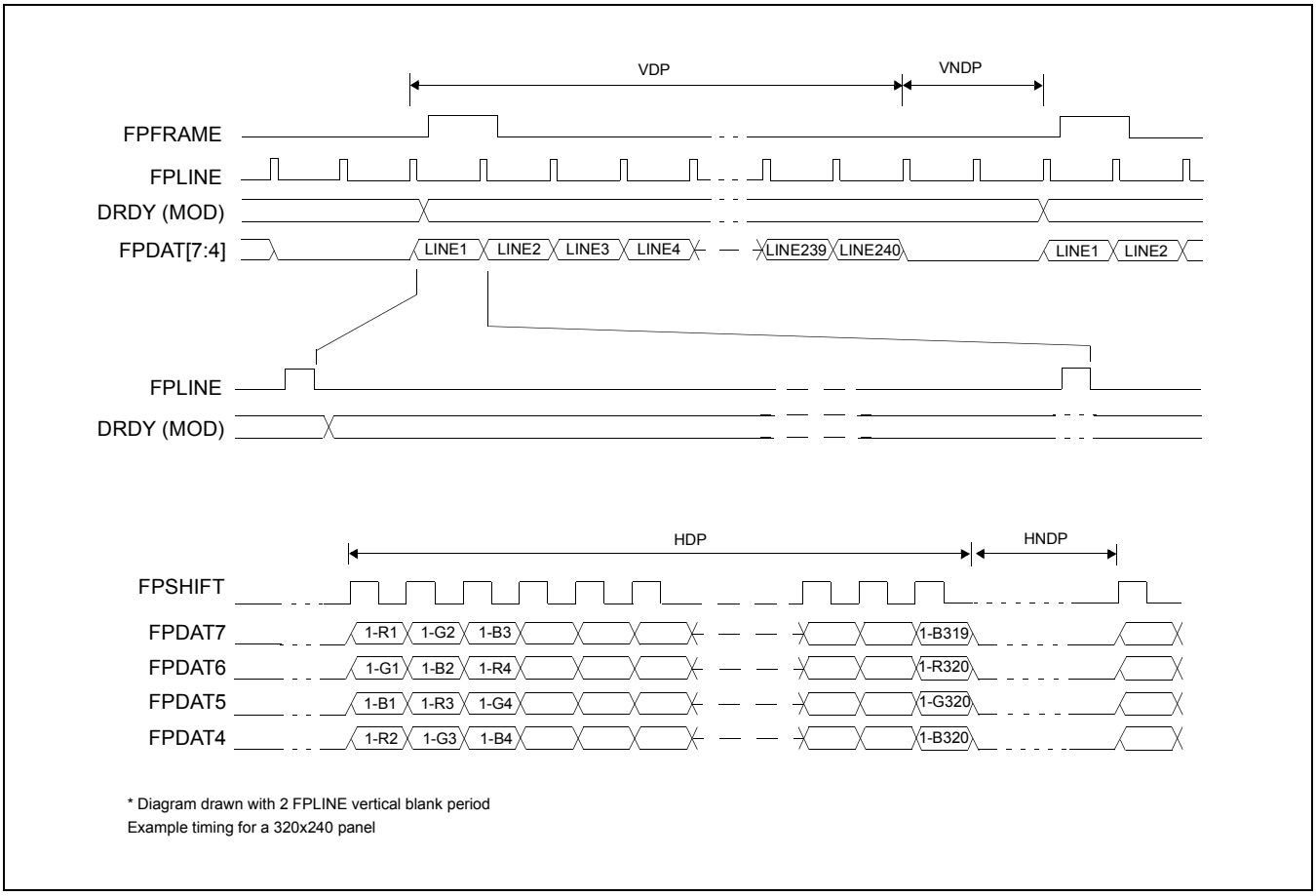


Figure 7-15: Single Color 4-Bit Panel Timing

VDP =	Vertical Display Period	= (REG[06h] bits 1-0, REG[05h] bits 7-0) + 1 Lines
VNDP =	Vertical Non-Display Period	= REG[0Ah] bits 5-0 Lines
HDP =	Horizontal Display Period	= ((REG[04h] bits 6-0) + 1) x 8Ts
HNDP =	Horizontal Non-Display Period	= (REG[08h] + 4) x 8Ts

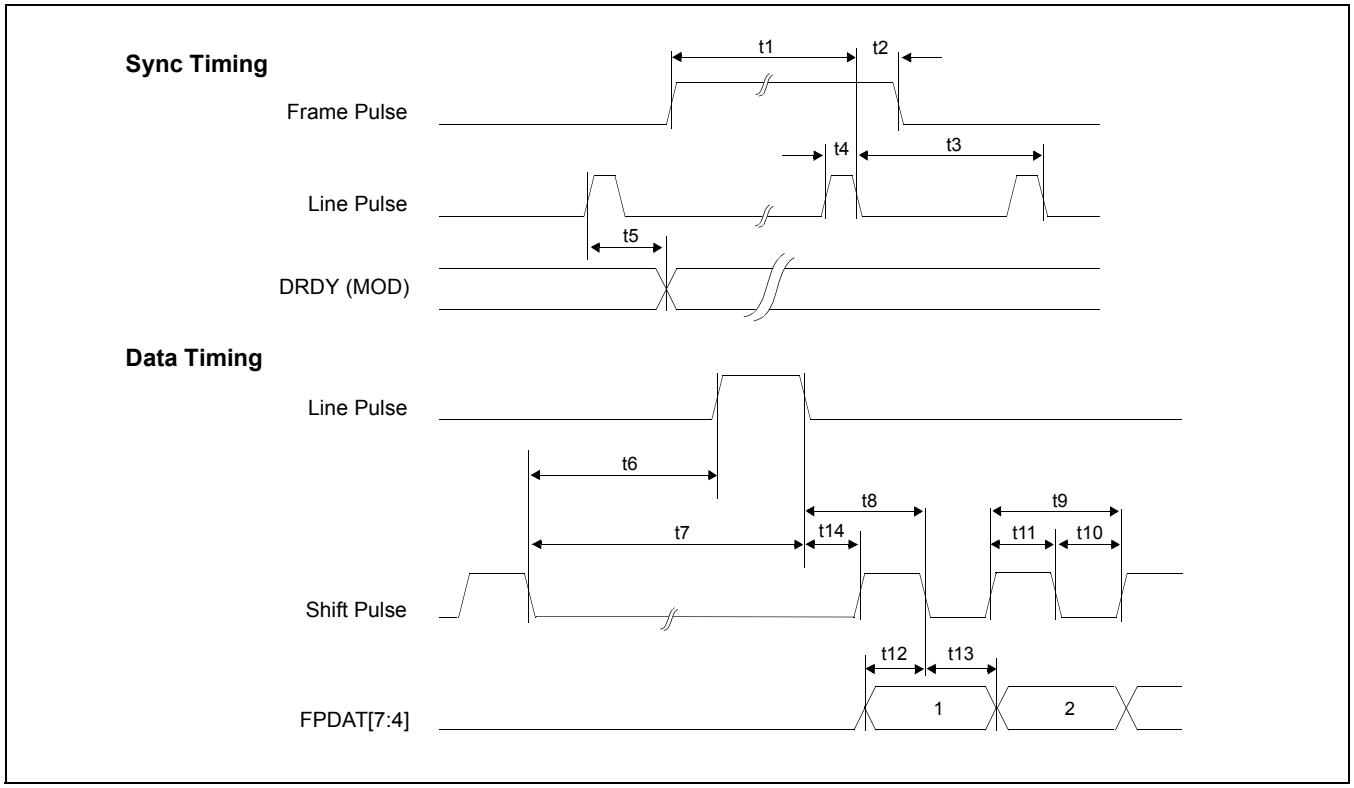


Figure 7-16: Single Color 4-Bit Panel A.C. Timing

Table 7-13: Single Color 4-Bit Panel A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Frame Pulse setup to Line Pulse falling edge	note 2			(note 1)
t2	Frame Pulse hold from Line Pulse falling edge	9			Ts
t3	Line Pulse period	note 3			
t4	Line Pulse pulse width	9			Ts
t5	MOD delay from Line Pulse rising edge	1			Ts
t6	Shift Pulse falling edge to Line Pulse rising edge	note 4			
t7	Shift Pulse falling edge to Line Pulse falling edge	note 5			
t8	Line Pulse falling edge to Shift Pulse falling edge	t14 + 0.5			Ts
t9	Shift Pulse period	1			Ts
t10	Shift Pulse pulse width low	0.5			Ts
t11	Shift Pulse pulse width high	0.5			Ts
t12	FPDAT[7:4] setup to Shift Pulse falling edge	0.5			Ts
t13	FPDAT[7:4] hold to Shift Pulse falling edge	0.5			Ts
t14	Line Pulse falling edge to Shift Pulse rising edge	24			Ts

1. Ts = pixel clock period
2. $t1_{min}$ = $t3_{min}$ - 9Ts
3. $t3_{min}$ = [((REG[04h] bits 6-0)+1) x 8 + ((REG[08h] bits 4-0) + 4) x 8]Ts
4. $t6_{min}$ = [(REG[08h] bits 4-0) x 8 + 1.5]Ts
5. $t7_{min}$ = [(REG[08h] bits 4-0) x 8 + 10]Ts

7.3.6 Single Color 8-Bit Panel Timing (Format 1)

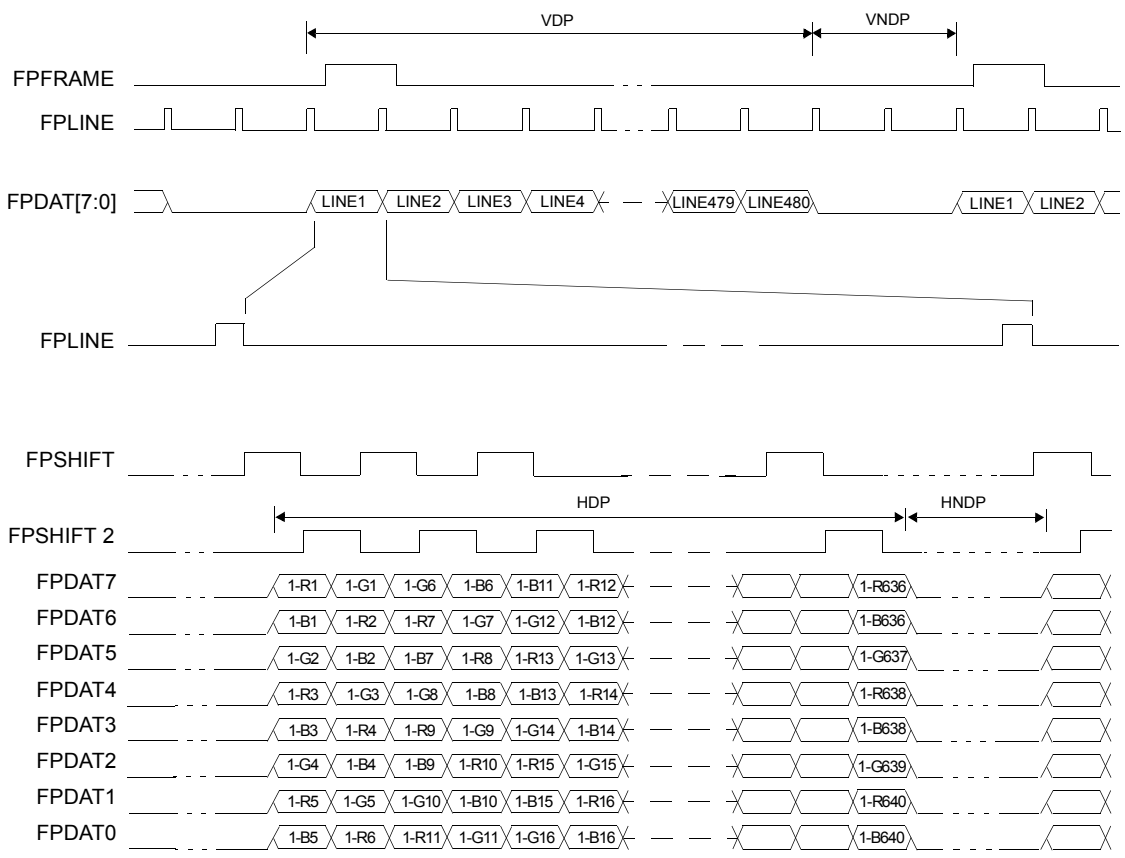


Figure 7-17: Single Color 8-Bit Panel Timing (Format 1)

VDP =	Vertical Display Period	= (REG[06h] bits 1-0, REG[05h] bits 7-0) + 1 Lines
VNDP =	Vertical Non-Display Period	= REG[0Ah] bits 5-0 Lines
HDP =	Horizontal Display Period	= ((REG[04h] bits 6-0) + 1) x 8Ts
HNDP =	Horizontal Non-Display Period	= (REG[08h] + 4) x 8Ts

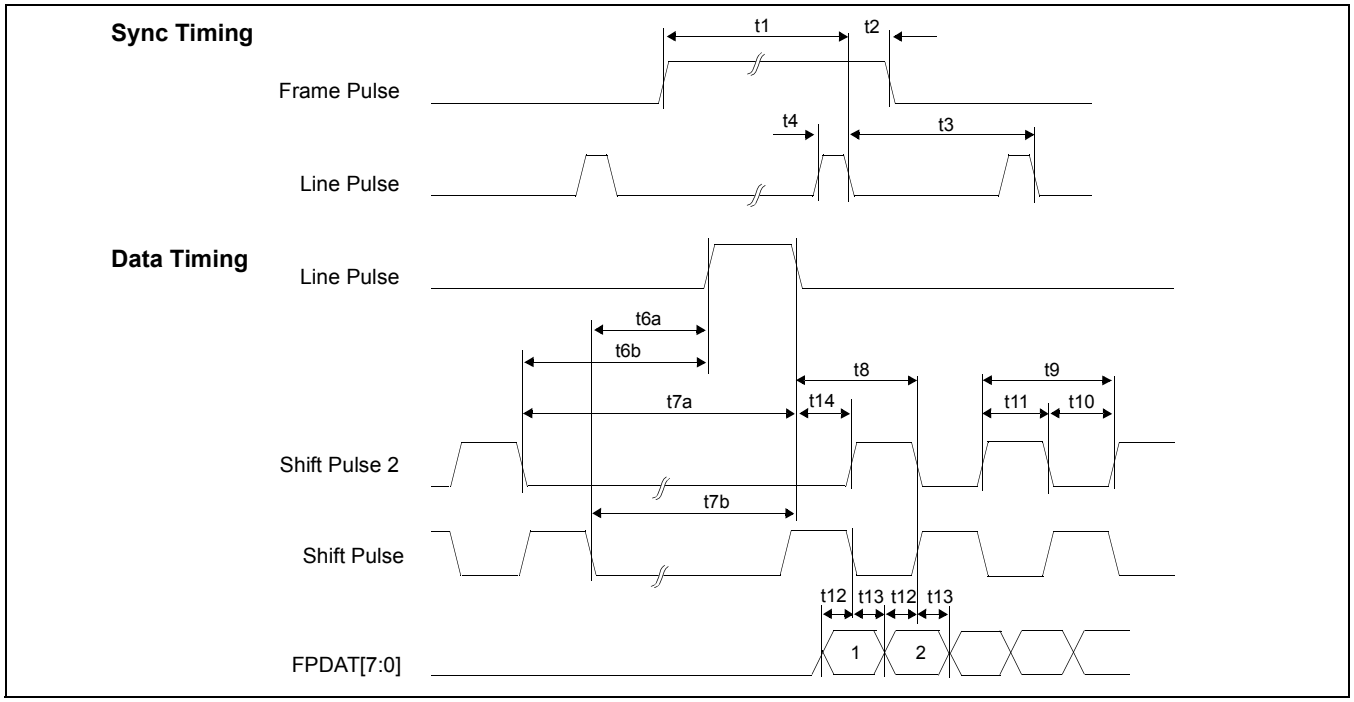


Figure 7-18: Single Color 8-Bit Panel A.C. Timing (Format 1)

Table 7-14: Single Color 8-Bit Panel A.C. Timing (Format 1)

Symbol	Parameter	Min	Typ	Max	Units
t1	Frame Pulse setup to Line Pulse falling edge	note 2			(note 1)
t2	Frame Pulse hold from Line Pulse falling edge	9			Ts
t3	Line Pulse period	note 3			
t4	Line Pulse pulse width	9			Ts
t6a	Shift Pulse falling edge to Line Pulse rising edge	note 4			
t6b	Shift Pulse 2 falling edge to Line Pulse rising edge	note 5			
t7a	Shift Pulse 2 falling edge to Line Pulse falling edge	note 6			
t7b	Shift Pulse falling edge to Line Pulse falling edge	note 7			
t8	Line Pulse falling edge to Shift Pulse rising, Shift Pulse 2 falling edge	t14 + 2			Ts
t9	Shift Pulse 2, Shift Pulse period	4			Ts
t10	Shift Pulse 2, Shift Pulse pulse width low	2			Ts
t11	Shift Pulse 2, Shift Pulse pulse width high	2			Ts
t12	FPDAT[7:0] setup to Shift Pulse 2, Shift Pulse falling edge	1			Ts
t13	FPDAT[7:0] hold from Shift Pulse 2, Shift Pulse falling edge	1			Ts
t14	Line Pulse falling edge to Shift Pulse rising edge	25			Ts

1. Ts = pixel clock period
2. $t1_{min}$ = $t3_{min}$ - 9Ts
3. $t3_{min}$ = [((REG[04h] bits 6-0)+1) x 8 + ((REG[08h] bits 4-0) + 4) x 8]Ts
4. $t6a_{min}$ = [(REG[08h] bits 4-0) x 8]Ts
5. $t6b_{min}$ = [(REG[08h] bits 4-0) x 8 + 2]Ts
6. $t7a_{min}$ = [(REG[08h] bits 4-0) x 8 + 11]Ts
7. $t7b_{min}$ = [(REG[08h] bits 4-0) x 8 + 11] - t10]Ts

7.3.7 Single Color 8-Bit Panel Timing (Format 2)

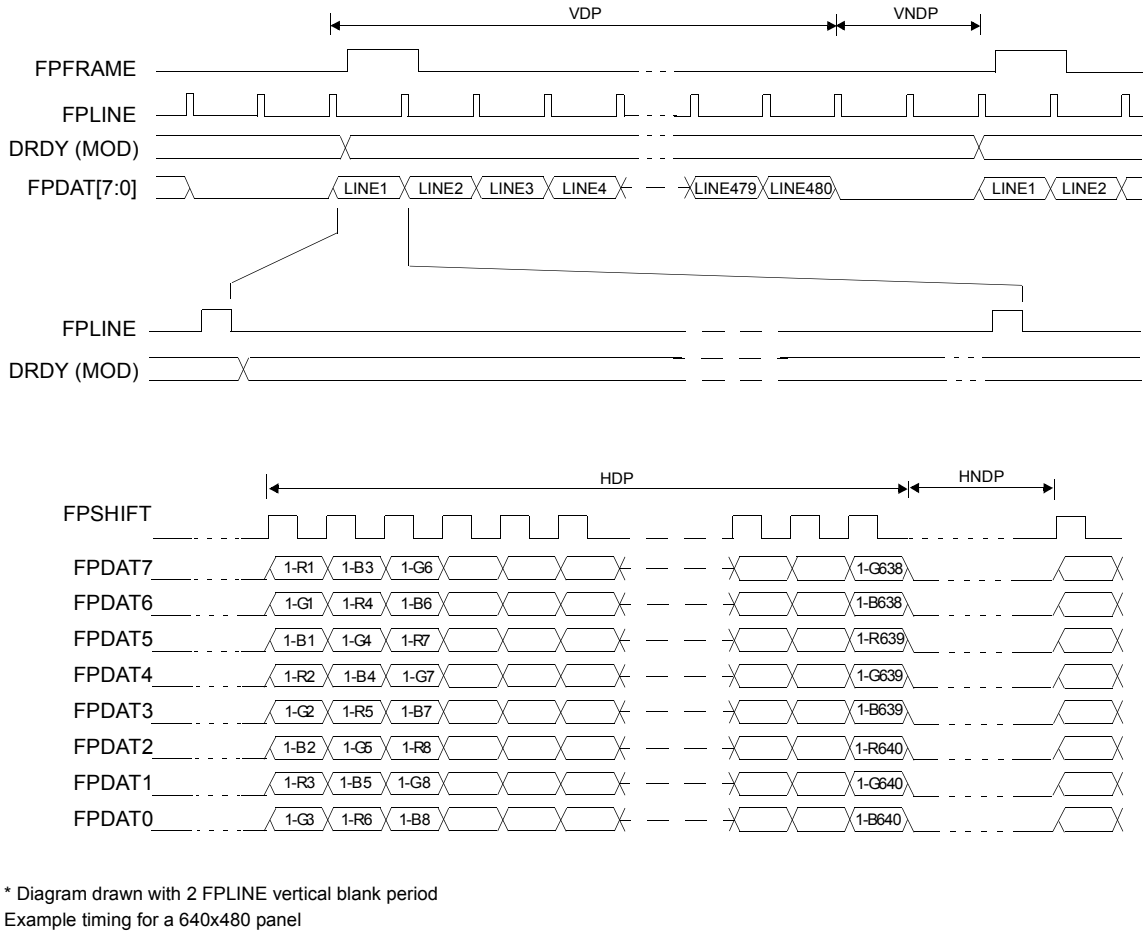


Figure 7-19: Single Color 8-Bit Panel Timing (Format 2)

VDP =	Vertical Display Period	= (REG[06h] bits 1-0, REG[05h] bits 7-0) + 1 Lines
VNDP =	Vertical Non-Display Period	= REG[0Ah] bits 5-0 Lines
HDP =	Horizontal Display Period	= ((REG[04h] bits 6-0) + 1) x 8Ts
HNDP =	Horizontal Non-Display Period	= (REG[08h] + 4) x 8Ts

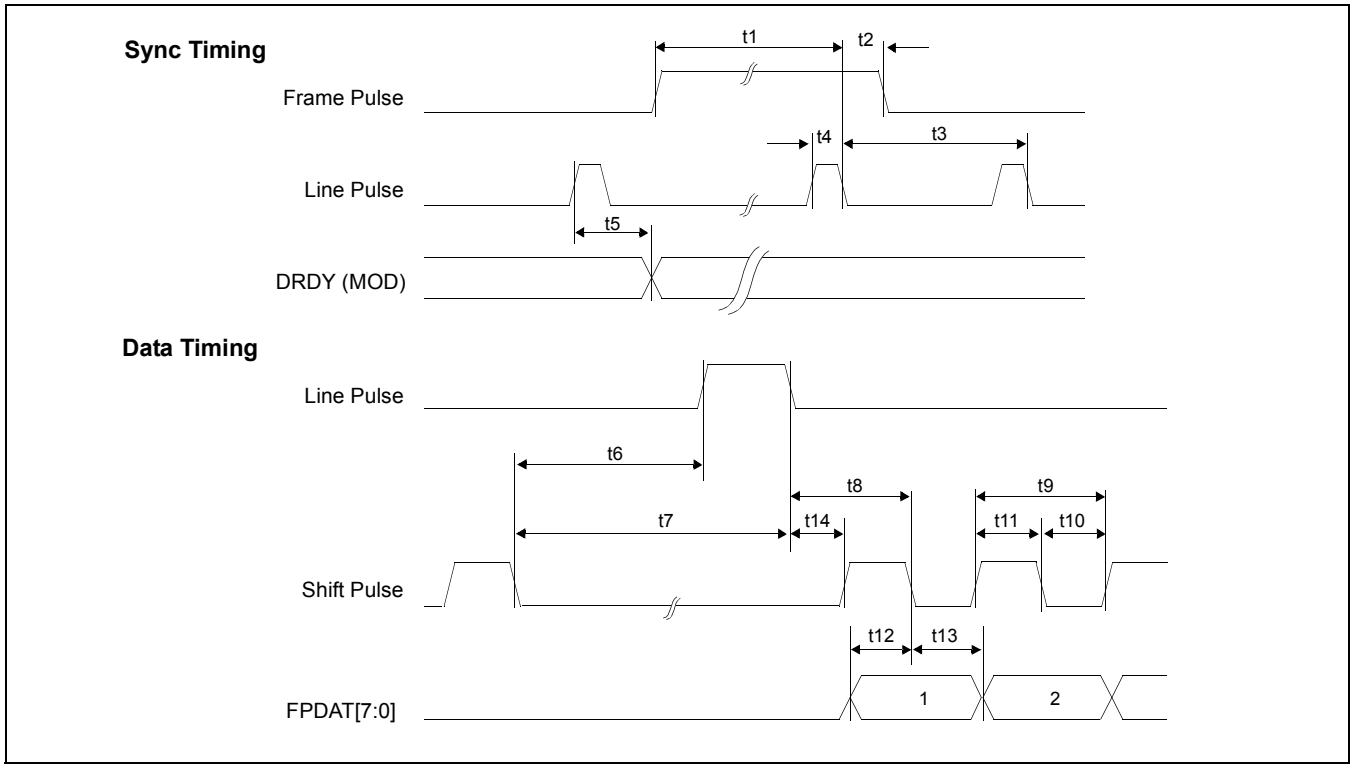


Figure 7-20: Single Color 8-Bit Panel A.C. Timing (Format 2)

Table 7-15: Single Color 8-Bit Panel A.C. Timing (Format 2)

Symbol	Parameter	Min	Typ	Max	Units
t1	Frame Pulse setup to Line Pulse falling edge	note 2			(note 1)
t2	Frame Pulse hold from Line Pulse falling edge	9			Ts
t3	Line Pulse period	note 3			
t4	Line Pulse pulse width	9			Ts
t5	MOD delay from Line Pulse rising edge	1			Ts
t6	Shift Pulse falling edge to Line Pulse rising edge	note 4			
t7	Shift Pulse falling edge to Line Pulse falling edge	note 5			
t8	Line Pulse falling edge to Shift Pulse falling edge	t14 + 2			Ts
t9	Shift Pulse period	2			Ts
t10	Shift Pulse pulse width low	1			Ts
t11	Shift Pulse pulse width high	1			Ts
t12	FPDAT[7:0] setup to Shift Pulse falling edge	1			Ts
t13	FPDAT[7:0] hold to Shift Pulse falling edge	1			Ts
t14	Line Pulse falling edge to Shift Pulse rising edge	23			Ts

1. Ts = pixel clock period
2. $t1_{min}$ = $t3_{min}$ - 9Ts
3. $t3_{min}$ = [((REG[04h] bits 6-0)+1) x 8 + ((REG[08h] bits 4-0) + 4) x 8]Ts
4. $t6_{min}$ = [(REG[08h] bits 4-0) x 8 + 1]Ts
5. $t7_{min}$ = [(REG[08h] bits 4-0) x 8 + 10]Ts

7.3.8 Dual Monochrome 8-Bit Panel Timing

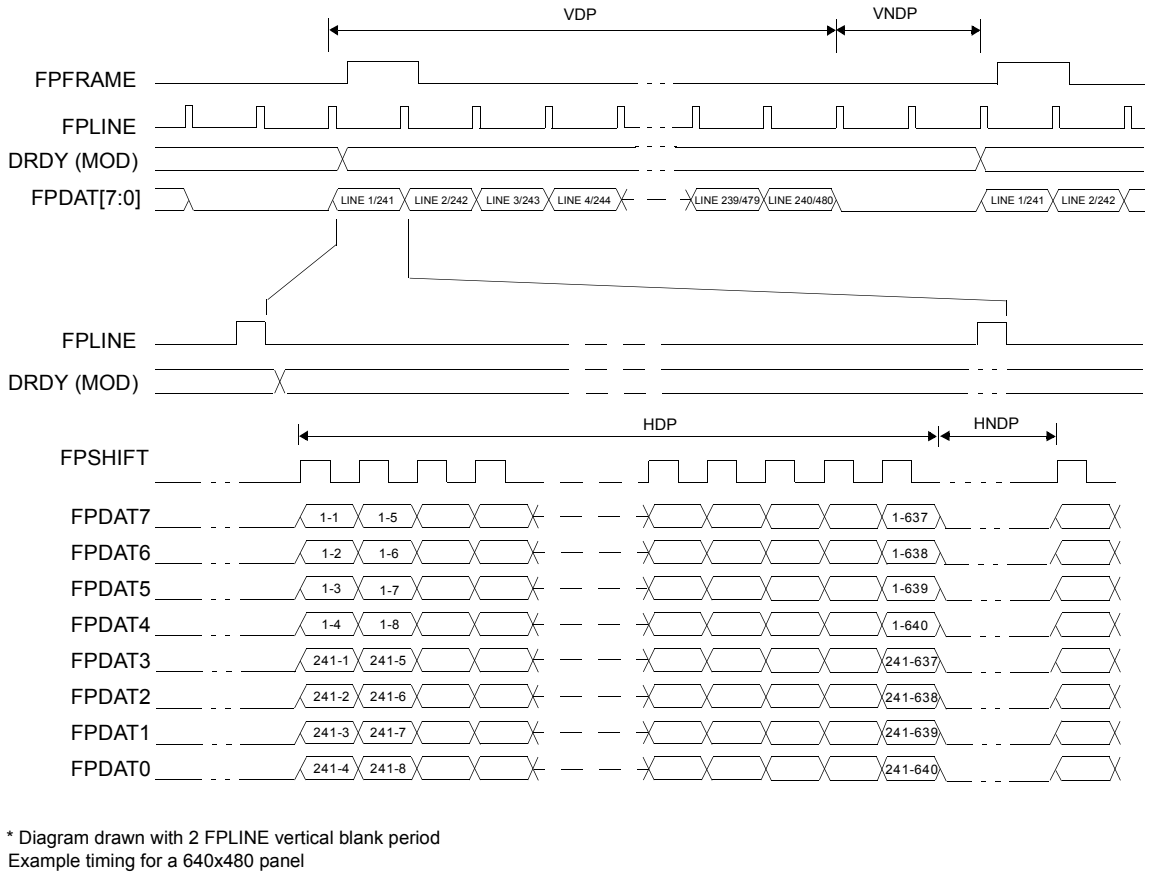


Figure 7-21: Dual Monochrome 8-Bit Panel Timing

VDP =	Vertical Display Period	= (REG[06h] bits 1-0, REG[05h] bits 7-0) + 1 Lines
VNDP =	Vertical Non-Display Period	= REG[0Ah] bits 5-0 Lines
HDP =	Horizontal Display Period	= ((REG[04h] bits 6-0) + 1) x 8Ts
HNDP =	Horizontal Non-Display Period	= (REG[08h] + 4) x 8Ts

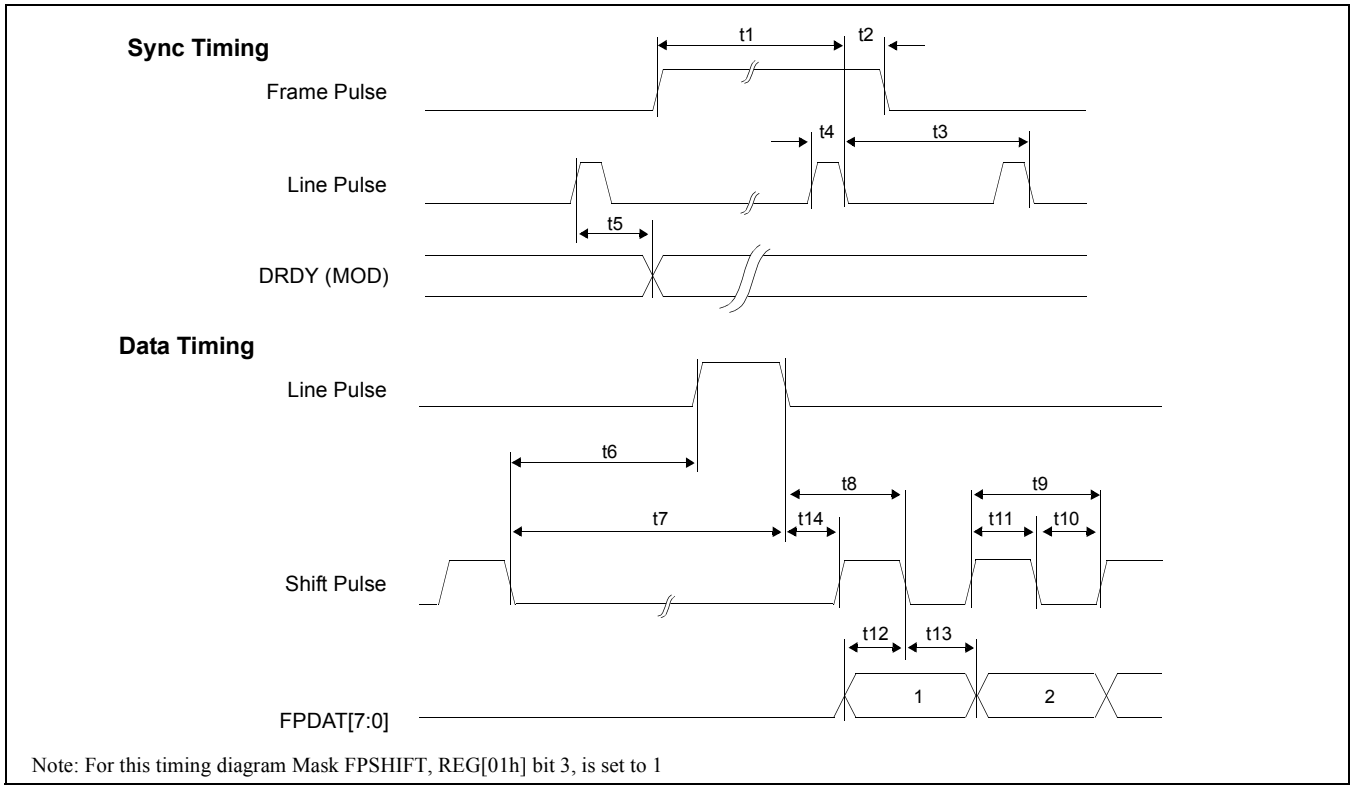


Figure 7-22: Dual Monochrome 8-Bit Panel A.C. Timing

Table 7-16: Dual Monochrome 8-Bit Panel A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Frame Pulse setup to Line Pulse falling edge	note 2			(note 1)
t2	Frame Pulse hold from Line Pulse falling edge	9			Ts
t3	Line Pulse period	note 3			
t4	Line Pulse pulse width	9			Ts
t5	MOD delay from Line Pulse falling edge	1			Ts
t6	Shift Pulse falling edge to Line Pulse rising edge	note 5			
t7	Shift Pulse falling edge to Line Pulse falling edge	note 6			
t8	Line Pulse falling edge to Shift Pulse falling edge	t14 + 2			Ts
t9	Shift Pulse period	8			Ts
t10	Shift Pulse pulse width low	4			Ts
t11	Shift Pulse pulse width high	4			Ts
t12	FPDAT[7:0] setup to Shift Pulse falling edge	4			Ts
t13	FPDAT[7:0] hold to Shift Pulse falling edge	4			Ts
t14	Line Pulse falling edge to Shift Pulse rising edge	39			Ts

1. Ts = pixel clock period
2. $t1_{min}$ = $t3_{min}$ - 9Ts
3. $t3_{min}$ = [(((REG[04h] bits 6-0)+1) x 8 + ((REG[08h] bits 4-0) + 4) x 8) x 2]Ts
5. $t6_{min}$ = [((REG[08h] bits 4-0) x 2)x 8 + 20]Ts
6. $t7_{min}$ = [((REG[08h] bits 4-0) x 2)x 8 + 29]Ts

7.3.9 Dual Color 8-Bit Panel Timing

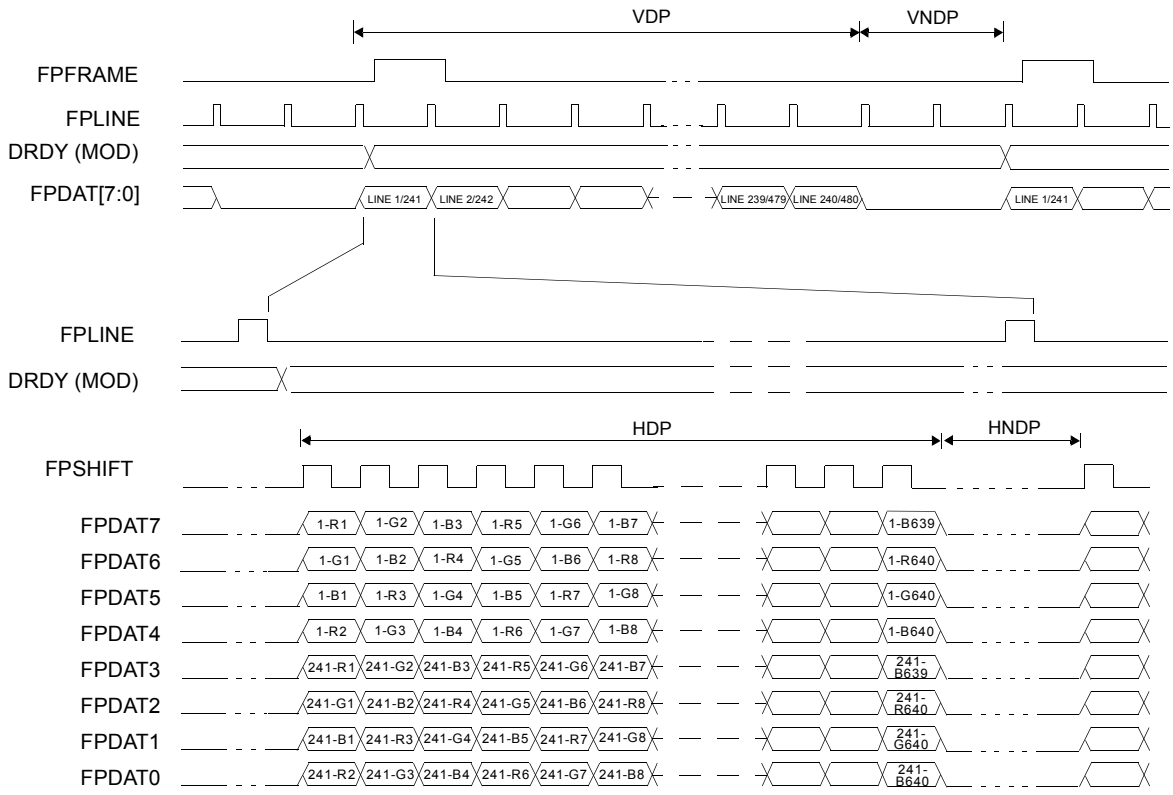


Figure 7-23: Dual Color 8-Bit Panel Timing

VDP =	Vertical Display Period	= (REG[06h] bits 1-0, REG[05h] bits 7-0) + 1 Lines
VNDP =	Vertical Non-Display Period	= REG[0Ah] bits 5-0 Lines
HDP =	Horizontal Display Period	= ((REG[04h] bits 6-0) + 1) x 8Ts
HNDP =	Horizontal Non-Display Period	= (REG[08h] + 4) x 8Ts

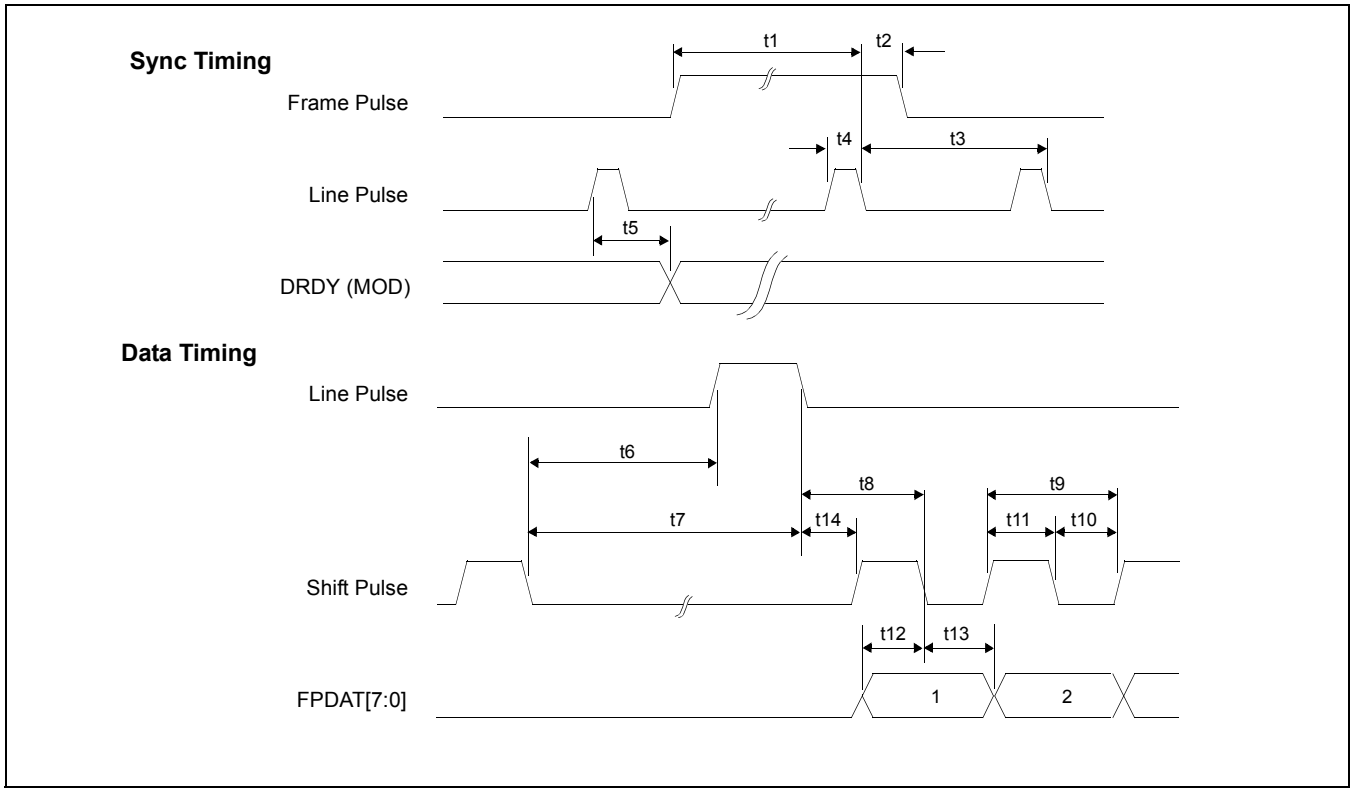


Figure 7-24: Dual Color 8-Bit Panel A.C. Timing

Table 7-17: Dual Color 8-Bit Panel A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Frame Pulse setup to Line Pulse falling edge	note 2			(note 1)
t2	Frame Pulse hold from Line Pulse falling edge	9			Ts
t3	Line Pulse period	note 3			
t4	Line Pulse pulse width	9			Ts
t5	MOD delay from Line Pulse falling edge	1			Ts
t6	Shift Pulse falling edge to Line Pulse rising edge	note 5			
t7	Shift Pulse falling edge to Line Pulse falling edge	note 6			
t8	Line Pulse falling edge to Shift Pulse falling edge	t14 + 1			Ts
t9	Shift Pulse period	2			Ts
t10	Shift Pulse pulse width low	1			Ts
t11	Shift Pulse pulse width high	1			Ts
t12	FPDAT[7:0] setup to Shift Pulse falling edge	1			Ts
t13	FPDAT[7:0] hold to Shift Pulse falling edge	1			Ts
t14	Line Pulse falling edge to Shift Pulse rising edge	39			Ts

1. Ts = pixel clock period
2. $t1_{min}$ = $t3_{min}$ - 9Ts
3. $t3_{min}$ = [(((REG[04h] bits 6-0)+1) x 8 + ((REG[08h] bits 4-0) + 4) x 8) x 2]Ts
5. $t6_{min}$ = [((REG[08h] bits 4-0) x 2)x 8 + 17]Ts
6. $t7_{min}$ = [((REG[08h] bits 4-0) x 2)x 8 + 26]Ts

7.3.10 9/12-Bit TFT/D-TFD Panel Timing

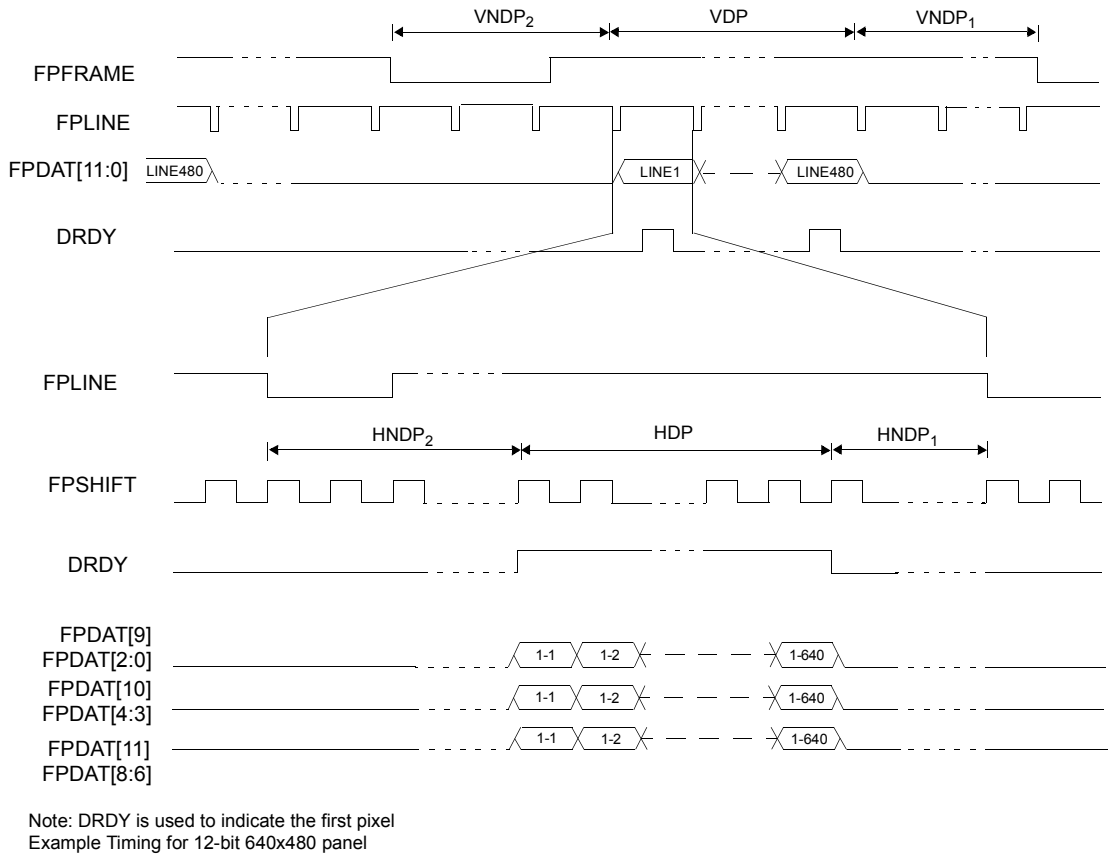


Figure 7-25: 12-Bit TFT/D-TFD Panel Timing

VDP =	Vertical Display Period	= (REG[06h] bits 1-0, REG[05h] bits 7-0) + 1 Lines
VNDP =	Vertical Non-Display Period	= VNDP1 + VNDP2 = (REG[0Ah] bits 5-0) Lines
VNDP1 =	Vertical Non-Display Period 1	= REG[09h] bits 5-0 Lines
VNDP2 =	Vertical Non-Display Period 2	= (REG[0Ah] bits 5-0) - (REG[09Ah] bits 5-0) Lines
HDP =	Horizontal Display Period	= ((REG[04h] bits 6-0) + 1) x 8Ts
HNDP =	Horizontal Non-Display Period	= HNDP1 + HNDP2 = (REG[08h] + 4) x 8Ts
HNDP1=	Horizontal Non-Display Period 1	= ((REG[07h] bits4-0) x 8) +16Ts
HNDP2=	Horizontal Non-Display Period 2	= (((REG[08h] bits4-0) - (REG[07h] bits 4-0)) x 8) +16Ts

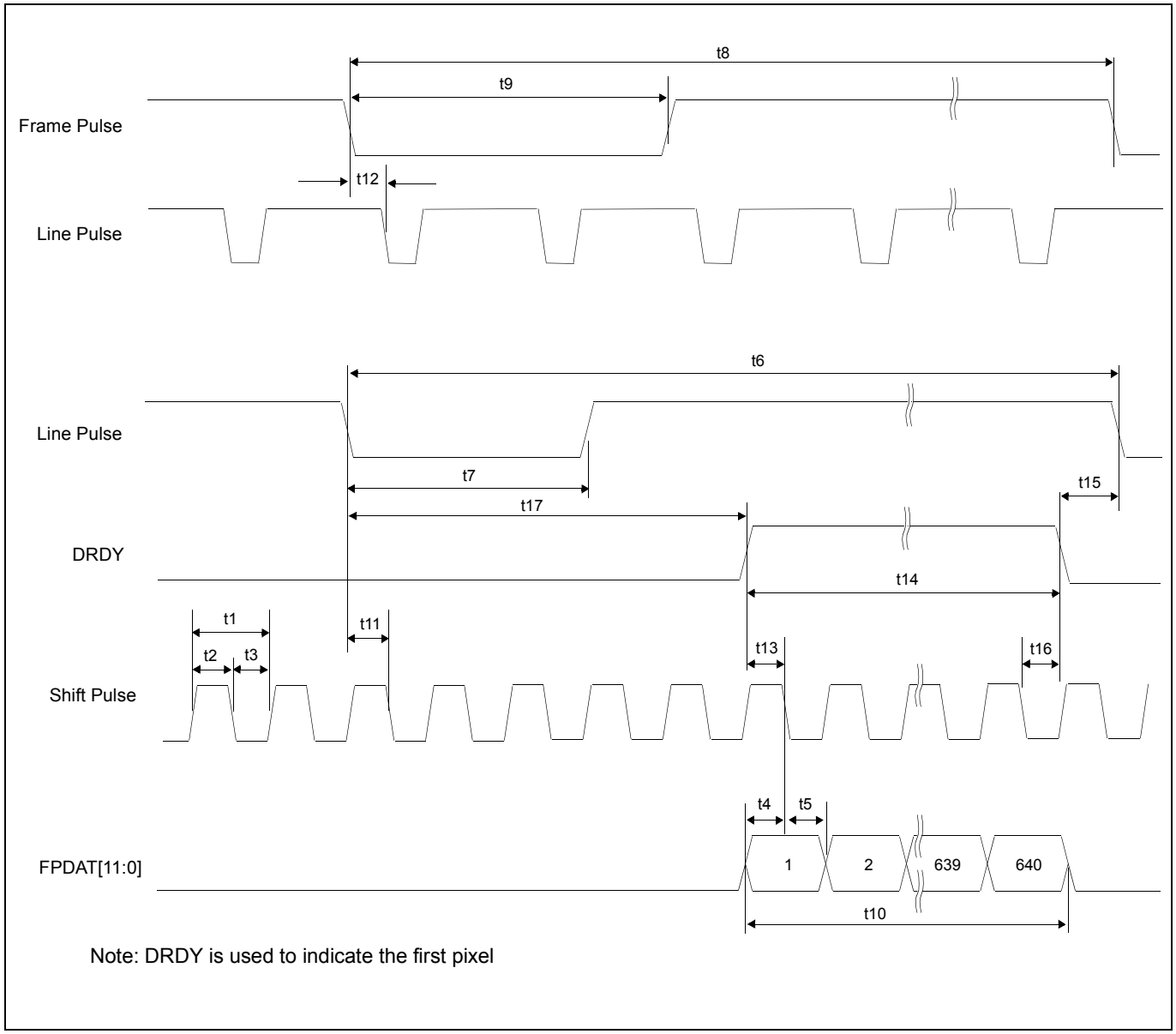


Figure 7-26: TFT/D-TFD A.C. Timing

Table 7-18: TFT/D-TFD A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Shift Pulse period	1			(note 1)
t2	Shift Pulse pulse width high	0.5			Ts
t3	Shift Pulse pulse width low	0.5			Ts
t4	data setup to Shift Pulse falling edge	0.5			Ts
t5	data hold from Shift Pulse falling edge	0.5			Ts
t6	Line Pulse cycle time	note 2			
t7	Line Pulse pulse width low	9			Ts
t8	Frame Pulse cycle time	note 3			
t9	Frame Pulse pulse width low	2t6			
t10	horizontal display period	note 4			
t11	Line Pulse setup to Shift Pulse falling edge	0.5			Ts
t12	Frame Pulse falling edge to Line Pulse falling edge phase difference	t6 - 18Ts			
t13	DRDY to Shift Pulse falling edge setup time	0.5			Ts
t14	DRDY pulse width	note 5			
t15	DRDY falling edge to Line Pulse falling edge	note 6			
t16	DRDY hold from Shift Pulse falling edge	0.5			Ts
t17	Line Pulse Falling edge to DRDY active	note 7		250	

1. Ts = pixel clock period
2. t6min = [((REG[04h] bits 6-0)+1) x 8 + ((REG[08h] bits 4-0)+4) x 8] Ts
3. t8 min = [((REG[06h] bits 1-0, REG[05h] bits 7-0)+1) + (REG[0Ah] bits 6-0)] Lines
4. t10min = [((REG[04h] bits 6-0)+1) x 8] Ts
5. t14min = [((REG[04h] bits 6-0)+1) x 8] Ts
6. t15min = [(REG[07h] bits 4-0) x 8 + 16] Ts
7. t17min = [(REG[08h] bits 4-0) - (REG[07]) x 8 + 16] Ts

8 Registers

8.1 Register Mapping

The S1D13705 registers are located in the upper 32 bytes of the 128K byte S1D13705 address range. The registers are accessible when CS# = 0 and AB[16:0] are in the range 1FFE0h through 1FFFFh.

8.2 Register Descriptions

Unless specified otherwise, all register bits are reset to 0 during power up.
All bits marked n/a should be programmed 0.

REG[00h] Revision Code Register
Address = 1FFE0h — Read Only.

Product Code Bit 5	Product Code Bit 4	Product Code Bit 3	Product Code Bit 2	Product Code Bit 1	Product Code Bit 0	Revision Code Bit 1	Revision Code Bit 0

bits 7-2 Product Code
This is a read-only register that indicates the product code of the chip. The product code is 001001.

bits 1-0 Revision Code
This is a read-only register that indicates the revision code of the chip. The revision code is 00.

REG[01h] Mode Register 0
Address = 1FFE1h — Read/Write.

TFT/STN	Dual/Single	Color/Mono	FPLine Polarity	FPFrame Polarity	Mask FPSHIFT	Data Width Bit 1	Data Width Bit 0

bit 7 TFT/STN
When this bit = 0, STN (passive) panel mode is selected. When this bit = 1, TFT/D-TFD panel mode is selected. If TFT/D-TFD panel mode is selected, Dual/Single (REG[01h] bit 6) and Color/Mono (REG[01h] bit5) are ignored. See Table 8-1: “Panel Data Format” for a comprehensive description of panel selection.

bit 6 Dual/Single
When this bit = 0, Single LCD panel drive is selected. When this bit = 1, Dual LCD panel drive is selected. See Table 8-1: “Panel Data Format” for a comprehensive description of panel selection.

bit 5 Color/Mono
When this bit = 0, Monochrome LCD panel drive is selected. When this bit = 1, Color LCD panel drive is selected. See Table 8-1: “Panel Data Format” for a comprehensive description of panel selection.

bit 4 FPLINE Polarity
This bit controls the polarity of FPLINE in TFT/D-TFD mode (no effect in passive panel mode). When this bit = 0, FPLINE is active low. When this bit = 1, FPLINE is active high.

bit 3 FPFRAME Polarity
This bit controls the polarity of FPFRAME in TFT/D-TFD mode (no effect in passive panel mode). When this bit = 0, FPFRAME is active low. When this bit = 1, FPFRAME is active high.

bit 2 Mask FPSHIFT
FPSHIFT is masked during non-display periods if either of the following two criteria is met:

1. Color passive panel is selected (REG[01h] bit 5 = 1)
2. This bit (REG[01h] bit 2) = 1

bits 1-0 Data Width Bits [1:0]
These bits select the display data format. See Table 8-1: "Panel Data Format" below for a comprehensive description of panel selection.

Table 8-1: Panel Data Format

TFT/STN REG[01h] bit 7	Color/Mono REG[01h] bit 5	Dual/Single REG[01h] bit 6	Data Width Bit 1 REG[01h] bit 1	Data Width Bit 0 REG[01h] bit 0	Function
0	0	0	0	0	Mono Single 4-bit passive LCD
				1	Mono Single 8-bit passive LCD
			1	0	reserved
				1	reserved
		1	0	0	reserved
				1	Mono Dual 8-bit passive LCD
			1	0	reserved
				1	reserved
	1	0	0	0	Color Single 4-bit passive LCD
				1	Color Single 8-bit passive LCD format 1
			1	0	reserved
				1	Color Single 8-bit passive LCD format 2
		1	0	0	reserved
				1	Color Dual 8-bit passive LCD
			1	0	reserved
				1	reserved
1	X (don't care)			0	9-bit TFT/D-TFD panel
				1	12-bit TFT/D-TFD panel

REG[02h] Mode Register 1 Address = 1FFE2h							Read/Write.
Bit-Per-Pixel Bit 1	Bit-Per-Pixel Bit 0	High Performance	Input Clock divide (CLKI/2)	Display Blank	Frame Repeat	Hardware Video Invert Enable	Software Video Invert

bits 7-6 Bit-Per-Pixel Bits [1:0]

These bits select the color or gray-scale depth (Display Mode).

Table 8-2: Gray Scale/Color Mode Selection

Color/Mono REG[01h] bit 5	Bit-Per-Pixel Bit 1 REG[02h] bit 7	Bit-Per-Pixel Bit 0 REG[02h] bit 6	Display Mode	
0	0	0	2 Gray scale	1 bit-per-pixel
		1	4 Gray scale	2 bit-per-pixel
	1	0	16 Gray scale	4 bit-per-pixel
		1	reserved	
1	0	0	2 Colors	1 bit-per-pixel
		1	4 Colors	2 bit-per-pixel
	1	0	16 Colors	4 bit-per-pixel
		1	256 Colors	8 bit-per-pixel

bit 5 High Performance (Landscape Modes Only)

When this bit = 0, the internal Memory Clock (MCLK) is a divided-down version of the Pixel Clock (PCLK). The denominator is dependent on the bit-per-pixel mode - see the table below.

Table 8-3: High Performance Selection

High Performance	BPP Bit 1	BPP Bit 0	Display Modes	
0	0	0	MClk = PClk/8	1 bit-per-pixel
		1	MClk = PClk/4	2 bit-per-pixel
	1	0	MClk = PClk/2	4 bit-per-pixel
		1	MClk = PClk	8 bit-per-pixel
1	X	X	MClk = PClk	

When this bit = 1, MCLK is fixed to the same frequency as PCLK for all bit-per-pixel modes. This provides a faster screen update performance in 1/2/4 bit-per-pixel modes, but also increases power consumption. This bit can be set to 1 just before a major screen update, then set back to 0 to save power after the update. This bit has no effect in Swivel-View mode. Refer to REG[1Bh] SwivelView Mode Register on page 66 for SwivelView mode clock selection.

bit 4 Input Clock Divide
When this bit = 0, the Operating Clock(CLK) is the same as the Input Clock (CLKI). When this bit = 1, CLK = CLKI/2.

In landscape mode PCLK=CLK and MCLK is selected as per Table 8-3: “High Performance Selection”.

In SwivelView mode, MCLK and PCLK are derived from CLK as shown in Table 8-8: “Selection of PCLK and MCLK in SwivelView Mode,” on page 67.

bit 3 Display Blank
This bit blanks the display image. When this bit = 1, the display is blanked (FPDAT lines to the panel are driven low). When this bit = 0, the display is enabled.

bit 2 Frame Repeat (EL support)
This feature is used to improve Frame Rate Modulation of EL panels. When this bit = 1, an internal frame counter runs from 0 to 3FFFFh. When the frame counter rolls over, the modulated image pattern is repeated (every 1 hour when the frame rate is 72Hz). When this bit = 0, the modulated image pattern is never repeated.

bit 1 Hardware Video Invert Enable
In passive panel modes (REG[01h] bit 7 = 0) FPDAT11 is available as either GPIO4 or hardware video invert. When this bit = 1, Hardware Video Invert is enabled via the FPDAT11 pin. When this bit = 0, FPDAT11 operates as GPIO4. See Table 8-4: “Inverse Video Mode Select Options” below.

Note
Video data is inverted after the Look-Up Table.

bit 0 Software Video Invert
When this bit = 1, Inverse Video Mode is selected. When this bit = 0, Standard Video Mode is selected. See Table 8-4: “Inverse Video Mode Select Options” below.

Note
Video data is inverted after the Look-Up Table.

Table 8-4: Inverse Video Mode Select Options

Hardware Video Invert Enable	Software Video Invert (Passive and Active Panels)	FPDAT11 (Passive Panels Only)	Video Data
0	0	X	Normal
0	1	X	Inverse
1	X	0	Normal
1	X	1	Inverse

REG[03h] Mode Register 2 Address = 1FFE3h							Read/Write
n/a	n/a	n/a	n/a	LCDPWR Override	Hardware Power Save Enable	Software Power Save Bit 1	Software Power Save Bit 0

bit 3 LCDPWR Override

This bit is used to override the panel on/off sequencing logic. When this bit = 0, LCDPWR and the panel interface signals are controlled by the sequencing logic. When this bit 1, LCDPWR is forced to off and the panel interface signals are forced low immediately upon entering power save mode. See Section 7.3.2, “Power Down/Up Timing” on page 36 for further information.

bit 2 Hardware Power Save Enable

When this bit = 1 GPIO0 is used as the Hardware Power Save input pin. When this bit = 0, GPIO0 operates normally.

Table 8-5: Hardware Power Save/GPIO0 Operation

RESET# State	Hardware Power Save Enable REG[03h] bit 2	GPIO0 Config REG[18h] bit 0	GPIO0 Status/Control REG[19h] bit 0	GPIO0 Operation
0	X	X	X	
1	0	0	reads pin status	GPIO0 Input (high impedance)
1	0	1	0	GPIO0 Output = 0
1	0	1	1	GPIO0 Output = 1
1	1	X	X	Hardware Power Save Input (active high)

bits 1-0 Software Power Save Bits [1: 0]

These bits select the Power Save Mode as shown in the following table.

Table 8-6: Software Power Save Mode Selection

Bit 1	Bit 0	Mode
0	0	Software Power Save
0	1	reserved
1	0	reserved
1	1	Normal Operation

Refer to Section 13, “Power Save Modes” on page 82 for a complete description of the power save modes.

REG[04h] Horizontal Panel Size Register Address = 1FFE4h							Read/Write
n/a	Horizontal Panel Size Bit 6	Horizontal Panel Size Bit 5	Horizontal Panel Size Bit 4	Horizontal Panel Size Bit 3	Horizontal Panel Size Bit 2	Horizontal Panel Size Bit 1	Horizontal Panel Size Bit 0

bits 6-0 Horizontal Panel Size Bits [6:0]

This register determines the horizontal resolution of the panel. This register must be programmed with a value calculated as follows:

$$\text{HorizontalPanelSizeRegister} = \left(\frac{\text{HorizontalPanelResolution(pixels)}}{8}\right) - 1$$

Note

This register must not be set to a value less than 03h.

REG[05h] Vertical Panel Size Register (LSB) Address = 1FFE5h							Read/Write
Vertical Panel Size Bit 7	Vertical Panel Size Bit 6	Vertical Panel Size Bit 5	Vertical Panel Size Bit 4	Vertical Panel Size Bit 3	Vertical Panel Size Bit 2	Vertical Panel Size Bit 1	Vertical Panel Size Bit 0

.

REG[06h] Vertical Panel Size Register (MSB) Address = 1FFE6h							Read/Write
n/a	n/a	n/a	n/a	n/a	n/a	Vertical Panel Size Bit 9	Vertical Panel Size Bit 8

REG[05h] bits 7-0 Vertical Panel Size Bits [9:0]

REG[06h] bits 1-0 This 10-bit register determines the vertical resolution of the panel. This register must be programmed with a value calculated as follows:

$$\text{VerticalPanelSizeRegister} = \text{VerticalPanelResolution(lines)} - 1$$

3FFh is the maximum value of this register for a vertical resolution of 1024 lines.

REG[07h] FPLINE Start Position Address = 1FFE7h							Read/Write
n/a	n/a	n/a	FPLINE Start Position Bit 4	FPLINE Start Position Bit 3	FPLINE Start Position Bit 2	FPLINE Start Position Bit 1	FPLINE Start Position Bit 0

bits 4-0 FPLINE Start Position

These bits are used in TFT/D-TFD mode to specify the position of the FPLINE pulse. These bits specify the delay, in 8-pixel resolution, from the end of a line of display data (FPDAT) to the leading edge of FPLINE. This register is effective in TFT/D-TFD mode only (REG[01h] bit 7 = 1). This register is programmed as follows:

$$FPLINEposition(pixels) = (REG[07h] + 2) \times 8$$

The following constraint must be satisfied:

$$REG[07h] \leq REG[08h]$$

REG[08h] Horizontal Non-Display Period Address = 1FFE8h							Read/Write
n/a	n/a	n/a	Horizontal Non-Display Period Bit 4	Horizontal Non-Display Period Bit 3	Horizontal Non-Display Period Bit 2	Horizontal Non-Display Period Bit 1	Horizontal Non-Display Period Bit 0

bits 4-0 Horizontal Non-Display Period

These bits specify the horizontal non-display period in 8-pixel resolution.

$$HorizontalNonDisplayPeriod(pixels) = (REG[08h] + 4) \times 8$$

REG[09h] FPFRAME Start Position Address = 1FFE9h							Read/Write
n/a	n/a	FPFRAME Start Position Bit 5	FPFRAME Start Position Bit 4	FPFRAME Start Position Bit 3	FPFRAME Start Position Bit 2	FPFRAME Start Position Bit 1	FPFRAME Start Position Bit 0

bits 5-0 FPFRAME Start Position

These bits are used in TFT/D-TFD mode to specify the position of the FPFRAME pulse. These bits specify the number of lines between the last line of display data (FPDAT) and the leading edge of FPFRAME. This register is effective in TFT/D-TFD mode only (REG[01h] bit 7 = 1). This register is programmed as follows:

$$FPFRAMEposition(lines) = REG[09h]$$

The contents of this register must be greater than zero and less than or equal to the Vertical Non-Display Period Register, i.e.

$$1 \leq REG[09h] \leq REG[0Ah]Bits\ 5{:}0$$

REG[0Ah] Vertical Non-Display Period Address = 1FFEAh							Read/Write
Vertical Non-Display Status	n/a	Vertical Non-Display Period Bit 5	Vertical Non-Display Period Bit 4	Vertical Non-Display Period Bit 3	Vertical Non-Display Period Bit 2	Vertical Non-Display Period Bit 1	Vertical Non-Display Period Bit 0

bit 7 Vertical Non-Display Status
This bit =1 during the Vertical Non-Display period.

bits 5-0 Vertical Non-Display Period
These bits specify the vertical non-display period. This register is programmed as follows:

VerticalNonDisplayPeriod(lines) = REG[0Ah] bits [5:0]

Note
This register should be set only once, on power-up during initialization.

.

REG[0Bh] MOD Rate Register Address = 1FFEBh							Read/Write
n/a	n/a	MOD Rate Bit 5	MOD Rate Bit 4	MOD Rate Bit 3	MOD Rate Bit 2	MOD Rate Bit 1	MOD Rate Bit 0

bits 5-0 MOD Rate Bits [5:0]
When the value of this register is 0, the MOD output signal toggles every FPFRAME. For a non-zero value, the value in this register + 1 specifies the number of FPLINEs between toggles of the MOD output signal. These bits are for passive LCD panels only.

REG[0Ch] Screen 1 Start Address Register (LSB)							
Address = 1FFECh							Read/Write
Screen 1 Start Address Bit 7	Screen 1 Start Address Bit 6	Screen 1 Start Address Bit 5	Screen 1 Start Address Bit 4	Screen 1 Start Address Bit 3	Screen 1 Start Address Bit 2	Screen 1 Start Address Bit 1	Screen 1 Start Address Bit 0

REG[0Dh] Screen 1 Start Address Register (MSB)							
Address = 1FFEDh							Read/Write
Screen 1 Start Address Bit 15	Screen 1 Start Address Bit 14	Screen 1 Start Address Bit 13	Screen 1 Start Address Bit 12	Screen 1 Start Address Bit 11	Screen 1 Start Address Bit 10	Screen 1 Start Address Bit 9	Screen 1 Start Address Bit 8

REG[0Dh] bits 7-0 Screen 1 Start Address Bits [15:0]

REG[0Ch] bits 7-0 These bits determine the **word address** of the start of Screen 1 in Landscape modes or the **byte address** of the start of Screen 1 in SwivelView modes.

Note

For SwivelView mode the most significant bit (bit 16) is located in REG[10h].

REG[0Eh] Screen 2 Start Address Register (LSB)							
Address = 1FFEEh							Read/Write
Screen 2 Start Address Bit 7	Screen 2 Start Address Bit 6	Screen 2 Start Address Bit 5	Screen 2 Start Address Bit 4	Screen 2 Start Address Bit 3	Screen 2 Start Address Bit 2	Screen 2 Start Address Bit 1	Screen 2 Start Address Bit 0

REG[0Fh] Screen 2 Start Address Register (MSB)							
Address = 1FFEFh							Read/Write
Screen 2 Start Address Bit 15	Screen 2 Start Address Bit 14	Screen 2 Start Address Bit 13	Screen 2 Start Address Bit 12	Screen 2 Start Address Bit 11	Screen 2 Start Address Bit 10	Screen 2 Start Address Bit 9	Screen 2 Start Address Bit 8

REG[0Fh] bits 7-0 Screen 2 Start Address Bits [15:0]

REG[0Eh] bits 7-0 These bits determine the **word address** of the start of Screen 2 in Landscape modes only and has no effect in SwivelView modes.

REG[10h] Screen Start Address Overflow Register							
Address = 1FFF0h							Read/Write
n/a	n/a	n/a	n/a	n/a	n/a	n/a	Screen 1 Start Address Bit 16

bit 0 Screen 1 Start Address Bit 16

This bit is the most significant bit of Screen 1 Start Address for SwivelView mode. This bit has no effect in Landscape mode.

REG[11h] Memory Address Offset Register Address = 1FFF1h							Read/Write
Memory Address Offset Bit 7	Memory Address Offset Bit 6	Memory Address Offset Bit 5	Memory Address Offset Bit 4	Memory Address Offset Bit 3	Memory Address Offset Bit 2	Memory Address Offset Bit 1	Memory Address Offset Bit 0

bits 7-0 Memory Address Offset Bits [7:0] (Landscape Modes Only)

This register is used to create a virtual image by setting a word offset between the last address of one line and the first address of the following line. If this register is not equal to zero, then a virtual image is formed. The displayed image is a window into the larger virtual image. See Figure 8-1: "Screen-Register Relationship, Split Screen," on page 64.

This register has no effect in SwivelView modes. See "REG[1Ch] Line Byte Count Register for SwivelView Mode" on page 67.

.

REG[12h] Screen 1 Vertical Size Register (LSB) Address = 1FFF2h							Read/Write
Screen 1 Vertical Size Bit 7	Screen 1 Vertical Size Bit 6	Screen 1 Vertical Size Bit 5	Screen 1 Vertical Size Bit 4	Screen 1 Vertical Size Bit 3	Screen 1 Vertical Size Bit 2	Screen 1 Vertical Size Bit 1	Screen 1 Vertical Size Bit 0

REG[13h] Screen 1 Vertical Size Register (MSB) Address = 1FFF3h							Read/Write
n/a	n/a	n/a	n/a	n/a	n/a	Screen 1 Vertical Size Bit 9	Screen 1 Vertical Size Bit 8

REG[13h] bits 1-0 Screen 1 Vertical Size Bits [9:0]

REG[12h] bits 7-0 This register is used to implement the Split Screen feature of the S1D13705. These bits determine the height (in lines) of Screen 1.

In landscape modes, if this register is programmed with a value, n, where n is less than the Vertical Panel Size (REG[06h], REG[05h]), then lines 0 to n of the panel contain Screen 1 and lines n+1 to REG[06h], REG[05h] of the panel contain Screen 2. See Figure 8-1: "Screen-Register Relationship, Split Screen," on page 64. If Split Screen is not desired, this register must be programmed greater than, or equal to the Vertical Panel Size, REG[06h] and REG[05h].

In SwivelView modes this register must be programmed greater than, or equal to the Vertical Panel Size, REG[06h] and REG[05h]. See "SwivelView™" on page 77.

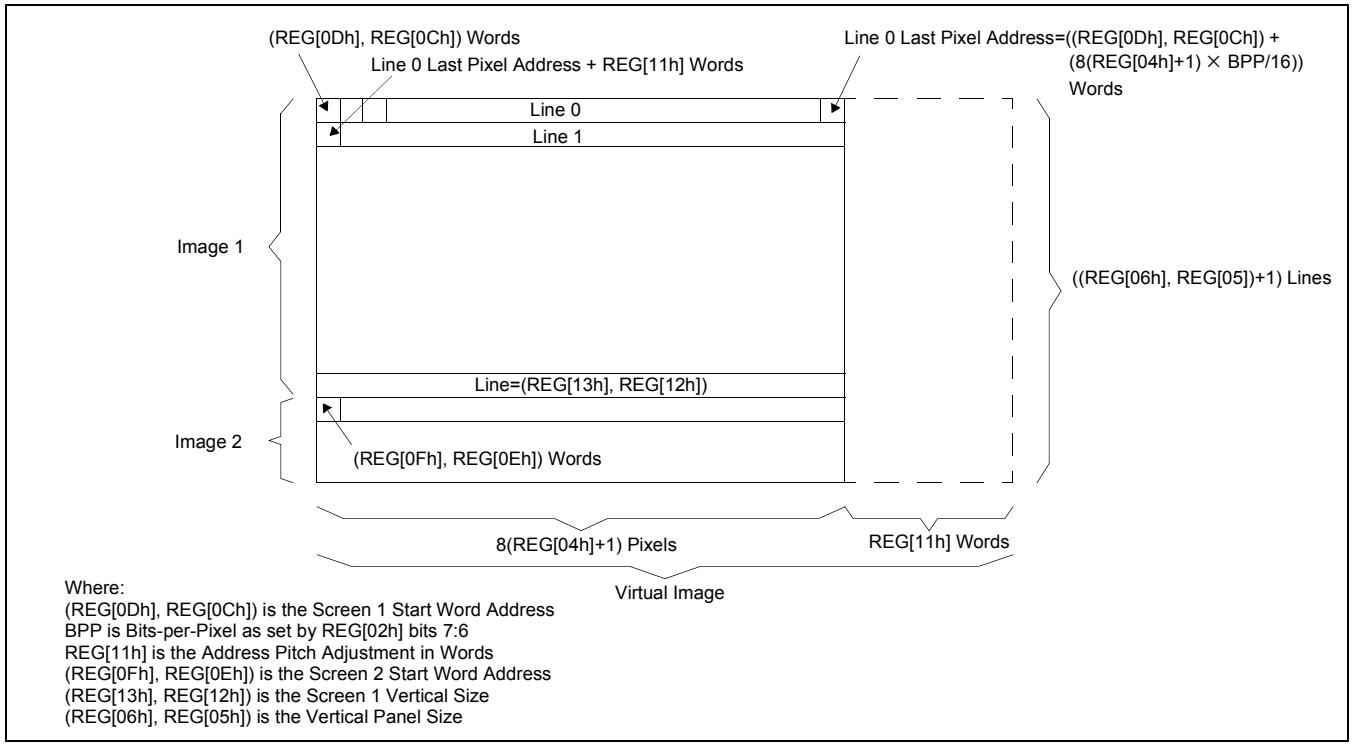


Figure 8-1: Screen-Register Relationship, Split Screen

Consider an example where REG[13h], REG[12] = 0CEh for a 320x240 display system. The upper 207 lines (CEh + 1) of the panel show an image from the Screen 1 Start Word Address. The remaining 33 lines show an image from the Screen 2 Start Word Address.

REG[15h] Look-Up Table Address Register
Address = 1FFF5h — Read/Write

LUT Address Bit 7	LUT Address Bit 6	LUT Address Bit 5	LUT Address Bit 4	LUT Address Bit 3	LUT Address Bit 2	LUT Address Bit 1	LUT Address Bit 0

bits 7-0 LUT Address Bits [7:0]

These 8 bits control a pointer into the Look-Up Tables (LUT). The S1D13705 has three 256-position, 4-bit wide LUTs, one for each of red, green, and blue – refer to Section 11, "Look-Up Table Architecture" on page 71 for details.

This register selects which LUT entry is read/write accessible through the LUT Data Register (REG[17h]). Writing the LUT Address Register automatically sets the pointer to the Red LUT. Accesses to the LUT Data Register automatically increment the pointer.

For example, writing a value 03h into the LUT Address Register sets the pointer to R[3]. A subsequent access to the LUT Data Register accesses R[3] and moves the pointer onto G[3]. Subsequent accesses to the LUT Data Register move the pointer onto B[3], R[4], G[4], B[4], R[5], etc.

Note
The RGB data is inserted into the LUT after the Blue data is written, i.e. all three colors must be written before the LUT is updated.

REG[17h] Look-Up Table Data Register Address = 1FFF7h							Read/Write
LUT Data Bit 3	LUT Data Bit 2	LUT Data Bit 1	LUT Data Bit 0	n/a	n/a	n/a	n/a

bits 7-4 LUT Data Bits [3:0]
This register is used to read/write the RGB Look-Up Tables. This register accesses the entry at the pointer controlled by the Look-Up Table Address Register (REG[15h]).

Accesses to the Look-Up Table Data Register automatically increment the pointer.

Note
The RGB data is inserted into the LUT after the Blue data is written, i.e. all three colors must be written before the LUT is updated.

REG[18h] GPIO Configuration Control Register Address = 1FFF8h							Read/Write
n/a	n/a	n/a	GPIO4 Pin IO Configuration	GPIO3 Pin IO Configuration	GPIO2 Pin IO Configuration	GPIO1 Pin IO Configuration	GPIO0 Pin IO Configuration

bits 4-0 GPIO[4:0] Pin IO Configuration
These bits determine the direction of the GPIO[4:0] pins.
When the GPIOn Pin IO Configuration bit = 0, the corresponding GPIOn pin is configured as an input. The input can be read at the GPIOn Status/Control Register bit. See REG[19h] GPIO Status/Control Register.

When the GPIOn Pin IO Configuration bit = 1, the corresponding GPIOn pin is configured as an output. The output can be controlled by writing the GPIOn Status/Control Register bit.

Note
These bits have no effect when the GPIOn pin is configured for a specific function (i.e. as FPDAT[11:8] for TFT/D-TFD operation).

When configured as IO, all unused pins must be tied to IO V_{DD}.

REG[19h] GPIO Status/Control Register Address = 1FFF9h							Read/Write
n/a	n/a	n/a	GPIO4 Pin IO Status	GPIO3 Pin IO Status	GPIO2 Pin IO Status	GPIO1 Pin IO Status	GPIO0 Pin IO Status

bits 4-0 GPIO[4:0] Status

When the GPIOn pin is configured as an input, the corresponding GPIO Status bit is used to read the pin input. See REG[18h] above.

When the GPIOn pin is configured as an output, the corresponding GPIO Status bit is used to control the pin output.

REG[1Ah] Scratch Pad Register Address = 1FFFAh							Read/Write
Scratch bit 7	Scratch bit 6	Scratch bit 5	Scratch bit 4	Scratch bit 3	Scratch bit 2	Scratch bit 1	Scratch bit 0

bits 7-0 Scratch Pad Register

This register contains general use read/write bits. These bits have no effect on hardware.

REG[1Bh] SwivelView Mode Register Address = 1FFFBh							Read/Write
SwivelView Mode Enable	SwivelView Mode Select	n/a	n/a	n/a	reserved	SwivelView Mode Pixel Clock Select Bit 1	SwivelView Mode Pixel Clock Select Bit 0

bit 7 SwivelView Mode Enable

When this bit = 1, SwivelView Mode is enabled. When this bit = 0, Landscape Mode is enabled.

bit 6 SwivelView Mode Select

When this bit = 0, Default SwivelView Mode is selected. When this bit = 1, Alternate SwivelView Mode is selected. See Section 12, “SwivelView™” on page 77 for further information on SwivelView Mode.

The following table shows the selection of SwivelView Mode.

Table 8-7: Selection of SwivelView Mode

SwivelView Mode Enable (REG[1Bh] bit 7)	SwivelView Mode Select (REG[1Bh] bit 6)	Mode
0	X	Landscape
1	0	Default SwivelView
1	1	Alternate SwivelView

bit 2 reserved
reserved bits must be set to 0.

bits 1-0 SwivelView Mode Pixel Clock Select Bits [1:0]
These two bits select the Pixel Clock (PCLK) source in SwivelView Mode - these bits have no effect in Landscape Mode. The following table shows the selection of PCLK and MCLK in SwivelView Mode - see Section 12, "SwivelView™" on page 77 for details.

Table 8-8: Selection of PCLK and MCLK in SwivelView Mode

SwivelView Mode Enable (REG[1Bh] bit 7)	SwivelView Mode Select (REG[1Bh] bit 6)	Pixel Clock (PCLK) Select (REG[1Bh] bits [1:0]		PCLK =	MCLK =
		Bit 1	Bit 0		
0	X	X	X	CLK	See Reg[02h] bit 5
1	0	0	0	CLK	CLK
1	0	0	1	CLK/2	CLK/2
1	0	1	0	CLK/4	CLK/4
1	0	1	1	CLK/8	CLK/8
1	1	0	0	CLK/2	CLK
1	1	0	1	CLK/2	CLK
1	1	1	0	CLK/4	CLK/2
1	1	1	1	CLK/8	CLK/4

Where CLK is CLKI (REG[02h] bit 4 = 0) or CLKI/2 (REG[02h] bit 4 = 1)

REG[1Ch] Line Byte Count Register for SwivelView Mode
Address = 1FFFCh Read/Write

Line Byte Count bit 7	Line Byte Count bit 6	Line Byte Count bit 5	Line Byte Count bit 4	Line Byte Count bit 3	Line Byte Count bit 2	Line Byte Count bit 1	Line Byte Count bit 0

bits 7-0 Line Byte Count Bits [7:0]
This register is the byte count from the beginning of one line to the beginning of the next consecutive line (commonly called "stride" by programmers). This register may be used to create a virtual image in SwivelView mode.

When this register = 00 the "stride" = 256 bytes. This value is used for 240x320 8 bpp default SwivelView mode

When the Line Byte Count Register = n, where 1 ≤ n ≤ FFh, the "stride" = n bytes.

REG[1Eh] and REG[1Fh]

REG[1Eh] and REG[1Fh] are reserved for factory S1D13705 testing and should not be written. Any value written to these registers may result in damage to the S1D13705 and/or any panel connected to the S1D13705.

9 Frame Rate Calculation

The following formulae are used to calculate the display frame rate.

TFT/D-TFD and Passive Single-Panel modes

$$\text{FrameRate} = \frac{f_{PCLK}}{(HDP + HNDP) \times (VDP + VNDP)}$$

Where: f_{PCLK} = PClk frequency (Hz)
HDP = Horizontal Display Period = ((REG[04h] bits 6-0) + 1) x 8 Pixels
HNDP = Horizontal Non-Display Period = ((REG[08h] bits 4-0) + 4) x 8 Pixels
VDP = Vertical Display Period = ((REG[06h] bits 1-0, REG[05h] bits 7-0) + 1) Lines
VNDP = Vertical Non-Display Period = (REG[0Ah] bits 5-0) Lines

Passive Dual-Panel mode

$$\text{FrameRate} = \frac{f_{PCLK}}{2 \times (HDP + HNDP) \times \left(\frac{VDP}{2} + VNDP\right)}$$

Where: f_{PCLK} = PClk frequency (Hz)
HDP = Horizontal Display Period = ((REG[04h] bits 6-0) + 1) x 8 Pixels
HNDP = Horizontal Non-Display Period = ((REG[08h] bits 4-0) + 4) x 8 Pixels
VDP = Vertical Display Period = ((REG[06h] bits 1-0, REG[05h] bits 7-0) + 1) Lines
VNDP = Vertical Non-Display Period = (REG[0Ah] bits 5-0) Lines

10 Display Data Formats

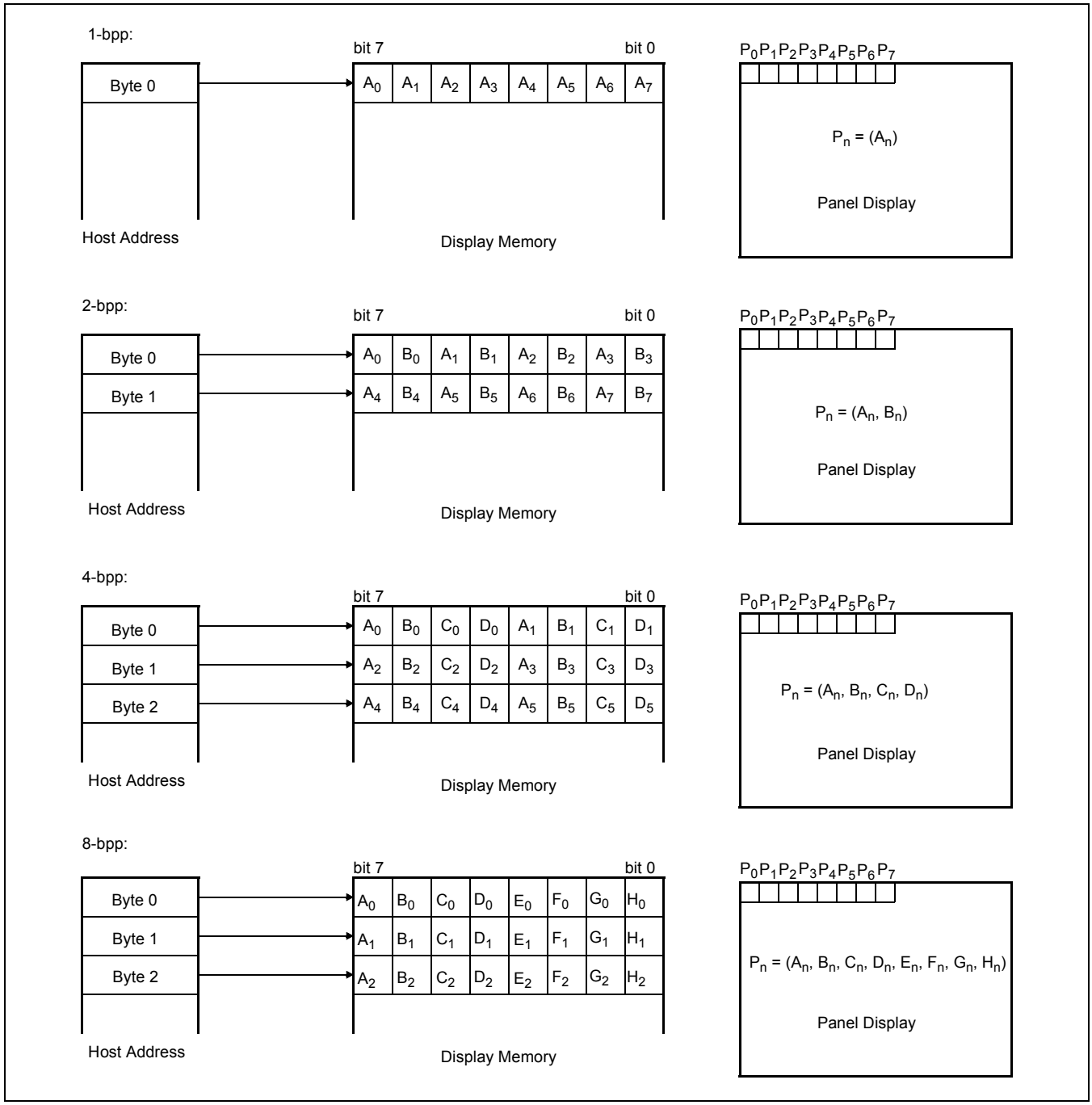


Figure 10-1: 1/2/4/8 Bit-Per-Pixel Display Data Memory Organization

11 Look-Up Table Architecture

The following figures are intended to show the display data output path only.

Note
When Video Data Invert is enabled the video data is inverted after the Look-Up Table.

11.1 Monochrome Modes

The green Look-Up Table (LUT) is used for all monochrome modes.

1 Bit-per-pixel Monochrome mode

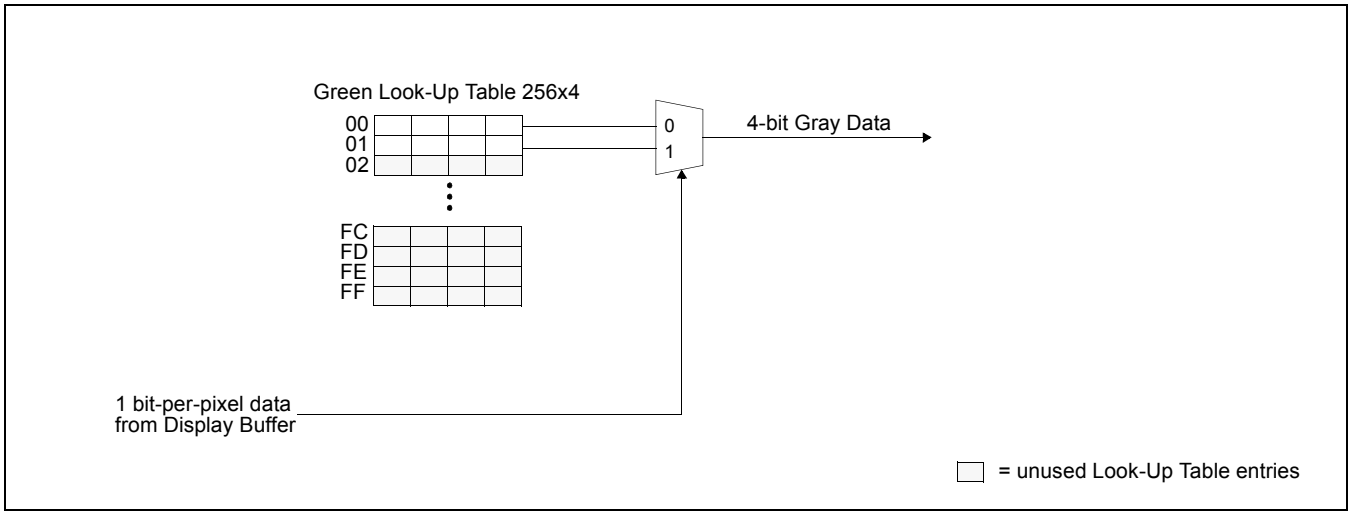


Figure 11-1: 1 Bit-per-pixel Monochrome Mode Data Output Path

2 Bit-per-pixel Monochrome Mode

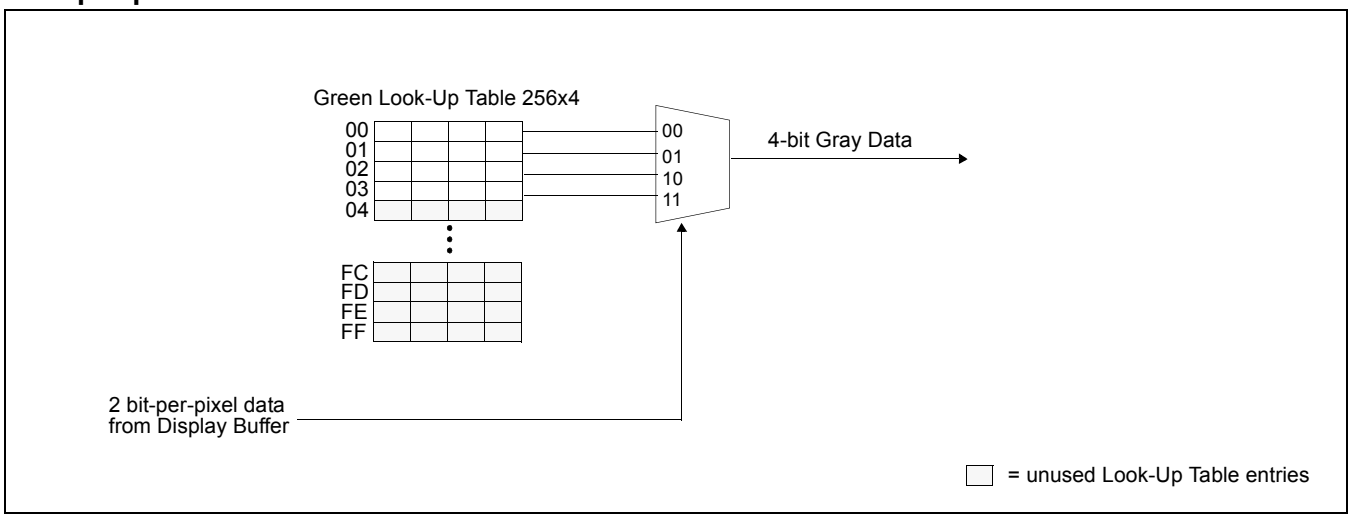


Figure 11-2: 2 Bit-per-pixel Monochrome Mode Data Output Path

4 Bit-per-pixel Monochrome Mode

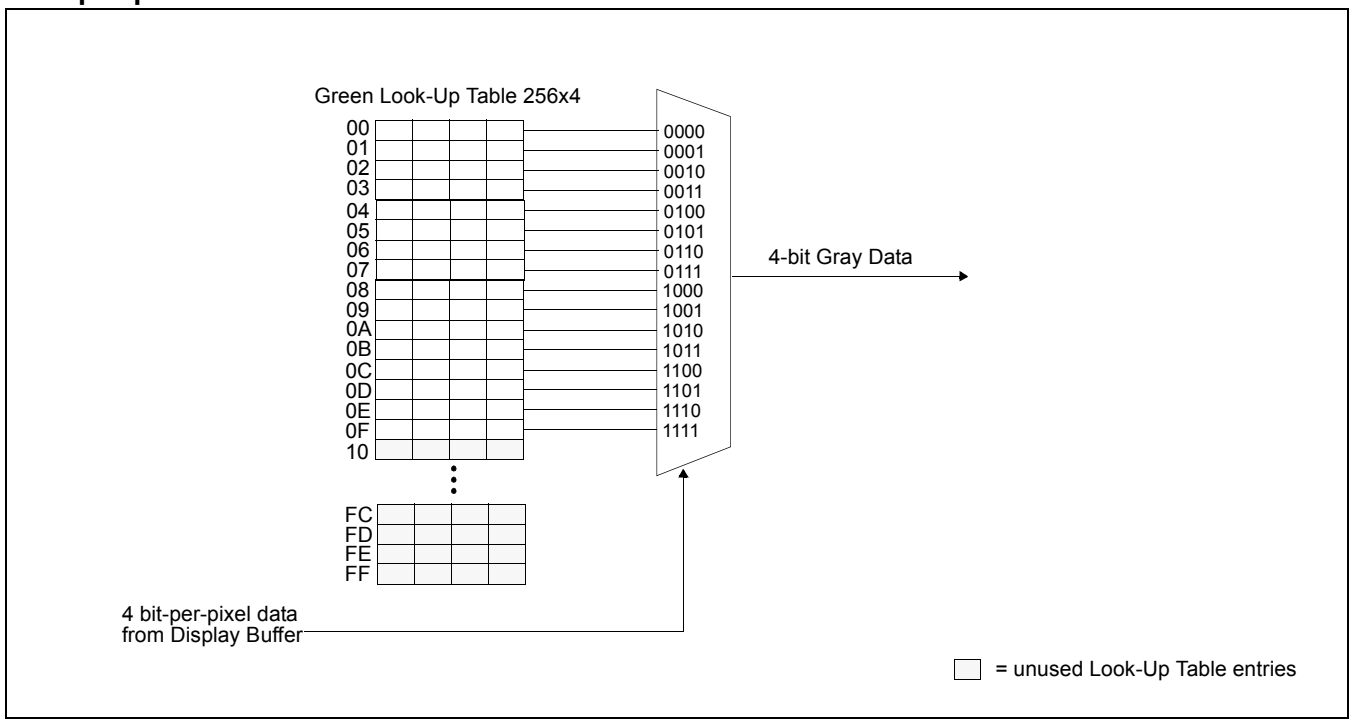


Figure 11-3: 4 Bit-per-pixel Monochrome Mode Data Output Path

11.2 Color Modes

1 Bit-per-pixel Color Mode

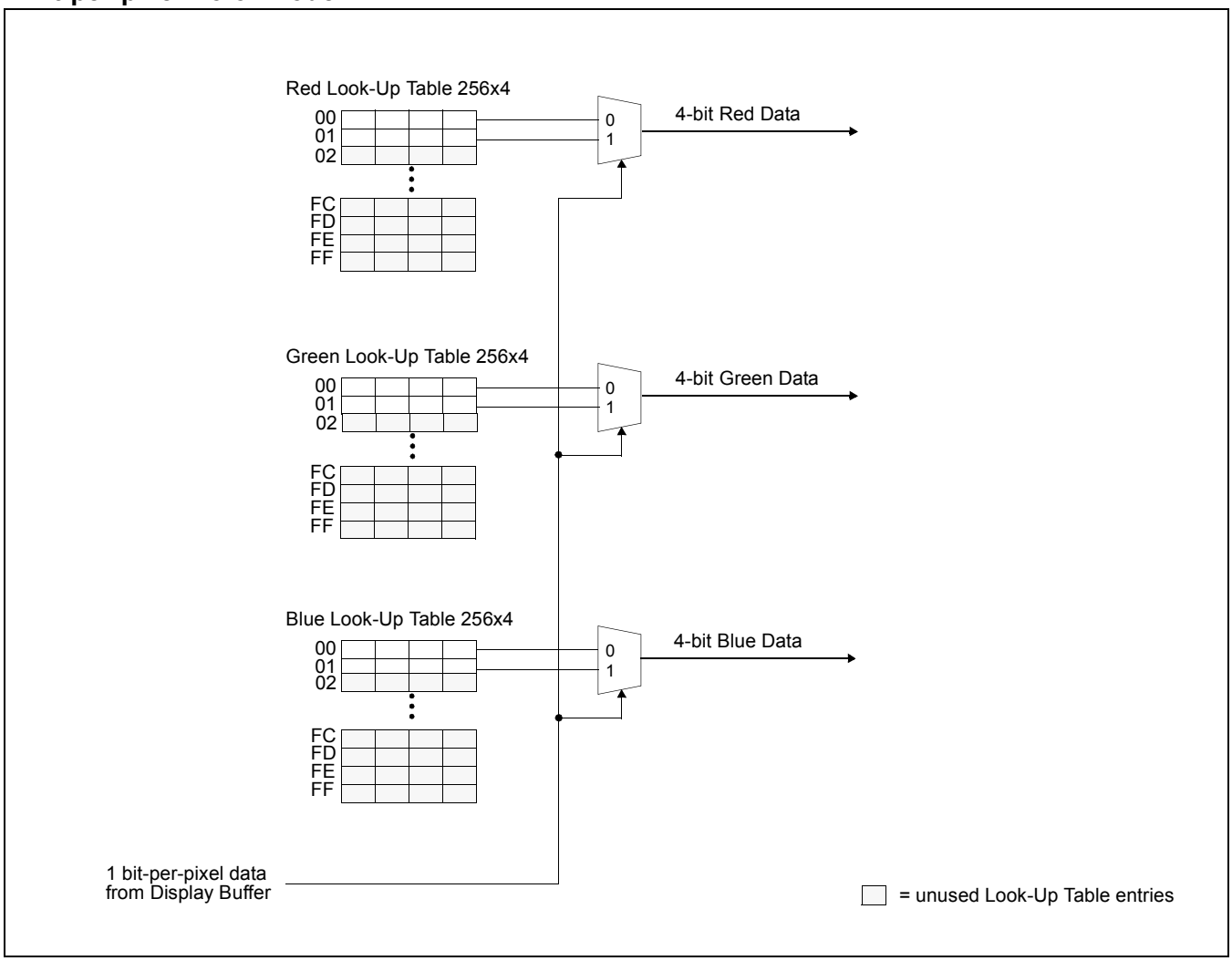


Figure 11-4: 1 Bit-per-pixel Color Mode Data Output Path

2 Bit-per-pixel Color Mode

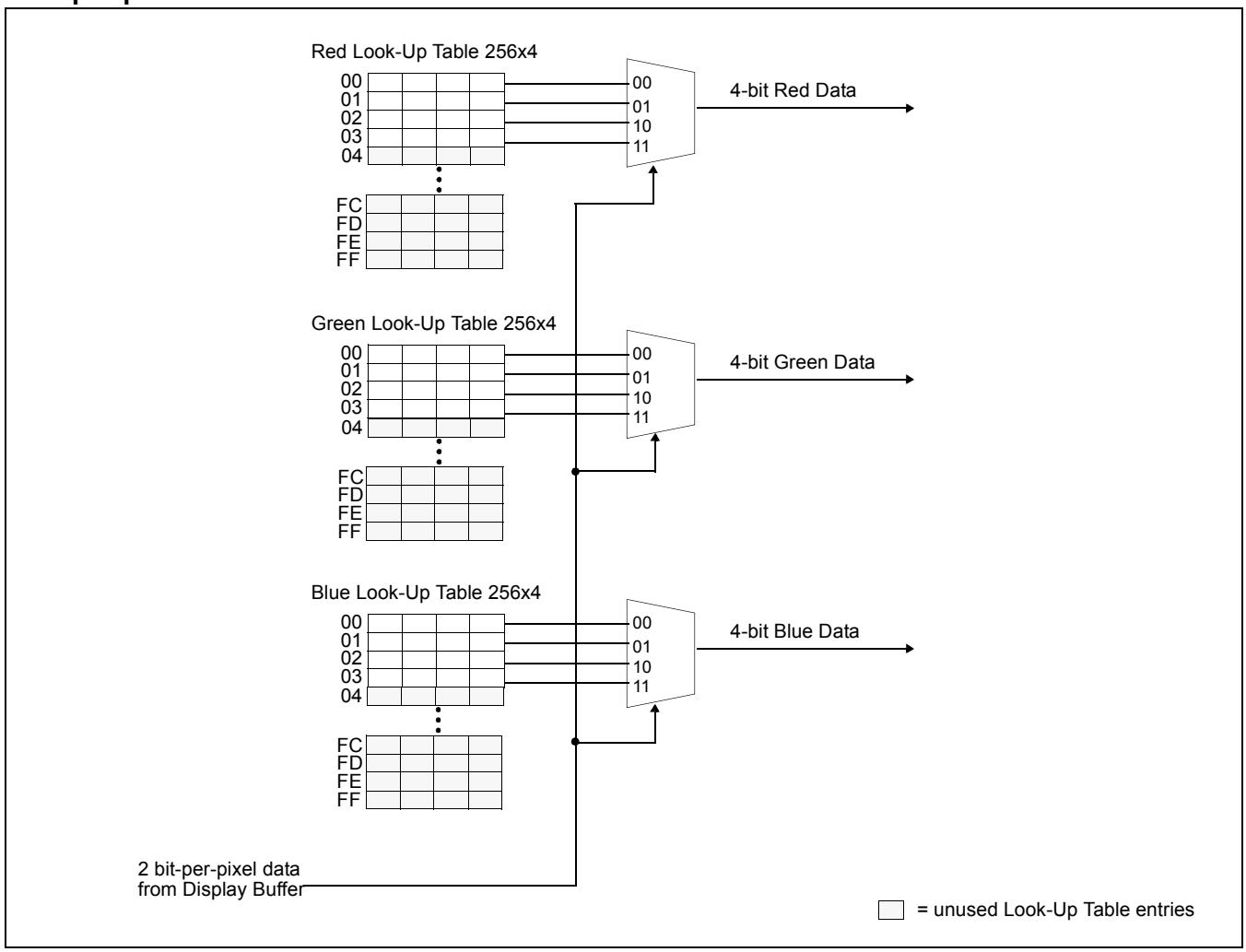


Figure 11-5: 2 Bit-per-pixel Color Mode Data Output Path

4 Bit-per-pixel Color Mode

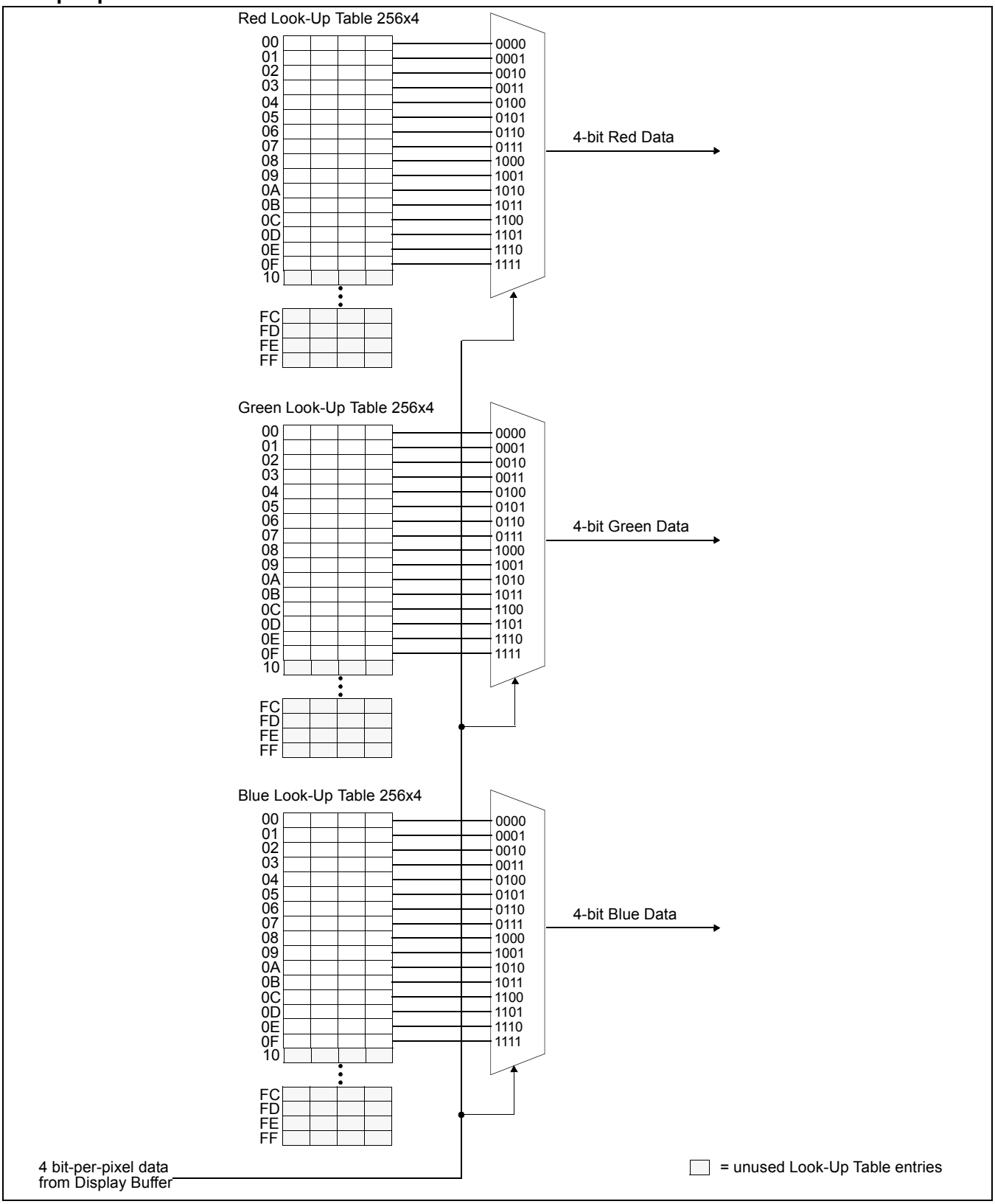


Figure 11-6: 4 Bit-per-pixel Color Mode Data Output Path

8 Bit-per-pixel Color Mode

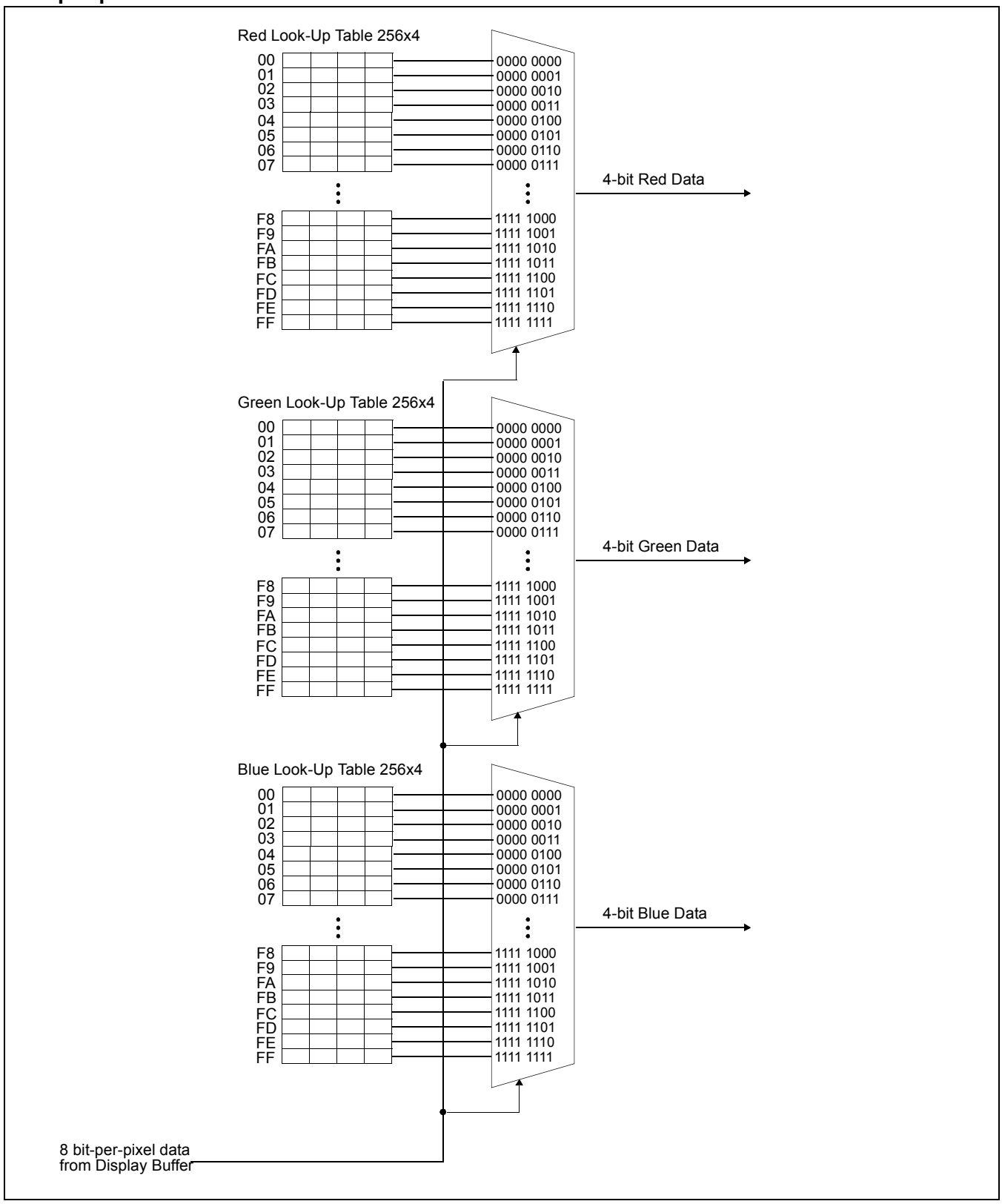


Figure 11-7: 8 Bit-per-pixel Color Mode Data Output Path

12 SwivelView™

Many of todays applications use the LCD panel in a portrait orientation. In this case it becomes necessary to "rotate" the displayed image by 90°. This rotation can be done by software at the expense of performance or, it can be done by the S1D13705 hardware with no CPU penalty.

There are two SwivelView modes: Default SwivelView Mode and Alternate SwivelView Mode.

12.1 Default SwivelView Mode

Default SwivelView Mode requires the SwivelView image width be a power of two, e.g. a 240-line panel requires a minimum virtual image width of 256. This mode should be used whenever the required virtual image can be contained within the integrated display buffer (i.e. virtual image size ≤ 80K bytes), as it consumes less power than the Alternate SwivelView Mode.

For example, the panel size is 320x240 and the display mode is 8 bit-per-pixel. The virtual image size is 320x256 which can be contained within the 80K Byte display buffer.

Default SwivelView Mode also requires Memory Clock (MCLK) ≥ Pixel Clock (PCLK).

The following figure shows how the programmer sees a 240x320 image and how the image is displayed. The application image is written to the S1D13705 in the following sense: A–B–C–D. The display is refreshed by the S1D13705 in the following sense: B-D-A-C.

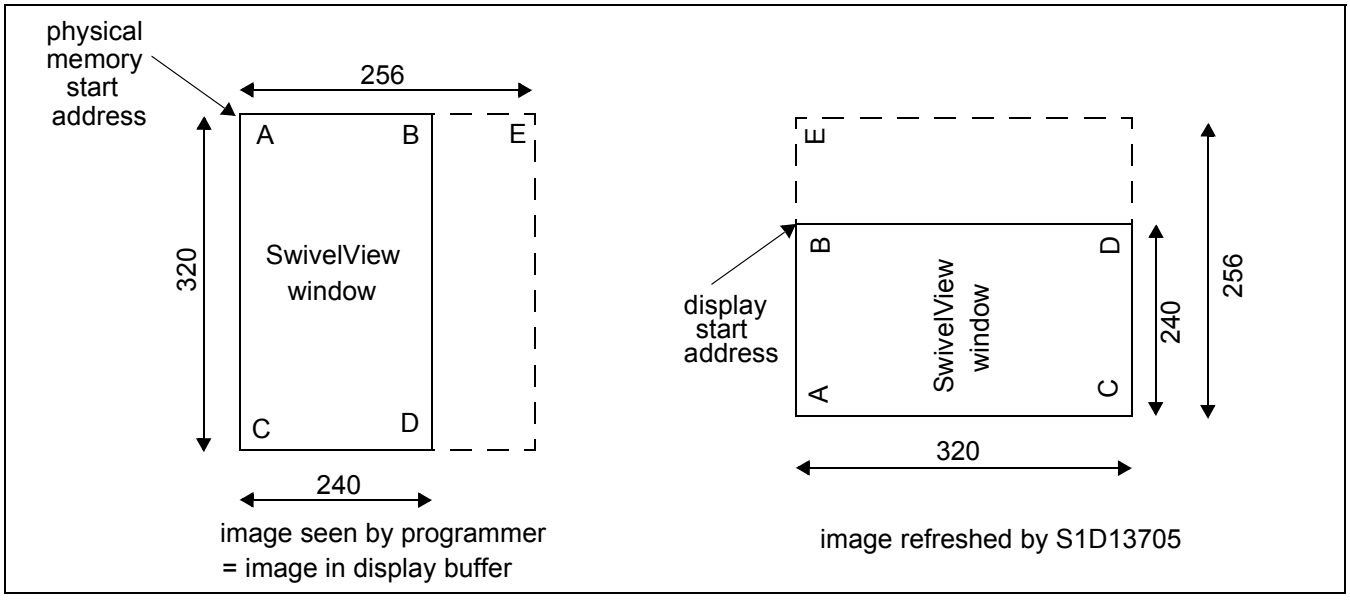


Figure 12-1: Relationship Between The Screen Image and the Image Refreshed by S1D13705 in Default Mode

12.1.1 How to Set Up Default SwivelView Mode

The following describes the register settings needed to set up Default SwivelView Mode for a 240x320x8 bpp image:

- Select Default SwivelView Mode: REG[1Bh] bit 7 = 1 and bit 6 = 0
- The display refresh circuitry starts at pixel "B", therefore the Screen 1 Start Address register must be programmed with the address of pixel "B", i.e.

$$\begin{aligned} \text{REG[10h], REG[0Dh], REG[0Ch]} &= \text{AddressOfPixelB} \\ &= (\text{AddressOfPixelA} + \text{ByteOffset}) \\ &= \text{AddressOfPixelA} + \left(\frac{240\text{pixels} \times 8\text{bpp}}{8\text{bpb}}\right) - 1 \\ &= \text{AddressOfPixelA} + \text{EFh} \end{aligned}$$

Where bpp is bits-per-pixel and bpb is bits-per-byte.

- The Line Byte Count Register for SwivelView Mode must be set to the virtual-image width in bytes, i.e.

$$\text{REG[1Ch]} = \frac{256}{(8\text{bpb}) \div (8\text{bpp})} = \frac{256}{1} = 256 = 00\text{h}$$:see REG[1Ch] for explanation

Where bpb is bits-per-byte and bpp is bits-per-pixel.

- Panning is achieved by changing the Screen 1 Start Address register:
  - Increment the register by 1 to pan horizontally by one byte, e.g. one pixel in 8 bpp mode
  - Increment the register by twice the effective value of the Line Byte Count register to pan vertically by two lines, e.g. add 200h to pan by two lines in the example above.

Note
Vertical panning by a single line is not supported in Default SwivelView Mode.

12.2 Alternate SwivelView Mode

Alternate SwivelView Mode may be used when the virtual image size of Default SwivelView Mode cannot be contained in the 80K byte integrated frame buffer. For example, the panel size is 480x320 and the display mode is 4 bit-per-pixel. The minimum virtual image size for Default SwivelView Mode would be 480x512 which requires 122,880 bytes. Alternate SwivelView Mode requires a panel size of only 480x320 which needs only 76,800 bytes.

Alternate SwivelView Mode requires the Memory Clock (MCLK) to be at least twice the frequency of the Pixel Clock (PCLK), i.e. MCLK ≥ 2 x PCLK. This makes the power consumption in Alternate SwivelView Mode higher than in Default SwivelView Mode while increasing performance.

The following figure shows how the programmer sees a 480x320 image and how the image is being displayed. The application image is written to the S1D13705 in the following sense: A–B–C–D. The display is refreshed by the S1D13705 in the following sense: B-D-A-C.

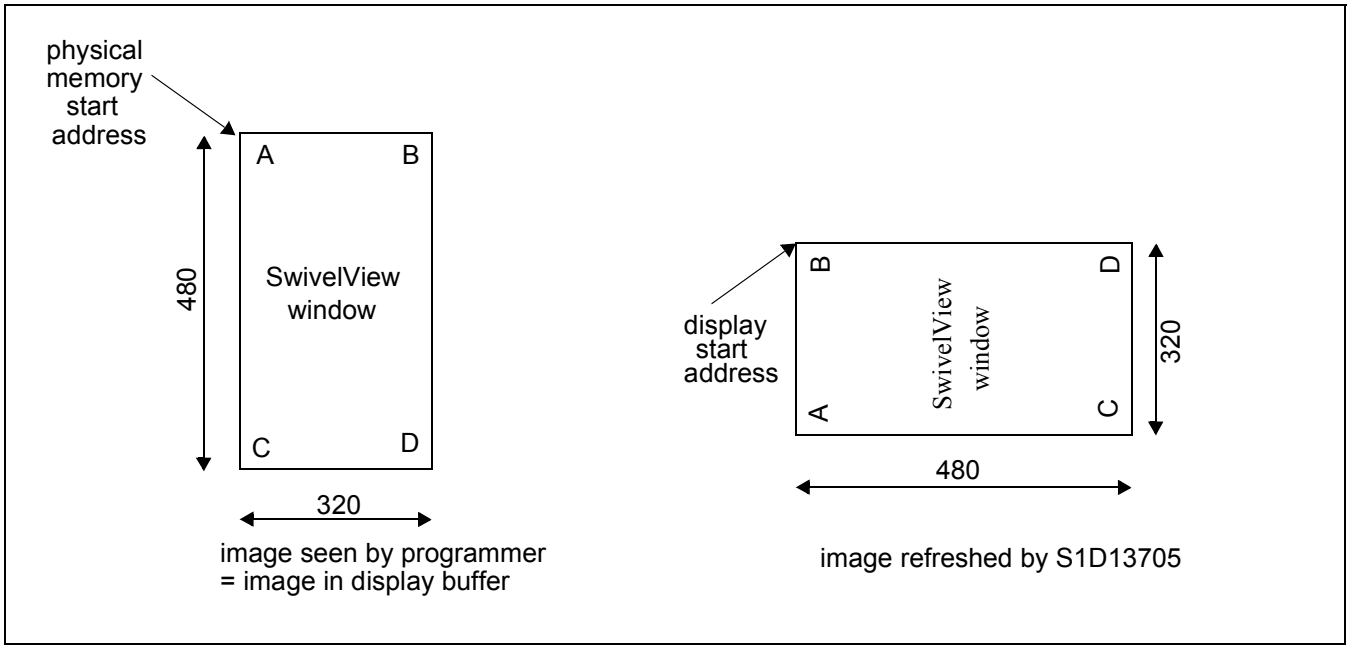


Figure 12-2: Relationship Between The Screen Image and the Image Refreshed by S1D13705 in Alternate Mode

12.2.1 How to Set Up Alternate SwivelView Mode

The following describes the register settings needed to set up Alternate SwivelView Mode for a 320x480x4 bpp image.

- Select Alternate SwivelView Mode:
  REG[1Bh] bit 7 = 1 and bit 6 = 1
- The display refresh circuitry starts at pixel "B", therefore the Screen 1 Start Address register must be programmed with the address of pixel "B", or

$$\begin{aligned} \text{REG[10h], REG[0Dh], REG[0Ch]} &= \text{AddressOfPixelB} \\ &= (\text{AddressOfPixelA} + \text{ByteOffset}) \\ &= \text{AddressOfPixelA} + \left(\frac{320\text{pixels} \times 4\text{bpp}}{8\text{bpb}}\right) - 1 \\ &= \text{AddressOfPixelA} + 9\text{Fh} \end{aligned}$$

  Where bpp is bits-per-pixel and bpb is bits-per-byte.

- The Line Byte Count Register for SwivelView Mode must be set to the image width in bytes, i.e.

$$\text{REG[1Ch]} = \frac{320}{(8\text{bpb}) \div (4\text{bpp})} = \frac{320}{2} = 160 = \text{A0h}$$

  Where bpb is bits-per-byte and bpp is bits-per-pixel.

- Panning is achieved by changing the Screen 1 Start Address register:
  - Increment the register by 1 to pan horizontally by one byte, e.g. two pixels in 4 bpp mode
  - Increment the register by the value in the Line Byte Count register to pan vertically by one line, e.g. add A0h to pan by one line in the example above

12.3 Comparison Between Default and Alternate SwivelView Modes

Table 12-1: Default and Alternate SwivelView Mode Comparison

Item	Default SwivelView Mode	Alternate SwivelView Mode
Memory Requirements	The width of the rotated image must be a power of 2. In most cases, a virtual image is required where the right-hand side of the virtual image is unused and memory is wasted. For example, a 320x480x4bpp image would normally require only 76,800 bytes - possible within the 80K byte address space, but the virtual image is 512x480x4bpp which needs 122,880 bytes - not possible.	Does not require a virtual image.
Clock Requirements	CLK need only be as fast as the required PCLK.	MCLK, and hence CLK, need to be 2x PCLK. For example, if the panel requires a 3MHz PCLK, then CLK must be 6MHz. Note that 25MHz is the maximum CLK, so PCLK cannot be higher than 12.5MHz in this mode.
Power Consumption	Lowest power consumption.	Higher than Default Mode.
Panning	Vertical panning in 2 line increments.	Vertical panning in 1 line increments.
Performance	Nominal performance.	Higher performance than Default Mode.

12.4 SwivelView Mode Limitations

The only limitation to using SwivelView mode on the S1D13705 is that split screen operation is not supported.

13 Power Save Modes

Two Power Save Modes have been incorporated into the S1D13705 to accommodate the need for power reduction in the hand-held devices market. These modes are enabled as follows:

Table 13-1: Power Save Mode Selection

Hardware Power Save	Software Power Save Bit 1	Software Power Save Bit 0	Mode
Not Configured or 0	0	0	Software Power Save Mode
Not Configured or 0	0	1	reserved
Not Configured or 0	1	0	reserved
Not Configured or 0	1	1	Normal Operation
Configured and 1	X	X	Hardware Power Save Mode

13.1 Software Power Save Mode

Software Power Save Mode saves power by powering down the panel and stopping display refresh accesses to the display buffer.

Table 13-2: Software Power Save Mode Summary

• Registers read/write accessible
• Memory read/write accessible
• Look-Up Table registers not accessible
• LCD outputs are forced low

13.2 Hardware Power Save Mode

Hardware Power Save Mode saves power by powering down the panel, stopping accesses to the display buffer and registers, and disabling the Host Bus Interface.

Table 13-3: Hardware Power Save Mode Summary

• Host Interface not accessible
• Memory read/write not accessible
• Look-Up Table registers not accessible
• LCD outputs are forced low

13.3 Power Save Mode Function Summary

Table 13-4: Power Save Mode Function Summary

	Hardware Power Save	Software Power Save	Normal
IO Access Possible?	No	Yes	Yes
Memory Access Possible?	No	Yes	Yes
Look-Up Table Registers Access Possible?	No	No	Yes
Sequence Controller Running?	No	No	Yes
Display Active?	No	No	Yes
LCDPWR	Inactive	Inactive	Active
FPDAT[11:0], FPSHIFT (see note)	Forced Low	Forced Low	Active
FPLINE, FPFRAME, DRDY	Forced Low	Forced Low	Active

Note

When FPDAT[11:8] are designated as GPIO outputs, the output state prior to enabling the Power Save Mode is maintained. When FPDAT[11:8] are designated as GPIO inputs, unused inputs must be tied to either IO V_{DD} or GND - see Table 5.5 “LCD Interface Pin Mapping,” on page 21.

13.4 Panel Power Up/Down Sequence

After chip reset or when entering/exiting a power save mode, the Panel Interface signals follow a power on/off sequence shown below. This sequence is essential to prevent damage to the LCD panel.

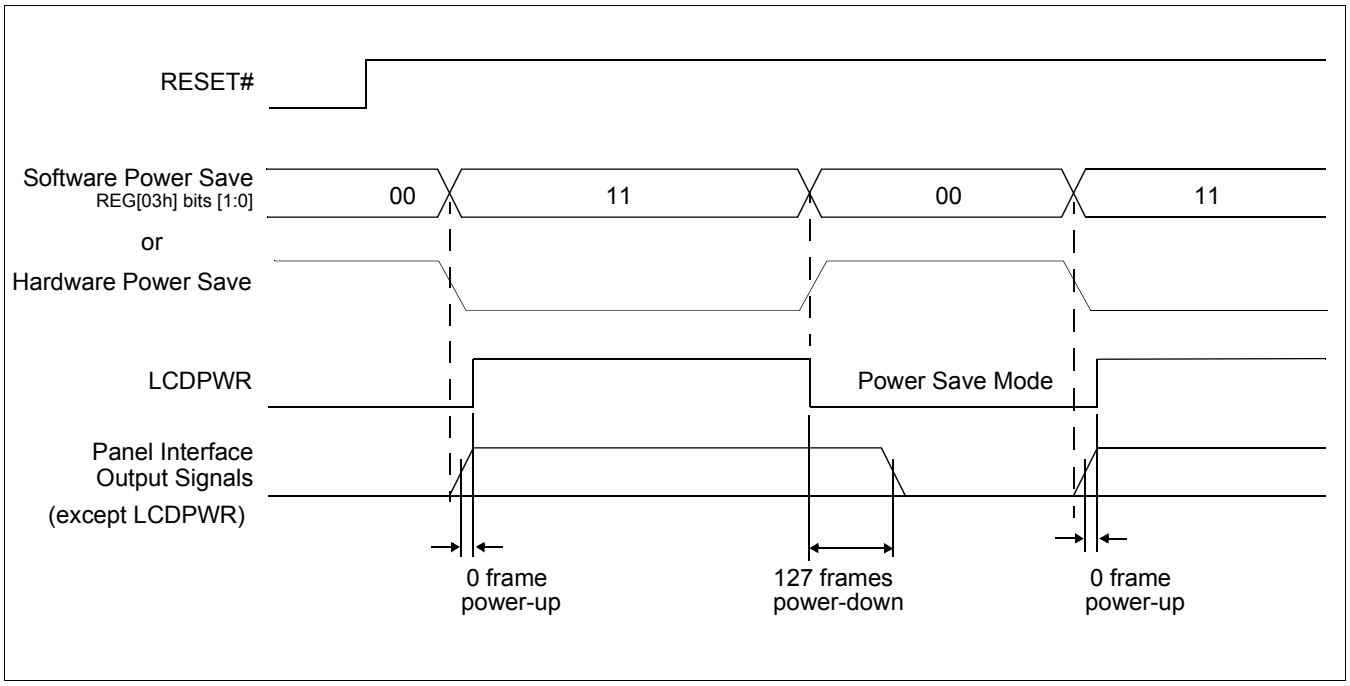


Figure 13-1: Panel On/Off Sequence

After chip reset, LCDPWR is inactive and the rest of the panel interface output signals are held "low". Software initializes the chip (i.e. programs all registers except the Look-Up Table registers) and then programs REG[03h] bits [1:0] to 11b. This starts the power-up sequence as shown. The power-up/power-down sequence delay is 127 frames. The Look-Up Table registers may be programmed any time after REG[03h] bits[1:0] = 11b.

The power-up/power-down sequence also occurs when exiting/entering Software Power Save Mode.

13.5 Turning Off BCLK Between Accesses

BCLK may be turned off (held low) between accesses if the following rules are observed:

1. BCLK must be turned off/on in a glitch free manner
2. BCLK must continue for a period equal to [$8T_{BCLK} + 12T_{MCLK}$] after the end of the access (RDY# asserted or WAIT# deasserted).
3. BCLK must be present for at least one T_{BCLK} before the start of an access.

13.6 Clock Requirements

The following table shows what clock is required for which function in the S1D13705

Table 13-5: S1D13705 Internal Clock Requirements

Function	BCLK	CLKI
Register Read/Write	Is required during register accesses. BCLK can be shut down between accesses: allow eight BCLK pulses plus 12 MCLK pulses ($8T_{BCLK} + 12T_{MCLK}$) after the last access before shutting BCLK off. Allow one BCLK pulse after starting up BCLK before the next access	Not Required
Memory Read/Write	Is required during memory accesses. BCLK can be shut down between accesses: allow eight BCLK pulses plus 12 MCLK pulses ($8T_{BCLK} + 12T_{MCLK}$) after the last access before shutting BCLK off. Allow one BCLK pulse after starting up BCLK before the next access	Required
Look-Up Table Register Read/Write	Is required during LUT register accesses. BCLK can be shut down between accesses: allow eight BCLK pulses plus 12 MCLK pulses ($8T_{BCLK} + 12T_{MCLK}$) after the last access before shutting BCLK off. Allow one BCLK pulse after starting up BCLK before the next access	Not Required
Software Power Save	Required	Can be stopped after 128 frames from entering Software Power Save, i.e. after REG[03h] bits 1-0 = 11
Hardware Power Save	Not Required	Can be stopped after 128 frames from entering Hardware Power Save

14 Mechanical Data

QFP14 - 80 pin

Unit: mm

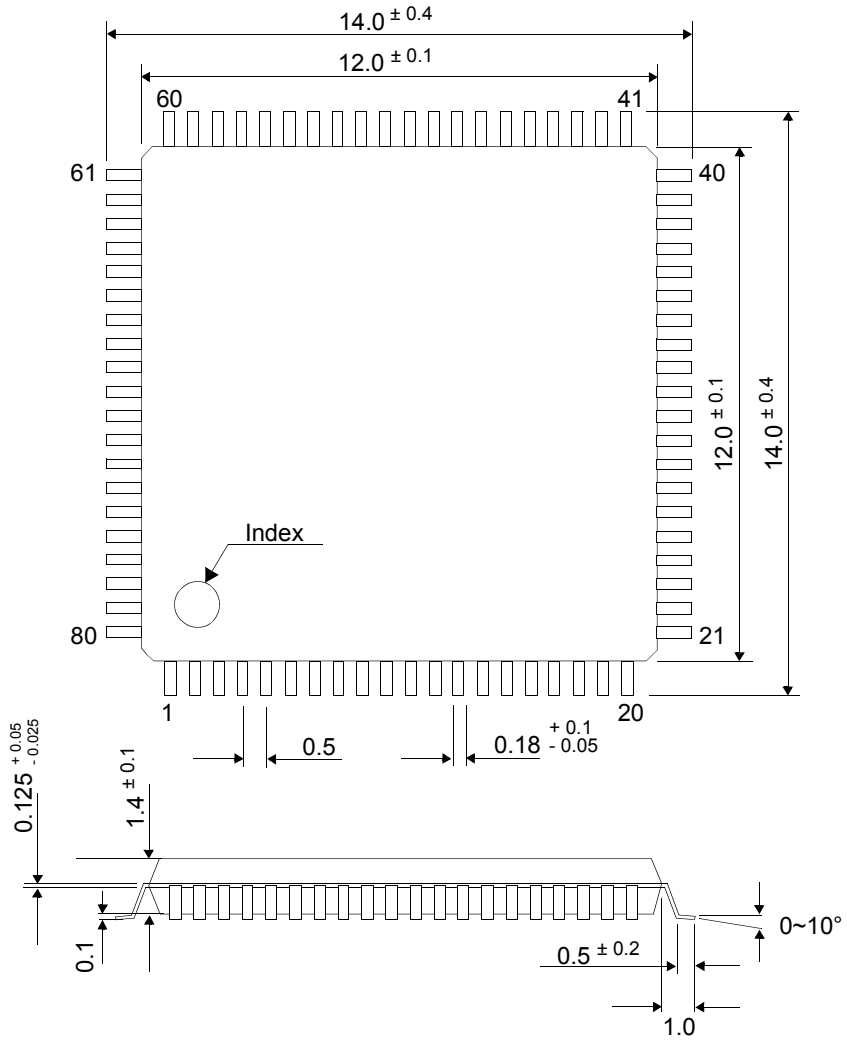


Figure 14-1: Mechanical Drawing QFP14

15 Change Record

X27A-A-001-10 Revision 10.03 - Issued: March 12, 2018

- updated Sales and Technical Support Section
- updated some formatting

X27A-A-001-10 Revision 10.02 - Issued: December 16, 2008

- release as revision 10.2 to align with Japan numbering
- updated Sales and Technical Support addresses

X27A-A-001-10 Revision 10.01 - Issued: September 18, 2007

- updated Epson tagline and copyright
- updated Sales and Technical Support addresses
- added Change Record

16 Sales and Technical Support

For more information on Epson Display Controllers, visit the Epson Global website.

https://global.epson.com/products_and_drivers/semicon/products/display_controllers/

For Sales and Technical Support, contact the Epson representative for your region.

https://global.epson.com/products_and_drivers/semicon/information/support.html