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S1D13700 Embedded Memory Graphics LCD Controller

S5U13700B00C Rev. 1.0 Evaluation Board User Manual

Document Number: X42A-G-002-01.1

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SEIKO EPSON CORPORATION

Rev. 1.1

Evaluation Board/Kit and Development Tool Important Notice

1. This evaluation board/kit or development tool is designed for use for engineering evaluation, demonstration, or development purposes only. Do not use it for other purposes. It is not intended to meet the requirements of design for finished products.
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3. The part used for this evaluation board/kit or development tool may be changed without any notice.

NOTICE

Table of Contents

1 Introduction

This manual describes the setup and operation of the S5U13700B00C Rev. 1.0 Evaluation Board. This evaluation board is designed as an evaluation platform for the S1D13700 Embedded Memory Graphics LCD Controller.

The S5U13700B00C is designed for connection to the Epson PC Card Extender (S5UPCMCIAB00C), thus providing an easy connection to a laptop or a desktop computer with a PC Card reader. This module can also be used with other native platforms via the host connectors which provide the appropriate signals to support a variety of CPUs.

This document is updated as appropriate. Please check for the latest revision of this document before beginning any development. The latest revision can be downloaded at vdc.epson.com.

We appreciate your comments on our documentation. Please contact us via email at vdc-documentation@ea.epson.com.

2 Features

The S5U13700B00C Rev. 1.0 evaluation board includes the following features:

- 64-pin TQFP13 S1D13700F0x Embedded Memory Graphics LCD Controller
- Headers for connecting to various Host Bus Interfaces or to the Epson PC Card Extender
- 0.1x0.1” header with all the LCD interface signals allowing connection to a LCD panel
- On-board 32MHz crystal and option to use an oscillator instead of the crystal
- On-board +3.3V regulator

3 Installation and Configuration

The S5U13700B00C evaluation board incorporates a DIP switch and 9 jumpers, which allow configuration of the board.

3.1 Configuration DIP Switches

An 8 position DIP switch (S1) is used to configure the S1D13700 for different Host Bus interfaces and to select the FPSHIFT cycle time. The following figure shows the location of DIP switch S1 on the S5U13700B00C.

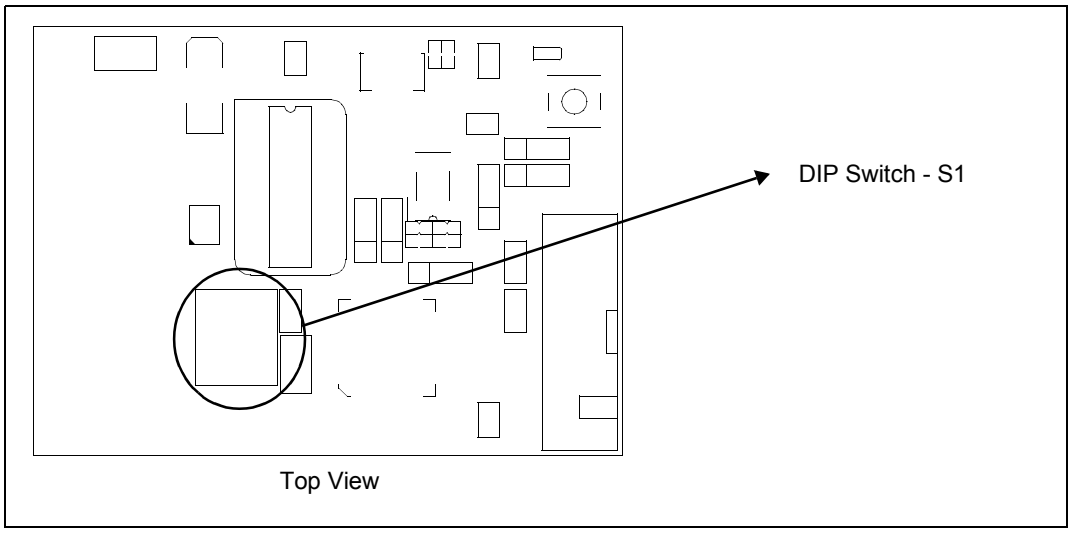

Figure 3-1: Configuration DIP Switch (S1) Location

All S1D13700 configuration inputs (CNF[4:0]) are fully configurable using DIP switch S1 as described below.

Table 3-1: Summary of Configuration Options

SDU13700B00C S1-[8:1] Configuration	S1D13700 Pin	Configuration State	
		1 (ON)	0 (OFF)
S1-[8:7]	-	Not used	
S1-[6]	AS#	Generic Bus or M6800 Family Bus Interface	M68K Family Bus Interface
S1-[5]	CNF4	Indirect Addressing Mode	Direct Addressing Mode
S1-[4:3]	CNF[3:2]	Selects the host bus interface as follows: **CNF3** **CNF2** **Host Bus** 0 0 Generic Bus 0 1 Reserved 1 0 M6800 Family Bus Interface 1 1 MC68K Family Bus Interface	
S1-[2:1]	CNF[1:0]	Selects the FPSHIFT cycle time (FPSHIFT:Clock Input) as follows: **CNF1** **CNF0** **FPSHIFT Cycle Time** 0 0 FPSHIFT Divide 4:1 0 1 FPSHIFT Divide 8:1 1 0 FPSHIFT Divide 16:1 1 1 Reserved	

= Required settings when using the PC Card adapter

3.2 Configuration Jumpers

The S5U13700B00C has 9 jumper blocks which allow the configuration of the board.

Table 3-2: Jumper Summary

Jumper	Function	Position 1-2	Position 2-3	No Jumper
JP1	HIOVDD	Normal	—	HIOVDD current measurement
JP2	NIOVDD	Normal	—	NIOVDD current measurement
JP3	COREVDD	Normal	—	COREVDD current measurement
JP4	CLKI Source	On Board Oscillator (U2)	Host Interface Connector	—
JP5	CLKI Input Disable	Disable CLKI Input (CLKI is tied to VSS)	Disable Crystal Input (XCG1 is tied to VSS)	—
JP6	Crystal Enable	Enable Crystal Output	Disable Crystal Output	—
JP7	HIOVDD Voltage	+3.3V	+5V	—
JP8	NIOVDD Voltage	+3.3V	+5V	—
JP9	RESET Source	Manual Reset	Host Interface Reset	—

= Required settings when using the PC Card adapter

JP1 - HIOVDD

JP1 can be used to measure the current consumption of the S1D13700 host interface.
When the jumper is at position 1-2, normal operation is selected.
When no jumper is installed, host interface current consumption can be measured across JP1.

Note
The HIOVDD voltage can be selected to be +3.3V or +5V using jumper JP7.

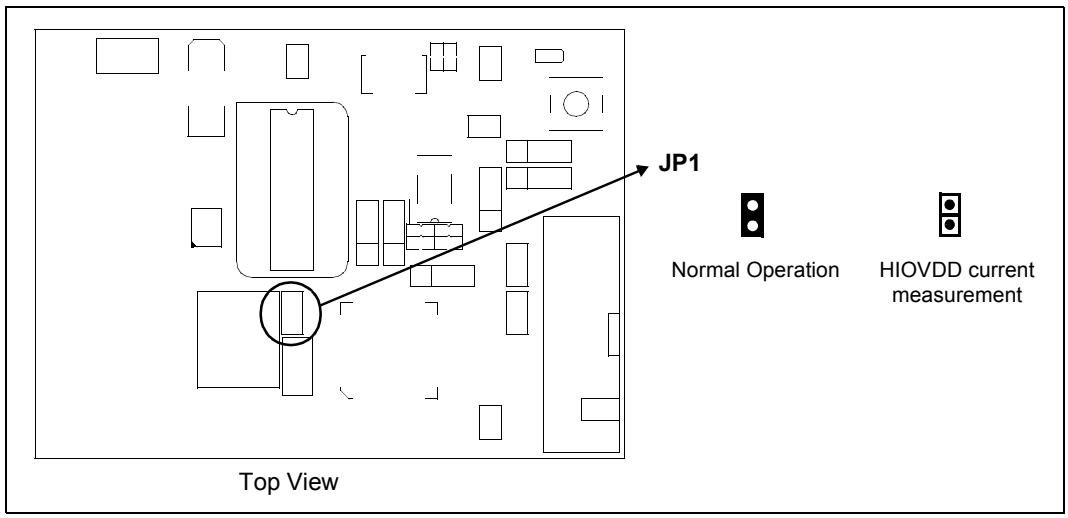

Figure 3-2: Configuration Jumper JP1 Location

JP2 - NIOVDD

JP2 can be used to measure the current consumption of the S1D13700 LCD panel interface.
When the jumper is at position 1-2, normal operation is selected.
When no jumper is installed, panel interface current consumption can be measured across JP2.

Note
The NIOVDD voltage can be selected to be +3.3V or +5V using jumper JP8.

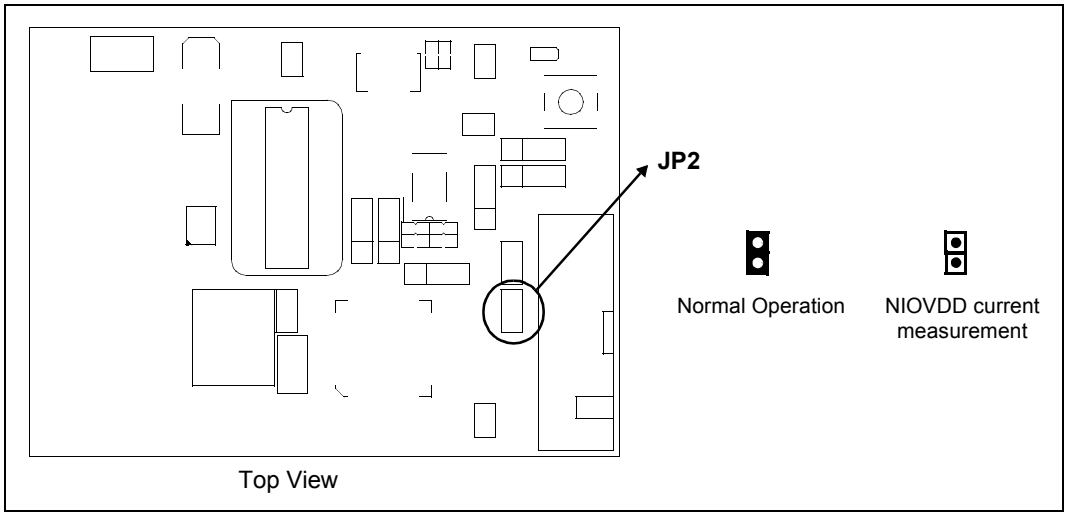

Figure 3-3: Configuration Jumper JP2 Location

JP3 - COREVDD

JP3 can be used to measure the current consumption of the S1D13700 core.
When the jumper is at position 1-2, normal operation is selected.
When no jumper is installed, core current consumption can be measured across JP3.

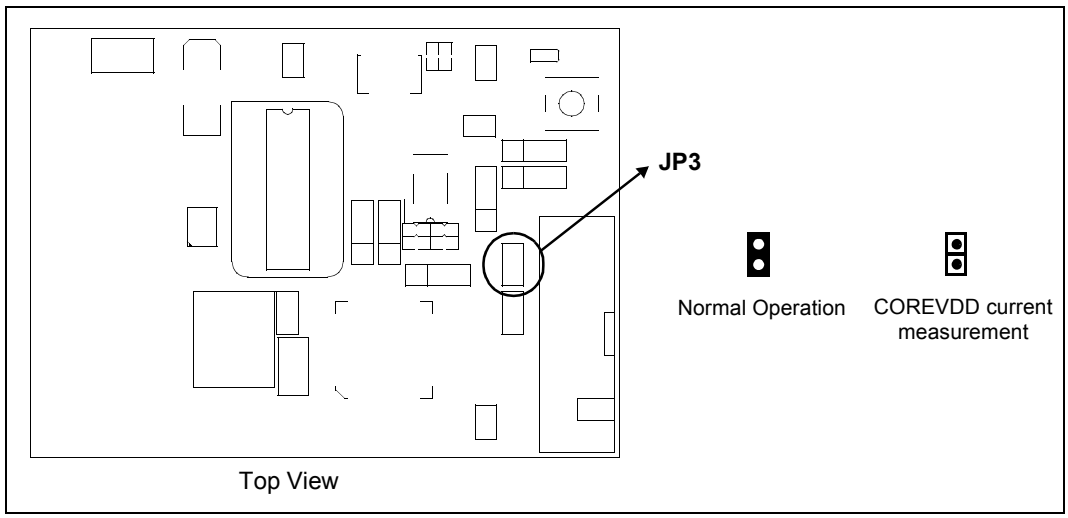

Figure 3-4: Configuration Jumper JP3 Location

JP4 - CLKI Source

JP4 is used to select the clock source for the S1D13700 CLKI input.
When the jumper is at position 1-2, the clock source is the on-board oscillator (U2).
When the jumper is at position 2-3, the clock source is from the host interface connector (connector P1, pin 4).

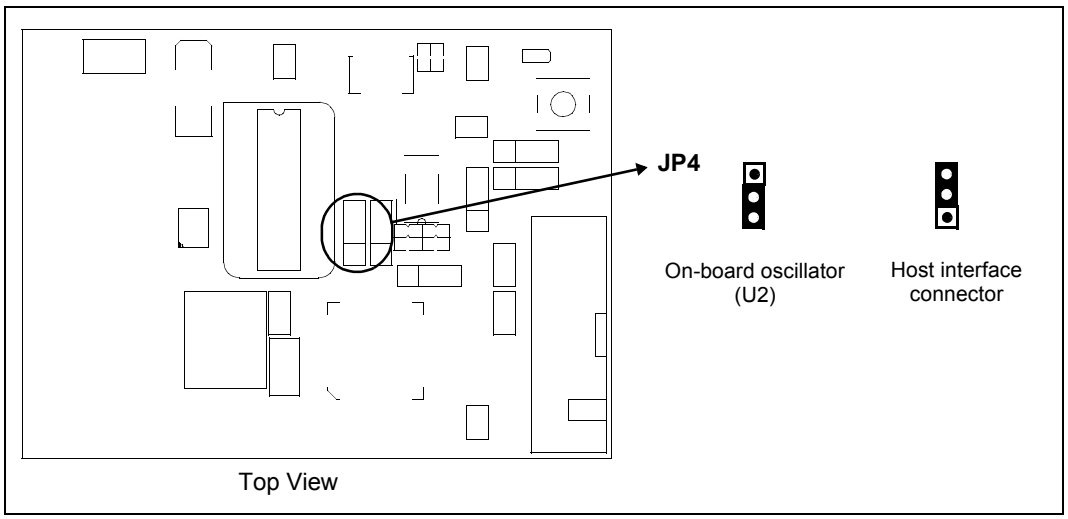

Figure 3-5: Configuration Jumper JP4 Location

JP5 - CLKI Input Disable

JP5 is used to disable the S1D13700 clock input that is not used by connecting it to ground.
When the jumper is at position 1-2, CLKI input is disabled.
When the jumper is at position 2-3, XCG1 input is disabled.

Note
When jumper JP5 is at position 1-2, jumper JP6 must also be at position 1-2.
When jumper JP5 is at position 2-3, jumper JP6 must also be at position 2-3.

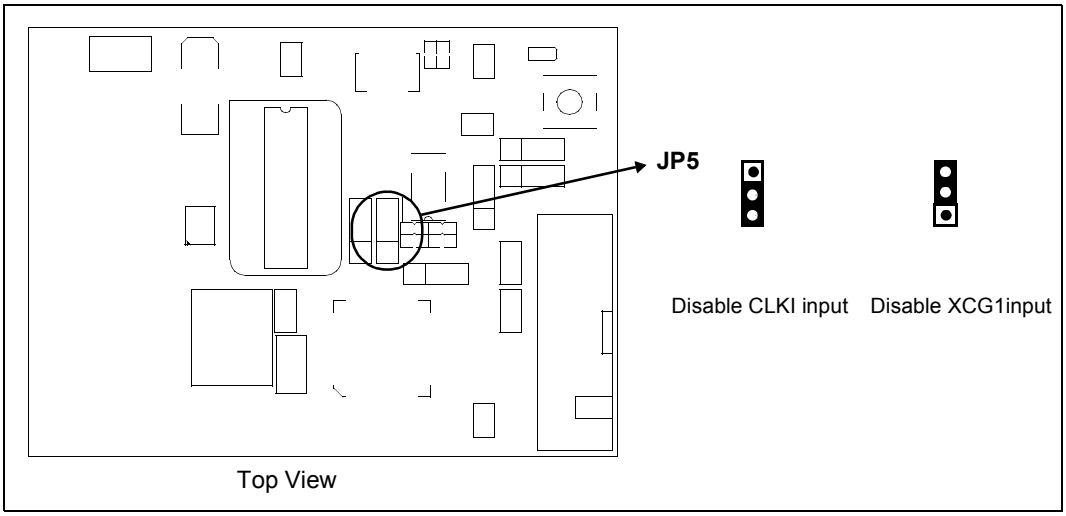

Figure 3-6: Configuration Jumper JP5 Location

JP6 - Crystal Enable

JP6 is used to enable or disable the S1D13700 crystal output (XCD1).
When the jumper is at position 1-2, XCD1 output is enabled by connecting it to the crystal.
When the jumper is at position 2-3, XCD1 output is disabled by disconnecting it from the crystal.

Note
When jumper JP6 is at position 1-2, jumper JP5 must also be at position 1-2.
When jumper JP6 is at position 2-3, jumper JP5 must also be at position 2-3.

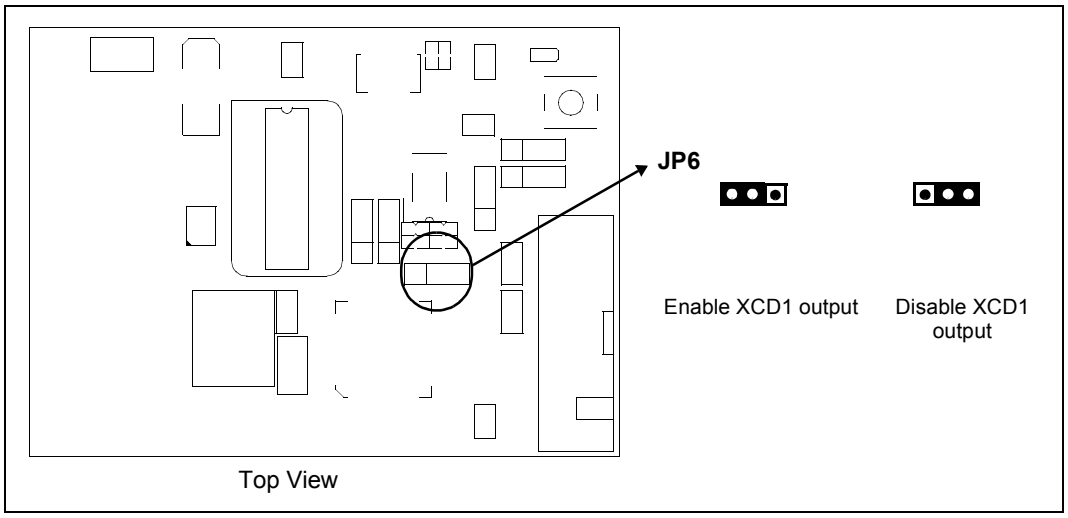

Figure 3-7: Configuration Jumper JP6 Location

JP7 - HIOVDD Voltage

JP7 is used to select the voltage for HIOVDD.
When the jumper is at position 1-2, HIOVDD is +3.3V.
When the jumper is at position 2-3, HIOVDD is +5V.

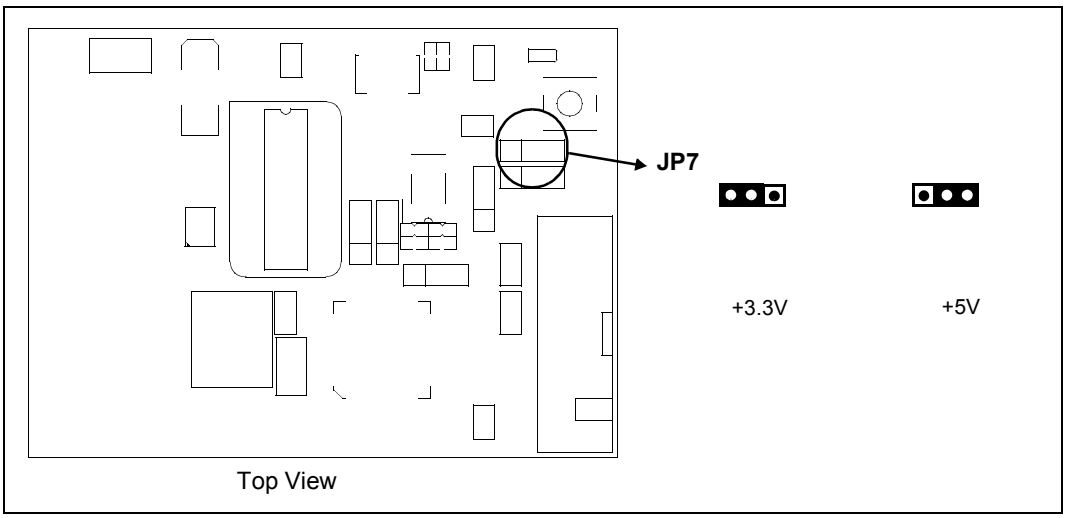

Figure 3-8: Configuration Jumper JP7 Location

JP8 - NIOVDD Voltage

JP8 is used to select the voltage for NIOVDD.
When the jumper is at position 1-2, NIOVDD is +3.3V.
When the jumper is at position 2-3, NIOVDD is +5V.

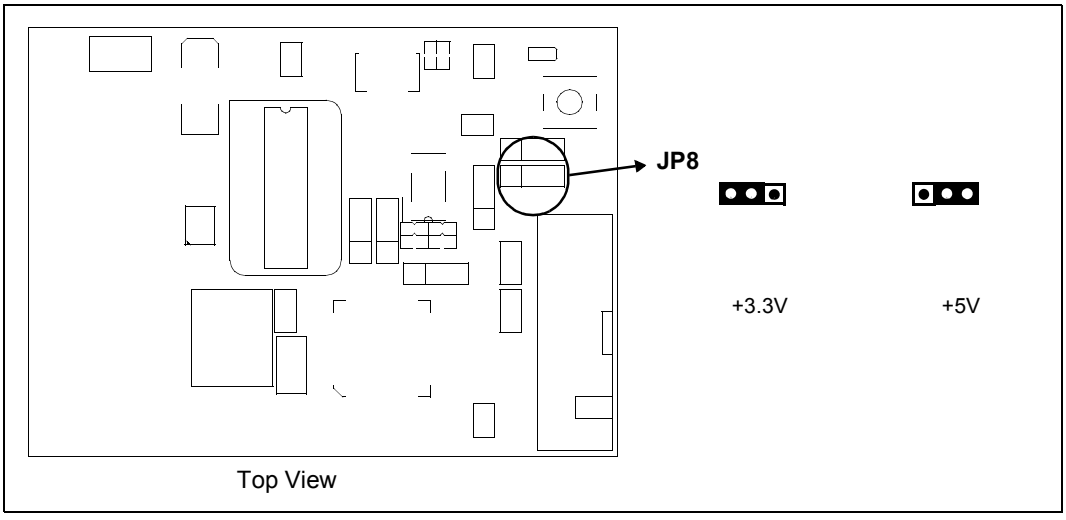

Figure 3-9: Configuration Jumper JP8 Location

JP9 - RESET# Source

JP9 is used to select the source of the RESET# signal to the S1D13700.
When the jumper is at position 1-2, the S1D13700 is reset by the on-board reset button (SW1).
When the jumper is at position 2-3, the S1D13700 is reset by the system (connector P1, pin 21).

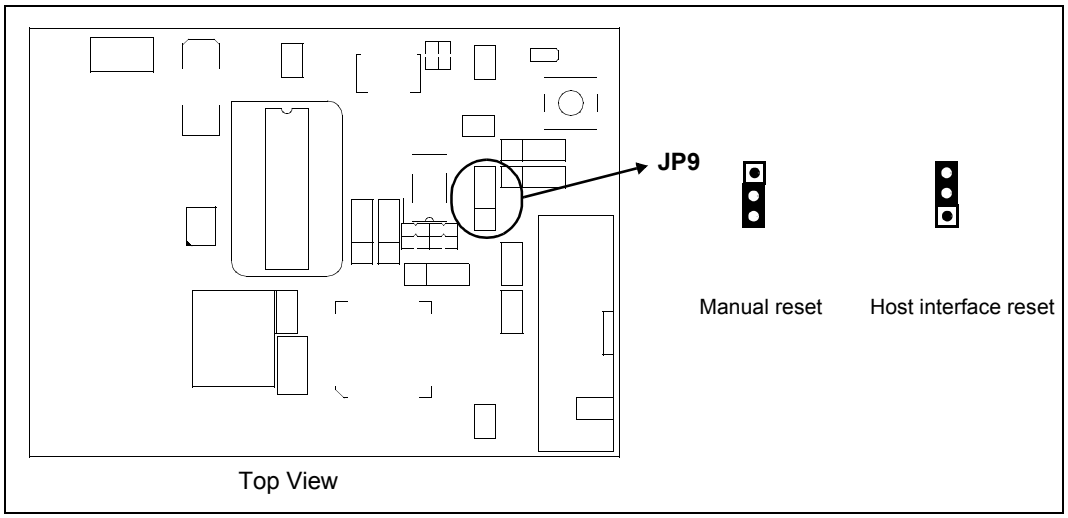

Figure 3-10: Configuration Jumper JP9 Location

4 Technical Description

4.1 Host interface

4.1.1 Epson PC Card Extender Support

The evaluation board is designed to connect to the Epson PC Card Extender (S5UPCMCIAB00C). The extender provides an easy connection to any computer with an available PC Card slot. The S5U13700B00C directly connects to the extender via connectors P1 and P2 (see Section 8, “Connecting the S5U13700B00C to the PC Card Adapter” on page 28).

Note

When using this evaluation board with the Epson PC Card Extender, the maximum current draw of 750mA provided by the PC Card slot may be exceeded. If the combination of module and LCD panel exceeds this limit, an external 5V power supply may be required. The 5V regulated power supply may be connected to the 5V test point (TP5V1) and the GND test point (TPGND1) to power the on-board regulator. In this case, the 0 Ohm resistor R2 must be removed from the board.

4.1.2 Host Bus Interface Support

The S1D13700 supports several host bus interfaces. All S1D13700 host interface pins are available on connectors P1 and P2 allowing the S5U13700B00C to be used for interfacing to other platforms.

All host interface signals must match HIOVDD of the S1D13700. The default value for HIOVDD on the board is +3.3V, so it will work with the Epson PC Card Extender (S5UPCMCIAB00C). HIOVDD can be selected between +3.3V and +5V using jumper JP7.

The following diagram shows the location of the host bus connectors (P1 and P2). Connectors P1 and P2 are 2x2mm headers, 40 pins (20x2) each.

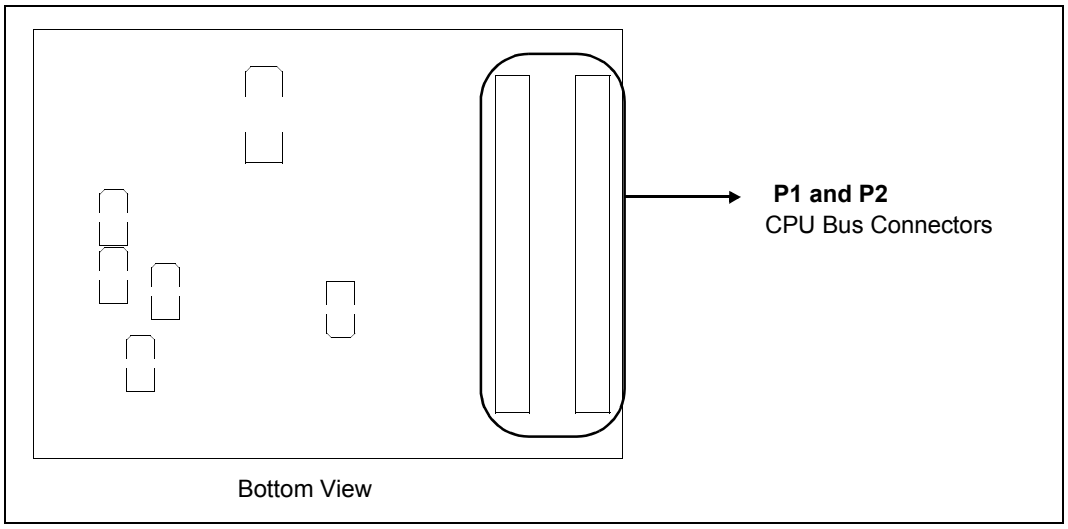

Figure 4-1: CPU Bus Connectors (P1 and P2) Location

For the pinout of connectors P1 and P2, refer to the schematics (see Section 6, “Schematic Diagrams” on page 23).

Note

1. When the board is connected to a PC using the Epson PC Card Extender, the signal AS# is not used and R12 must NOT be populated. AS# input of S1D13700 should be connected to HIOVDD by setting the dip switch (S1) position 6 to ON.
2. When the board is connected to different platforms, the Epson PC Card Extender is not used. If using MC68K Family Bus interface, the signal AS# is used and it can be provided to the P2 connector by populating R12 and the dip switch (S1) position 6 must be set to OFF position to disconnect AS# input from HIOVDD.

4.2 LCD Panel Interface

All the LCD interface signals are available on connector H1. Connector H1 is a 8x2 header, 0.1x0.1" pitch. The following diagram shows the location of the LCD connector (H1).

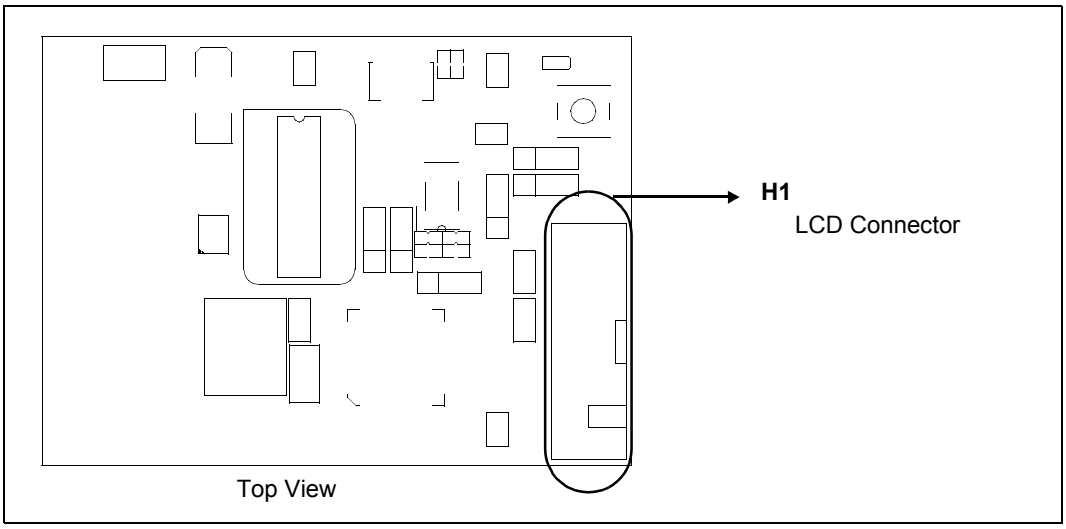

Figure 4-2: LCD Connector (H1) Location

For the pinout of connector H1, refer to the schematics (see Section 6, "Schematic Diagrams" on page 23).

4.3 Clock

The S1D13700 accepts a clock signal from an oscillator or from a crystal. If the oscillator is used, the crystal input (XCG1) must be connected to ground and the crystal output (XCD1) must not be connected. If the crystal is used, the clock input (CLKI) must be connected to ground. For details on connecting CLKI or XCG1 to ground, refer to the JP5 description (see "JP6 - Crystal Enable" on page 15).

The default configuration of the S5U13700B00C uses a 32MHz crystal. Jumper JP5 is in position 1-2 to connect the CLKI input to ground because it is not used. Jumper JP6 is in position 1-2 to connect the XCD1 output to the crystal.

The board can use the CLKI input instead of the crystal. To use the CLKI input, JP5 must be moved to position 2-3 to connect the XCG1 input to ground. Also, jumper JP6 must be moved to position 2-3 to disconnect the XCD1 output from the crystal.

The CLKI signal can be provided on the host interface connector or by an on-board oscillator. Jumper JP4 is used to select the clock source. In position 1-2, the clock is provided by populating an oscillator into the 14-pin DIP socket U2. In position 2-3, the clock must be provided on pin 4 of the host interface connector P1.

5 Parts List

Table 5-1: Parts List

Item	Qty	Reference	Part	Mfg / PN	Notes
1	5	C1,C12,C13,C20, C22	47uF 10V	Kemet T494B476M010AS	CAPACITOR TANT 47UF 10V 20% SMT
2	8	C2,C3,C4,C10, C11,C14,C15,C16	0.01uF	Panasonic - ECG PCC103BQCT	
3	16	C5,C6,C7,C8,C9, C17,C18,C19,C21, C23,C25,C26,C27, C29,C32,C33	0.1uF	Yageo America 04022F104Z7B20D	
4	2	C24,C28	100uF 10V T	Kemet T494D107K010AS	CAPACITOR TANT 100UF 10V 10% SMT
5	2	C31,C30	12 pF	Panasonic - ECG ECJ-1VC1H120J	CAP 12PF 50V CERAMIC 0603 SMD
6	1	D1	Power	Panasonic - SSG LNJ308G8LRA	LED GREEN SS TYPE LOW CUR SMD
7	1	F1	MINISMDC110-2, 1100mA	Raychem Corp/Polyswitch Division MINISMDC110-2	POLYSWITCH 1.1A RESET FUSE SMD
8	1	H1	HEADER 8X2	3M/ESD 2516-6002UB	
9	3	JP1,JP2,JP3			CONN HEADER VERT 2POS .100 TIN or GENERIC
10	6	JP4,JP5,JP6,JP7, JP8,JP9			CONN HEADER VERT 3POS .100 TIN or GENERIC
11	2	P1,P2		Sullins Electronics Corp. PRPN202PAEN	
12	1	R1	22K	CTS Corporation 742C163223JTR	RES ARRAY 16TRM 8RES SMD
13	1	R2	0		
14	1	R3	120R,0.1%	Panasonic - ECG ERA-3YEB120V	Or equivalent
15	1	R4	240R		
16	1	R5	200R,0.1%	Panasonic - ECG ERA-3YEB200V	RES 200 OHM 0.1% SMD 0603
17	1	R6	1M		
18	1	R7	100R		
19	0	R8,R9,R12	NP		
20	2	R10,R11	0		
21	1	R13	22k		
22	9	SH1,SH2,SH3, SH4,SH5,SH6, SH7,SH8,SH9	.100 in. Jumper Shunt	Sullins Electronics Corp. STC02SYAN	JUMPER SHORTING TIN
23	1	SW1	SW TACT-SPST	ITT Industries KSC241J	SWITCH TACT SILVER PLT J-TYPE
24	1	S1	CONFIG SW	C&K TDA08H0SK1	SWITCH DIP 8POS HALF PITCH SMT

Table 5-1: Parts List

Item	Qty	Reference	Part	Mfg / PN	Notes
25	3	TPGND1,TP5V1, TPP3.3V1	TP_SMT	Keystone 5015	PC TEST POINT MINIATURE SMT
26	1	U1	S1D13700_TQFP13-64		
27	1	U2	Oscillator Socket		14 pin narrow DIP, screw machine socket
28	1	U3	LT1117CST	Linear Technology LT1117CST	IC LDO REG ADJUSTBL 800MA SOT223
29	1	U4	SN74LVC2G17	Texas Instruments SN74LVC2G17DBVR	IC BUFFER DUAL SHMT-TRG SOT-23-6
30	1	U5	TPS3801K33DCKR	Texas Instruments TPS3801K33DCKR	IC 2.93V SUPPLY MON SOT-323-5
31	1	X1	Crystal32MHz_MA306	Epson MA-306 32.0000M-C0	

6 Schematic Diagrams

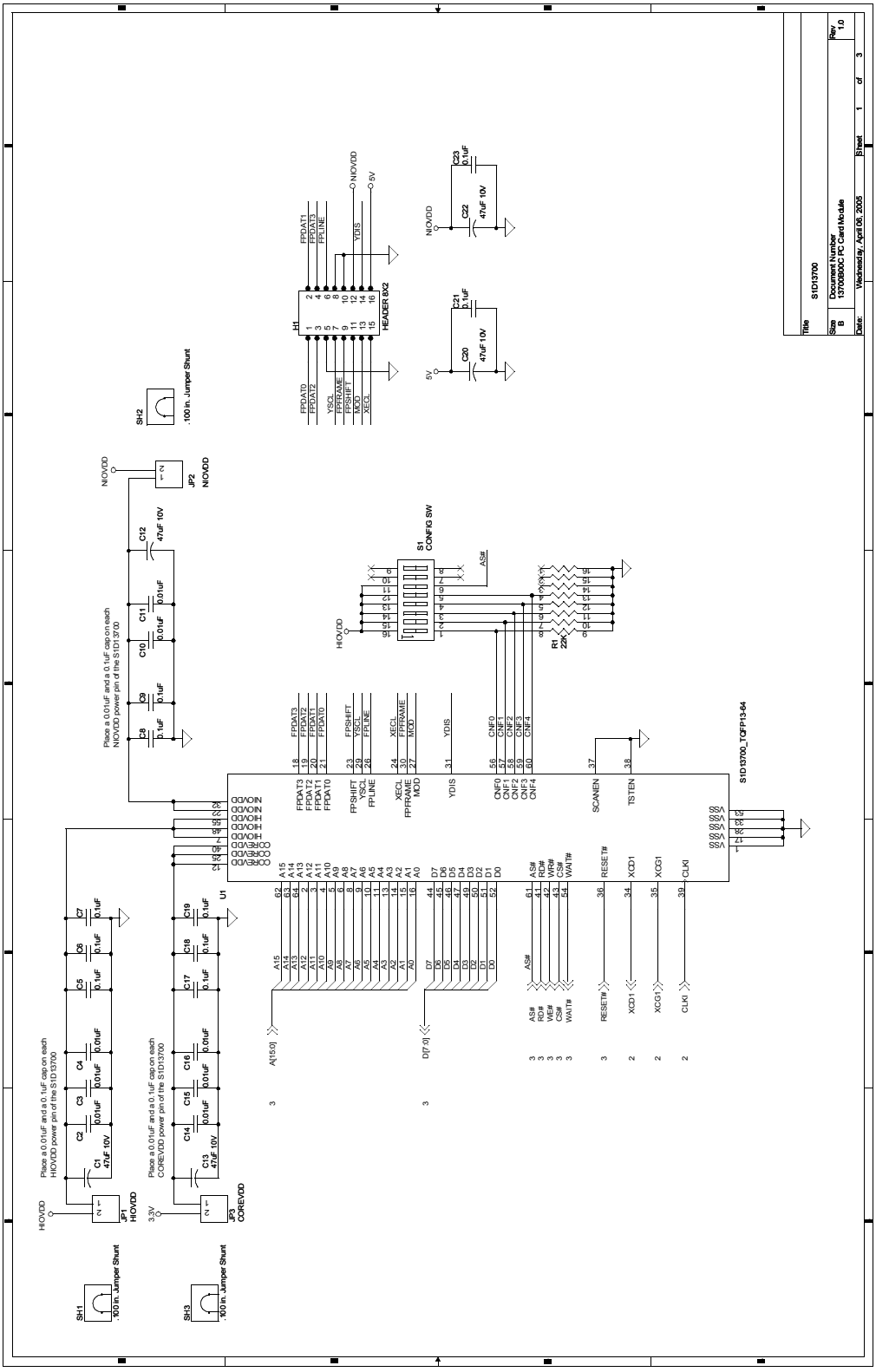

Figure 6-1: S5U13700B00C Schematics (1 of 3)

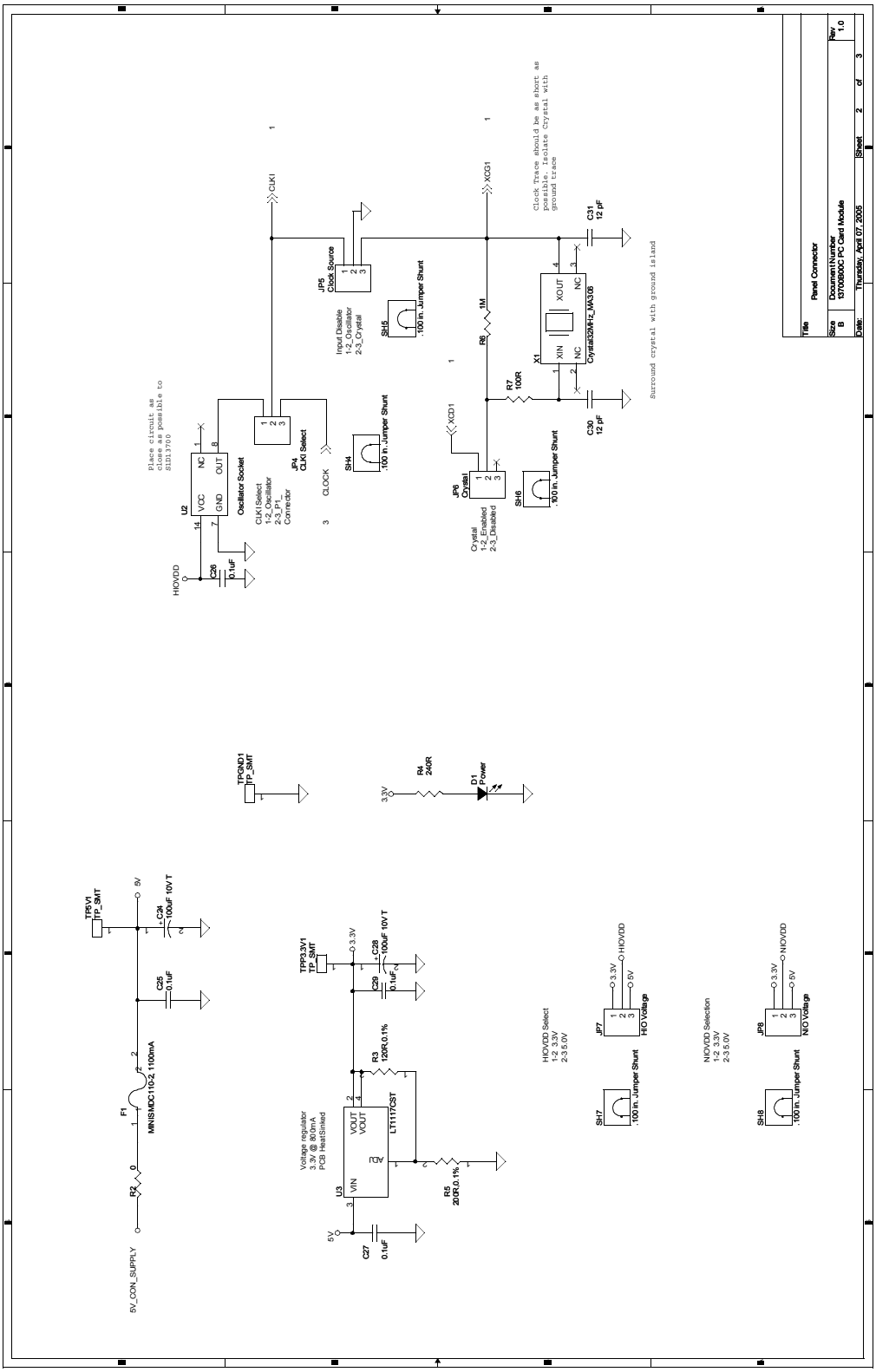

Figure 6-2: S5U13700B00C Schematics (2 of 3)

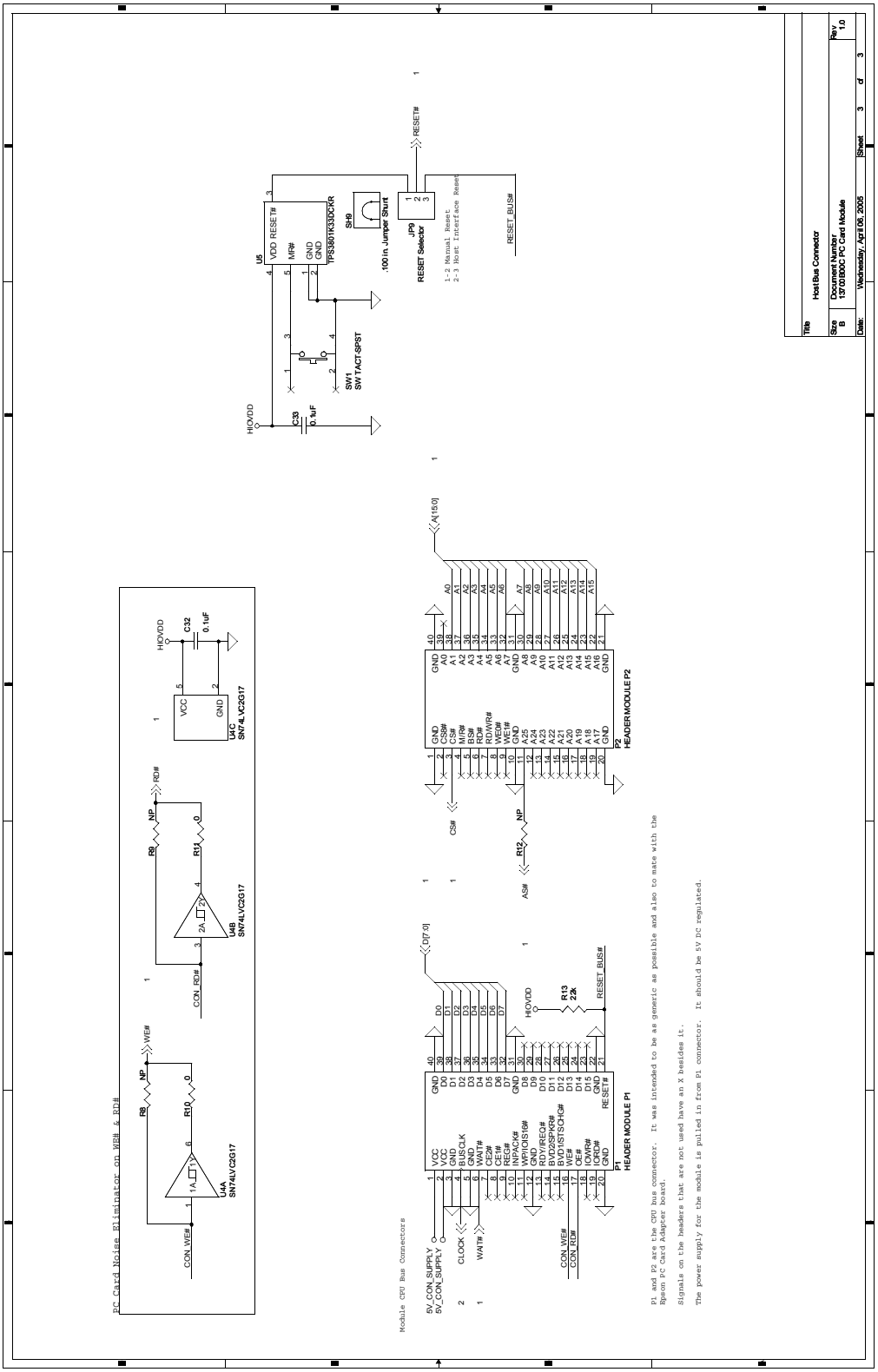

Figure 6-3: S5U13700B00C Schematics (3 of 3)

7 S5U13700B00C Board Layout

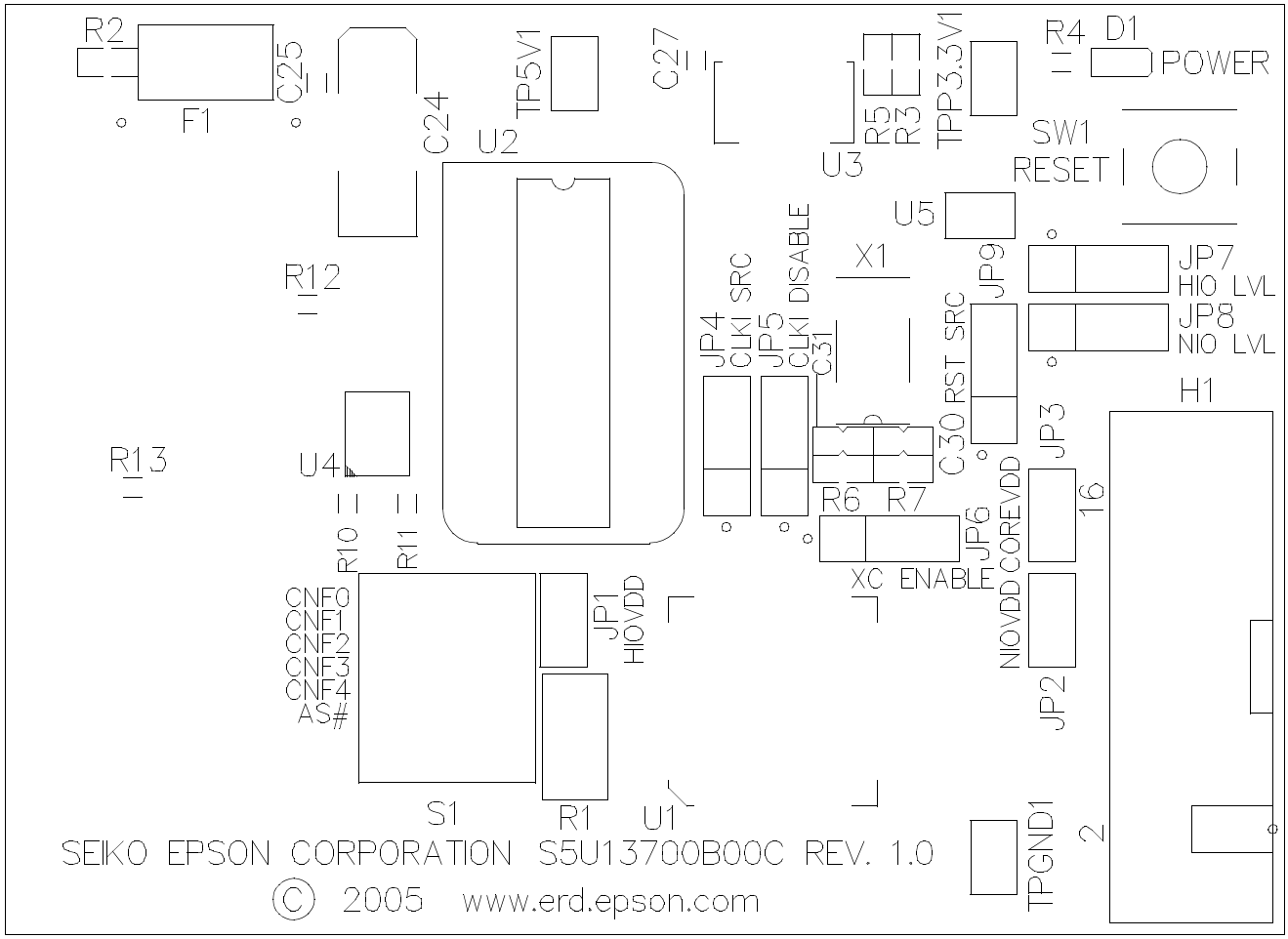

Figure 7-1: S5U13700B00C Board Layout (Top View)

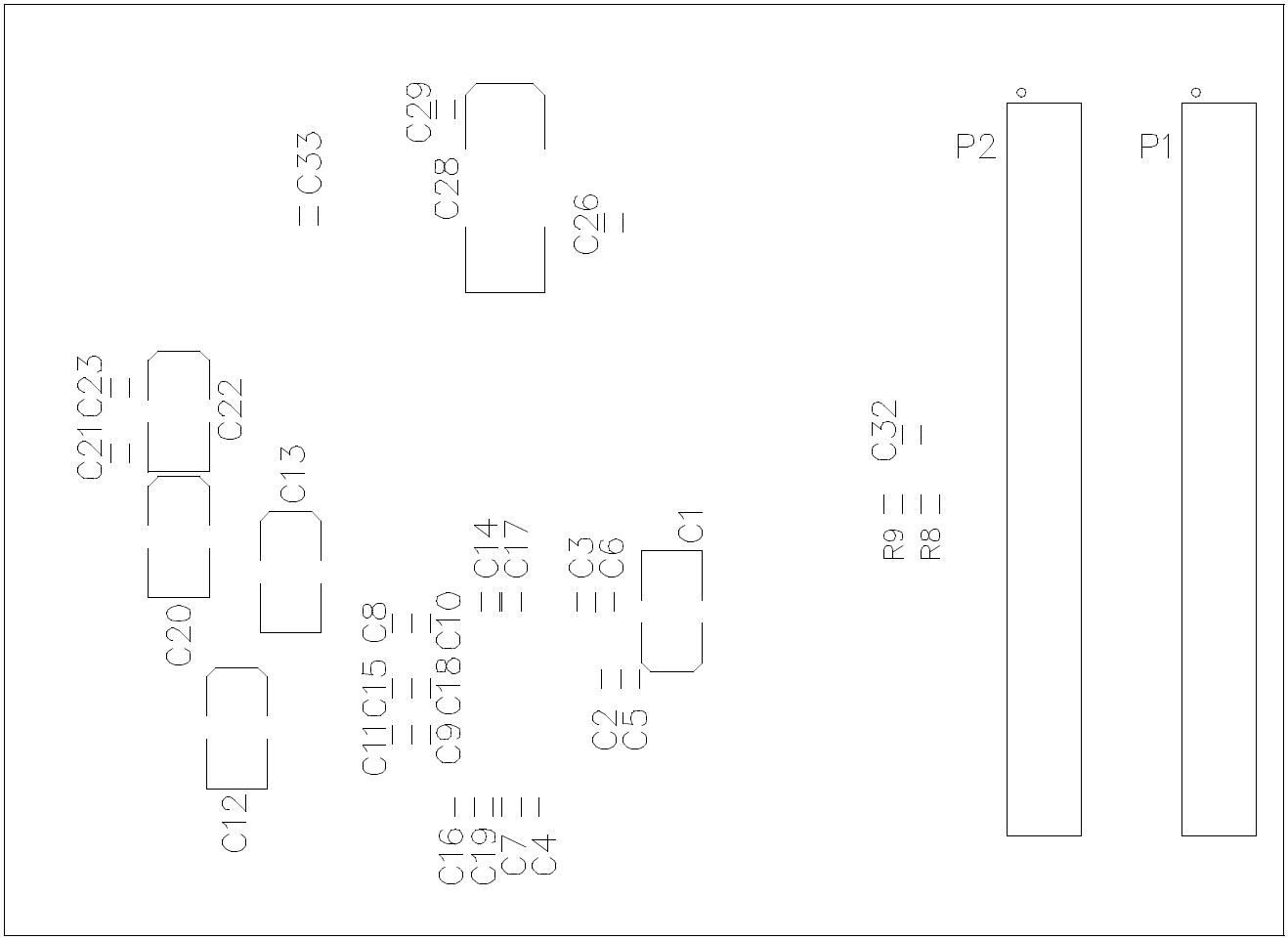

Figure 7-2: S5U13700B00C Board Layout (Bottom View)

8 Connecting the S5U13700B00C to the PC Card Adapter

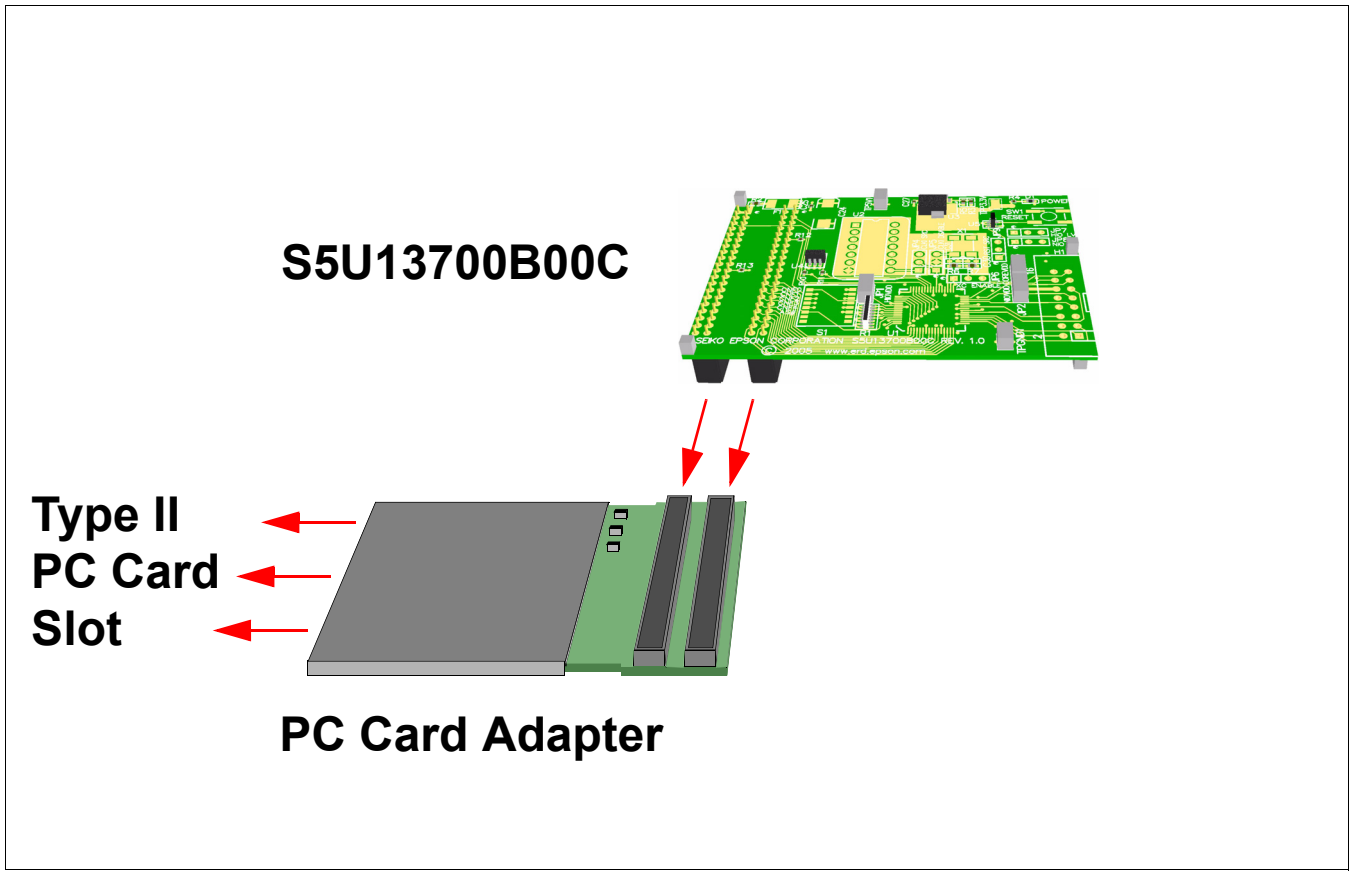

Figure 8-1: Connecting the S5U13700B00C to the PC Card Adapter

9 Change Record

X42A-G-002-01 Revision 1.1 - Issued: March 28, 2018

- updated Sales and Technical Support Section
- updated some formatting

X42A-G-002-01 Revision 1.0

- released as revision 1.0

10 Sales and Technical Support

For more information on Epson Display Controllers, visit the Epson Global website.

https://global.epson.com/products_and_drivers/semicon/products/display_controllers/

For Sales and Technical Support, contact the Epson representative for your region.

https://global.epson.com/products_and_drivers/semicon/information/support.html

Appendix A Epson PC Card Extender

This section describes the setup and operation of the PC Card Extender Board Rev 1.0. This board was designed as an evaluation interface for connecting Epson S1D137xx Mobile Graphics Engine Evaluation Boards to the PC Card Bus.

A.1 Features

The PC Card Extender Board Rev 1.0 includes the following features.

- Header Signals for connecting Epson S1D137xx Mobile Graphics Engine Evaluation Boards
- Epson Identification EEPROM
- Current limiting, resettable fuse
- LED power indicators
- Voltage Level shifting to 3.3V

A.2 General

The PC Card Extender Board is designed to be connected to a laptop supporting a PC Card Type II or Type III slot. The extender board includes an EEPROM containing the identification to specify it as an EPSON LCD controller. The software driver supplied by Epson will recognize this PC Card as an Epson LCD Controller.

The power supplies from the PC Card host are passed to the evaluation board headers. A resettable PolySwitch fuse (750mA) is placed on Vcc to protect the PC Card bus from excessive current consumption. If necessary, the evaluation board can be connected to an external power supply.

Note

Permanent damage to the host is possible if signals are shorted on the connector. Care must be taken in attaching the modules.

The performance of the Mobile Graphics Engine in this environment is directly proportional to the PC Card bus speeds. The maximum data bus transfer speed is 10MHz. The maximum transfer rate is 20M bytes/sec in 16-bit mode and 10M Bytes/sec in 8-bit mode. Note that the PC Card bus itself is 100% asynchronous and has no clock signals.

A.3 Power

The PC Card Extender Board requires 5V to be supplied / supported from the PC Card Slot. The extender board will not operate in a 3.3V only PC Card slot.

A.4 Bus Disable

Switch SW1 is used to disable the bus to the Epson Mobile Graphics Engine evaluation board. When the bus is disabled, the red LED (D2) turns "ON". For normal operations, the bus should be enabled, with SW1 positioned towards the clock X1 location.

Note

On some systems, the Bus Disable function must be "ON" when the PC Card Extender Board/Evaluation board combination is first plugged into the PC Card host. Once the OS has detected the PC Card, the Bus Disable function can be turned "OFF".

A.5 16-Bit PC Card Mode

To select 16-bit PC Card mode, switch SW2 must be positioned toward the clock X1 location. The S1D13700 is a 16-bit device and the drivers for the PC Card have been configured for 16-bit devices only. Therefore, 8-bit byte steering logic is not needed from the PC Card and should be placed in the 16-bit position.

A.6 Generic #1 / #2 Bus

Switch SW3 selects the control signals between Generic #1 or Generic #2 bus. The S5U13700B00C Evaluation Board does not require the setting of this switch and it should be positioned towards the clock X1 location.

A.7 Epson Evaluation Boards

The extender card provides a header to interface to Epson Mobile Graphics Engine Evaluation Boards. The header contains all the signals necessary for interfacing to the PC Card bus. The signals on the bus have been level shifted from 5V to 3.3V.

Vcc from the PC Card Bus is provided on the header, but considerations to the current draw should be noted. The evaluation board needs to supply it's own Vcc if the current draw is greater than what the PC Card bus can provide.

A.8 Epson Evaluation Board Header Pin Mapping

The CPU interface uses two female connectors (P1 and P2) which provide all the signals and power connections needed for direct PC Card. Generic #1 and Generic#2 bus control signals have been decoded and are selectable using SW2.

Refer to the schematics for the pinout of P1 and P2.