

**S1D13517 Display Controller**

# **Interfacing to TIANMA TFT Panels**

**Document Number: X92A-G-002-01.2**

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## Chapter 1 Introduction

This document provides complete information for enabling EPSON Display Controllers to control a variety of TIANMA Co., Ltd LCD panels. This document includes connector details, pin mappings, and example register settings.

For detailed technical information on EPSON Display Controllers or TIANMA LCD panels, please refer to the specification or technical manual for each product.

This document is updated as appropriate. Please check for the latest revision of this document before beginning any development. The latest revision of this document can be downloaded at [vdc.epson.com](http://vdc.epson.com).

This document discusses interfacing the S1D13517 to the following TIANMA TFT panel.

- TM104SBH01 (TFT 10.4inch, SVGA)

Refer to the TIANMA LCD products web site for more details on these panels:  
<http://tianma-europe.com/products/tftcolormodules/index.html>.

For inquiry, please visit SM Electronic Technologies Pvt. Ltd. (Epson sales representative) web site,  
<http://www.smetgroup.com/default.html>

## Chapter 2 Interfacing to the TIANMA TM104SBH01

The TIANMA TM104SBH01 TFT panel is compatible with the S1D13517 display controller. The following sections will provide connector details, pin mappings, and example register settings for these combinations.

### 2.1 TM104SBH01 Pin Mapping

The information in this section provides a connection example for the S1D13517 display controller. In addition to the pin connections for the selected display controller, the TM104SBH01 requires the following power supplies.

- VDD = +3.3V ( $\pm 0.3V$ )
- VF = +19.2V (LEDA = +19.2V, LEDK = 0V)

For VDD, select a voltage within the supportable range of the Display Controller.

For further details on the TM104SBH01, such as power consumption and absolute maximum ratings, please contact your TIANMA representative.

*Table 2-1: TM104SBH01 (CN1) Pin Mapping*

Pin #	Symbol	I/O	Description
1	VDD	P	Power Supply
2	VDD	P	Power Supply
3	GND	P	Ground
4	GND	P	Ground
5	IN0-	I	LVDS receiver negative signal channel 0
6	IN0+	I	LVDS receiver positive signal channel 0
7	GND	P	Ground
8	IN1-	I	LVDS receiver negative signal channel 1
9	IN1+	I	LVDS receiver positive signal channel 1
10	GND	P	Ground
11	IN2-	I	LVDS receiver negative signal channel 2
12	IN2+	I	LVDS receiver positive signal channel 2
13	GND	P	Ground
14	CLK-	I	LVDS receiver negative signal clock
15	CLK+	I	LVDS receiver positive signal clock
16	GND	P	Ground
17	NC	-	No connection
18	NC	-	No connection
19	GND	P	Ground
20	GND	P	Ground
<b>I---Input, O---Output, P--- Power/Ground</b>			

Table 2-2: Backlight Connector (CN2) Pin Mapping

Pin #	Symbol	I/O	Description
1	LEDA	P	LED driving anode (high voltage)
2	LEDK	P	LED driving cathode (low voltage)

Table 2-3: TP FPC (CN3) Pin Mapping

Pin #	Symbol	I/O	Description
1	Y2	I	ITO film
2	X2	I	ITO glass
3	Y1	I	ITO film
4	X1	I	ITO glass

## 2.2 Connecting the TM104SBH01 to the S1D13517

The following diagram shows an example implementation of the TM104SBH01 panel connected to the S1D13517.

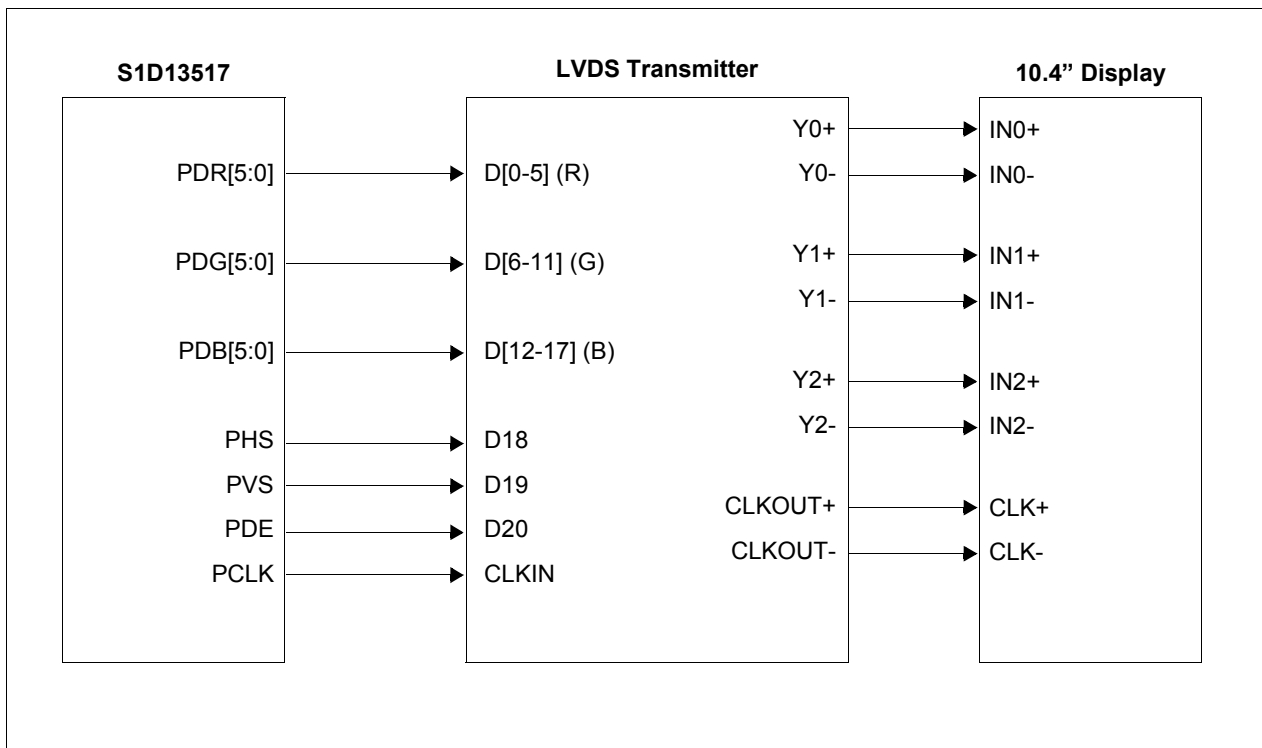


Figure 2-1: Connecting the TM104SBH01 to the S1D13517

## 2.3 S1D13517 Registers Settings for TM104SBH01 TFT Display

In addition to the pin connections, the S1D13517 internal registers must be configured appropriately for the TM104SBH01 LCD panel. The following tables provide example settings for display controller. However, these values are for reference only and may differ according to each specific implementation. For details on configuring the S1D13517 register values, see the S1D13517 Hardware Functional Specification, document number X92A-A-001-xx.

Table 2-4: S1D13517 Registers Settings for TM104SBH01 TFT Display

Register Index and Name	Parameter Value ( See Note )	Register Value Description
REG[04h] PLL D-Divider Register	0x17h	PLL Enable
REG[06h] PLL Setting Register 0	0x51h	Frequency of VCO
REG[08h] PLL Setting Register 1	0x01h	Dividing frequency of PLL clock
REG[0Ch] PLL N-Divider Register	0x59h	PLL Setting
REG[12h] CLK Source Select Register	0x01h	Clock Source selection bit
REG[04h] PLL D-Divider Register	0x97h	PLL Enable
REG[0Eh] SS Control Register 0	0x6Fh	Spread Spectrum Enable
REG[12h] CLK Source Select Register	0x91h	Clock Source selection bit
REG[68h] Power Save Register	0x01h	Note
REG[16h] Horizontal display width register	0x64h	Note
REG[18h] Horizontal non display period register	0x7Fh	Note
REG[1Ah] Vertical display height register0	0x57h	Note
REG[1Ch] Vertical display height register1	0x02h	Note
REG[1Eh] Vertical non display period register	0x16h	Note
REG[20h] PHS Pulse Width Register	0x27h	PHS Pulse Polarity
REG[22h] PHS Pulse Start Position Register	0x78h	Note
REG[24h] PVS Pulse Width Register	0x0Ah	PVS Pulse Polarity
REG[26h] PVS Pulse Start Position Register	0x04h	Note
REG[14h] LCD Panel Type Register	0x05h	Note
REG[28h] PCLK Polarity Register	0x00h	PCLK Polarity
REG[2Ah] Display Mode Register	0x01h	Note
REG[82h] SDRAM control Register 0	0x03h	Note
REG[84h] SDRAM Status Register 0	0x02h	Note
REG[90h] SDRAM Write Buffer Memory Size Register 0	0x60h	Note
REG[5Ah] Write Window X Start Position Register	0x00	Note
REG[5Ch] Write Window Y Start Position Register 0	0x00	Note
REG[5Eh] Write Window Y Start Position Register 1	0x00	Note
REG[60h] Write Window X End Position Register	0xC6	Note
REG[62h] Write Window Y End Position Register 0	0x4A	Note
REG[64h] Write Window Y End Position Register 1	0x03	Note

### Note

Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13517 register values, see the S1D13517 Hardware Functional Specification, document number X92A-A-001-xx.



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## Chapter 3 Change Record

### **X92A-G-002-01 Revision 1.2 - Issued: March 28, 2018**

- updated Sales and Technical Support Section
- updated some formatting

### **X92A-G-002-01 Revision 1.1 - Issued: December 4, 2012**

- chapter 1 Introduction - add “For inquiry, please visit SM Electronic Technologies Pvt. Ltd...”

### **X92A-G-002-01 Revision 1.0 - Issued: November 6, 2012**

- Initial release of this document

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## Chapter 4 Sales and Technical Support

For more information on Epson Display Controllers, visit the Epson Global website.

[https://global.epson.com/products\\_and\\_drivers/semicon/products/display\\_controllers/](https://global.epson.com/products_and_drivers/semicon/products/display_controllers/)



For Sales and Technical Support, contact the Epson representative for your region.

[https://global.epson.com/products\\_and\\_drivers/semicon/information/support.html](https://global.epson.com/products_and_drivers/semicon/information/support.html)

