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S1D13742 Mobile Graphics Engine

Interfacing to TIANMA TFT Panels

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SEIKO EPSON CORPORATION

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Chapter 1 Introduction

This document provides complete information for enabling EPSON Display Controllers to control a variety of TIANMA Co., Ltd LCD panels. This document includes connector details, pin mappings, and example register settings.

For detailed technical information on EPSON Display Controllers or TIANMA LCD panels, please refer to the specification or technical manual for each product.

This document is updated as appropriate. Please check for the latest revision of this document before beginning any development. The latest revision of this document can be downloaded at vdc.epson.com.

This document discusses interfacing the S1D13742 to the following TIANMA TFT panels.

- TM035KBH02 (TFT 3.5inch, QVGA)
- TM047NBH03 (TFT 4.7inch, QVGA)
- TM057KDH01 (TFT 5.7inch, QVGA)
- TM070RBH10 (TFT 7.0inch, WVGA)

Each TIANMA TFT panel is compatible with the S1D13742 (QFP 144-pin or PBGA 144-pin) Epson display controller.

The following table summarizes the TIANMA TFT panels which are compatible with the S1D13742.

Table 1-1 : S1D13742 Compatible TIANMA TFT Panels

S1D13742	TIANMA Panel
✓	TM035KBH02
✓	TM047NBH03
✓	TM057KDH01
✓	TM070KBH01

Refer to the TIANMA LCD products web site for more details on these panels,
http://tianma-europe.com/products/tftcolormodules/index.html.

For inquiry, please visit SM Electronic Technologies Pvt. Ltd. (Epson sales representative) web site,
http://www.smetgroup.com/default.html

Chapter 2 Interfacing to the TIANMA TM035KBH02

The TIANMA TM035KBH02 TFT panel is compatible with the S1D13742 display controller. The following sections will provide connector details, pin mappings, and example register settings for these combinations.

2.1 TM035KBH02 Pin Mapping

The information in this section provides a connection example for the S1D13742 display controller. In addition to the pin connections for the display controller, the TM035KBH02 requires the following power supplies.

- VDD = +3.3V (±0.3V)
- VF = +19.2V (LED Anode = +19.2V, LED Cathode = 0V)

For VDD, select a voltage within the supportable range of the Display Controller.

For further details on the TM035KBH02, such as power consumption and absolute maximum ratings, please contact your TIANMA representative.

Table 2-1 : TM035KBH02 Pin Mapping

Pin #	Symbol	I/O	Description
1, 2	LED Cathode	I	LED Cathode
3, 4	LED Anode	I	LED Anode
5	NC	-	No Connect
6	RESET	I	Reset
7	NC	-	No Connect
8	NC	-	No Connect
9	NC	-	No Connect
10	NC	-	No Connect
11	NC	-	No Connect
12	D00	I	Data 00
13	D01	I	Data 01
14	D02	I	Data 02
15	D03	I	Data 03
16	D04	I	Data 04
17	D05	I	Data 05
18	D06	I	Data 06
19	D07	I	Data 07
20	D08	I	Data 08
21	D09	I	Data 09
22	D10	I	Data 10
23	D11	I	Data 11
24	D12	I	Data 12

Table 2-1 : TM035KBH02 Pin Mapping

Pin #	Symbol	I/O	Description
25	D13	I	Data 13
26	D14	I	Data 14
27	D15	I	Data 15
28	D16	I	Data 16
29	D17	I	Data 17
30	D18	I	Data 18
31	D19	I	Data 19
32	D20	I	Data 20
33	D21	I	Data 21
34	D22	I	Data 22
35	D23	I	Data 23
36	HSYNC	I	Horizontal Synchronous Signal
37	VSYNC	I	Vertical Synchronous Signal
38	CLK	I	Data Clock
39	NC	-	No Connect
40	NC	-	No Connect
41	VDD	P	power supply
42	VDD	P	power supply
43	SPENA	I	Serial port data enable signal
44	NC	-	No Connect
45	NC	-	No Connect
46	NC	-	No Connect
47	NC	-	No Connect
48	NC	-	No Connect
49	SPCK	I	SPI Serial Clock
50	SPDA	I/O	SPI Serial Data Input/output
51	NC	-	No Connect
52	DEN	I	Data enabling signal
53	GND	P	Ground
54	GND	P	Ground

I---Input, O---Output, P--- Power/Ground

2.2 Connecting the TM035KBH02 to the S1D13742

The following diagram shows an example implementation of the TM035KBH02 panel connected to the S1D13742.

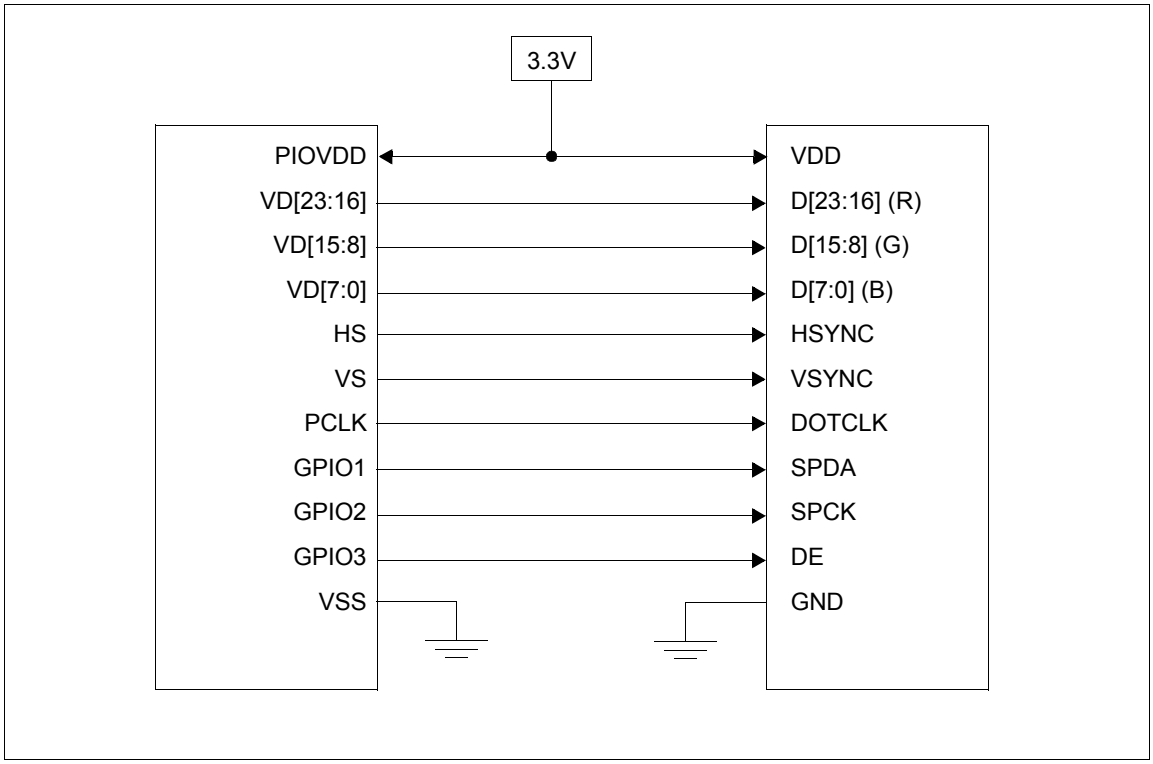

Figure 2-1: Connecting the TM035KBH02 to the S1D13742

The following table provides a detailed pin listing for the required connections between the TM035KBH02 and the S1D13742.

Table 2-2 : Required Connections Between the TM035KBH02 and the S1D13742

LCD Pin #	LCD Symbol	LCD Pin Description	S1D13742 QFP Pin #	S1D13742 Pin Name
1, 2	LED Cathode	LED Cathode	—	—
3, 4	LED Anode	LED Anode	—	—
5	NC	No Connect	—	—
6	RESET	Reset	97	RESET#
7	NC	No Connect	—	—
8	NC	No Connect	—	—
9	NC	No Connect	—	—
10	NC	No Connect	—	—
11	NC	No Connect	—	—
12	D00	Data 00(B0)	45	VD0
13	D01	Data 01(B1)	49	VD1

Table 2-2 : Required Connections Between the TM035KBH02 and the S1D13742 (Continued)

LCD Pin #	LCD Symbol	LCD Pin Description	S1D13742 QFP Pin #	S1D13742 Pin Name
14	D02	Data 02(B2)	54	VD2
15	D03	Data 03(B3)	59	VD3
16	D04	Data 04(B4)	62	VD4
17	D05	Data 05(B5)	65	VD5
18	D06	Data 06(B6)	—	—
19	D07	Data 07(B7)	—	—
20	D08	Data 08(G0)	66	VD6
21	D09	Data 09(G1)	42	VD7
22	D10	Data 10(G2)	44	VD8
23	D11	Data 11(G3)	48	VD9
24	D12	Data 12(G4)	51	VD10
25	D13	Data 13(G5)	58	VD11
26	D14	Data 14(G6)	—	—
27	D15	Data 15(G7)	—	—
28	D16	Data 16(R0)	61	VD12
29	D17	Data 17(R1)	64	VD13
30	D18	Data 18(R2)	30	VD14
31	D19	Data 19(R3)	29	VD15
32	D20	Data 20(R4)	43	VD16
33	D21	Data 21(R5)	47	VD17
34	D22	Data 22(R6)	—	—
35	D23	Data 23(R7)	—	—
36	HSYNC	Horizontal Synchronous Signal	9	HS
37	VSYNC	Vertical Synchronous Signal	10	VS
38	CLK	Data Clock	11	PCK
39	NC	No Connect	—	—
40	NC	No Connect	—	—
41	VDD	power supply	Note 2	PIOVDD
42	VDD	power supply	Note 2	PIOVDD
43	SPENA	Serial port data enable signal	88	GPIO0
44	NC	No Connect	—	—
45	NC	No Connect	—	—
46	NC	No Connect	—	—
47	NC	No Connect	—	—
48	NC	No Connect	—	—
49	SPCK	SPI Serial Clock	87	GPIO1
50	SPDA	SPI Serial Data Input/output	83	GPIO2

Table 2-2 : Required Connections Between the TM035KBH02 and the S1D13742 (Continued)

LCD Pin #	LCD Symbol	LCD Pin Description	S1D13742 QFP Pin #	S1D13742 Pin Name
51	NC	No Connect	—	—
52	DEN	Data enabling signal	8	DE
53	GND	Ground	Note 1	VSS
54	GND	Ground	Note 1	VSS

Note

1. Allocation of VSS pins: 5, 7, 18, 21, 32, 34, 39, 41, 53, 56, 68, 70, 78, 90, 103, 105, 112, 116, 119, 135, 144, 129
2. Allocation of VDD pins: 4, 17, 20, 33, 38, 52, 55, 69, 77, 102, 113, 120, 128, 143

2.3 S1D13742 Register Settings for the TM035KBH02 TFT Display

In addition to the pin connections, the S1D13742 internal registers must be configured appropriately for the TM035KBH02 LCD panel. The following tables provide example settings for display controller. However, these values are for reference only and may differ according to each specific implementation. For details on configuring the S1D13742 register values, see the S1D13742 Hardware Functional Specification, document number X63A-A-001-xx.

Table 2-3 : S1D13742 Register Settings for the TM035KBH02

Register Index and Name	Parameter Value (See Note)	Register Value Description
REG[56h] Power Save Register	0x02h	Sleep mode is enabled
REG[04h] PLL M-Divide Register	0x18h	Depending on CLKI that is 25MHz (Note)
REG[06h] PLL Setting Register 0	0xF8h	Value Fixed
REG[08h] PLL Setting Register 1	0x80h	Value Fixed
REG[0Ah] PLL Setting Register 2	0x28h	Value Fixed
REG[0Ch] PLL Setting Register 3	0x00h	Value Fixed
REG[0Eh] PLL Setting Register 4	0x3Ch	Register are used to configure PLL O/P (Note)
REG[12h] CLK Source Select Register	0x31h	Clock source for PCLK is SYSCLK
REG[14h] Panel Type Register	0x00h	Interface is 16 bit
REG[16h] Horizontal display width register	0x28h	Note
REG[18h] Horizontal non display period register	0x64h	Note
REG[1Ah] Vertical display height register0	0xF0h	Note
REG[1Ch] Vertical display height register1	0x00h	Note
REG[1Eh] Vertical non display period register	0x09h	Note
REG[20h] HS Pulse Width register	0x14h	Note
REG[22h] HS Pulse Start position register 0	0x28h	Note
REG[24h] VS Pulse width register	0x02h	Note
REG[26h] VS Pulse Start position register 0	0x01h	Note
REG[28h] PCLK polarity register	0x80h	PCLK O/P data at falling edge

Table 2-3 : S1D13742 Register Settings for the TM035KBH02 (Continued)

Register Index and Name	Parameter Value (See Note)	Register Value Description
REG[2Ah] Input mode register	0x01h	Default
REG[56h] Power Save Register	0x00h	Sleep mode is disabled
REG[38h] Window X start position register 0	0x00h	Horizontal start Position (LSB)
REG[3Ah] Window X start position register 1	0x00h	Horizontal start Position (MSB)
REG[3Ch] Window Y start position register 0	0x00h	Vertical start position (LSB)
REG[3Eh] Window Y start position register 1	0x00h	Vertical start Position (MSB)
REG[40h] Window X End position register 0	0x3Fh	Horizontal end Position (LSB)
REG[42h] Window X End position register 1	0x01h	Horizontal end Position (MSB)
REG[44h] Window Y End position register 0	0xEFh	Vertical end position (LSB)
REG[46h] Window Y End position register 1	0x00h	Vertical end position (MSB)

Note

Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13742 register values, see the S1D13742 Hardware Functional Specification, document number X63A-A-001-xx.

Chapter 3 Interfacing to the TIANMA TM047NBH03

The TIANMA TM047NBH03 TFT panel is compatible with the S1D13742 display controller. The following sections provide connector details, pin mappings, and example register settings for these combinations.

3.1 TM047NBH03 Pin mapping

The information in this section provides a connection example for the S1D13742 display controller. In addition to the pin connections for the display controller, the TM047NBH03 requires the following power supplies.

- VDD = +3.3V (±0.3V)
- VF = +16V (LED + = +16V, LED - = 0V)

For VDD, select a voltage within the supportable range of the Display Controller.

For further details on the TM047NBH03, such as power consumption and absolute maximum ratings, please contact your TIANMA representative.

Table 3-1: TM047NBH03 Pin mapping

Pin #	Symbol	I/O	Description
1	VLED-	P	Power for LED
2	VLED+	P	Power for LED
3	GND	P	Power Ground
4	VDD	P	Power Supply (+3.3V)
5	R0	I	Red data
6	R1	I	Red data
7	R2	I	Red data
8	R3	I	Red data
9	R4	I	Red data
10	R5	I	Red data
11	R6	I	Red data
12	R7	I	Red data
13	G0	I	Green data
14	G1	I	Green data
15	G2	I	Green data
16	G3	I	Green data
17	G4	I	Green data
18	G5	I	Green data
19	G6	I	Green data
20	G7	I	Green data
21	B0	I	Blue data
22	B1	I	Blue data

Table 3-1: TM047NBH03 Pin mapping (Continued)

Pin #	Symbol	I/O	Description
23	B2	I	Blue data
24	B3	I	Blue data
25	B4	I	Blue data
26	B5	I	Blue data
27	B6	I	Blue data
28	B7	I	Blue data
29	GND	P	Power Ground
30	PCLK	I	Pixel clock
31	DISP	I	Display on/off
32	HSYNC	I	Horizontal sync signal
33	VSYNC	I	Vertical sync signal
34	DE	I	Date enable
35	NC	-	No connection
36	GND	P	Power Ground
37	X1	P	Touch Panel X (Right Side)
38	Y1	P	Touch Panel Y (6 Clock Side)
39	X2	P	Touch Panel X (Left Side)
40	Y2	P	Touch Panel Y (12 Clock Side)

I = Input, O = Output, P = Power/Ground

3.2 Connecting the TM047NBH03 to the S1D13742

The following diagram shows an example implementation of the TM047NBH03 panel connected to the S1D13742.

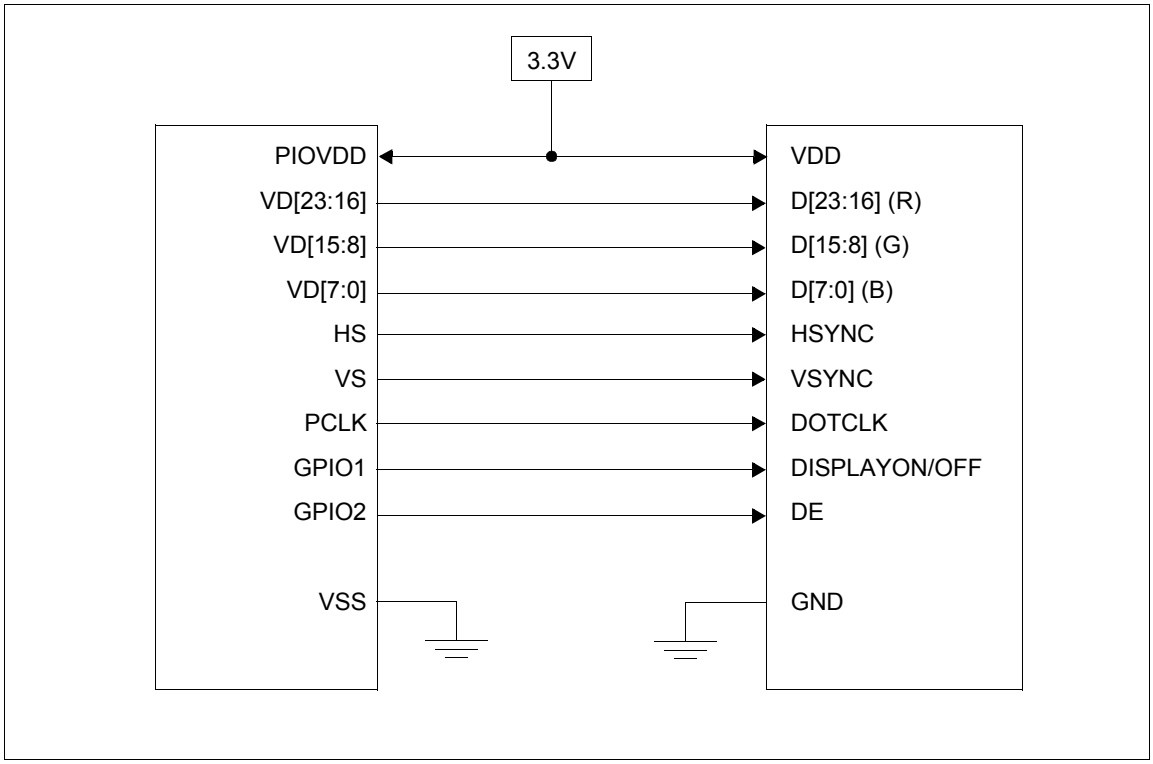

Figure 3-1: Connecting the TM047NBH03 to the S1D13742

The following table provides a detailed pin listing for the required connections between the TM047NBH03 and the S1D13742

Table 3-2 : Required Connections Between the TM047NBH03 and the S1D13742

LCD Pin #	LCD Symbol	LCD Description	S1D13742 QFP Pin #	S1D13742 Pin Name
1	VLED-	Power for LED	-	-
2	VLED+	Power for LED	-	-
3	GND	Power Ground	Note 1	VSS
4	VDD	Power Supply (+3.3V)	Note 2	PIOVDD
5	R0	Red data	61	VD12
6	R1	Red data	64	VD13
7	R2	Red data	30	VD14
8	R3	Red data	29	VD15
9	R4	Red data	43	VD16
10	R5	Red data	47	VD17
11	R6	Red data	-	-

Table 3-2 : Required Connections Between the TM047NBH03 and the S1D13742 (Continued)

LCD Pin #	LCD Symbol	LCD Description	S1D13742 QFP Pin #	S1D13742 Pin Name
12	R7	Red data	-	-
13	G0	Green data	66	VD6
14	G1	Green data	42	VD7
15	G2	Green data	44	VD8
16	G3	Green data	48	VD9
17	G4	Green data	51	VD10
18	G5	Green data	58	VD11
19	G6	Green data	-	-
20	G7	Green data	-	-
21	B0	Blue data	45	VD0
22	B1	Blue data	49	VD1
23	B2	Blue data	54	VD2
24	B3	Blue data	59	VD3
25	B4	Blue data	62	VD4
26	B5	Blue data	65	VD5
27	B6	Blue data	-	-
28	B7	Blue data	-	-
29	GND	Power Ground	Note 1	VSS
30	PCLK	Pixel clock	11	PCLK
31	DISP	Display on/off	88	GPIO0
32	HSYNC	Horizontal sync signal	9	HS
33	VSYNC	Vertical sync signal	10	VS
34	DE	Date enable	8	DE
35	NC	No connection	-	-
36	GND	Power Ground	Note 1	VSS
37	X1	Touch Panel X (Right Side)	-	-
38	Y1	Touch Panel Y (6 Clock Side)	-	-
39	X2	Touch Panel X (Left Side)	-	-
40	Y2	Touch Panel Y (12 Clock Side)	-	-

Note

1. Allocation of VSS pins: 5, 7, 18, 21, 32, 34, 39, 41, 53, 56, 68, 70, 78, 90, 103, 105, 112, 116, 119, 135, 144, 129
2. Allocation of VDD pins: 4, 17, 20, 33, 38, 52, 55, 69, 77, 102, 113, 120, 128, 143

3.3 S1D13742 Register Settings for the TM047NBH03 TFT Display

In addition to the pin connections, the S1D13742 internal registers must be configured appropriately for the TM047NBH03 LCD panel. The following tables provide example settings for display controller. However, these values are for reference only and may differ according to each specific implementation. For details on configuring the S1D13742 register values, see the S1D13742 Hardware Functional Specification, document number X63A-A-001-xx

Table 3-3 : S1D13742 Register Settings for the TM047NBH03

Register Index and Name	Parameter Value (See Note)	Register Value Description
REG[56h] Power Save Register	0x02h	Sleep mode is enabled
REG[04h] PLL M-Divide Register	0x18h	Depending on CLKI that is 25MHz (Note)
REG[06h] PLL Setting Register 0	0xF8h	Value Fixed
REG[08h] PLL Setting Register 1	0x80h	Value Fixed
REG[0Ah] PLL Setting Register 2	0x28h	Value Fixed
REG[0Ch] PLL Setting Register 3	0x00h	Value Fixed
REG[0Eh] PLL Setting Register 4	0x2Dh	Register are used to configure PLL O/P (Note)
REG[12h] CLK Source Select Register	0x09h	Clock source for PCLK is SYSCLK
REG[14h] Panel Type Register	0x00h	Interface is 16 bit
REG[16h] Horizontal display width register	0x50h	Note
REG[18h] Horizontal non display period register	0x3Ch	Note
REG[1Ah] Vertical display height register0	0x10h	Note
REG[1Ch] Vertical display height register1	0x01h	Note
REG[1Eh] Vertical non display period register	0x06h	Note
REG[20h] HS Pulse Width register	0x14h	Note
REG[22h] HS Pulse Start position register 0	0x28h	Note
REG[24h] VS Pulse width register	0x02h	Note
REG[26h] VS Pulse Start position register 0	0x08h	Note
REG[28h] PCLK polarity register	0x80h	PCLK O/P data at falling edge
REG[2Ah] Input mode register	0x01h	Default
REG[56h] Power Save Register	0x00h	Sleep mode is disabled
REG[38h] Window X start position register 0	0x00h	Horizontal start Position (LSB)
REG[3Ah] Window X start position register 1	0x00h	Horizontal start Position (MSB)
REG[3Ch] Window Y start position register 0	0x00h	Vertical start position (LSB)
REG[3Eh] Window Y start position register 1	0x00h	Vertical start Position (MSB)
REG[40h] Window X End position register 0	0xDFh	Horizontal end Position (LSB)
REG[42h] Window X End position register 1	0x01h	Horizontal end Position (MSB)
REG[44h] Window Y End position register 0	0x0Fh	Vertical end position (LSB)
REG[46h] Window Y End position register 1	0x01h	Vertical end position (MSB)

Note

Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13742 register values, see the S1D13742 Hardware Functional Specification, document number X63A-A-001-xx.

Chapter 4 Interfacing to the TIANMA TM057KDH01

The TIANMA TM057KDH01 TFT panel is compatible with the S1D13742 display controller. The following sections provide connector details, pin mappings, and example register settings for these combinations.

4.1 TM057KDH01 Pin Mapping

The information in this section provides a connection example for the S1D13742 display controller. In addition to the pin connections for the display controller, the TM057KDH01 requires the following power supplies.

- VDD = +3.3V (±0.3V)
- VF = +18.15V (AN1-3 = +18.15V, CA1-3 = 0V)

For VDD, select a voltage within the supportable range of the Display Controller.

For further details on the TM057KDH01, such as power consumption and absolute maximum ratings, please contact your TIANMA representative.

Table 4-1 : TM057KDH01 Pin Mapping

Pin #	Symbol	I/O	Description
1	GND	P	Ground
2	DOTCLK	I	Dot clock: latch data at falling edge of DOTCLOCK
3	HSYNC	I	Horizontal sync signal. Pull low or floating in DE mode
4	VSYNC	I	Vertical sync signal. Pull low or floating in DE mode
5	GND	P	Ground
6	R0	I	Red data (LSB)
7	R1	I	Red data
8	R2	I	Red data
9	R3	I	Red data
10	R4	I	Red data
11	R5	I	Red data (MSB)
12	GND	P	Ground
13	G0	I	Green data (LSB)
14	G1	I	Green data
15	G2	I	Green data
16	G3	I	Green data
17	G4	I	Green data
18	G5	I	Green data (MSB)
19	GND	P	Ground
20	B0	I	Blue data (LSB)
21	B1	I	Blue data
22	B2	I	Blue data

Table 4-1 : TM057KDH01 Pin Mapping (Continued)

Pin #	Symbol	I/O	Description
23	B3	I	Blue data
24	B4	I	Blue data
25	B5	I	Blue data (MSB)
26	GND	P	Ground
27	ENABLE	I	Data enable signal in DE mode
28	VCC	P	Power Supply
29	VCC	P	Power Supply
30	R/L	I	Set horizontal scan direction: Low/NC: left to right; High: right to left
31	U/D	I	Set vertical scan direction: High/NC: up to down; Low: down to up
32	NC	I	No Connection
33	GND	P	Ground

I---Input, O---Output, P--- Power/Ground

4.2 Connecting the TM057KDH01 to the S1D13742

The following diagram shows an example implementation of the TM057KDH01 panel connected to the S1D13742.

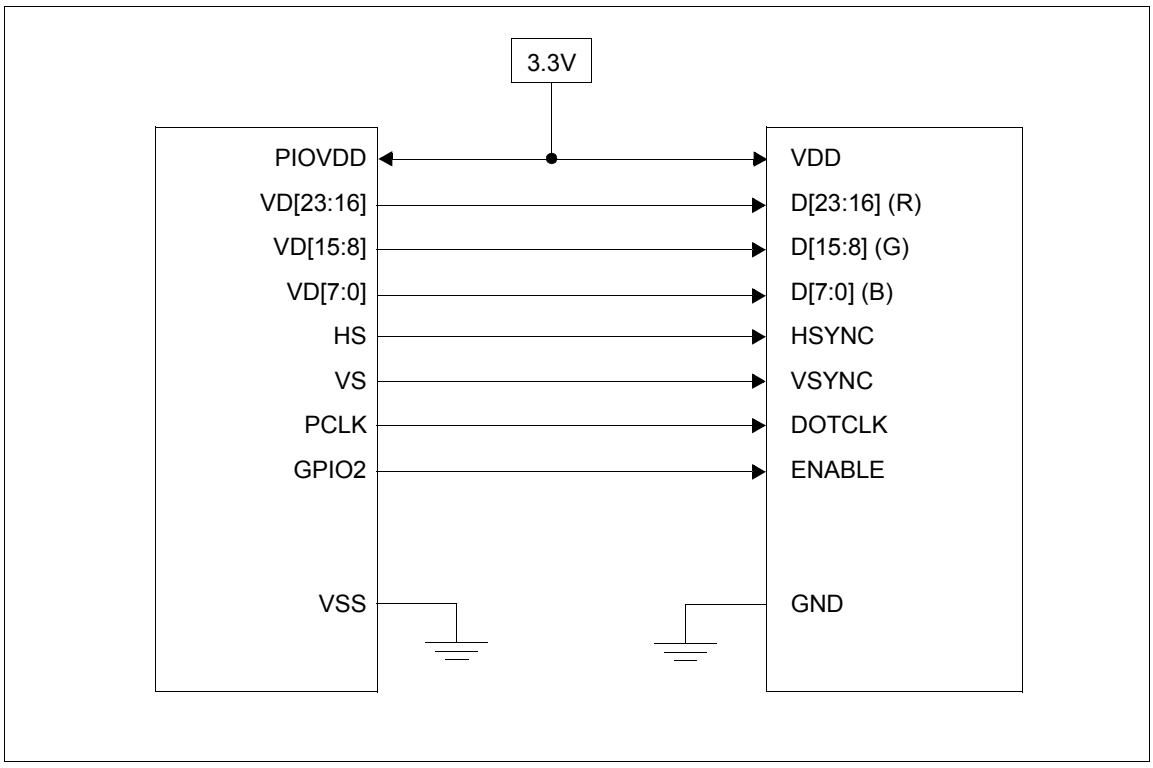

Figure 4-1: Connecting the TM057KDH01 to the S1D13742

The following table provides a detailed pin listing for the required connections between the TM057KDH01 and the S1D13742

Table 4-2 : Required Connections Between the TM057KDH01 and the S1D13742

LCD Pin #	LCD Symbol	LCD Description	S1D13742 QFP Pin #	S1D13742 Pin Name
1	GND	Ground	Note 1	VSS
2	DOTCLK	Dot clock: latch data at falling edge of DOTCLOCK	11	PCLK
3	HSYNC	Horizontal sync signal. Pull low or floating in DE mode	9	HS
4	VSYNC	Vertical sync signal. Pull low or floating in DE mode	10	VS
5	GND	Ground	Note 1	VSS
6	R0	Red data (LSB)	61	VD12
7	R1	Red data	64	VD13
8	R2	Red data	30	VD14
9	R3	Red data	29	VD15
10	R4	Red data	43	VD16
11	R5	Red data (MSB)	47	VD17
12	GND	Ground	Note 1	VSS
13	G0	Green data (LSB)	66	VD6
14	G1	Green data	42	VD7
15	G2	Green data	44	VD8
16	G3	Green data	48	VD9
17	G4	Green data	51	VD10
18	G5	Green data (MSB)	58	VD11
19	GND	Ground	Note 1	VSS
20	B0	Blue data (LSB)	45	VD0
21	B1	Blue data	49	VD1
22	B2	Blue data	54	VD2
23	B3	Blue data	59	VD3
24	B4	Blue data	62	VD4
25	B5	Blue data (MSB)	65	VD5
26	GND	Ground	Note 1	VSS
27	ENABLE	Data enable signal in DE mode	8	DE
28	VCC	Power Supply	Note 2	PIOVDD
29	VCC	Power Supply	Note 2	PIOVDD
30	R/L	Set horizontal scan direction: Low/NC: left to right; High: right to left	—	—
31	U/D	Set vertical scan direction: High/NC: up to down; Low: down to up	—	—
32	NC	No Connection	—	—
33	GND	Ground	Note 1	VSS

Note

1. Allocation of VSS pins: 5, 7, 18, 21, 32, 34, 39, 41, 53, 56, 68, 70, 78, 90, 103, 105, 112, 116, 119, 135, 144, 129
2. Allocation of VDD pins: 4, 17, 20, 33, 38, 52, 55, 69, 77, 102, 113, 120, 128, 143

4.3 S1D13742 Register Settings for the TM057KDH01 TFT Display

In addition to the pin connections, the S1D13742 internal registers must be configured appropriately for the TM057KDH01 LCD panel. The following tables provide example settings for display controller. However, these values are for reference only and may differ according to each specific implementation. For details on configuring the S1D13742 register values, see the S1D13742 Hardware Functional Specification, document number X63A-A-001-xx.

Table 4-3: Register Settings for the TM057KDH01 TFT Display

Register Index and Name	Parameter Value (See Note)	Register Value Description
REG[56h] Power Save Register	0x02h	Sleep mode is enabled
REG[04h] PLL M-Divide Register	0x18h	Depending on CLKI that is 25MHz (Note)
REG[06h] PLL Setting Register 0	0xF8h	Value Fixed
REG[08h] PLL Setting Register 1	0x80h	Value Fixed
REG[0Ah] PLL Setting Register 2	0x28h	Value Fixed
REG[0Ch] PLL Setting Register 3	0x00h	Value Fixed
REG[0Eh] PLL Setting Register 4	0x2Dh	Register are used to configure PLL O/P (Note)
REG[12h] CLK Source Select Register	0x09h	Clock source for PCLK is SYSCLK
REG[14h] Panel Type Register	0x00h	Interface is 16 bit
REG[16h] Horizontal display width register	0x28h	Note
REG[18h] Horizontal non display period register	0x14h	Note
REG[1Ah] Vertical display height register0	0xF0h	Note
REG[1Ch] Vertical display height register1	0x00h	Note
REG[1Eh] Vertical non display period register	0x06h	Note
REG[20h] HS Pulse Width register	0x14h	Note
REG[22h] HS Pulse Start position register 0	0x2Dh	Note
REG[24h] VS Pulse width register	0x02h	Note
REG[26h] VS Pulse Start position register 0	0x01h	Note
REG[28h] PCLK polarity register	0x80h	PCLK O/P data at falling edge
REG[2Ah] Input mode register	0x01h	Default
REG[56h] Power Save Register	0x00h	Sleep mode is disabled
REG[38h] Window X start position register 0	0x00h	Horizontal start Position (LSB)
REG[3Ah] Window X start position register 1	0x00h	Horizontal start Position (MSB)
REG[3Ch] Window Y start position register 0	0x00h	Vertical start position (LSB)
REG[3Eh] Window Y start position register 1	0x00h	Vertical start Position (MSB)
REG[40h] Window X End position register 0	0x3Fh	Horizontal end Position (LSB)
REG[42h] Window X End position register 1	0x01h	Horizontal end Position (MSB)
REG[44h] Window Y End position register 0	0xEFh	Vertical end position (LSB)
REG[46h] Window Y End position register 1	0x00h	Vertical end position (MSB)

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13742 register values, see the S1D13742 Hardware Functional Specification, document number X63A-A-001-xx.

Chapter 5 Interfacing to the TIANMA TM070RBH10

The TIANMA TM070RBH10 TFT panel is compatible with the S1D13742 display controller. The following sections will provide connector details, pin mappings, and example register settings for these combinations.

5.1 TM070RBH10 Pin Mapping

The information in this section provides a connection example for the S1D13742 display controller. In addition to the pin connections for the display controller, the TM070RBH10 requires the following power supplies.

- VDD = +3.3V (±0.3V)
- VGH = +22V
- VGL = -7.0V
- VCOM = +3.8V
- VF = +9.6V (VLED + = +9.6V, VLED - = 0V)

For VDD, select a voltage within the supportable range of the Display Controller.

For further details on the TM070RBH10, such as power consumption and absolute maximum ratings, please contact your TIANMA representative.

Table 5-1 : TM070RBH10 Pin Mapping

Pin #	Symbol	I/O	Description
1	VLED+	P	LED Anode
2	VLED+	P	LED Anode
3	VLED-	P	LED Cathode
4	VLED-	P	LED Cathode
5	GND	P	Ground
6	VCOM	P	Common voltage input
7	VCC	P	Digital power supply
8	MODE	I	DE/SYNC mode select. H:DE mode, L:SYNC mode
9	DE	I	Data enable signal, active high to enable data
10	VSYNC	I	Vertical Synchronous Signal
11	HSYNC	I	Horizontal Synchronous Signal
12	B7(MSB)	I	Blue data
13	B6	I	Blue data
14	B5	I	Blue data
15	B4	I	Blue data
16	B3	I	Blue data
17	B2	I	Blue data
18	B1	I	Blue data

Table 5-1 : TM070RBH10 Pin Mapping (Continued)

Pin #	Symbol	I/O	Description
19	B0(LSB)	I	Blue data
20	G7(MSB)	I	Green data
21	G6	I	Green data
22	G5	I	Green data
23	G4	I	Green data
24	G3	I	Green data
25	G2	I	Green data
26	G1	I	Green data
27	G0(LSB)	I	Green data
28	R7(MSB)	I	Red data
29	R6	I	Red data
30	R5	I	Red data
31	R4	I	Red data
32	R3	I	Red data
33	R2	I	Red data
34	R1	I	Red data
35	R0(LSB)	I	Red data
36	GND	P	Ground
37	DCLK	I	Clock for input data
38	GND	P	Ground
39	LR	I	Source left or right sequence control
40	UD	I	Gate up or down scan control
41	VGH	P	Positive power of TFT
42	VGL	P	Negative power of TFT
43	AVDD	P	Analog power supply
44	RESET	I	Global reset pin
45	NC	-	No Connect
46	VCOM	P	Common voltage input
47	DITHB	I	Dithering setting: H: 6bit resolution, L: 8bit resolution
48	GND	P	Ground
49	NC	-	No Connect
50	NC	-	No Connect

I---Input, O---Output, P--- Power/Ground

5.2 Connecting the TM070RBH10 to the S1D13742

The following diagram shows an example implementation of the TM070RBH10 panel connected to the S1D13742.

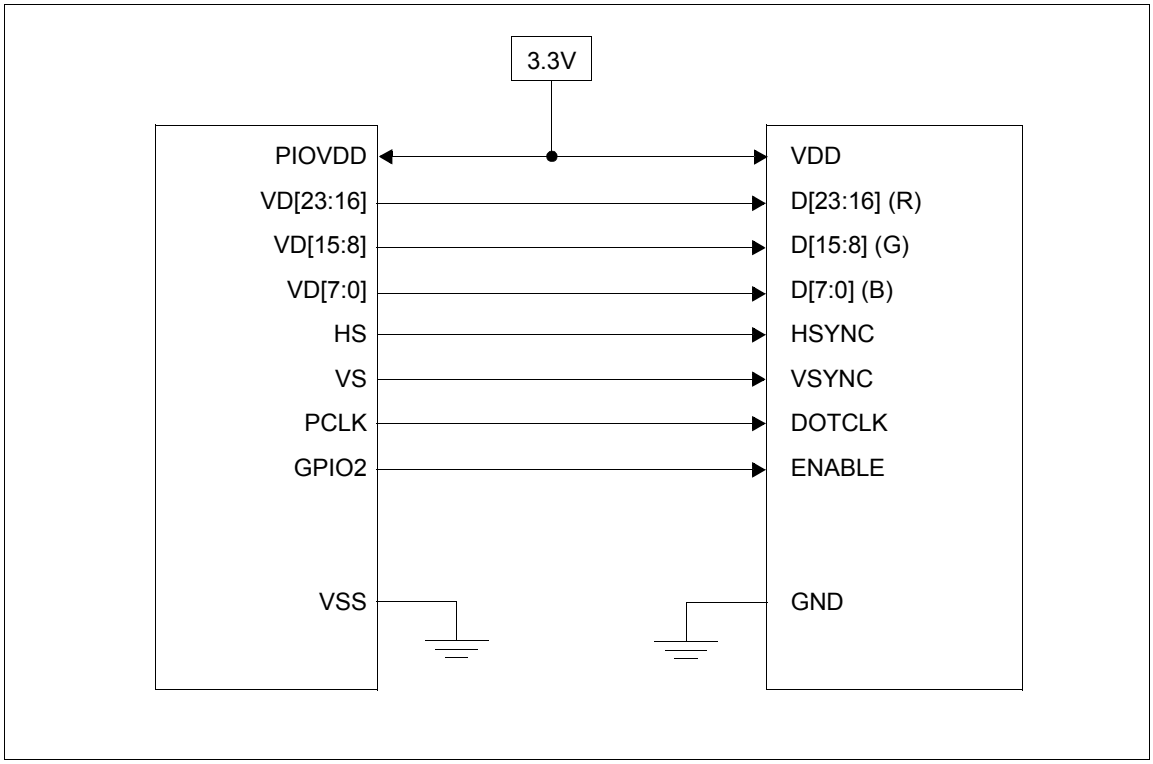

Figure 5-1: Connecting the TM070RBH10 to the S1D13742

The following table provides a detailed pin listing for the required connections between the TM070RBH10 and the S1D13742

Table 5-2: Required Connections Between the TM070RBH10 and the S1D13742

LCD Pin #	LCD Symbol	Description	S1D13742 QFP Pin #	S1D13742 Pin Name
1	VLED+	LED Anode	-	-
2	VLED+	LED Anode	-	-
3	VLED-	LED Cathode	-	-
4	VLED-	LED Cathode	-	-
5	GND	Ground	Note 1	VSS
6	VCOM	Common voltage input	-	-
7	VCC	Digital power supply	Note 2	PIOVDD
8	MODE	DE/SYNC mode select. H:DE mode, L:SYNC mode	-	-
9	DE	Data enable signal, active high to enable data	8	DE
10	VSYNC	Vertical Synchronous Signal	10	VS
11	HSYNC	Horizontal Synchronous Signal	9	VS
12	B7(MSB)	Blue data	-	-
13	B6	Blue data	-	-

Table 5-2: Required Connections Between the TM070RBH10 and the S1D13742 (Continued)

LCD Pin #	LCD Symbol	Description	S1D13742 QFP Pin #	S1D13742 Pin Name
14	B5	Blue data	65	VD5
15	B4	Blue data	62	VD4
16	B3	Blue data	59	VD3
17	B2	Blue data	54	VD2
18	B1	Blue data	49	VD1
19	B0(LSB)	Blue data	45	VD0
20	G7(MSB)	Green data	-	-
21	G6	Green data	-	-
22	G5	Green data	58	VD11
23	G4	Green data	51	VD10
24	G3	Green data	48	VD9
25	G2	Green data	44	VD8
26	G1	Green data	42	VD7
27	G0(LSB)	Green data	66	VD6
28	R7(MSB)	Red data	-	-
29	R6	Red data	-	-
30	R5	Red data	47	VD17
31	R4	Red data	43	VD16
32	R3	Red data	29	VD15
33	R2	Red data	30	VD14
34	R1	Red data	64	VD13
35	R0(LSB)	Red data	61	VD12
36	GND	Ground	Note 1	VSS
37	DCLK	Clock for input data	11	PCLK
38	GND	Ground	Note 1	VSS
39	LR	Source left or right sequence control	-	-
40	UD	Gate up or down scan control	-	-
41	VGH	Positive power of TFT	-	-
42	VGL	Negative power of TFT	-	-
43	AVDD	Analog power supply	-	-
44	RESET	Global reset pin	97	RESET#
45	NC	No Connect	-	-
46	VCOM	Common voltage input	-	-
47	DITHB	Dithering setting: H: 6bit resolution, L: 8bit resolution		
48	GND	Ground	Note 1	VSS
49	NC	No Connect	-	-
50	NC	No Connect	-	-

Note

1. Allocation of VSS pins: 5, 7, 18, 21, 32, 34, 39, 41, 53, 56, 68, 70, 78, 90, 103, 105, 112, 116, 119, 135, 144, 129
2. Allocation of VDD pins: 4, 17, 20, 33, 38, 52, 55, 69, 77, 102, 113, 120, 128, 143

5.3 S1D13742 Register Settings for the TM070RBH10 TFT Display

In addition to the pin connections, the S1D13742 internal registers must be configured appropriately for the TM070RBH10 LCD panel. The following tables provide example settings for display controller. However, these values are for reference only and may differ according to each specific implementation. For details on configuring the S1D13742 register values, see the S1D13742 Hardware Functional Specification, document number X63A-A-001-xx.

Table 5-3: Register Settings for the TM070RBH10 TFT Display

Register Index and Name	Parameter Value (See Note)	Register Value Description
REG[56h] Power Save Register	0x02h	Sleep mode is enabled
REG[04h] PLL M-Divide Register	0x18h	Depending on CLKI that is 25MHz (Note)
REG[06h] PLL Setting Register 0	0xF8h	Value Fixed
REG[08h] PLL Setting Register 1	0x80h	Value Fixed
REG[0Ah] PLL Setting Register 2	0x28h	Value Fixed
REG[0Ch] PLL Setting Register 3	0x00h	Value Fixed
REG[0Eh] PLL Setting Register 4	0x3Ch	Register are used to configure PLL O/P (Note)
REG[12h] CLK Source Select Register	0x11h	Clock source for PCLK is SYSCLK
REG[14h] Panel Type Register	0x00h	Interface is 16 bit
REG[16h] Horizontal display width register	0x64h	Note
REG[18h] Horizontal non display period register	0x5Ah	Note
REG[1Ah] Vertical display height register0	0xE0h	Note
REG[1Ch] Vertical display height register1	0x01h	Note
REG[1Eh] Vertical non display period register	0x06h	Note
REG[20h] HS Pulse Width register	0x14h	Note
REG[22h] HS Pulse Start position register 0	0x2Dh	Note
REG[24h] VS Pulse width register	0x02h	Note
REG[26h] VS Pulse Start position register 0	0x01h	Note
REG[28h] PCLK polarity register	0x80h	PCLK O/P data at falling edge
REG[2Ah] Input mode register	0x01h	Default
REG[56h] Power Save Register	0x00h	Sleep mode is disabled
REG[38h] Window X start position register 0	0x00h	Horizontal start Position (LSB)
REG[3Ah] Window X start position register 1	0x00h	Horizontal start Position (MSB)
REG[3Ch] Window Y start position register 0	0x00h	Vertical start position (LSB)
REG[3Eh] Window Y start position register 1	0x00h	Vertical start Position (MSB)
REG[40h] Window X End position register 0	0x1Fh	Horizontal end Position (LSB)
REG[42h] Window X End position register 1	0x03h	Horizontal end Position (MSB)
REG[44h] Window Y End position register 0	0xDFh	Vertical end position (LSB)
REG[46h] Window Y End position register 1	0x01h	Vertical end position (MSB)

Note

Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13742 register values, see the S1D13742 Hardware Functional Specification, document number X63A-A-001-xx.

Chapter 6 Change Record

X63A-G-008-01 Revision 1.2 - Issued: March 28, 2018

- updated Sales and Technical Support Section
- updated some formatting

X63A-G-008-01 Revision 1.1 - Issued: December 4, 2012

- globally change “TM035KBH07” to “TM035KBH02”
- chapter 1 Introduction - add “For inquiry, please visit SM Electronic Technologies Pvt. Ltd...”

X63A-G-008-01 Revision 1.0 - Issued: November 5, 2012

- Initial release of this document

Chapter 7 Sales and Technical Support

For more information on Epson Display Controllers, visit the Epson Global website.

https://global.epson.com/products_and_drivers/semicon/products/display_controllers/

For Sales and Technical Support, contact the Epson representative for your region.

https://global.epson.com/products_and_drivers/semicon/information/support.html