EPSON
EXCEED YOUR VISION

Connecting EPSON Display Controllers to Ortustech LCD Panels

Document Number: X00A-G-008-01

Issue Date: 2013/06/24

SEIKO EPSON CORPORATION

Rev.1.4

Evaluation board/kit and Development tool important notice

1. This evaluation board/kit or development tool is designed for use for engineering evaluation, demonstration, or development purposes only. Do not use it for other purposes. It is not intended to meet the requirements of design for finished products.
2. This evaluation board/kit or development tool is intended for use by an electronics engineer and is not a consumer product. The user should use it properly and in a safe manner. Seiko Epson dose not assume any responsibility or liability of any kind of damage and/or fire coursed by the use of it. The user should cease to use it when any abnormal issue occurs even during proper and safe use.
3. The part used for this evaluation board/kit or development tool may be changed without any notice.

NOTICE

Table of Contents

1 Introduction

This document provides connection information enabling EPSON Display Controllers to control a variety of Ortus Technology Co., Ltd LCD panels. This document includes connector details, pin mappings, and example register settings.

For detailed technical information on EPSON Display Controllers or Ortustech LCD panels, please refer to the specification or technical manual for each product.

This document is updated as appropriate. Please check for the latest revision of this document before beginning any development.

The latest revision can be downloaded at
http://www.epson.jp/device/semicon_e/product/index.htm#lcd_controllers

2 Display Controller Compatibility

This document discusses the following Ortustech TFT panels.

- COM35H3827 (TFT 3.5inch, QVGA, portrait)
- COM41T4148 (TFT 4.1inch, QVGA)
- COM57T5139 (TFT 5.7inch, QVGA, Full monitor type)
- COM57T5M26 (TFT 5.7inch, QVGA BL monitor type)
- COM57T5M71 (TFT Monochrome 5.7inch, QVGA BL monitor type)
- COM57T5140 (TFT 5.7inch, QVGA BL monitor type)
- COM57T5M21 (TFT 5.7inch, QVGA BL monitor type)
- COM37H3M77 (TFT 3.7inch, VGA, portrait)
- COM43H4M71 (TFT 4.3inch, WQVGA, 480x272)
- COM57T5M54 (TFT 5.7inch, VGA BL monitor type)
- COM65T6111 (TFT 6.5inch, VGA Full monitor type)
- COM65T6112 (TFT 6.5inch, VGA, BL monitor type)
- COM43H4M85 (TFT 4.3inch, WVGA, portrait)

Each Ortustech TFT panel is compatible with one or more of the following EPSON display controllers.

- S1D13513 (QFP 208-pin or PBGA 256-pin)
- S1D13517 (QFP 128-pin)
- S1D13706 (TQFP 100-pin)
- S1D13A05 (PFBGA 121-pin or QFP 128-pin)
- S1D13719 (PFBGA 180-pin or QFP 208-pin)
- S1D13742 (QFP 144-pin)
- S1D13743 (QFP 144-pin)
- S1D13748 (PFBGA 121-pin or QFP 144-pin)
- S1D13781 (QFP 100-pin)

The following table summarizes which EPSON display controllers are compatible with each Ortustech TFT panels.

Table 2-1 Compatible EPSON display controllers with each Ortustech TFT panels

Ortustech Panel	S1D13513	S1D13517	S1D13781	S1D13706	S1D13A05	S1D13719	S1D13742	S1D13743	S1D13748
COM35H3827	√	—	√	√	√	√	√	√	√
COM41T4148	√	—	√	√	√	√	√	√	√
COM57T5139	√	—	√	√	√	√	√	√	√
COM57T5M26	√	—	√	√	√	√	√	√	√
COM57T5M71	√	—	√	√	√	√	√	√	√
COM57T5140	√	—	√	√	√	√	√	√	√
COM57T5M21	√	—	√	√	√	√	√	√	√
COM37H3M77	√	√	√	√	√	√	√	√	√
COM43H4M71	√	√	√	√	√	√	√	√	√
COM57T5M54	√	√	√	√	√	√	√	—	√
COM65T6111	√	√	√	√	√	√	√	—	√
COM65T6112	√	√	√	√	√	√	√	—	√
COM43H4M85	√	√	√	√	√	√	√	—	√

The following table shows other compatible panels with above listed standard panels. These panels can also be connected to EPSON display controllers.

Table 2-2 Product list of Ortustech TFT panels

Ortustech Panel	Same Interface Model
COM35H3827	COM24H2N62, COM27H2M90, COM27H2N25, COM35H3833, COM35H3M09, COM35H3M10
COM41T4148	COM22T2M59, COM22H2N81, COM22H2M74,COM35T3N54, COM35T3818, COM35T3829,COM35T3830, COM35T3831, COM35T3832,COM35H3835, COM35T3149, COM41T4150,COM41H4156, COM41T4M17, COM50T5119,COM50T5117, COM50T5123, COM50T5124,COM50H5125
COM57T5139	COM57T5M04, COM57H5M06
COM57T5M26	COM57H5M55
COM57T5M71	—
COM57T5140	—
COM57T5M21	—
COM37H3M77	COM35H3M73, COM37H3M99
COM43H4M71	COM43H4M09, COM43T4M10, COM43T4M81
COM57T5M54	COM57H5M64, COM57T5M61, COM57H5M10
COM65T6111	COM65H6114, COM57H5137, COM57H5M24
COM65T6112	COM57T5M20, COM57T5M25, COM65H6115
COM43H4M85	—

Link for Ortust Technology Corporation LCD products web site
http://www.ortustech.co.jp/english/products/prd_1.html

3 Connecting to the Ortustech COM35H3827

The Ortustech COM35H3827 TFT panel is compatible with the S1D13513 and S1D13748 display controllers. The following sections will provide connector details, pin mappings, and example register settings for these combinations.

3.1 COM35H3827 Pin Mapping

The COM35H3827 TFT panel uses a 39-pin connector with the following pin mapping.

COM35H3827 Pin Mapping

Table 3-1 COM35H3827 Pin Mapping

Connector Pin#	Pin Name	Pin Description
1	VSS	GND
2	VSS	GND
3	VDD	Power supply for logic 2.7V ≤ VDD ≤ 3.6V
4	VDD	Power supply for logic 2.7V ≤ VDD ≤ 3.6V
5	VSS	GND
6	RESETB	RESET(Lo-active)
7	HSYNC	Horizontal synchronous signal (Negative)
8	VSYNC	Vertical synchronous signal (Negative)
9	CLK	Dot clock (Capture at the falling edge)
10	VSS	GND
11	D00	BLUE data signal (LSB)
12	D01	BLUE data signal
13	D02	BLUE data signal
14	D03	BLUE data signal
15	D04	BLUE data signal
16	D05	BLUE data signal (MSB)
17	D10	GREEN data signal (LSB)
18	D11	GREEN data signal
19	D12	GREEN data signal
20	D13	GREEN data signal
21	D14	GREEN data signal
22	D15	GREEN data signal (MSB)
23	D20	RED data signal (LSB)
24	D21	RED data signal
25	D22	RED data signal
26	D23	RED data signal
27	D24	RED data signal
28	D25	RED data signal (MSB)
29	VSS	GND
30	DE	Input data enable (Hi-active)
31	STBYB	Display control signal; Lo: Standby, Hi: Normal
32	TEST1	Connect to GND
33	NC	OPEN
34	NC	OPEN
35	NC	OPEN
36	NC	OPEN
37	TEST2	Connect to GND
38	BLH	Power supply for back light LED (anode)
39	BLL	Power supply for back light LED (cathode)

Note
The recommended connector is a FH23-39S-0.3SHW(0.5) from Hirose Electric Co., Ltd. The connector is a 0.3mm pitch 39-pin FPC connector (12.0mm x 0.2mm gold plate).

3.2 Connection Examples

The information in this section provides connection examples for the S1D13513 and S1D13748 display controllers. For the S1D13513 and S1D13748, the display controller is available in two packages. The connection information differs for each package and is listed separately.

In addition to the pin connections for the selected display controller, the COM35H3827 requires the following power supplies.

VDD +3.0V (2.7V ≤ VDD ≤ 3.6V)

VL +19.2V (VL ≤ 21V)

For VDD, select a voltage within the supportable range of the Display Controller.

For further details on the COM35H3827, such as power consumption and absolute maximum ratings, please contact your Ortustech representative.

3.2.1 Connecting the COM35H3827 to the S1D13513

The following diagram shows an example implementation of the COM35H3827 panel connected to the S1D13513.

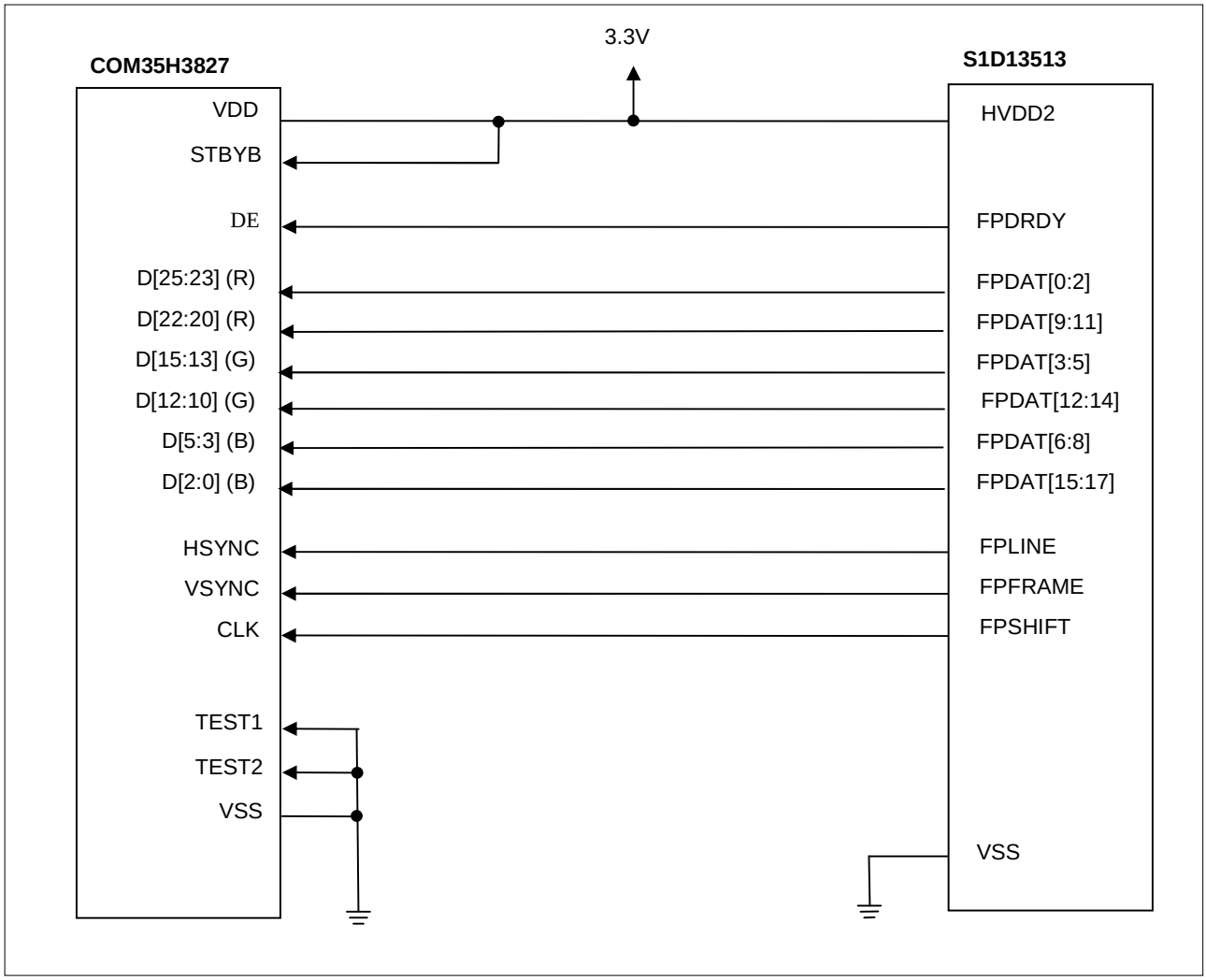

Figure 3-1 Connecting the COM35H3827 to the S1D13513

The following table provides a detailed pin listing for the required connections between the COM35H3827 and the S1D13513. Pin mappings are shown for both S1D13513 package types.

Table 3-2 Connecting the COM35H3827 to the S1D13513

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
1	VSS	GND	Note	Note	VSS
2	VSS	GND	Note	Note	VSS
3	VDD	Power supply for logic +3.3V	57,65,75	L5,L8,T6	HVDD2
4	VDD	Power supply for logic +3.3V	57,65,75	L5,L8,T6	HVDD2
5	VSS	GND	Note	Note	VSS
6	RESETB	RESET(Lo-active)	—	—	—
7	HSYNC	Horizontal synchronous signal (Negative)	79	R8	FPLINE
8	VSYNC	Vertical synchronous signal (Negative)	78	T8	FPFRAME
9	CLK	Dot clock (Capture at the falling edge)	77	P8	FPSHIFT
10	VSS	GND	Note	Note	VSS
11	D00	BLUE data signal (LSB)	53	N4	FPDAT17
12	D01	BLUE data signal	54	P4	FPDAT16
13	D02	BLUE data signal	55	T2	FPDAT15
14	D03	BLUE data signal	64	R6	FPDAT8
15	D04	BLUE data signal	67	K6	FPDAT7
16	D05	BLUE data signal (MSB)	68	M6	FPDAT6
17	D10	GREEN data signal (LSB)	56	R4	FPDAT14
18	D11	GREEN data signal	59	T4	FPDAT13
19	D12	GREEN data signal	60	T5	FPDAT12
20	D13	GREEN data signal	69	L7	FPDAT5
21	D14	GREEN data signal	70	P7	FPDAT4
22	D15	GREEN data signal (MSB)	71	R7	FPDAT3
23	D20	RED data signal (LSB)	61	N5	FPDAT11
24	D21	RED data signal	62	M5	FPDAT10
25	D22	RED data signal	63	P6	FPDAT9
26	D23	RED data signal	72	T7	FPDAT2
27	D24	RED data signal	73	N7	FPDAT1
28	D25	RED data signal (MSB)	74	M7	FPDAT0
29	VSS	GND	Note	Note	VSS
30	DE	Input data enable (Hi-active)	80	M8	FPDRDY
31	STBYB	Display control signal; Lo: Standby, Hi: Normal	57,65,75	L5,L8,T6	HVDD2
32	TEST1	Connect to GND	Note	Note	VSS
33	NC	OPEN	—	—	—
34	NC	OPEN	—	—	—
35	NC	OPEN	—	—	—
36	NC	OPEN	—	—	—
37	TEST2	Connect to GND	Note	Note	VSS

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
38	BLH	Power supply for back light LED(anode)	—	—	—
39	BLL	Power supply for back light LED(cathode)	—	—	—

S1D13513 HVDD2 and COM35H3827 VDD must be configured between +3.0V to +3.6V.

Note
Allocation of VSS pin for each packages are as follows.
QFP: 10, 20, 38, 58, 66, 76, 92, 99, 106, 120, 133, 139, 151, 163, 169, 175, 184, 197
BGA: A1, A16, D4, D8, D13, G7-G10, G13, H7-H10, J1, J7-J10, K2, K7-K10, K13, N3, N6, N9, N13, T1, T16

3.2.2 Connecting the COM35H3827 to the S1D13748

The following diagram shows an example implementation of the COM35H3827 panel connected to the S1D13748.

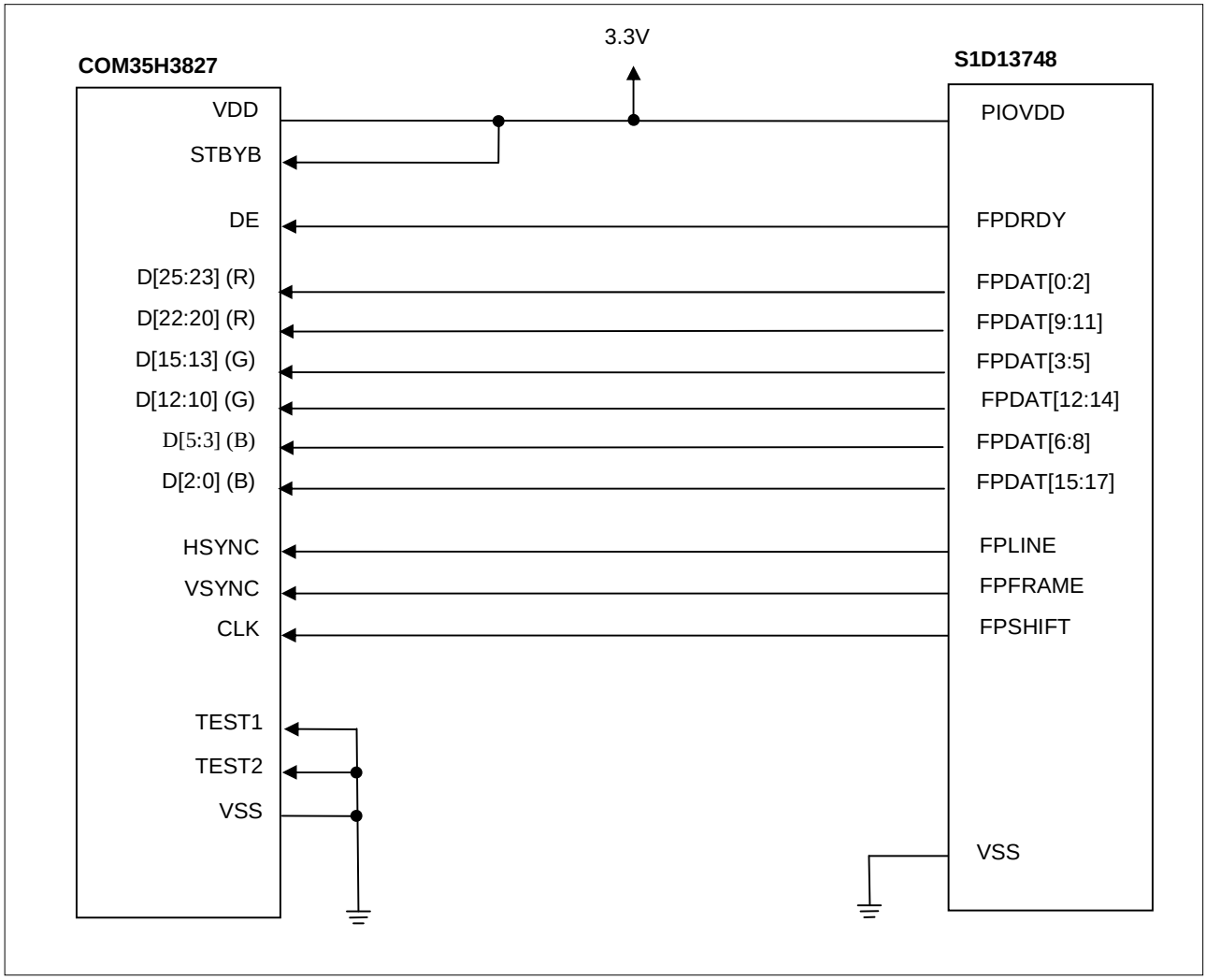

Figure 3-2 Connecting the COM35H3827 to the S1D13748

The following table provides a detailed pin listing for the required connections between the COM35H3827 and the S1D13748. Pin mappings are shown for both S1D13748 package types.

Table 3-3 Connecting the COM35H3827 to the S1D13748

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13513 Pin Name
1	VSS	GND	Note	Note	VSS
2	VSS	GND	Note	Note	VSS
3	VDD	Power supply for logic +3.3V	19,26,35, 40,46,55, 67,73,83, 87	E8, F4, H7, J4	PIOVDD
4	VDD	Power supply for logic +3.3V	19,26,35, 40,46,55, 67,73,83, 87	E8,F4. H7,J4	PIOVDD
5	VSS	GND	Note	Note	VSS
6	RESETB	RESET(Lo-active)	—	—	—
7	HSYNC	Horizontal synchronous signal (Negative)	77	H10	FPLINE
8	VSYNC	Vertical synchronous signal (Negative)	76	J10	FPFRAME
9	CLK	Dot clock (Capture at the falling edge)	75	J11	FPSHIFT
10	VSS	GND	Note	Note	VSS
11	D00	BLUE data signal (LSB)	72	J9	FPDAT17
12	D01	BLUE data signal	71	K10	FPDAT16
13	D02	BLUE data signal	70	L10	FPDAT15
14	D03	BLUE data signal	60	K7	FPDAT8
15	D04	BLUE data signal	59	J7	FPDAT7
16	D05	BLUE data signal (MSB)	58	L7	FPDAT6
17	D10	GREEN data signal (LSB)	69	H8	FPDAT14
18	D11	GREEN data signal	68	K9	FPDAT13
19	D12	GREEN data signal	64	L9	FPDAT12
20	D13	GREEN data signal	54	L6	FPDAT5
21	D14	GREEN data signal	53	J6	FPDAT4
22	D15	GREEN data signal (MSB)	52	H6	FPDAT3
23	D20	RED data signal (LSB)	63	L8	FPDAT11
24	D21	RED data signal	62	J8	FPDAT10
25	D22	RED data signal	61	K8	FPDAT9
26	D23	RED data signal	51	K5	FPDAT2
27	D24	RED data signal	50	L5	FPDAT1
28	D25	RED data signal (MSB)	49	J5	FPDAT0
29	VSS	GND	Note	Note	VSS
30	DE	Input data enable (Hi-active)	78	G7	FPDRDY

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13513 Pin Name
31	STBYB	Display control signal; Lo: Standby, Hi: Normal	19,26,35, 40,46,55, 67,73,83, 87	E8,F4,H7, J4	PIOVDD
32	TEST1	Connect to GND	Note	Note	VSS
33	NC	OPEN	—	—	—
34	NC	OPEN	—	—	—
35	NC	OPEN	—	—	—
36	NC	OPEN	—	—	—
37	TEST2	Connect to GND	Note	Note	VSS
38	BLH	Power supply for back light LED(anode)	—	—	—
39	BLL	Power supply for back light LED(cathode)	—	—	—

S1D13748 PIOVDD and COM41T4148 VDD must be configured between +3.0V to +3.6V.

Note
Allocation of VSS pin for each packages are as follows.
QFP: 6, 13, 20, 31, 36, 39, 47, 56, 66, 74, 82, 91, 97, 102, 108, 115, 129, 138, 144
PFBGA: B1, C4, C8, D10, E6, F2, F8, G4, K6, K11

3.3 Example Register Settings

In addition to the pin connections, the S1D13513/S1D13748 internal registers must be configured appropriately for the COM35H3827 LCD panel. The following tables provide example settings for each display controller. However, these values are for reference only and may differ according to each specific implementation.

Also included in the table is an example clock configuration designed to achieve a 50Hz or greater LCD refresh.

Table 3-4 Example Register Settings for the S1D13513

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0800h] LCD Panel Type Select Register	0280h	—
REG[0802h] LCD Horizontal Total Register	011Eh	287
REG[0804h] LCD Horizontal Display Period Register	0077h	240
REG[0806h] LCD Horizontal Display Period Start Position Register	0001h	2
REG[0808h] LCD Horizontal Pulse Width	0009h	10
REG[080Ah] LCD Horizontal Pulse Start Position	0000h	0
REG[080Ch] LCD Vertical Total Register	0144h	325
REG[080Eh] LCD Vertical Display Period Resister	013Fh	320
REG[0810h] Vertical Display Period Start Position Register	0003h	2
REG[0812h] LCD Vertical Pulse Width	0000h	1
REG[0814h] LCD Vertical Pulse Start Position	0000h	0
PLL2 output frequency in MHz	—	100
REG[0446h] LCD Clock Control Register	0011h	18

Register Index and Name	Register Setting	Parameter Value (see Note)
FPSHIFT in MHz	—	5.56
LCD Refresh in Hz	—	59.6

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13513 register values, see the *S1D13513 Hardware Functional Specification*, document number X78B-A-001-xx.

Table 3-5 Example Register Settings for the S1D13748

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0040h] LCD1 Horizontal Total Register	35	287
REG[0042h] LCD1 Horizontal Display Period Register	119	240
REG[0044h] LCD1 Horizontal Display Period Start Position Register	0	9
REG[0046h] LCD1 Horizontal Pulse Register	0	1
REG[0048h] LCD1 Horizontal Pulse Start Position Register	0	1
REG[004Ah] LCD1 Vertical Total Register	324	325
REG[004Ch] LCD1 Vertical Display Period Resister	319	320
REG[004Eh] LCD1 Vertical Display Period Start Position Register	2	2
REG[0050h] LCD1 Vertical Pulse Register	0	1
REG[0052h] LCD1 Vertical Pulse Start Position Register	0	1
REG[0246h] Main1 Window Image Horizontal Size Register	239	240
REG[0248h] Main1 Window Image Vertical Size Register	319	320
PLL output frequency in MHz	—	50
REG[0030h] LCD Interface Clock Setting Register	0507h	9
FPSHIFT in MHz	—	5.56
LCD Refresh in Hz	—	59.6

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13748 register values, see the *S1D13748 Hardware Functional Specification*, document number X80A-A-001-xx.

4 Connecting to the Ortustech COM41T4148

The Ortustech COM41T4148 TFT panel is compatible with the S1D13513, S1D13719, and S1D13748 display controllers. The following sections will provide connector details, pin mappings, and example register settings for these combinations.

4.1 COM41T4148 Pin Mapping

The COM41T4148 TFT panel uses a 67-pin connector with the following pin mapping.

Table 4-1 COM41T4148 Pin Mapping

Connector Pin#	Pin Name	Pin Description
1	VCOM	Common driver signal
2	D27	BLUE data signal (MSB)
3	D26	BLUE data signal
4	D25	BLUE data signal
5	D24	BLUE data signal
6	D23	BLUE data signal
7	D22	24bit mode: BLUE data signal 18bit mode: BLUE data signal (LSB)
8	D21	24bit mode: BLUE data signal 18bit mode: Connect to VSS
9	D20	24bit mode: BLUE data signal (LSB) 18bit mode: Connect to VSS
10	D17	GREEN data signal (MSB)
11	D16	GREEN data signal
12	D15	GREEN data signal
13	D14	GREEN data signal
14	D13	GREEN data signal
15	D12	24bit mode: GREEN data signal 18bit mode: GREEN data signal (LSB)
16	D11	24bit mode: GREEN data signal 18bit mode: Connect to VSS
17	D10	24bit mode: GREEN data signal (LSB) 18bit mode: Connect to VSS
18	D07	RED data signal (MSB)
19	D06	RED data signal
20	D05	RED data signal
21	D04	RED data signal
22	D03	RED data signal
23	D02	24bit mode: RED data signal 18bit mode: RED data signal (LSB)
24	D01	24bit mode: RED data signal 18bit mode: Connect to VSS
25	D00	24bit mode: RED data signal (LSB) 18bit mode: Connect to VSS

Connector Pin#	Pin Name	Pin Description
26	BLON	24bit mode: External back light control logic output signal 18bit mode: Open
27	CS / STBY	24bit mode: Serial chip select (Lo-active) 18bit mode: Standby control signal input (Lo: Normal, Hi: Standby)
28	DI / DE	24bit mode: Serial data input 18bit mode: Input data enable (Hi-active)
29	SCK / REV	24bit mode: Serial clock 18bit mode: Vertical and Horizontal reverse control signal input (Lo: Normal, Hi: Reverse)
30	VSYNC	24bit mode: Vertical synchronous signal (Negative) 18bit mode: Vertical synchronous signal (Negative)
31	HSYNC	24bit mode: Horizontal synchronous signal (Negative) 18bit mode: Horizontal synchronous signal (Negative)
32	CLK	24bit mode: Dot clock (Capture at the falling edge) 18bit mode: Dot clock (Capture at the falling edge)
33	VSS	GND
34	MODE	Input mode select; Lo: 24bit, Hi: 18bit
35	POCB	Power on clear input (Lo-active)
36	NC	OPEN
37	RVDD	Internal power
38	COMDC	Common driver DC output
39	NC	OPEN
40	VSREF	Internal DAC reference power
41	C1P	For charge pump capacitor connection
42	C1M	For charge pump capacitor connection
43	C2M	For charge pump capacitor connection
44	C2P	For charge pump capacitor connection
45	VDD	Power +3.0V ($2.7V \leq VDD \leq 3.6V$)
46	COMOUT	Rectangular wave output for common driver
47	VDD2	Internal power
48	VSS	GND
49	VSS	GND
50	VSS	GND
51	C3M	For charge pump capacitor connection
52	C3P	For charge pump capacitor connection
53	C4M	For charge pump capacitor connection
54	C4P	For charge pump capacitor connection
55	VVCOM	COMOUT power output
56	NC	OPEN
57	NC	OPEN
58	VGH	Gate driver power (+)
59	C5P	For charge pump capacitor connection
60	C5M	For charge pump capacitor connection
61	VGL	Gate driver power (-)

Connector Pin#	Pin Name	Pin Description
62	BLL2	LED drive power2 (cathode)
63	BLH2	LED drive power2 (anode)
64	NC	OPEN
65	NC	OPEN
66	BLH1	LED drive power1 (anode)
67	BLL1	LED drive power1 (cathode)

Note
The recommended connectors are
FH26G-67S-0.3SHBW(0.5) from Hirose Electric Co., Ltd.
or
04-6281-267-2X2-846+ from Kyocera elco.
The connector is a 0.3mm pitch 67-pin FPC connector (20.8mm x 0.2mm gold plate).

4.2 Connection Examples

The information in this section provides connection examples for the S1D13513, S1D13719, and S1D13748 display controllers. Each display controller is available in two packages. The connection information differs for each package and is listed separately.

In addition to the pin connections for the selected display controller, the COM41T4148 requires the following power supply.

VDD +3.0V (2.7V ≤ VDD ≤ 3.6V)

VL +15.5V (VL ≤ 16.9V)

For VDD, select a voltage within the supportable range of the Display Controller.

For further details on the COM41T4148, such as power consumption, absolute maximum ratings, and charge pump capacitor connections (see pins 41-44, 51-54, 59-60), please contact your Ortustech representative.

4.2.1 Connecting the COM41T4148 to the S1D13513

The following diagram shows an example implementation of the COM41T4148 panel connected to the S1D13513. This example is for the setting of 18-bit panel mode (MODE="VDD") on COM41T4148.

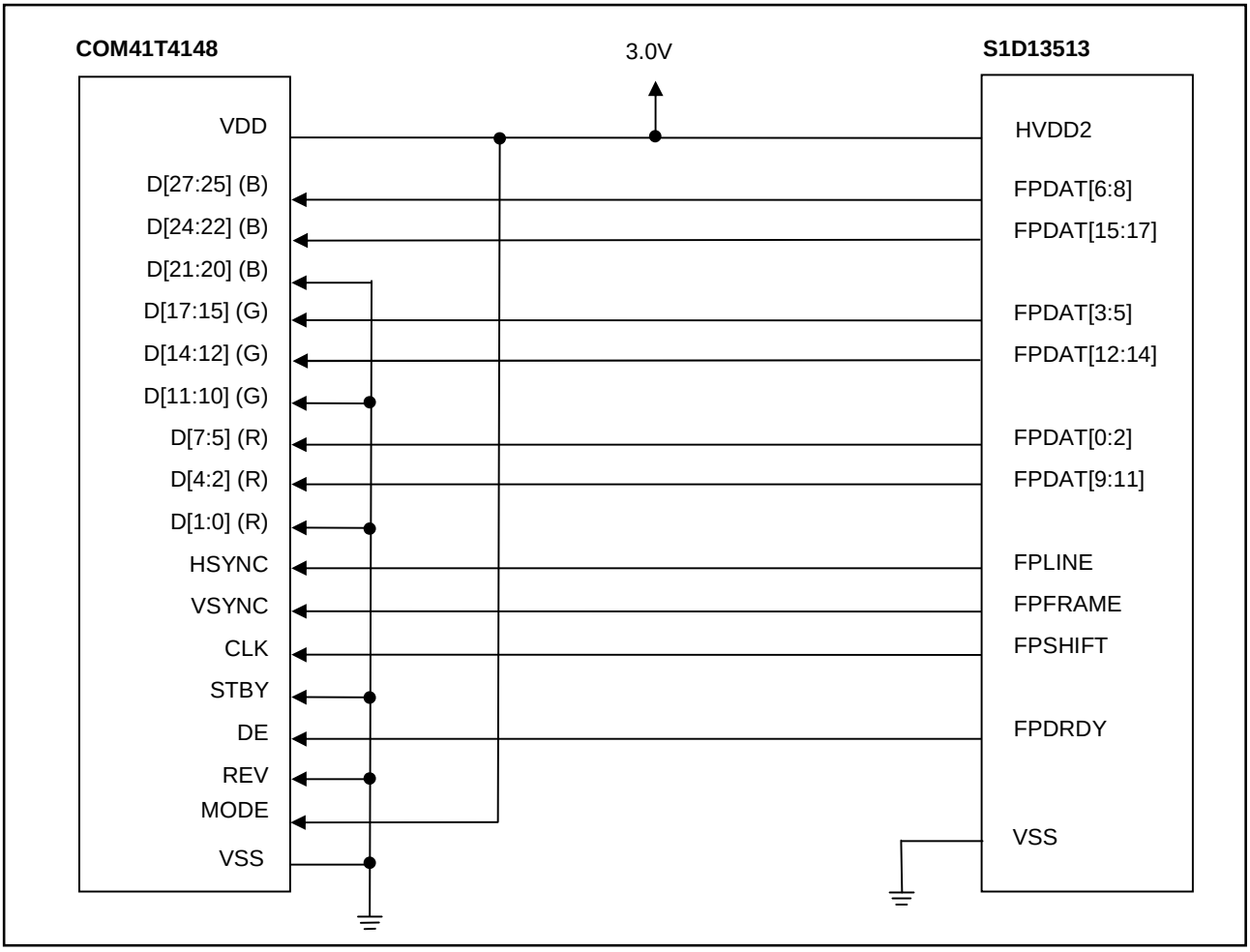

Figure 4-1 Connecting the COM41T4148 to the S1D13513 (18-bit Panel Mode, MODE = "VDD")

The following diagram shows an example implementation of the COM41T4148 panel connected to the S1D13513. This example is for the setting of 24-bit panel mode (MODE="VSS") on COM41T4148.

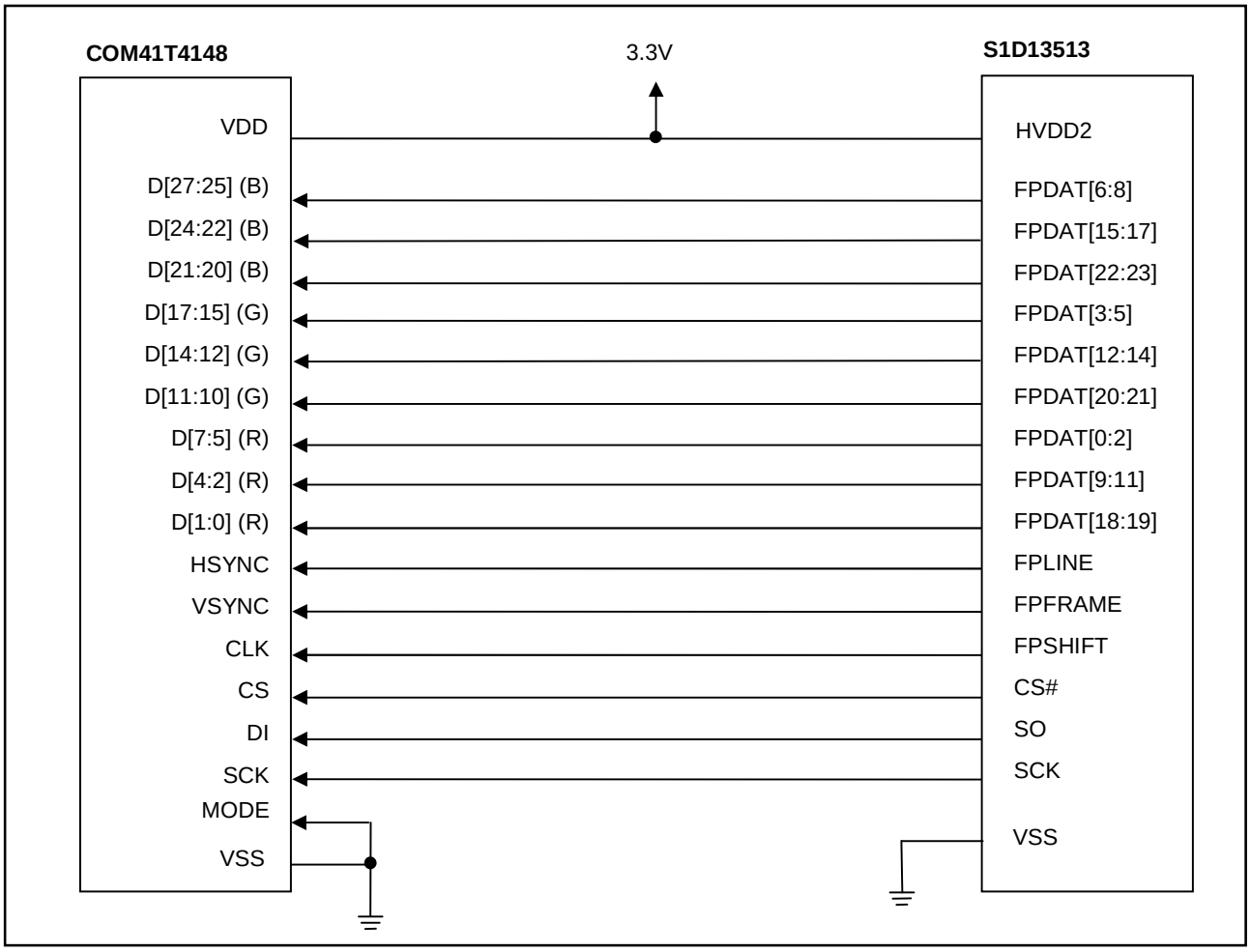

Figure 4-2 Connecting the COM41T4148 to the S1D13513 (24-bit Panel Mode, MODE = "VSS")

The following table provides a detailed pin listing for the required connections between the COM41T4148 and the S1D13513. This table is for the setting of 18-bit panel mode (MODE="VDD") on COM41T4148. Pin mappings are shown for both S1D13513 package types.

Table 4-2 Connecting the COM41T4148 to the S1D13513 (18-bit Panel Mode, MODE = "VDD")

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
1	VCOM	Common driver signal	—	—	—
2	D27	BLUE data signal (MSB)	68	M6	FPDAT6
3	D26	BLUE data signal	67	K6	FPDAT7
4	D25	BLUE data signal	64	R6	FPDAT8
5	D24	BLUE data signal	55	T2	FPDAT15
6	D23	BLUE data signal	54	P4	FPDAT16

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
7	D22	BLUE data signal (LSB)	53	N4	FPDAT17
8	D21	Connect to VSS	Note	Note	VSS
9	D20	Connect to VSS	Note	Note	VSS
10	D17	GREEN data signal (MSB)	71	R7	FPDAT3
11	D16	GREEN data signal	70	P7	FPDAT4
12	D15	GREEN data signal	69	L7	FPDAT5
13	D14	GREEN data signal	60	T5	FPDAT12
14	D13	GREEN data signal	59	T4	FPDAT13
15	D12	GREEN data signal (LSB)	56	R4	FPDAT14
16	D11	Connect to VSS	Note	Note	VSS
17	D10	Connect to VSS	Note	Note	VSS
18	D07	RED data signal (MSB)	74	M7	FPDAT0
19	D06	RED data signal	73	N7	FPDAT1
20	D05	RED data signal	72	T7	FPDAT2
21	D04	RED data signal	63	P6	FPDAT9
22	D03	RED data signal	62	M5	FPDAT10
23	D02	RED data signal (LSB)	61	N5	FPDAT11
24	D01	Connect to VSS	Note	Note	VSS
25	D00	Connect to VSS	Note	Note	VSS
26	BLON	Open	—	—	—
27	STBY	Standby control signal input (Lo: Normal, Hi: Standby)	Note	Note	VSS
28	DE	Input data enable (Hi-active)	80	M8	FPDRDY
29	REV	Vertical and Horizontal reverse control signal input (Lo: Normal, Hi: Reverse)	Note	Note	VSS
30	VSYNC	Vertical synchronous signal (Negative)	78	T8	FPFRAME
31	HSYNC	Horizontal synchronous signal (Negative)	79	R8	FPLINE
32	CLK	Dot clock (Capture at the falling edge)	77	P8	FPSHIFT
33	VSS	GND	Note	Note	VSS
34	MODE	Input mode select, Lo: 24bit, Hi: 18bit	57, 65, 75	L5, L8, T6	HVDD2
35	POCB	Power on clear input (Lo-active)	—	—	—
36	NC	OPEN	—	—	—
37	RVDD	Internal power	—	—	—
38	COMDC	Common driver DC output	—	—	—
39	NC	OPEN	—	—	—
40	VSREF	Internal DAC reference power	—	—	—
41	C1P	For charge pump capacitor connection	—	—	—
42	C1M	For charge pump capacitor connection	—	—	—
43	C2M	For charge pump capacitor connection	—	—	—
44	C2P	For charge pump capacitor connection	—	—	—
45	VDD	Power +3.3V	57, 65, 75	L5, L8, T6	HVDD2

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
46	COMOUT	Rectangular wave output for common driver	—	—	—
47	VDD2	Internal power	—	—	—
48	VSS	GND	Note	Note	VSS
49	VSS	GND	Note	Note	VSS
50	VSS	GND	Note	Note	VSS
51	C3M	For charge pump capacitor connection	—	—	—
52	C3P	For charge pump capacitor connection	—	—	—
53	C4M	For charge pump capacitor connection	—	—	—
54	C4P	For charge pump capacitor connection	—	—	—
55	VVCOM	COMOUT power output	—	—	—
56	NC	OPEN	—	—	—
57	NC	OPEN	—	—	—
58	VGH	Gate driver power (+)	—	—	—
59	C5P	For charge pump capacitor connection	—	—	—
60	C5M	For charge pump capacitor connection	—	—	—
61	VGL	Gate driver power (-)	—	—	—
62	BLL2	LED drive power2 (cathode)	—	—	—
63	BLH2	LED drive power2 (anode)	—	—	—
64	NC	OPEN	—	—	—
65	NC	OPEN	—	—	—
66	BLH1	LED drive power1 (anode)	—	—	—
67	BLL1	LED drive power1 (cathode)	—	—	—

S1D13513 HVDD2 and COM41T4148 VDD must be configured between +3.0V to +3.6V.

Note
Allocation of VSS pin for each packages are as follows.
QFP: 10, 20, 38, 58, 66, 76, 92, 99, 106, 120, 133, 139, 151, 163, 169, 175, 184, 197
BGA: A1, A16, D4, D8, D13, G7-G10, G13, H7-H10, J1, J7-J10, K2, K7-K10, K13, N3, N6, N9, N13, T1, T16

The following table provides a detailed pin listing for the required connections between the COM41T4148 and the S1D13513. This table is for the setting of 24-bit panel mode (MODE="VSS") on COM41T4148. Pin mappings are shown for both S1D13513 package types.

Table 4-3 Connecting the COM41T4148 to the S1D13513 (24-bit Panel Mode, MODE = "VSS")

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
1	VCOM	Common driver signal	—	—	—
2	D27	BLUE data signal (MSB)	68	M6	FPDAT6
3	D26	BLUE data signal	67	K6	FPDAT7
4	D25	BLUE data signal	64	R6	FPDAT8
5	D24	BLUE data signal	55	T2	FPDAT15

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
6	D23	BLUE data signal	54	P4	FPDAT16
7	D22	BLUE data signal	53	N4	FPDAT17
8	D21	BLUE data signal	Note 2	R3	FPDAT22
9	D20	BLUE data signal (LSB)	Note 2	K4	FPDAT23
10	D17	GREEN data signal (MSB)	71	R7	FPDAT3
11	D16	GREEN data signal	70	P7	FPDAT4
12	D15	GREEN data signal	69	L7	FPDAT5
13	D14	GREEN data signal	60	T5	FPDAT12
14	D13	GREEN data signal	59	T4	FPDAT13
15	D12	GREEN data signal	56	R4	FPDAT14
16	D11	GREEN data signal	Note 2	P5	FPDAT20
17	D10	GREEN data signal (LSB)	Note 2	T3	FPDAT21
18	D07	RED data signal (MSB)	74	M7	FPDAT0
19	D06	RED data signal	73	N7	FPDAT1
20	D05	RED data signal	72	T7	FPDAT2
21	D04	RED data signal	63	P6	FPDAT9
22	D03	RED data signal	62	M5	FPDAT10
23	D02	RED data signal	61	N5	FPDAT11
24	D01	RED data signal	Note 2	R5	FPDAT18
25	D00	RED data signal (LSB)	Note 2	K5	FPDAT19
26	BLON	External back light control logic output signal	—	—	—
27	CS	Serial chip select (Lo-active)	85	L9	CS#
28	DI	Serial data input	82	T9	SO
29	SCK	Serial clock	84	P9	SCK
30	VSYNC	Vertical synchronous signal (Negative)	78	T8	FPFRAME
31	HSYNC	Horizontal synchronous signal (Negative)	79	R8	FPLINE
32	CLK	Dot clock (Capture at the falling edge)	77	P8	FPSHIFT
33	VSS	GND	Note 1	Note 1	VSS
34	MODE	Input mode select, Lo: 24bit, Hi: 18bit	57, 65, 75	L5, L8, T6	HVDD2
35	POCB	Power on clear input (Lo-active)	—	—	—
36	NC	OPEN	—	—	—
37	RVDD	Internal power	—	—	—
38	COMDC	Common driver DC output	—	—	—
39	NC	OPEN	—	—	—
40	VSREF	Internal DAC reference power	—	—	—
41	C1P	For charge pump capacitor connection	—	—	—
42	C1M	For charge pump capacitor connection	—	—	—
43	C2M	For charge pump capacitor connection	—	—	—
44	C2P	For charge pump capacitor connection	—	—	—
45	VDD	Power +3.3V	57, 65, 75	L5, L8, T6	HVDD2

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
46	COMOUT	Rectangular wave output for common driver	—	—	—
47	VDD2	Internal power	—	—	—
48	VSS	GND	Note 1	Note 1	VSS
49	VSS	GND	Note 1	Note 1	VSS
50	VSS	GND	Note 1	Note 1	VSS
51	C3M	For charge pump capacitor connection	—	—	—
52	C3P	For charge pump capacitor connection	—	—	—
53	C4M	For charge pump capacitor connection	—	—	—
54	C4P	For charge pump capacitor connection	—	—	—
55	VVCOM	COMOUT power output	—	—	—
56	NC	OPEN	—	—	—
57	NC	OPEN	—	—	—
58	VGH	Gate driver power (+)	—	—	—
59	C5P	For charge pump capacitor connection	—	—	—
60	C5M	For charge pump capacitor connection	—	—	—
61	VGL	Gate driver power (-)	—	—	—
62	BLL2	LED drive power2 (cathode)	—	—	—
63	BLH2	LED drive power2 (anode)	—	—	—
64	NC	OPEN	—	—	—
65	NC	OPEN	—	—	—
66	BLH1	LED drive power1 (anode)	—	—	—
67	BLL1	LED drive power1 (cathode)	—	—	—

S1D13513 HVDD2 and COM41T4148 VDD must be configured between +3.0V to +3.6V.

Note 1
Allocation of VSS pin for each packages are as follows.
QFP: 10,20,38,58,66,76,92,99,106,120,133,139,151,163,169,175,184,197
BGA: A1,A16,D4,D8,D13,G7-G10,G13,H7-H10,J1,J7-J10,K2,K7-K10,K13,N3,N6,N9,N13,T1,T16

Note 2
Connect to VSS pin for QFP package.

4.2.2 Connecting the COM41T4148 to the S1D13719

The following diagram shows an example implementation of the COM41T4148 panel connected to the S1D13719. This example is for the setting of 18-bit panel mode (MODE="VDD") on COM41T4148.

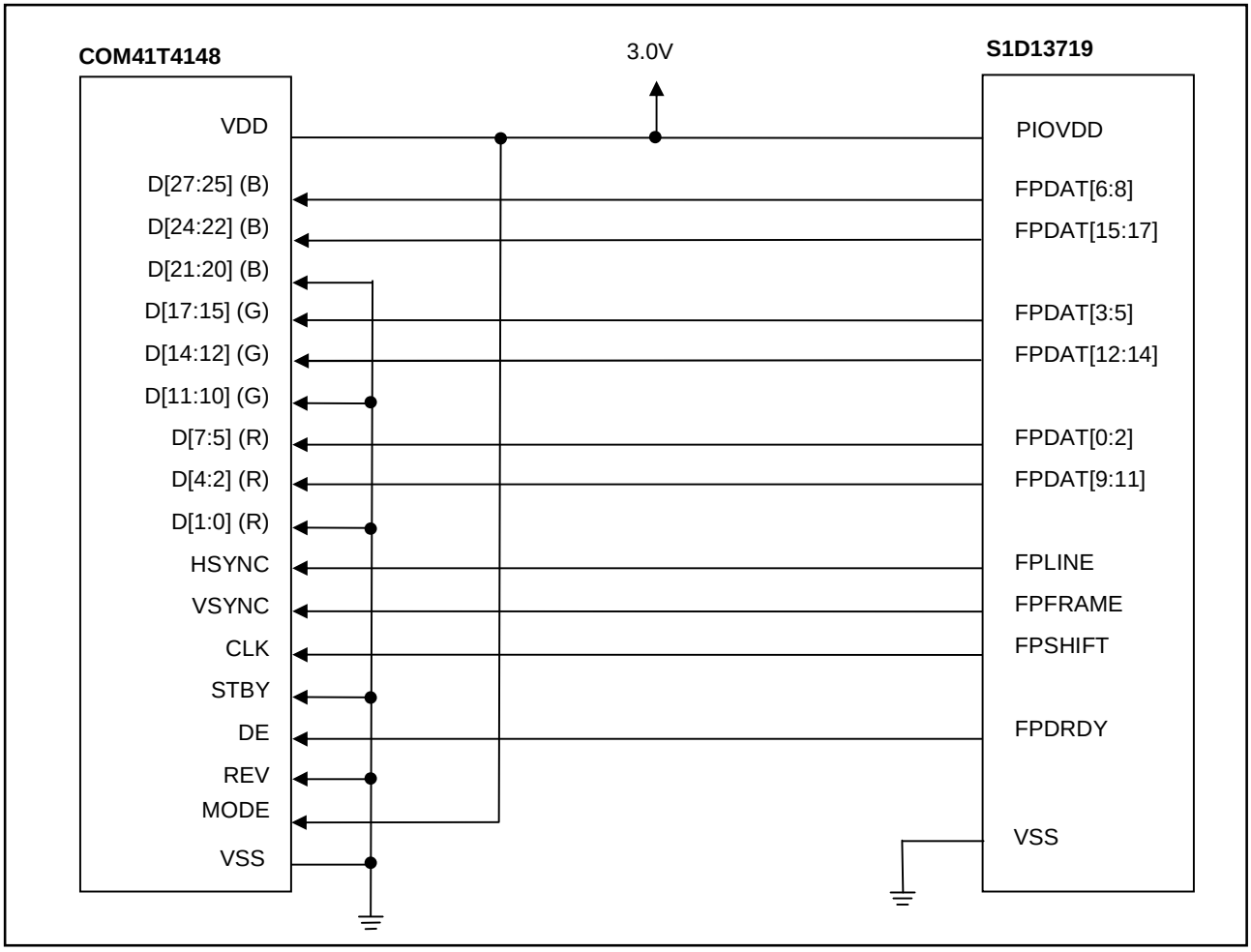

Figure 4-3 Connecting the COM41T4148 to the S1D13719 (18-bit Panel Mode, MODE = "VDD")

The following diagram shows an example implementation of the COM41T4148 panel connected to the S1D13719. This example is for the setting of 24-bit panel mode (MODE=”VSS”) on COM41T4148

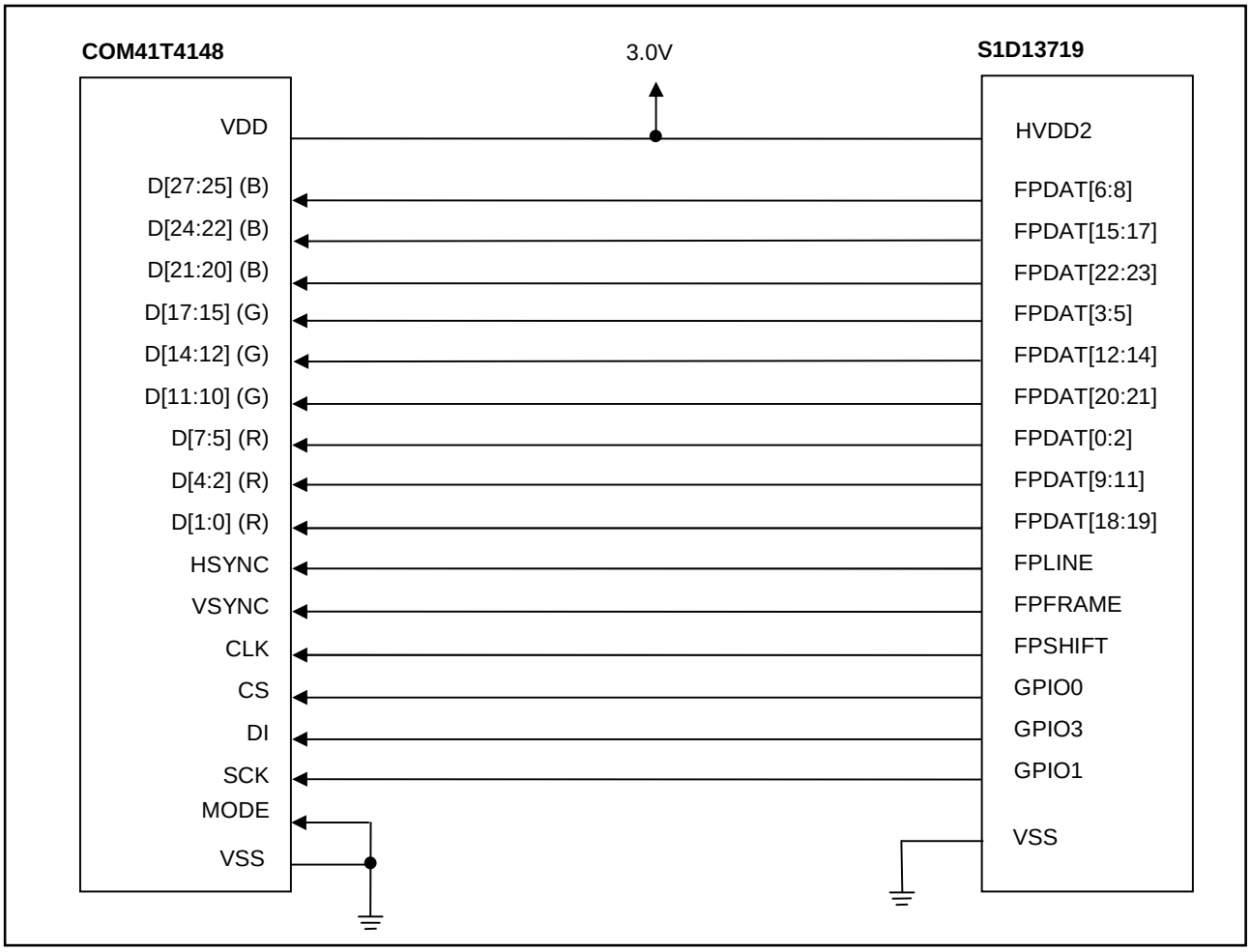

Figure 4-4 Connecting the COM41T4148 to the S1D13719 (24-bit Panel Mode, MODE = “VSS”)

The following table provides a detailed pin listing for the required connections between the COM41T4148 and the S1D13719. This table is for the setting of 18-bit panel mode (MODE=”VDD”) on COM41T4148. Pin mappings are shown for both S1D13719 package types.

Table 4-4 Connecting the COM41T4148 to the S1D13719 (18-bit Panel Mode, MODE = “VDD”)

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13719 PFBGA Pin#	S1D13719 QFP Pin#	S1D13719 Pin Name
1	VCOM	Common driver signal	—	—	—
2	D27	BLUE data signal (MSB)	M3	56	FPDAT6
3	D26	BLUE data signal	L6	68	FPDAT7
4	D25	BLUE data signal	L2	45	FPDAT8
5	D24	BLUE data signal	M4	60	FPDAT15
6	D23	BLUE data signal	L7	74	FPDAT16

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13719 PFBGA Pin#	S1D13719 QFP Pin#	S1D13719 Pin Name
7	D22	BLUE data signal (LSB)	N6	73	FPDAT17
8	D21	Connect to VSS	Note	Note	VSS
9	D20	Connect to VSS	Note	Note	VSS
10	D17	GREEN data signal (MSB)	P2	53	FPDAT3
11	D16	GREEN data signal	N2	54	FPDAT4
12	D15	GREEN data signal	N3	55	FPDAT5
13	D14	GREEN data signal	P8	81	FPDAT12
14	D13	GREEN data signal	N8	80	FPDAT13
15	D12	GREEN data signal (LSB)	M7	79	FPDAT14
16	D11	Connect to VSS	Note	Note	VSS
17	D10	Connect to VSS	Note	Note	VSS
18	D07	RED data signal (MSB)	L3	47	FPDAT0
19	D06	RED data signal	N1	48	FPDAT1
20	D05	RED data signal	K4	49	FPDAT2
21	D04	RED data signal	M6	72	FPDAT9
22	D03	RED data signal	M8	83	FPDAT10
23	D02	RED data signal (LSB)	L8	82	FPDAT11
24	D01	Connect to VSS	Note	Note	VSS
25	D00	Connect to VSS	Note	Note	VSS
26	BLON	Open	—	—	—
27	STBY	Standby control signal input (Lo: Normal, Hi: Standby)	Note	Note	VSS
28	DE	Input data enable (Hi-active)	M1	44	DRDY
29	REV	Vertical and Horizontal reverse control signal input (Lo: Normal, Hi: Reverse)	Note	Note	VSS
30	VSYNC	Vertical synchronous signal (Negative)	P3	57	FPFRAME
31	HSYNC	Horizontal synchronous signal (Negative)	P4	58	FPLINE
32	CLK	Dot clock (Capture at the falling edge)	P5	66	FPSHIFT
33	VSS	GND	Note	Note	VSS
34	MODE	Input mode select, Lo: 24bit, Hi: 18bit	J3, H4, P6, M10	35, 52, 71, 96	PIOVDD
35	POCB	Power on clear input (Lo-active)	—	—	—
36	NC	OPEN	—	—	—
37	RVDD	Internal power	—	—	—
38	COMDC	Common driver DC output	—	—	—
39	NC	OPEN	—	—	—
40	VSREF	Internal DAC reference power	—	—	—
41	C1P	For charge pump capacitor connection	—	—	—

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13719 PFBGA Pin#	S1D13719 QFP Pin#	S1D13719 Pin Name
42	C1M	For charge pump capacitor connection	—	—	—
43	C2M	For charge pump capacitor connection	—	—	—
44	C2P	For charge pump capacitor connection	—	—	—
45	VDD	Power +3.0V	J3, H4, P6, M10	35, 52, 71, 96	PIOVDD
46	COMOUT	Rectangular wave output for common driver	—	—	—
47	VDD2	Internal power	—	—	—
48	VSS	GND	Note	Note	VSS
49	VSS	GND	Note	Note	VSS
50	VSS	GND	Note	Note	VSS
51	C3M	For charge pump capacitor connection	—	—	—
52	C3P	For charge pump capacitor connection	—	—	—
53	C4M	For charge pump capacitor connection	—	—	—
54	C4P	For charge pump capacitor connection	—	—	—
55	VVCOM	COMOUT power output	—	—	—
56	NC	OPEN	—	—	—
57	NC	OPEN	—	—	—
58	VGH	Gate driver power (+)	—	—	—
59	C5P	For charge pump capacitor connection	—	—	—
60	C5M	For charge pump capacitor connection	—	—	—
61	VGL	Gate driver power (-)	—	—	—
62	BLL2	LED drive power2 (cathode)	—	—	—
63	BLH2	LED drive power2 (anode)	—	—	—
64	NC	OPEN	—	—	—
65	NC	OPEN	—	—	—
66	BLH1	LED drive power1 (anode)	—	—	—
67	BLL1	LED drive power1 (cathode)	—	—	—

S1D13719 PIOVDD and COM41T4148 VDD must be configured between +2.75V to +3.25V.

Note

Allocation of VSS pin for each packages are as follows.
PFBGA: B1, J2, E10, K2, M5, P9, H10, L11, B14
QFP: 2, 31, 43, 65, 85, 112, 131, 149, 158, 188

The following table provides a detailed pin listing for the required connections between the COM41T4148 and the S1D13719. This table is for the setting of 24-bit panel mode (MODE="VSS") on COM41T4148. Pin mappings are shown for both S1D13719 package types.

Table 4-5 Connecting the COM41T4148 to the S1D13719 (24-bit Panel Mode, MODE = "VSS")

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13719 PFBGA Pin#	S1D13719 QFP Pin#	S1D13719 Pin Name
1	VCOM	Common driver signal	—	—	—
2	D27	BLUE data signal (MSB)	M3	56	FPDAT6
3	D26	BLUE data signal	L6	68	FPDAT7
4	D25	BLUE data signal	L2	45	FPDAT8
5	D24	BLUE data signal	M4	60	FPDAT15
6	D23	BLUE data signal	L7	74	FPDAT16
7	D22	BLUE data signal	N6	73	FPDAT17
8	D21	BLUE data signal	N12	98	FPDAT22
9	D20	BLUE data signal (LSB)	P10	89	FPDAT23
10	D17	GREEN data signal (MSB)	P2	53	FPDAT3
11	D16	GREEN data signal	N2	54	FPDAT4
12	D15	GREEN data signal	N3	55	FPDAT5
13	D14	GREEN data signal	P8	81	FPDAT12
14	D13	GREEN data signal	N8	80	FPDAT13
15	D12	GREEN data signal	M7	79	FPDAT14
16	D11	GREEN data signal	M11	100	FPDAT20
17	D10	GREEN data signal (LSB)	P12	99	FPDAT21
18	D07	RED data signal (MSB)	L3	47	FPDAT0
19	D06	RED data signal	N1	48	FPDAT1
20	D05	RED data signal	K4	49	FPDAT2
21	D04	RED data signal	M6	72	FPDAT9
22	D03	RED data signal	M8	83	FPDAT10
23	D02	RED data signal	L8	82	FPDAT11
24	D01	RED data signal	M13	102	FPDAT18
25	D00	RED data signal (LSB)	M12	101	FPDAT19
26	BLON	External back light control logic output signal	—	—	—
27	CS	Serial chip select (Lo-active)	L1	39	GPIO0
28	DI	Serial data input	P13	105	GPIO3
29	SCK	Serial clock	L10	108	GPIO1
30	VSYNC	Vertical synchronous signal (Negative)	P3	57	FPFRAME
31	HSYNC	Horizontal synchronous signal (Negative)	P4	58	FPLINE
32	CLK	Dot clock (Capture at the falling edge)	P5	66	FPSHIFT
33	VSS	GND	Note	Note	VSS

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13719 PFBGA Pin#	S1D13719 QFP Pin#	S1D13719 Pin Name
34	MODE	Input mode select, Lo: 24bit, Hi: 18bit	Note	Note	VSS
35	POCB	Power on clear input (Lo-active)	—	—	—
36	NC	OPEN	—	—	—
37	RVDD	Internal power	—	—	—
38	COMDC	Common driver DC output	—	—	—
39	NC	OPEN	—	—	—
40	VSREF	Internal DAC reference power	—	—	—
41	C1P	For charge pump capacitor connection	—	—	—
42	C1M	For charge pump capacitor connection	—	—	—
43	C2M	For charge pump capacitor connection	—	—	—
44	C2P	For charge pump capacitor connection	—	—	—
45	VDD	Power +3.0V	J3, H4, P6, M10	35, 52, 71, 96	PIOVDD
46	COMOUT	Rectangular wave output for common driver	—	—	—
47	VDD2	Internal power	—	—	—
48	VSS	GND	Note	Note	VSS
49	VSS	GND	Note	Note	VSS
50	VSS	GND	Note	Note	VSS
51	C3M	For charge pump capacitor connection	—	—	—
52	C3P	For charge pump capacitor connection	—	—	—
53	C4M	For charge pump capacitor connection	—	—	—
54	C4P	For charge pump capacitor connection	—	—	—
55	VVCOM	COMOUT power output	—	—	—
56	NC	OPEN	—	—	—
57	NC	OPEN	—	—	—
58	VGH	Gate driver power (+)	—	—	—
59	C5P	For charge pump capacitor connection	—	—	—
60	C5M	For charge pump capacitor connection	—	—	—
61	VGL	Gate driver power (-)	—	—	—
62	BLL2	LED drive power2 (cathode)	—	—	—
63	BLH2	LED drive power2 (anode)	—	—	—
64	NC	OPEN	—	—	—

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13719 PFBGA Pin#	S1D13719 QFP Pin#	S1D13719 Pin Name
65	NC	OPEN	—	—	—
66	BLH1	LED drive power1 (anode)	—	—	—
67	BLL1	LED drive power1 (cathode)	—	—	—

S1D13719 PIOVDD and COM41T4148 VDD must be configured between +2.75V to +3.25V.

Note
Allocation of VSS pin for each packages are as follows.
PFBGA: B1, J2, E10, K2, M5, P9, H10, L11, B14
QFP: 2, 31, 43, 65, 85, 112, 131, 149, 158, 188

4.2.3 Connecting the COM41T4148 to the S1D13748

The following diagram shows an example implementation of the COM41T4148 panel connected to the S1D13748. This example is for the setting of 18-bit panel mode (MODE="VDD") on COM41T4148.

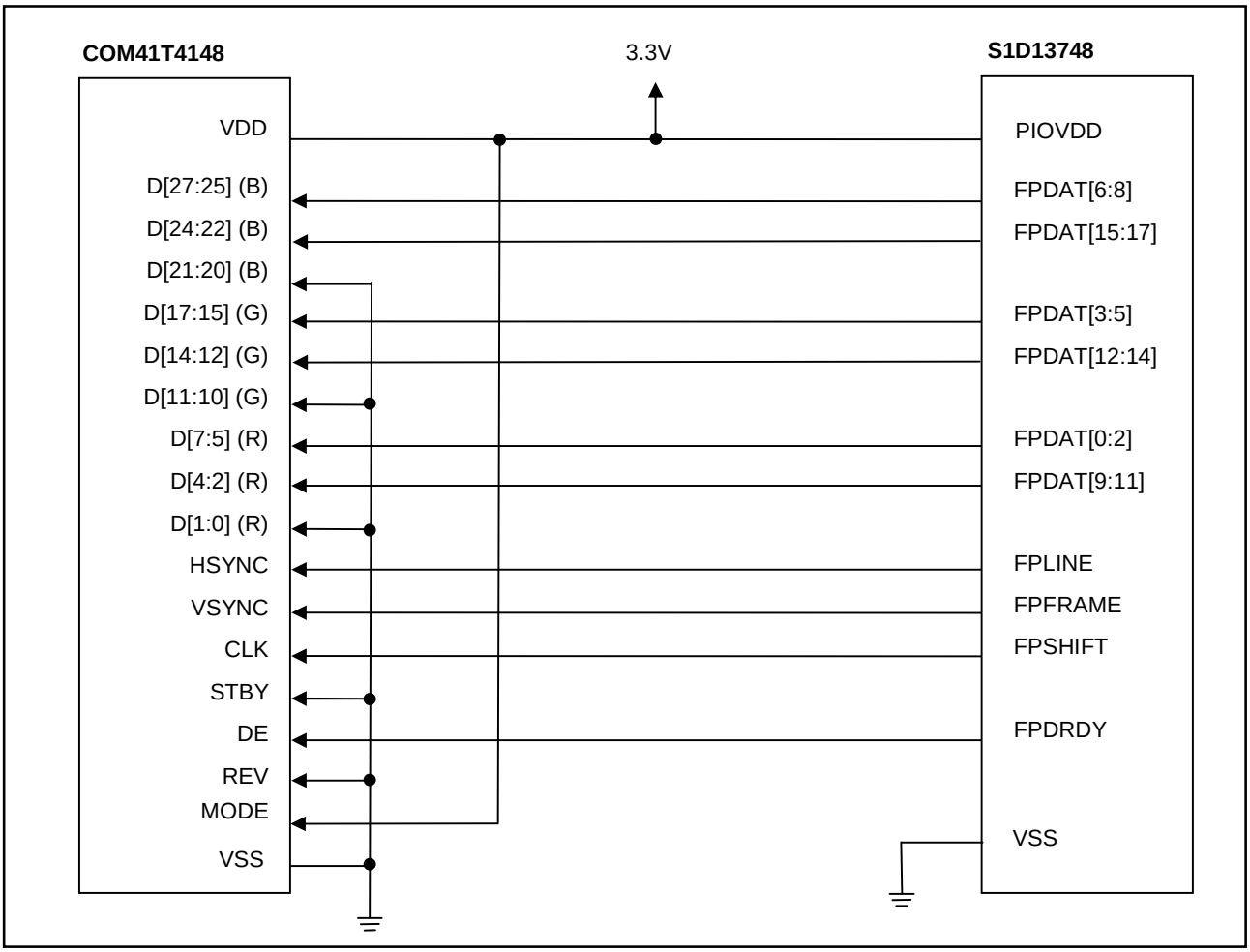

Figure 4-5 Connecting the COM41T4148 to the S1D13748 (18-bit Panel Mode, MODE = "VDD")

The following diagram shows an example implementation of the COM41T4148 panel connected to the S1D13748. This example is for the setting of 24-bit panel mode (MODE="VSS") on COM41T4148.

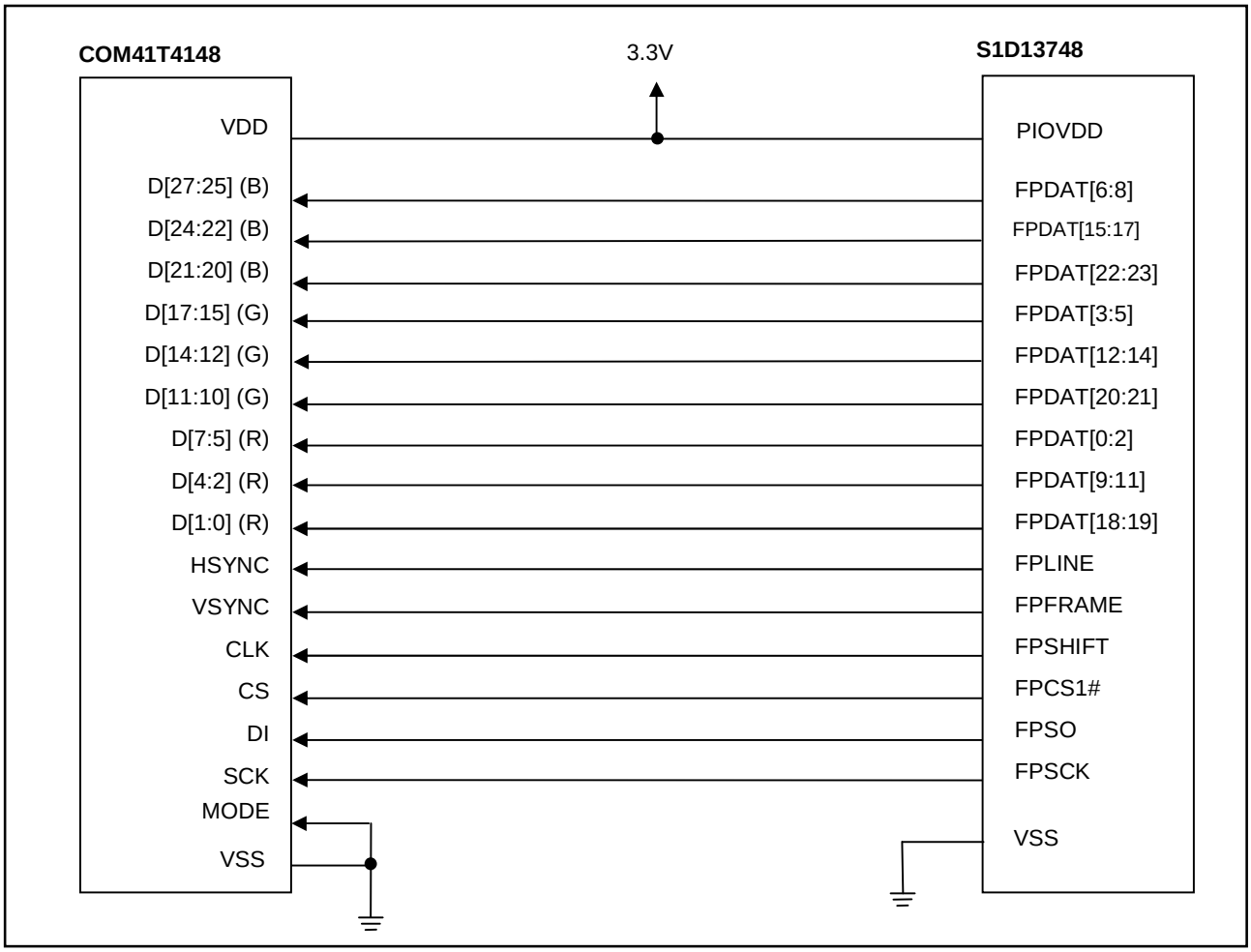

Figure 4-6 Connecting the COM41T4148 to the S1D13748 (24-bit Panel Mode, MODE = "VSS")

The following table provides a detailed pin listing for the required connections between the COM41T4148 and the S1D13748. This table is for the setting of 18-bit panel mode (MODE="VDD") on COM41T4148. Pin mappings are shown for both S1D13748 package types.

Table 4-6 Connecting the COM41T4148 to the S1D13748 (18-bit panel mode, MODE = "VDD")

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
1	VCOM	Common driver signal	—	—	—
2	D27	BLUE data signal (MSB)	58	L7	FPDAT6
3	D26	BLUE data signal	59	J7	FPDAT7
4	D25	BLUE data signal	60	K7	FPDAT8
5	D24	BLUE data signal	70	L10	FPDAT15
6	D23	BLUE data signal	71	K10	FPDAT16

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
7	D22	BLUE data signal (LSB)	72	J9	FPDAT17
8	D21	Connect to VSS	Note	Note	VSS
9	D20	Connect to VSS	Note	Note	VSS
10	D17	GREEN data signal (MSB)	52	H6	FPDAT3
11	D16	GREEN data signal	53	J6	FPDAT4
12	D15	GREEN data signal	54	L6	FPDAT5
13	D14	GREEN data signal	64	L9	FPDAT12
14	D13	GREEN data signal	68	K9	FPDAT13
15	D12	GREEN data signal (LSB)	69	H8	FPDAT14
16	D11	Connect to VSS	Note	Note	VSS
17	D10	Connect to VSS	Note	Note	VSS
18	D07	RED data signal (MSB)	49	J5	FPDAT0
19	D06	RED data signal	50	L5	FPDAT1
20	D05	RED data signal	51	K5	FPDAT2
21	D04	RED data signal	61	K8	FPDAT9
22	D03	RED data signal	62	J8	FPDAT10
23	D02	RED data signal (LSB)	63	L8	FPDAT11
24	D01	Connect to VSS	Note	Note	VSS
25	D00	Connect to VSS	Note	Note	VSS
26	BLON	Open	—	—	—
27	STBY	Standby control signal input (Lo: Normal, Hi: Standby)	Note	Note	VSS
28	DE	Input data enable (Hi-active)	78	G7	FPDRDY
29	REV	Vertical and Horizontal reverse control signal input (Lo: Normal, Hi: Reverse)	Note	Note	VSS
30	VSYNC	Vertical synchronous signal (Negative)	76	J10	FPFRAME
31	HSYNC	Horizontal synchronous signal (Negative)	77	H10	FPLINE
32	CLK	Dot clock (Capture at the falling edge)	75	J11	FPSHIFT
33	VSS	GND	Note	Note	VSS
34	MODE	Input mode select, Lo: 24bit, Hi: 18bit	19, 26, 35, 40, 46, 55, 67, 73, 83, 87	E8, F4, H7, J4	PIOVDD
35	POCB	Power on clear input (Lo-active)	—	—	—
36	NC	OPEN	—	—	—
37	RVDD	Internal power	—	—	—
38	COMDC	Common driver DC output	—	—	—
39	NC	OPEN	—	—	—
40	VSREF	Internal DAC reference power	—	—	—
41	C1P	For charge pump capacitor connection	—	—	—
42	C1M	For charge pump capacitor connection	—	—	—
43	C2M	For charge pump capacitor connection	—	—	—

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
44	C2P	For charge pump capacitor connection	—	—	—
45	VDD	Power +3.3V	19, 26, 35, 40, 46, 55, 67, 73, 83, 87	E8, F4, H7, J4	PIOVDD
46	COMOUT	Rectangular wave output for common driver	—	—	—
47	VDD2	Internal power	—	—	—
48	VSS	GND	Note	Note	VSS
49	VSS	GND	Note	Note	VSS
50	VSS	GND	Note	Note	VSS
51	C3M	For charge pump capacitor connection	—	—	—
52	C3P	For charge pump capacitor connection	—	—	—
53	C4M	For charge pump capacitor connection	—	—	—
54	C4P	For charge pump capacitor connection	—	—	—
55	VVCOM	COMOUT power output	—	—	—
56	NC	OPEN	—	—	—
57	NC	OPEN	—	—	—
58	VGH	Gate driver power(+)	—	—	—
59	C5P	For charge pump capacitor connection	—	—	—
60	C5M	For charge pump capacitor connection	—	—	—
61	VGL	Gate driver power (-)	—	—	—
62	BLL2	LED drive power2 (cathode)	—	—	—
63	BLH2	LED drive power2 (anode)	—	—	—
64	NC	OPEN	—	—	—
65	NC	OPEN	—	—	—
66	BLH1	LED drive power1 (anode)	—	—	—
67	BLL1	LED drive power1 (cathode)	—	—	—

S1D13748 PIOVDD and COM41T4148 VDD must be configured between +3.0V to +3.6V.

Note

Allocation of VSS pin for each packages are as follows.
PFBGA: B1, C4, C8, D10, E6, F2, F8, G4, K6, K11
QFP: 6, 13, 20, 31, 36, 39, 47, 56, 66, 74, 82, 91, 97, 102, 108, 115, 129, 138, 144

The following table provides a detailed pin listing for the required connections between the COM41T4148 and the S1D13748. This table is for the setting of 24-bit panel mode (MODE="VSS") on COM41T4148. Pin mappings are shown for both S1D13748 package types.

Table 4-7 Connecting the COM41T4148 to the S1D13748 (24-bit Panel Mode, MODE = "VSS")

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
1	VCOM	Common driver signal	—	—	—
2	D27	BLUE data signal (MSB)	58	L7	FPDAT6
3	D26	BLUE data signal	59	J7	FPDAT7
4	D25	BLUE data signal	60	K7	FPDAT8
5	D24	BLUE data signal	70	L10	FPDAT15
6	D23	BLUE data signal	71	K10	FPDAT16
7	D22	BLUE data signal	72	J9	FPDAT17
8	D21	BLUE data signal	45	L4	FPDAT22
9	D20	BLUE data signal (LSB)	48	H5	FPDAT23
10	D17	GREEN data signal (MSB)	52	H6	FPDAT3
11	D16	GREEN data signal	53	J6	FPDAT4
12	D15	GREEN data signal	54	L6	FPDAT5
13	D14	GREEN data signal	64	L9	FPDAT12
14	D13	GREEN data signal	68	K9	FPDAT13
15	D12	GREEN data signal	69	H8	FPDAT14
16	D11	GREEN data signal	43	K4	FPDAT20
17	D10	GREEN data signal (LSB)	44	G6	FPDAT21
18	D07	RED data signal (MSB)	49	J5	FPDAT0
19	D06	RED data signal	50	L5	FPDAT1
20	D05	RED data signal	51	K5	FPDAT2
21	D04	RED data signal	61	K8	FPDAT9
22	D03	RED data signal	62	J8	FPDAT10
23	D02	RED data signal	63	L8	FPDAT11
24	D01	RED data signal	41	K3	FPDAT18
25	D00	RED data signal (LSB)	42	L3	FPDAT19
26	BLON	External back light control logic output signal	—	—	—
27	CS	Serial chip select (Lo-active)	80	G9	FPCS1#
28	DI	Serial data input	86	G11	FPSO
29	SCK	Serial clock	84	H11	FPSCK
30	VSYNC	Vertical synchronous signal (Negative)	76	J10	FPFRAME
31	HSYNC	Horizontal synchronous signal (Negative)	77	H10	FPLINE
32	CLK	Dot clock (Capture at the falling edge)	75	J11	FPSHIFT
33	VSS	GND	Note	Note	VSS
34	MODE	Input mode select, Lo: 24bit, Hi: 18bit	Note	Note	VSS
35	POCB	Power on clear input (Lo-active)	—	—	—
36	NC	OPEN	—	—	—

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
37	RVDD	Internal power	—	—	—
38	COMDC	Common driver DC output	—	—	—
39	NC	OPEN	—	—	—
40	VSREF	Internal DAC reference power	—	—	—
41	C1P	For charge pump capacitor connection	—	—	—
42	C1M	For charge pump capacitor connection	—	—	—
43	C2M	For charge pump capacitor connection	—	—	—
44	C2P	For charge pump capacitor connection	—	—	—
45	VDD	Power +3.0V	19, 26, 35, 40, 46, 55, 67, 73, 83, 87	E8, F4, H7, J4	PIOVDD
46	COMOUT	Rectangular wave output for common driver	—	—	—
47	VDD2	Internal power	—	—	—
48	VSS	GND	Note	Note	VSS
49	VSS	GND	Note	Note	VSS
50	VSS	GND	Note	Note	VSS
51	C3M	For charge pump capacitor connection	—	—	—
52	C3P	For charge pump capacitor connection	—	—	—
53	C4M	For charge pump capacitor connection	—	—	—
54	C4P	For charge pump capacitor connection	—	—	—
55	VVCOM	COMOUT power output	—	—	—
56	NC	OPEN	—	—	—
57	NC	OPEN	—	—	—
58	VGH	Gate driver power (+)	—	—	—
59	C5P	For charge pump capacitor connection	—	—	—
60	C5M	For charge pump capacitor connection	—	—	—
61	VGL	Gate driver power (-)	—	—	—
62	BLL2	LED drive power2 (cathode)	—	—	—
63	BLH2	LED drive power2 (anode)	—	—	—
64	NC	OPEN	—	—	—
65	NC	OPEN	—	—	—
66	BLH1	LED drive power1 (anode)	—	—	—
67	BLL1	LED drive power1 (cathode)	—	—	—

S1D13748 PIOVDD and COM41T4148 VDD must be configured between +3.0V to +3.6V.

Note

Allocation of VSS pin for each packages are as follows.
PFBGA: B1, C4, C8, D10, E6, F2, F8, G4, K6, K11
QFP: 6, 13, 20, 31, 36, 39, 47, 56, 66, 74, 82, 91, 97, 102, 108, 115, 129, 138, 144

4.3 Example Register Settings

In addition to the pin connections, the S1D13513/S1D13719/S1D13748 internal registers must be configured appropriately for the COM41T4148 LCD panel. The following tables provide example settings for each display controller. However, these values are for reference only and may differ according to each specific implementation.

Also included in the table is an example clock configuration designed to achieve a 50Hz or greater LCD refresh.

Table 4-8 Example Register Settings for the S1D13513

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0800h] LCD Panel Type Select Register	0300h	—
REG[0802h] LCD Horizontal Total Register	01FFh	512
REG[0804h] LCD Horizontal Display Period Register	009Fh	320
REG[0806h] LCD Horizontal Display Period Start Position Register	0009h	10
REG[0808h] LCD Horizontal Pulse Width	8000h+000Dh	14
REG[080Ah] LCD Horizontal Pulse Start Position	0000h	0
REG[080Ch] LCD Vertical Total Register	00F0h	241
REG[080Eh] LCD Vertical Display Period Resister	00EFh	240
REG[0810h] Vertical Display Period Start Position Register	0000h	0
REG[0812h] LCD Vertical Pulse Width	8000h+0000h	0
REG[0814h] LCD Vertical Pulse Start Position	0000h	0
PLL2 output frequency in MHz	—	90
REG[0446h] LCD Clock Control Register	000Fh	16
FPSHIFT in MHz	—	6.67
LCD Refresh in Hz	—	54

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13513 register values, see the *S1D13513 Hardware Functional Specification*, document number X78B-A-001-xx.

Table 4-9 Example Serial Output Sequence for the S1D13513

Sequence	Register	Data	Contents
1	0448h	000Eh	LCD serial clock divide 100MHz/15
2	0816h	00A3h	LCD serial 24-bit command interface setting
3	081Ch	0016h	Command
4	081Ch	0835h	Command
5	081Ch	0471h	Command
6	081Ch	0C00h	Command
7	081Ch	0210h	Command
8	081Ch	0A4Ch	Command
9	081Ch	0618h	Command
10	081Ch	0ED0h	Command
11	081Ch	0100h	Command
12	081Ch	0980h	Command
13	081Ch	0500h	Command
14	081Ch	0D40h	Command
15	081Ch	0300h	Command
16	081Ch	0B00h	Command
17	081Ch	0700h	Command
18	081Ch	0F02h	Command

Table 4-10 Example Register Settings for the S1D13719

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0040h] Horizontal Total Register	53	432
REG[0042h] Horizontal Display Period Register	159	320
REG[0044h] Horizontal Display Period Start Position Register	11	20
REG[0046h] LCD1 FPLINE Register	0080h+1	2
REG[0048h] LCD1 FPLINE Pulse Position Register	17	18
REG[004Ah] Vertical Total Register	242	243
REG[004Ch] Vertical Display Period Resister	240	241
REG[004E] Vertical Display Period Start Position Register	2	2
REG[0050h] LCD1 FPFRAME Register	0080h+1	2
REG[0052h] LCD1 FPFRAME Pulse Position Register	2	2
PLL output in MHz	—	54
REG[0030h] LCD Interface Clock Configuration Register	0503h	8
FPSHIFT in MHz	—	6.75
LCD Refresh in Hz	—	64.3

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13719 register values, see the *S1D13719 Hardware Functional Specification*, document number X59A-A-001-xx.

Table 4-11 Example Serial Output Sequence for the S1D13719

Sequence	Register	Data	Contents
1	030Ch	0016h	Command
2	030Ch	0835h	Command
3	030Ch	0471h	Command
4	030Ch	0C00h	Command
5	030Ch	0210h	Command
6	030Ch	0A4Ch	Command
7	030Ch	0618h	Command
8	030Ch	0ED0h	Command
9	030Ch	0100h	Command
10	030Ch	0980h	Command
11	030Ch	0500h	Command
12	030Ch	0D40h	Command
13	030Ch	0300h	Command
14	030Ch	0B00h	Command
15	030Ch	0700h	Command
16	030Ch	0F02h	Command

Note
GPIO0, GPIO1, and GPIO3 are used for serial communications.

Table 4-12 Example Register Settings for the S1D13748

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0040h] LCD1 Horizontal Total Register	63	512
REG[0042h] LCD1 Horizontal Display Period Register	159	320
REG[0044h] LCD1 Horizontal Display Period Start Position Register	2	10
REG[0046h] LCD1 Horizontal Pulse Register	0080h+13	14
REG[0048h] LCD1 Horizontal Pulse Start Position Register	0	1
REG[004Ah] LCD1 Vertical Total Register	240	241
REG[004Ch] LCD1 Vertical Display Period Resister	239	240
REG[004Eh] LCD1 Vertical Display Period Start Position Register	0	0
REG[0050h] LCD1 Vertical Pulse Register	0080h+0	1
REG[0052h] LCD1 Vertical Pulse Start Position Register	0	1
REG[0246h] Main1 Window Image Horizontal Size Register	319	320
REG[0248h] Main1 Window Image Vertical Size Register	239	240
PLL output frequency in MHz	—	50
REG[0030h] LCD Interface Clock Setting Register	0507h	8
FPSHIFT in MHz	—	6.25
LCD Refresh in Hz	—	50.7

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13748 register values, see the *S1D13748 Hardware Functional Specification*, document number X80A-A-001-xx.

Table 4-13 Example Serial Output Sequence for the S1D13748

Sequence	Register	Data	Contents
1	0034h	0016h	Command
2	0034h	0835h	Command
3	0034h	0471h	Command
4	0034h	0C00h	Command
5	0034h	0210h	Command
6	0034h	0A4Ch	Command
7	0034h	0618h	Command
8	0034h	0ED0h	Command
9	0034h	0100h	Command
10	0034h	0980h	Command
11	0034h	0500h	Command
12	0034h	0D40h	Command
13	0034h	0300h	Command
14	0034h	0B00h	Command
15	0034h	0700h	Command
16	0034h	0F02h	Command

5 Connecting to the Ortustech COM57T5139

The Ortustech COM57T5139 TFT panel is compatible with the S1D13513 and S1D13748 display controllers. The following sections will provide connector details, pin mappings, and example register settings for these combinations.

5.1 COM57T5139 Pin Mapping

The COM57T5139 TFT panel uses a 45-pin connector with the following pin mapping.

Table 5-1 COM57T5139 Pin Mapping

Connector Pin#	Pin Name	Pin Description
1	VSS	GND
2	CLK	24bit mode: Dot clock 18bit mode: Dot clock (Capture at the falling edge)
3	VSS	GND
4	HSYNC	24bit mode: Horizontal synchronous signal 18bit mode: Horizontal synchronous signal (Negative)
5	VSYNC	24bit mode: Vertical synchronous signal 18bit mode: Vertical synchronous signal (Negative)
6	VSS	GND
7	D20	24bit mode: BLUE data signal (LSB) 18bit mode: Connect to VSS
8	D21	24bit mode: BLUE data signal 18bit mode: Connect to VSS
9	D22	24bit mode: BLUE data signal 18bit mode: BLUE data signal (LSB)
10	D23	BLUE data signal
11	D24	BLUE data signal
12	D25	BLUE data signal
13	D26	BLUE data signal
14	D27	BLUE data signal (MSB)
15	VSS	GND
16	D10	24bit mode: GREEN data signal (LSB) 18bit mode: Connect to VSS
17	D11	24bit mode: GREEN data signal 18bit mode: Connect to VSS
18	D12	24bit mode: GREEN data signal 18bit mode: GREEN data signal (LSB)
19	D13	GREEN data signal
20	D14	GREEN data signal
21	D15	GREEN data signal
22	D16	GREEN data signal
23	D17	GREEN data signal (MSB)
24	VSS	GND
25	D00	24bit mode: RED data signal (LSB) 18bit mode: Connect to VSS
26	D01	24bit mode: RED data signal 18bit mode: Connect to VSS

Connector Pin#	Pin Name	Pin Description
27	D02	24bit mode: RED data signal 18bit mode: RED data signal (LSB)
28	D03	RED data signal
29	D04	RED data signal
30	D05	RED data signal
31	D06	RED data signal
32	D07	RED data signal (MSB)
33	VSS	GND
34	MODE	Input mode select, Lo: 24bit Hi: 18bit
35	VDD	Power supply for logic +3.3V (3.0V≤VDD≤3.6V)
36	VDD	Power supply for logic +3.3V (3.0V≤VDD≤3.6V)
37	CS/STBY	24bit mode: Serial chip select (Lo-active) 18bit mode: Standby control signal input (Lo: Normal, Hi: Standby)
38	DI/DE	24bit mode: Serial data input 18bit mode: DATA ENABLE (Hi-active)
39	SCK/REV	24bit mode: Serial clock 18bit mode: Vertical and Horizontal reverse control signal input (Lo: Normal, Hi:Reverse)
40	VSS	GND
41	VBL	Power supply for back light +12.0V (10.8V≤VBL≤13.2V)
42	VBL	Power supply for back light +12.0V (10.8V≤VBL≤13.2V)
43	PDM	Back light pulse input, Lo: OFF（0%）, Hi: ON（100%）
44	VSS	GND
45	VSS	GND

Note
The recommended connector is a 04-6240-045-023-846+ from Kyocera elco.

5.2 Connection Examples

The information in this section provides connection examples for the S1D13513 and S1D13748 display controllers. For the S1D13513 and S1D13748, the display controller is available in two packages. The connection information differs for each package and is listed separately.

In addition to the pin connections for the selected display controller, the COM57T5139 requires the following power supplies.

VDD +3.3V (3.0V ≤ VDD ≤ 3.6V)

VBL +12.0V (10.8V ≤ VBL ≤ 13.2V)

For VDD, select a voltage within the supportable range of the Display Controller.

For further details on the COM57T5139, such as power consumption and absolute maximum ratings, please contact your Ortustech representative.

5.2.1 Connecting the COM57T5139 to the S1D13513

The following diagram shows an example implementation of the COM57T5139 panel connected to the S1D13513. This example is for the setting of 18-bit panel mode (MODE=”VDD”) on COM57T5139.

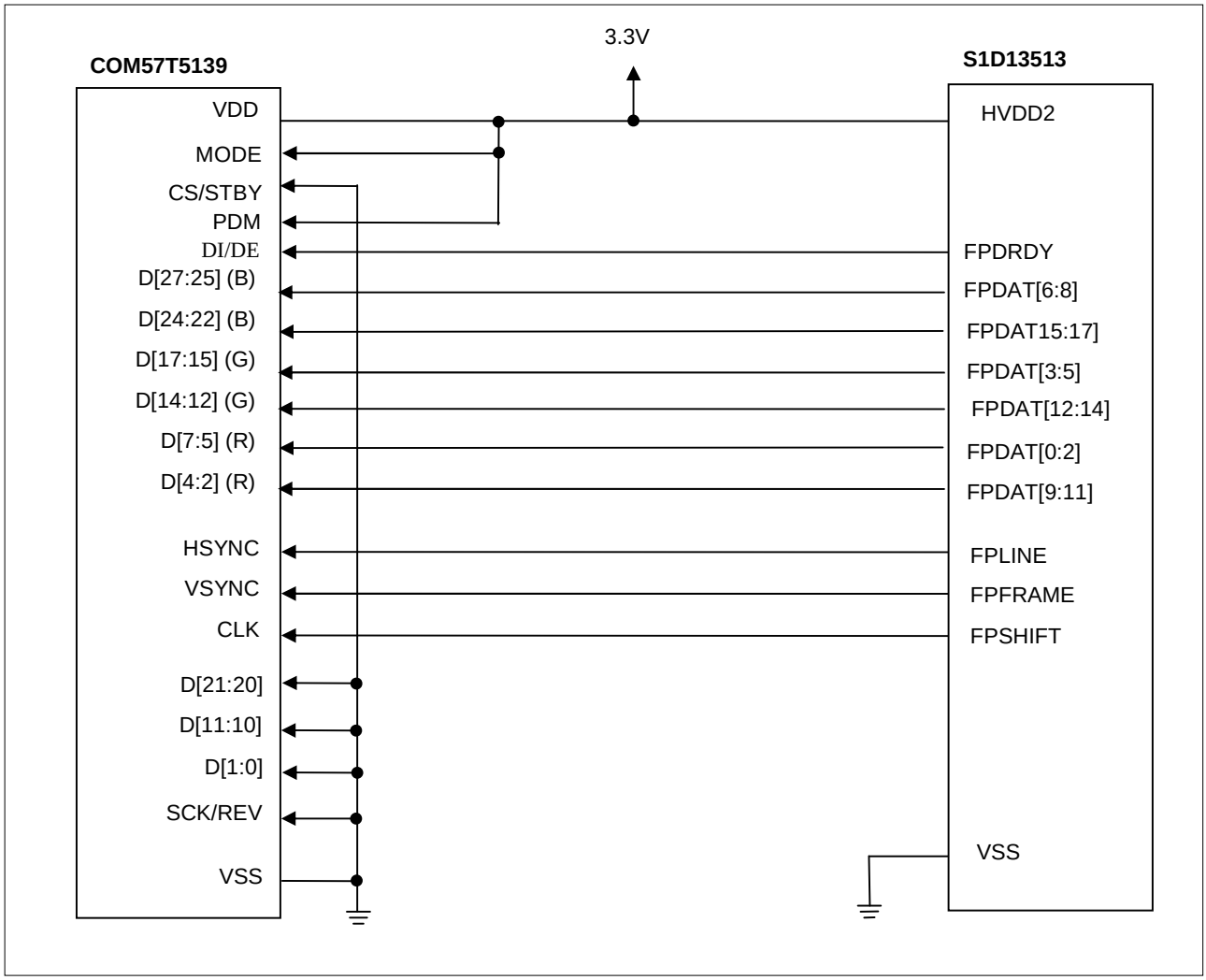

Figure 5-1 Connecting the COM57T5139 to the S1D13513 (18-bit panel mode, MODE = “VDD”)

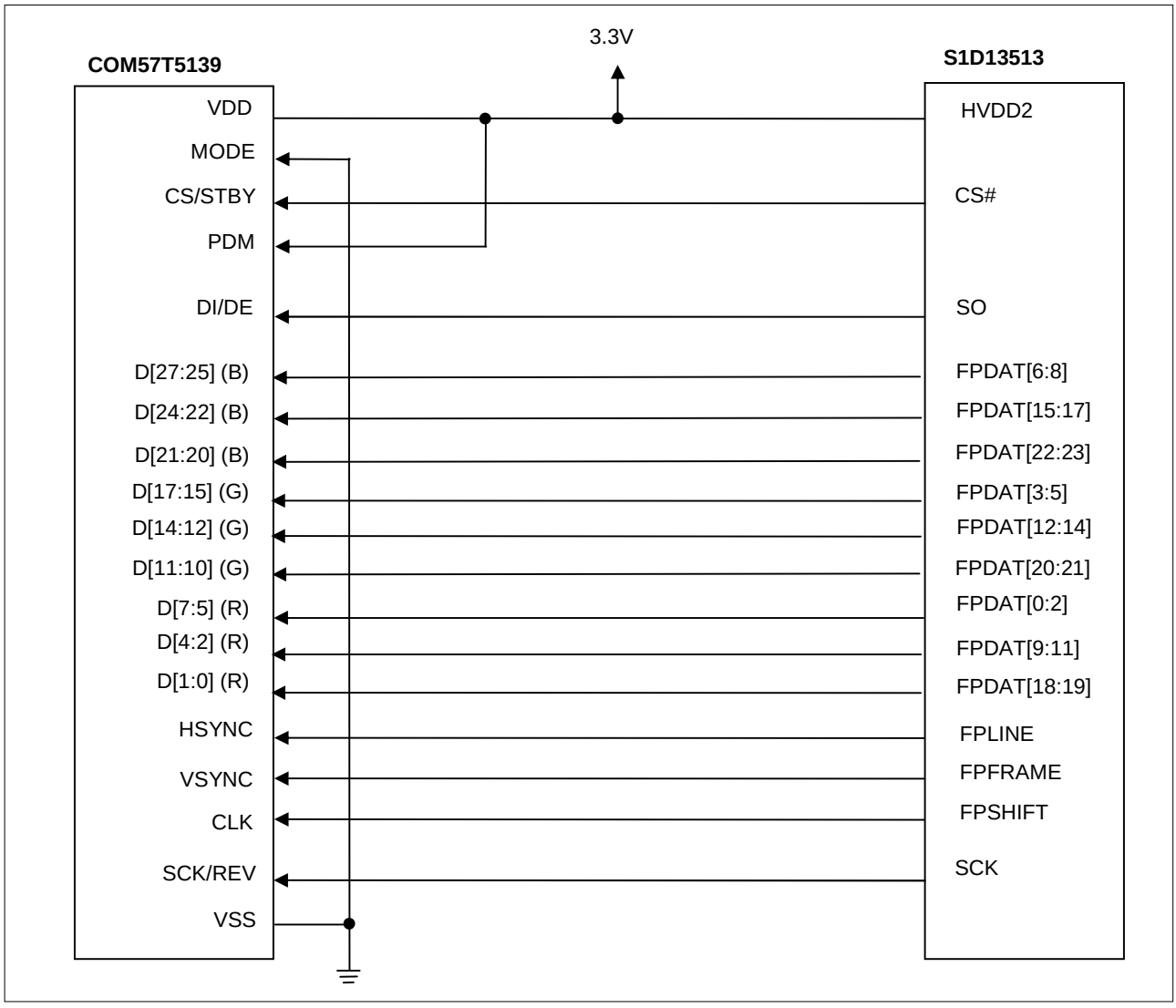

Figure 5-2 Connecting the COM57T5139 to the S1D13513 (24-bit panel mode, MODE = "VSS")

The following table provides a detailed pin listing for the required connections between the COM57T5139 and the S1D13513. This table is for the setting of 18-bit panel mode (MODE="VDD") on COM57T5139. Pin mappings are shown for both S1D13513 package types.

Table 5-2 Connecting the COM57T5139 to the S1D13513 (18-bit panel mode)

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
1	VSS	GND	Note	Note	VSS
2	CLK	Dot clock (Capture at the falling edge)	77	P8	FPSHIFT
3	VSS	GND	Note	Note	VSS
4	HSYNC	Horizontal synchronous signal (Negative)	79	R8	FPLINE
5	VSYNC	Vertical synchronous signal (Negative)	78	T8	FPFRAME
6	VSS	GND	Note	Note	VSS
7	D20	Connect to VSS	Note	Note	VSS
8	D21	Connect to VSS	Note	Note	VSS
9	D22	BLUE data signal (LSB)	53	N4	FPDAT17
10	D23	BLUE data signal	54	P4	FPDAT16
11	D24	BLUE data signal	55	T2	FPDAT15
12	D25	BLUE data signal	64	R6	FPDAT8
13	D26	BLUE data signal	67	K6	FPDAT7
14	D27	BLUE data signal (MSB)	68	M6	FPDAT6
15	VSS	GND	Note	Note	VSS
16	D10	Connect to VSS	Note	Note	VSS
17	D11	Connect to VSS	Note	Note	VSS
18	D12	GREEN data signal (LSB)	56	R4	FPDAT14
19	D13	GREEN data signal	59	T4	FPDAT13
20	D14	GREEN data signal	60	T5	FPDAT12
21	D15	GREEN data signal	69	L7	FPDAT5
22	D16	GREEN data signal	70	P7	FPDAT4
23	D17	GREEN data signal (MSB)	71	R7	FPDAT3
24	VSS	GND	Note	Note	VSS
25	D00	Connect to VSS	Note	Note	VSS
26	D01	Connect to VSS	Note	Note	VSS
27	D02	RED data signal (LSB)	61	N5	FPDAT11
28	D03	RED data signal	62	M5	FPDAT10
29	D04	RED data signal	63	P6	FPDAT9
30	D05	RED data signal	72	T7	FPDAT2
31	D06	RED data signal	73	N7	FPDAT1
32	D07	RED data signal (MSB)	74	M7	FPDAT0
33	VSS	GND	Note	Note	VSS
34	MODE	Input mode select. Lo: 24bit, Hi: 18bit	57,65,75	L5,L8,T6	HVDD2
35	VDD	Power supply for logic +3.3V	57,65,75	L5,L8,T6	HVDD2
36	VDD	Power supply for logic +3.3V	57,65,75	L5,L8,T6	HVDD2
37	STBY	Standby control signal input (Lo: Normal, Hi: Standby)	Note	Note	VSS
38	DE	Input data enable (Hi-active)	80	M8	FPDRDY
39	REV	Vertical and Horizontal reverse control signal input (Lo: Normal, Hi:Reverse)	Note	Note	VSS
40	VSS	GND	Note	Note	VSS

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
41	VBL	Power supply for back light +12V	—	—	—
42	VBL	Power supply for back light +12V	—	—	—
43	PDM	Back light pulse input. Lo: OFF（0%）, Hi: ON（100%）	57,65,75	L5,L8,T6	HVDD2
44	VSS	GND	Note	Note	VSS
45	VSS	GND	Note	Note	VSS

S1D13513 HVDD2 and COM57T5139 VDD must be configured between +3.0V to +3.6V.

Note
Allocation of VSS pin for each packages are as follows.
QFP: 10, 20, 38, 58, 66, 76, 92, 99, 106, 120, 133, 139, 151, 163, 169, 175, 184, 197
BGA: A1, A16, D4, D8, D13, G7-G10, G13, H7-H10, J1, J7-J10, K2, K7-K10, K13, N3, N6, N9, N13, T1, T16

The following table provides a detailed pin listing for the required connections between the COM57T5139 and the S1D13513. This table is for the setting of 24-bit panel mode (MODE="VSS") on COM57T5139. Pin mappings are shown for both S1D13513 package types.

Table 5-3 Connecting the COM57T5139 to the S1D13513 (24-bit panel mode)

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
1	VSS	GND	Note 1	Note 1	VSS
2	CLK	Dot clock (Capture at the falling edge)	77	P8	FPSHIFT
3	VSS	GND	Note 1	Note 1	VSS
4	HSYNC	Horizontal synchronous signal (Negative)	79	R8	FPLINE
5	VSYNC	Vertical synchronous signal (Negative)	78	T8	FPFRAME
6	VSS	GND	Note 1	Note 1	VSS
7	D20	Connect to VSS	Note 2	K4	FPDAT23
8	D21	Connect to VSS	Note 2	R3	FPDAT22
9	D22	BLUE data signal (LSB)	53	N4	FPDAT17
10	D23	BLUE data signal	54	P4	FPDAT16
11	D24	BLUE data signal	55	T2	FPDAT15
12	D25	BLUE data signal	64	R6	FPDAT8
13	D26	BLUE data signal	67	K6	FPDAT7
14	D27	BLUE data signal (MSB)	68	M6	FPDAT6
15	VSS	GND	Note 1	Note 1	VSS
16	D10	Connect to VSS	Note 2	T3	FPDAT21
17	D11	Connect to VSS	Note 2	P5	FPDAT20
18	D12	GREEN data signal (LSB)	56	R4	FPDAT14
19	D13	GREEN data signal	59	T4	FPDAT13
20	D14	GREEN data signal	60	T5	FPDAT12
21	D15	GREEN data signal	69	L7	FPDAT5
22	D16	GREEN data signal	70	P7	FPDAT4
23	D17	GREEN data signal (MSB)	71	R7	FPDAT3
24	VSS	GND	Note 1	Note 1	VSS

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
25	D00	Connect to VSS	Note 2	K5	FPDAT19
26	D01	Connect to VSS	Note 2	R5	FPDAT18
27	D02	RED data signal (LSB)	61	N5	FPDAT11
28	D03	RED data signal	62	M5	FPDAT10
29	D04	RED data signal	63	P6	FPDAT9
30	D05	RED data signal	72	T7	FPDAT2
31	D06	RED data signal	73	N7	FPDAT1
32	D07	RED data signal (MSB)	74	M7	FPDAT0
33	VSS	GND	Note 1	Note 1	VSS
34	MODE	Input mode select. Lo: 24bit, Hi: 18bit	Note 1	Note 1	VSS
35	VDD	Power supply for logic +3.3V	57,65,75	L5,L8,T6	HVDD2
36	VDD	Power supply for logic +3.3V	57,65,75	L5,L8,T6	HVDD2
37	STBY	Standby control signal input (Lo: Normal, Hi: Standby)	85	L9	CS#
38	DE	Input data enable (Hi-active)	82	T9	SO
39	REV	Vertical and Horizontal reverse control signal input (Lo: Normal, Hi:Reverse)	84	P9	SCK
40	VSS	GND	Note 1	Note 1	VSS
41	VBL	Power supply for back light +12V	—	—	—
42	VBL	Power supply for back light +12V	—	—	—
43	PDM	Back light pulse input. Lo: OFF（0%）, Hi: ON（100%）	57,65,75	L5,L8,T6	HVDD2
44	VSS	GND	Note 1	Note 1	VSS
45	VSS	GND	Note 1	Note 1	VSS

S1D13513 HVDD2 and COM57T5139 VDD must be configured between +3.0V to +3.6V.

Note
Allocation of VSS pin for each packages are as follows.
QFP: 10, 20, 38, 58, 66, 76, 92, 99, 106, 120, 133, 139, 151, 163, 169, 175, 184, 197
BGA: A1, A16, D4, D8, D13, G7-G10, G13, H7-H10, J1, J7-J10, K2, K7-K10, K13, N3, N6, N9, N13, T1, T16

5.2.2 Connecting the COM57T5139 to the S1D13748

The following diagram shows an example implementation of the COM57T5139 panel connected to the S1D13748. This example is for the setting of 18-bit panel mode (MODE=”VDD”) on COM57T5139.

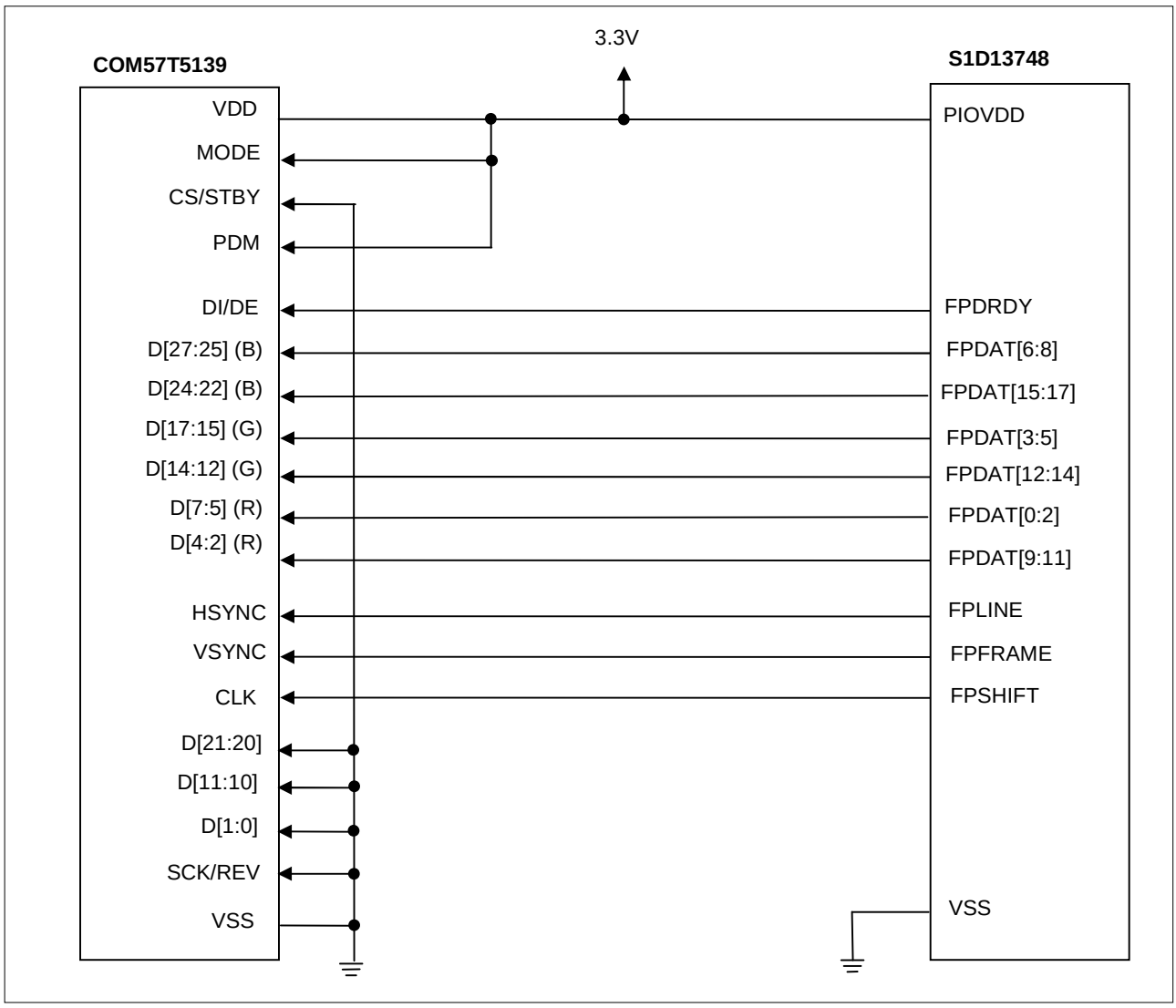

Figure 5-3 Connecting the COM57T5139 to the S1D13748 (18-bit panel mode, MODE = “VDD”)

The following diagram shows an example implementation of the COM57T5139 panel connected to the S1D13748. This example is for the setting of 24-bit panel mode (MODE="VSS") on COM57T5139.

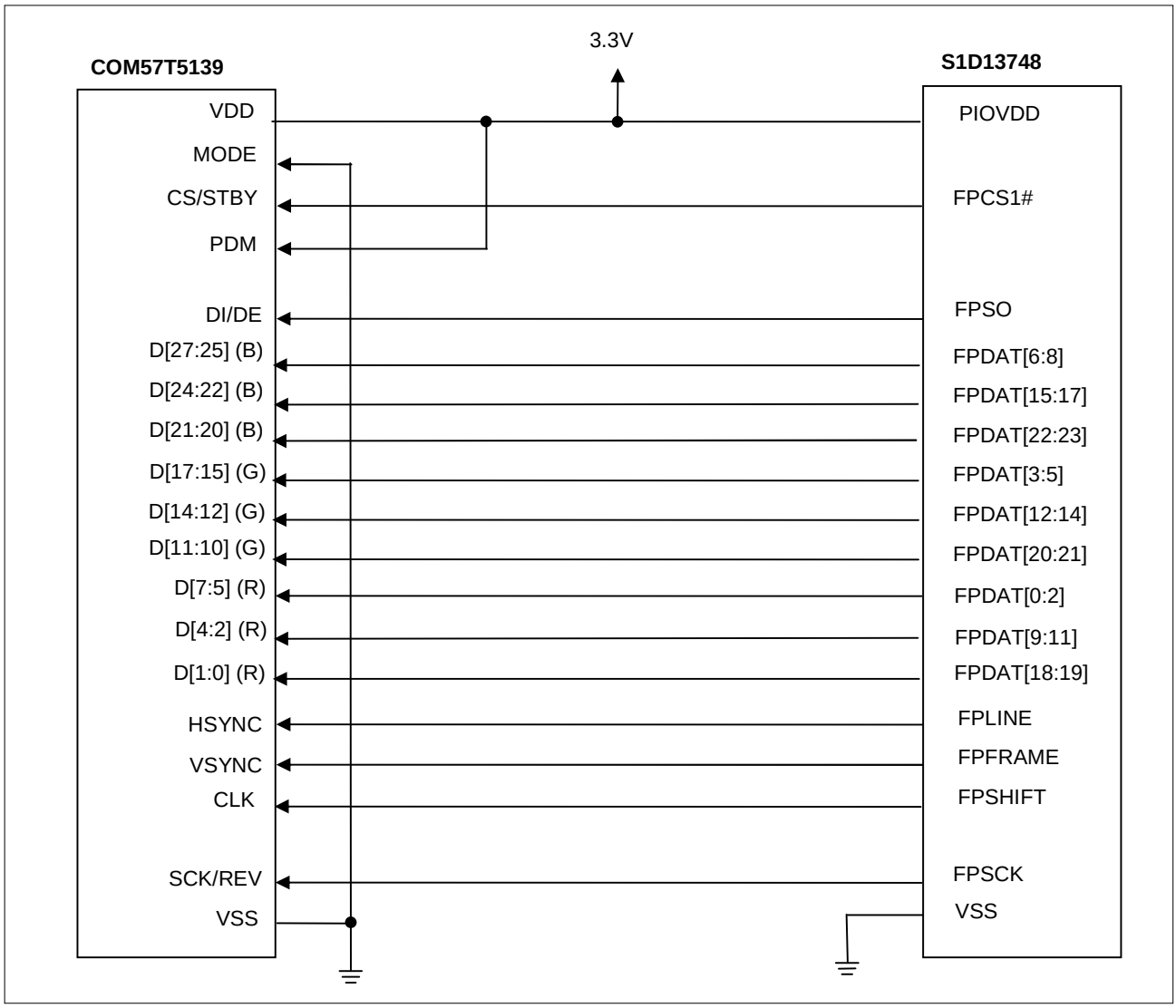

Figure 5-4 Connecting the COM57T5139 to the S1D13748 (24-bit panel mode, MODE = "VSS")

The following table provides a detailed pin listing for the required connections between the COM57T5139 and the S1D13748. This table is for the setting of 18-bit panel mode (MODE="VDD") on COM57T5139. Pin mappings are shown for both S1D13748 package types.

Table 5-4 Connecting the COM57T5139 to the S1D13748 (18-bit Panel Mode, MODE = "VDD")

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
1	VSS	GND	Note	Note	VSS
2	CLK	Dot clock (Capture at the falling edge)	75	J11	FPSHIFT

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
3	VSS	GND	Note	Note	VSS
4	HSYNC	Horizontal synchronous signal (Negative)	77	H10	FPLINE
5	VSYNC	Vertical synchronous signal (Negative)	76	J10	FPFRAME
6	VSS	GND	Note	Note	VSS
7	D20	Connect to VSS	Note	Note	VSS
8	D21	Connect to VSS	Note	Note	VSS
9	D22	BLUE data signal (LSB)	72	J9	FPDAT17
10	D23	BLUE data signal	71	K10	FPDAT16
11	D24	BLUE data signal	70	L10	FPDAT15
12	D25	BLUE data signal	60	K7	FPDAT8
13	D26	BLUE data signal	59	J7	FPDAT7
14	D27	BLUE data signal (MSB)	58	L7	FPDAT6
15	VSS	GND	Note	Note	VSS
16	D10	Connect to VSS	Note	Note	VSS
17	D11	Connect to VSS	Note	Note	VSS
18	D12	GREEN data signal (LSB)	69	H8	FPDAT14
19	D13	GREEN data signal	68	K9	FPDAT13
20	D14	GREEN data signal	64	L9	FPDAT12
21	D15	GREEN data signal	54	L6	FPDAT5
22	D16	GREEN data signal	53	J6	FPDAT4
23	D17	GREEN data signal (MSB)	52	H6	FPDAT3
24	VSS	GND	Note	Note	VSS
25	D00	Connect to VSS	Note	Note	VSS
26	D01	Connect to VSS	Note	Note	VSS
27	D02	RED data signal (LSB)	63	L8	FPDAT11
28	D03	RED data signal	62	J8	FPDAT10
29	D04	RED data signal	61	K8	FPDAT9
30	D05	RED data signal	51	K5	FPDAT2
31	D06	RED data signal	50	L5	FPDAT1
32	D07	RED data signal (MSB)	49	J5	FPDAT0
33	VSS	GND	Note	Note	VSS
34	MODE	Input mode select. Lo: 24bit, Hi: 18bit	19,26,35, 40,46,55, 67,73,83, 87	E8,F4, H7,J4	PIOVDD
35	VDD	Power supply for logic +3.3V	19,26,35, 40,46,55, 67,73,83, 87	E8,F4, H7,J4	PIOVDD
36	VDD	Power supply for logic +3.3V	19,26,35, 40,46,55, 67,73,83, 87	E8,F4, H7,J4	PIOVDD
37	STBY	Standby control signal input (Lo: Normal, Hi: Standby)	Note	Note	VSS
38	DE	Input data enable (Hi-active)	78	G7	FPDRDY

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
39	REV	Vertical and Horizontal reverse control signal input (Lo: Normal, Hi:Reverse)	Note	Note	VSS
40	VSS	GND	Note	Note	VSS
41	VBL	Power supply for back light +12V	—	—	—
42	VBL	Power supply for back light +12V	—	—	—
43	PDM	Back light pulse input. Lo: OFF（0%）, Hi: ON（100%）	19,26,35, 40,46,55, 67,73,83, 87	E8,F4, H7,J4	PIOVDD
44	VSS	GND	Note	Note	VSS
45	VSS	GND	Note	Note	VSS

S1D13748 PIOVDD and COM41T4148 VDD must be configured between +3.0V to +3.6V.

Note
Allocation of VSS pin for each packages are as follows.
QFP: 6, 13, 20, 31, 36, 39, 47, 56, 66, 74, 82, 91, 97, 102, 108, 115, 129, 138, 144
PFBGA: B1, C4, C8, D10, E6, F2, F8, G4, K6, K11

The following table provides a detailed pin listing for the required connections between the COM57T5139 and the S1D13748. This table is for the setting of 24-bit panel mode (MODE="VSS") on COM57T5139. Pin mappings are shown for both S1D13748 package types.

Table 5-5 Connecting the COM57T5139 to the S1D13748 (24-bit Panel Mode, MODE = "VSS")

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
1	VSS	GND	Note	Note	VSS
2	CLK	Dot clock	75	J11	FPSHIFT
3	VSS	GND	Note	Note	VSS
4	HSYNC	Horizontal synchronous signal	77	H10	FPLINE
5	VSYNC	Vertical synchronous signal	76	J10	FPFRAME
6	VSS	GND	Note	Note	VSS
7	D20	BLUE data signal (LSB)	48	H5	FPDAT23
8	D21	BLUE data signal	45	L4	FPDAT22
9	D22	BLUE data signal	72	J9	FPDAT17
10	D23	BLUE data signal	71	K10	FPDAT16
11	D24	BLUE data signal	70	L10	FPDAT15
12	D25	BLUE data signal	60	K7	FPDAT8
13	D26	BLUE data signal	59	J7	FPDAT7
14	D27	BLUE data signal (MSB)	58	L7	FPDAT6
15	VSS	GND	Note	Note	VSS
16	D10	GREEN data signal (LSB)	44	G6	FPDAT21
17	D11	GREEN data signal	43	K4	FPDAT20
18	D12	GREEN data signal	69	H8	FPDAT14

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
19	D13	GREEN data signal	68	K9	FPDAT13
20	D14	GREEN data signal	64	L9	FPDAT12
21	D15	GREEN data signal	54	L6	FPDAT5
22	D16	GREEN data signal	53	J6	FPDAT4
23	D17	GREEN data signal (MSB)	52	H6	FPDAT3
24	VSS	GND	Note	Note	VSS
25	D00	RED data signal (LSB)	42	L3	FPDAT19
26	D01	RED data signal	41	K3	FPDAT18
27	D02	RED data signal	63	L8	FPDAT11
28	D03	RED data signal	62	J8	FPDAT10
29	D04	RED data signal	61	K8	FPDAT9
30	D05	RED data signal	51	K5	FPDAT2
31	D06	RED data signal	50	L5	FPDAT1
32	D07	RED data signal (MSB)	49	J5	FPDAT0
33	VSS	GND	Note	Note	VSS
34	MODE	Input mode select, Lo: 24bit, Hi: 18bit	Note	Note	VSS
35	VDD	Power supply for logic +3.3V	19,26,35, 40,46,55, 67,73,83, 87	E8,F4, H7,J4	PIOVDD
36	VDD	Power supply for logic +3.3V	19,26,35, 40,46,55, 67,73,83, 87	E8,F4, H7,J4	PIOVDD
37	CS	Serial chip select (Lo-active)	80	G9	FPCS1#
38	DI	Serial data input	86	G11	FPSO
39	SCK	Serial clock	84	H11	FPSCK
40	VSS	GND	Note	Note	VSS
41	VBL	Power supply for back light +12V	—	—	—
42	VBL	Power supply for back light +12V	—	—	—
43	PDM	Back light pulse input, Lo:OFF（0%）, Hi:ON（100%）	19,26,35, 40,46,55, 67,73,83, 87	E8,F4, H7,J4	PIOVDD
44	VSS	GND	Note	Note	VSS
45	VSS	GND	Note	Note	VSS

S1D13748 PIOVDD and COM41T4148 VDD must be configured between +3.0V to +3.6V.

Note
Allocation of VSS pin for each packages are as follows.
QFP: 6, 13, 20, 31, 36, 39, 47, 56, 66, 74, 82, 91, 97, 102, 108, 115, 129, 138, 144
PFBGA: B1, C4, C8, D10, E6, F2, F8, G4, K6, K11

5.3 Example Register Settings

In addition to the pin connections, the S1D13513/S1D13748 internal registers must be configured appropriately for the COM57T5139 LCD panel. The following tables provide example settings for each

display controller. However, these values are for reference only and may differ according to each specific implementation.

Also included in the table is an example clock configuration designed to achieve a 50Hz or greater LCD refresh.

Table 5-6 Example Register Settings for the S1D13513

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0800h] LCD Panel Type Select Register	0280h	—
REG[0802h] LCD Horizontal Total Register	01ACh	429
REG[0804h] LCD Horizontal Display Period Register	009Fh	320
REG[0806h] LCD Horizontal Display Period Start Position Register	0029h	42
REG[0808h] LCD Horizontal Pulse Width	000Ah	11
REG[080Ah] LCD Horizontal Pulse Start Position	0000h	0
REG[080Ch] LCD Vertical Total Register	0105h	262
REG[080Eh] LCD Vertical Display Period Resister	00EFh	240
REG[0810h] Vertical Display Period Start Position Register	0006h	6
REG[0812h] LCD Vertical Pulse Width	0002h	3
REG[0814h] LCD Vertical Pulse Start Position	0000h	0
PLL2 output frequency in MHz	—	80
REG[0446h] LCD Clock Control Register	000Bh	12
FPSHIFT in MHz	—	6.67
LCD Refresh in Hz	—	59.3

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13513 register values, see the *S1D13513 Hardware Functional Specification*, document number X78B-A-001-xx.

Table 5-7 Example Serial Output Sequence for the S1D13513

Sequence	Register	Data	Contents
1	0448h	000Eh	LCD serial clock divide 100MHz/15
2	0816h	00A3h	LCD serial 24bit command I/F setting
3	081Ch	0016h	Command
4	081Ch	083Fh	Command
5	081Ch	0671h	Command
6	081Ch	0C00h	Command
7	081Ch	0210h	Command
8	081Ch	0A4Ch	Command
9	081Ch	0618h	Command
10	081Ch	0ED0h	Command
11	081Ch	0100h	Command
12	081Ch	0980h	Command
13	081Ch	0501h	Command
14	081Ch	0D40h	Command
15	081Ch	0300h	Command
16	081Ch	0B00h	Command
17	081Ch	0700h	Command
18	081Ch	0F02h	Command

Table 5-8 Example Register Settings for the S1D13748

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0040h] LCD1 Horizontal Total Register	53	429
REG[0042h] LCD1 Horizontal Display Period Register	159	320
REG[0044h] LCD1 Horizontal Display Period Start Position Register	33	42
REG[0046h] LCD1 Horizontal Pulse Register	10	11
REG[0048h] LCD1 Horizontal Pulse Start Position Register	0	1
REG[004Ah] LCD1 Vertical Total Register	261	262
REG[004Ch] LCD1 Vertical Display Period Resister	239	240
REG[004Eh] LCD1 Vertical Display Period Start Position Register	6	6
REG[0050h] LCD1 Vertical Pulse Register	2	3
REG[0052h] LCD1 Vertical Pulse Start Position Register	0	1
REG[0246h] Main1 Window Image Horizontal Size Register	319	320
REG[0248h] Main1 Window Image Vertical Size Register	279	280
PLL output frequency in MHz	—	54
REG[0030h] LCD Interface Clock Setting Register	0506h	8
FPSHIFT in MHz	—	6.75
LCD Refresh in Hz	—	60.1

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13748 register values, see the *S1D13748 Hardware Functional Specification*, document number X80A-A-001-xx.

Table 5-9 Example Serial Output Sequence for the S1D13748

Sequence	Register	Data	Contents
1	0034h	0016h	Command
2	0034h	083Fh	Command
3	0034h	0671h	Command
4	0034h	0C00h	Command
5	0034h	0210h	Command
6	0034h	0A4Ch	Command
7	0034h	0618h	Command
8	0034h	0ED0h	Command
9	0034h	0100h	Command
10	0034h	0980h	Command
11	0034h	0501h	Command
12	0034h	0D40h	Command
13	0034h	0300h	Command
14	0034h	0B00h	Command
15	0034h	0700h	Command
16	0034h	0F02h	Command

6 Connecting to the Ortustech COM57T5M26

The Ortustech COM57T5M26 TFT panel is compatible with the S1D13513 and S1D13748 display controllers. The following sections will provide connector details, pin mappings, and example register settings for these combinations.

6.1 COM57T5M26 Pin Mapping

The COM57T5M26 TFT panel uses a 33-pin connector with the following pin mapping.

Table 6-1 COM57T5M26 Pin Mapping

Connector Pin#	Pin Name	Pin Description
1	GND	GND
2	CLK	Dot clock (Capture at the falling edge)
3	HSYNC	Horizontal synchronous signal (Negative)
4	VSYNC	Vertical synchronous signal (Negative)
5	GND	GND
6	R0	RED data signal Data 00h displays black. R0: LSB R5: MSB Gamma correction is done inside the driver.
7	R1	
8	R2	
9	R3	
10	R4	
11	R5	
12	GND	GND
13	G0	GREEN data signal Data 00h displays black. G0: LSB G5: MSB Gamma correction is done inside the driver.
14	G1	
15	G2	
16	G3	
17	G4	
18	G5	
19	GND	GND
20	B0	BLUE data signal Data 00h displays black. B0: LSB B5: MSB Gamma correction is done inside the driver.
21	B1	
22	B2	
23	B3	
24	B4	
25	B5	
26	GND	GND
27	ENAB	Input data enable (Hi-active)
28	VDD	Power +3.3V (3.0V ≤ VDD ≤ 3.6V)
29	VDD	Power +3.3V (3.0V ≤ VDD ≤ 3.6V)
30	RL_UD	Horizontally and Vertically Flipped signal Lo: Normal, Hi: Reverse
31	NC1	NC
32	NC2	NC
33	GND	GND

Note

The recommended connector is a 04-6240-033-023-846+ from Kyocera elco.

6.2 Connection Examples

The information in this section provides connection examples for the S1D13513 and S1D13748 display controllers. For the S1D13513 and S1D13748, the display controller is available in two packages. The connection information differs for each package and is listed separately.

In addition to the pin connections for the selected display controller, the COM57T5M26 requires the following power supplies.

VDD +3.3V (3.0V ≤ VDD ≤ 3.6V)

VL +15V (VL ≤ 17V)

For VDD, select a voltage within the supportable range of the Display Controller.

For further details on the COM57T5M26, such as power consumption and absolute maximum ratings, please contact your Ortustech representative.

6.2.1 Connecting the COM57T5M26 to the S1D13513

The following diagram shows an example implementation of the COM57T5M26 panel connected to the S1D13513.

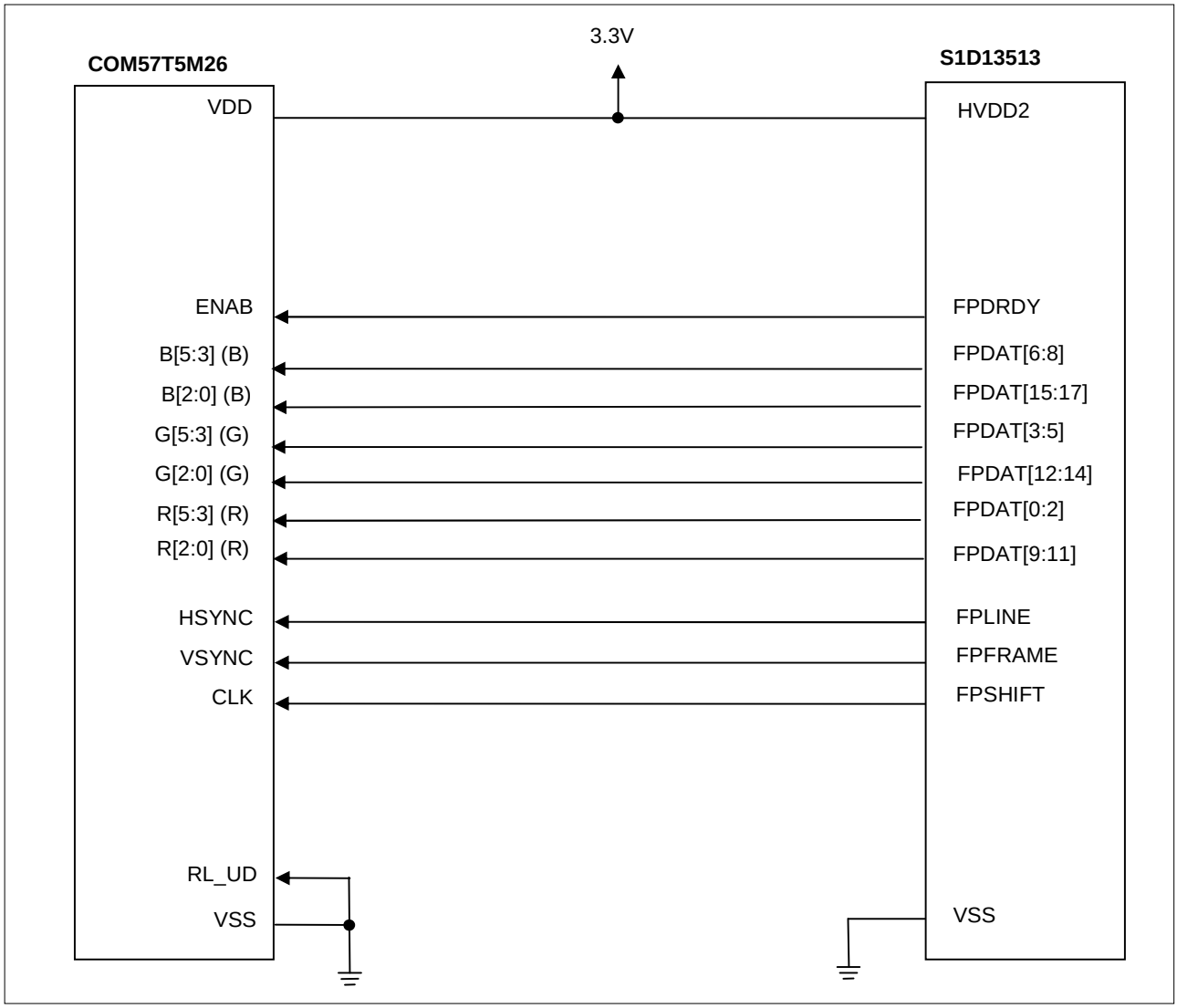

Figure 6-1 Connecting the COM57T5M26 to the S1D13513

The following table provides a detailed pin listing for the required connections between the COM57T5M26 and the S1D13513. Pin mappings are shown for both S1D13513 package types.

Table 6-2 Connecting the COM57T5M26 to the S1D13513

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
1	GND	GND	Note	Note	VSS
2	CLK	Dot clock (Capture at the falling edge)	77	P8	FPSHIFT
3	HSYNC	Horizontal synchronous signal (Negative)	79	R8	FPLINE
4	VSYNC	Vertical synchronous signal (Negative)	78	T8	FPFRAME
5	GND	GND	Note	Note	VSS
6	R0	RED data signal	61	N5	FPDAT11
7	R1	Data 00h displays black.	62	M5	FPDAT10
8	R2	R0: LSB	63	P6	FPDAT9
9	R3	R5: MSB	72	T7	FPDAT2
10	R4	Gamma correction is done inside the driver.	73	N7	FPDAT1
11	R5		74	M7	FPDAT0
12	GND	GND	Note	Note	VSS
13	G0	GREEN data signal	56	R4	FPDAT14
14	G1	Data 00h displays black.	59	T4	FPDAT13
15	G2	G0: LSB	60	T5	FPDAT12
16	G3	G5: MSB	69	L7	FPDAT5
17	G4	Gamma correction is done inside the driver.	70	P7	FPDAT4
18	G5		71	R7	FPDAT3
19	GND	GND	Note	Note	VSS
20	B0	BLUE data signal	53	N4	FPDAT17
21	B1	Data 00h displays black.	54	P4	FPDAT16
22	B2	B0: LSB	55	T2	FPDAT15
23	B3	B5: MSB	64	R6	FPDAT8
24	B4	Gamma correction is done inside the driver.	67	K6	FPDAT7
25	B5		68	M6	FPDAT6
26	GND	GND	Note	Note	VSS
27	ENAB	Input data enable (Hi-active)	78	G7	FPDRDY
28	VDD	Power +3.3V	57,65,75	L5,L8,T6	HVDD2
29	VDD	Power +3.3V	57,65,75	L5,L8,T6	HVDD2
30	RL_UD	Horizontally and Vertically Flipped signal Lo: Normal, Hi: Reverse	Note	Note	VSS
31	NC1	NC	—	—	—
32	NC2	NC	—	—	—
33	GND	GND	Note	Note	VSS

S1D13513 HVDD2 and COM57T5M26 VDD must be configured between +3.0V to +3.6V.

Note

Allocation of VSS pin for each packages are as follows.
QFP: 10, 20, 38, 58, 66, 76, 92, 99, 106, 120, 133, 139, 151, 163, 169, 175, 184, 197
BGA: A1, A16, D4, D8, D13, G7-G10, G13, H7-H10, J1, J7-J10, K2, K7-K10, K13, N3, N6, N9, N13, T1, T16

6.2.2 Connecting the COM57T5M26 to the S1D13748

The following diagram shows an example implementation of the COM57T5M26 panel connected to the S1D13748.

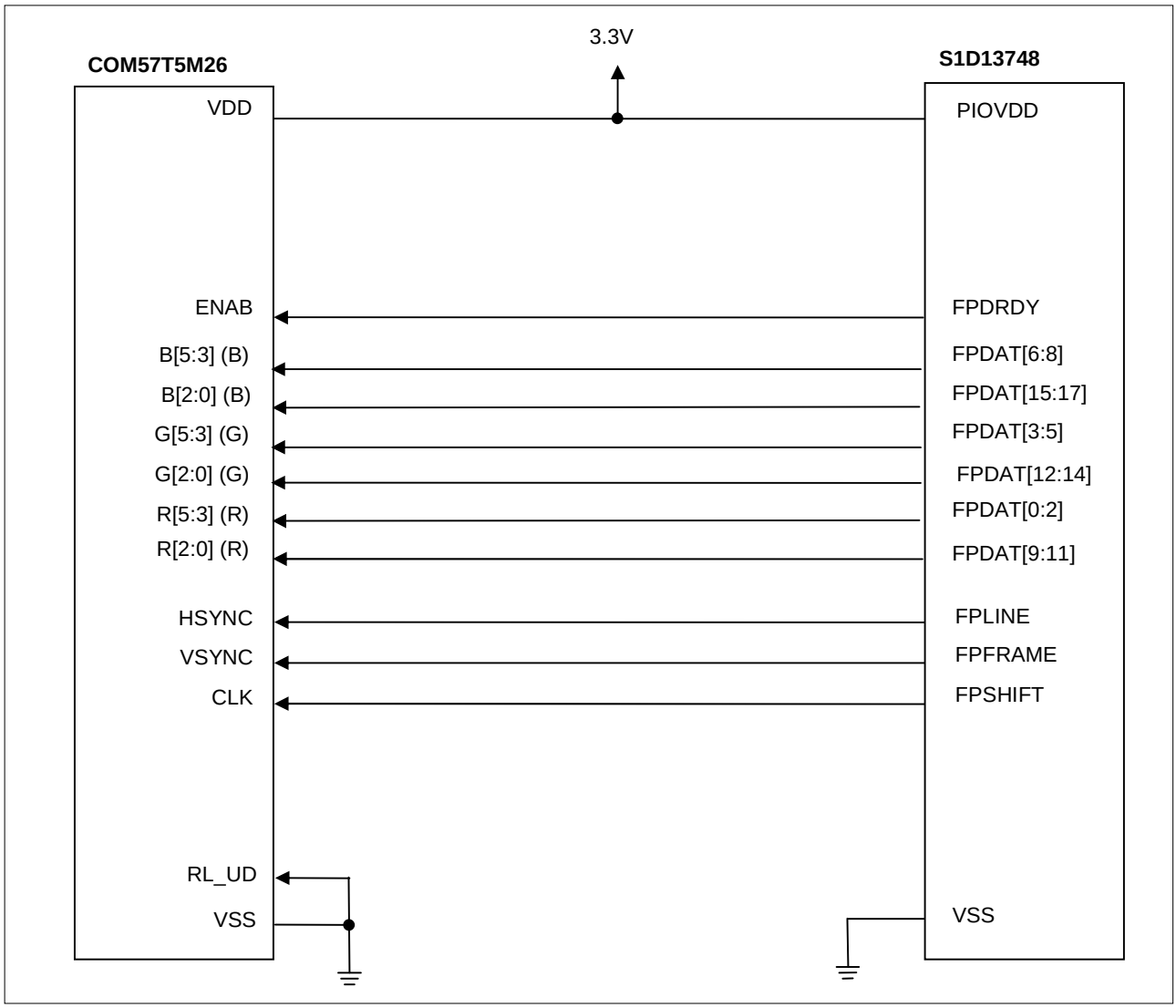

Figure 6-2 Connecting the COM57T5M26 to the S1D13748

The following table provides a detailed pin listing for the required connections between the COM57T5M26 and the S1D13748. Pin mappings are shown for both S1D13748 package types.

Table 6-3 Connecting the COM57T5M26 to the S1D13748

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
1	GND	GND	Note	Note	VSS
2	CLK	Dot clock (Capture at the falling edge)	75	J11	FPSHIFT
3	HSYNC	Horizontal synchronous signal (Negative)	77	H10	FPLINE

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
4	VSYNC	Vertical synchronous signal (Negative)	76	J10	FPFRAME
5	GND	GND	Note	Note	VSS
6	R0	RED data signal Data 00h displays black. R0: LSB R5: MSB Gamma correction is done inside the driver.	63	L8	FPDAT11
7	R1		62	J8	FPDAT10
8	R2		61	K8	FPDAT9
9	R3		51	K5	FPDAT2
10	R4		50	L5	FPDAT1
11	R5		49	J5	FPDAT0
12	GND	GND	Note	Note	VSS
13	G0	GREEN data signal Data 00h displays black. G0: LSB G5: MSB Gamma correction is done inside the driver.	69	H8	FPDAT14
14	G1		68	K9	FPDAT13
15	G2		64	L9	FPDAT12
16	G3		54	L6	FPDAT5
17	G4		53	J6	FPDAT4
18	G5		52	H6	FPDAT3
19	GND	GND	Note	Note	VSS
20	B0	BLUE data signal Data 00h displays black. B0: LSB B5: MSB Gamma correction is done inside the driver.	72	J9	FPDAT17
21	B1		71	K10	FPDAT16
22	B2		70	L10	FPDAT15
23	B3		60	K7	FPDAT8
24	B4		59	J7	FPDAT7
25	B5		58	L7	FPDAT6
26	GND	GND	Note	Note	VSS
27	ENAB	Input data enable (Hi-active)	78	G7	FPDRDY
28	VDD	Power +3.3V	19, 26, 35, 40, 46, 55, 67, 73, 83, 87	E8, F4, H7, J4	PIOVDD
29	VDD	Power +3.3V	19, 26, 35, 40, 46, 55, 67, 73, 83, 87	E8, F4, H7, J4	PIOVDD
30	RL_UD	Horizontally and Vertically Flipped signal Lo: Normal, Hi: Reverse	Note	Note	VSS
31	NC1	NC	—	—	—
32	NC2	NC	—	—	—
33	GND	GND	Note	Note	VSS

S1D13748 PIOVDD and COM57T5M26 VDD must be configured between +3.0V to +3.6V.

Note
Allocation of VSS pin for each packages are as follows.
QFP: 6, 13, 20, 31, 36, 39, 47, 56, 66, 74, 82, 91, 97, 102, 108, 115, 129, 138, 144
PFBGA: B1, C4, C8, D10, E6, F2, F8, G4, K6, K11

6.3 Example Register Settings

In addition to the pin connections, the S1D13513/S1D13748 internal registers must be configured appropriately for the COM57T5M26 LCD panel. The following tables provide example settings for each display controller. However, these values are for reference only and may differ according to each specific implementation.

Also included in the table is an example clock configuration designed to achieve a 50Hz or greater LCD refresh.

Table 6-4 Example Register Settings for the S1D13513

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0800h] LCD Panel Type Select Register	0280h	—
REG[0802h] LCD Horizontal Total Register	01ACh	429
REG[0804h] LCD Horizontal Display Period Register	009Fh	320
REG[0806h] LCD Horizontal Display Period Start Position Register	0029h	42
REG[0808h] LCD Horizontal Pulse Width	000Ah	11
REG[080Ah] LCD Horizontal Pulse Start Position	0000h	0
REG[080Ch] LCD Vertical Total Register	0105h	262
REG[080Eh] LCD Vertical Display Period Resister	00EFh	240
REG[0810h] LCD Vertical Display Period Start Position Register	0006h	6
REG[0812h] LCD Vertical Pulse Width	0002h	3
REG[0814h] LCD Vertical Pulse Start Position	0000h	0
PLL2 output frequency in MHz	—	80
REG[0446h] LCD Clock Control Register	000Bh	12
FPSHIFT in MHz	—	6.67
LCD Refresh in Hz	—	59.3

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13513 register values, see the *S1D13513 Hardware Functional Specification*, document number X78B-A-001-xx.

Table 6-5 Example Register Settings for the S1D13748

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0040h] LCD1 Horizontal Total Register	53	429
REG[0042h] LCD1 Horizontal Display Period Register	159	320
REG[0044h] LCD1 Horizontal Display Period Start Position Register	33	42
REG[0046h] LCD1 Horizontal Pulse Register	10	11
REG[0048h] LCD1 Horizontal Pulse Start Position Register	0	1
REG[004Ah] LCD1 Vertical Total Register	261	262
REG[004Ch] LCD1 Vertical Display Period Resister	239	240
REG[004Eh] LCD1 Vertical Display Period Start Position Register	6	6
REG[0050h] LCD1 Vertical Pulse Register	2	3
REG[0052h] LCD1 Vertical Pulse Start Position Register	0	1
REG[0246h] Main1 Window Image Horizontal Size Register	319	320
REG[0248h] Main1 Window Image Vertical Size Register	279	280
PLL output frequency in MHz	—	54
REG[0030h] LCD Interface Clock Setting Register	0506h	8
FPSHIFT in MHz	—	6.75
LCD Refresh in Hz	—	60.1

Note
Parameter values are determined using a formula based on the register setting. For details on configuring

the S1D13748 register values, see the *S1D13748 Hardware Functional Specification*, document number X80A-A-001-xx.

7 Connecting to the Ortustech COM57T5M71

The Ortustech COM57T5M71 TFT panel is compatible with the S1D13513 and S1D13748 display controllers. The following sections will provide connector details, pin mappings, and example register settings for these combinations.

7.1 COM57T5M71 Pin Mapping

The COM57T5M71 TFT panel uses a 33-pin connector with the following pin mapping.

Table 7-1 COM57T5M71 Pin Mapping

Connector Pin#	Pin Name	Pin Description
1	GND	GND
2	CLK	Dot clock (Capture at the falling edge)
3	HSYNC	Horizontal synchronous signal (Negative)
4	VSYNC	Vertical synchronous signal (Negative)
5	GND	GND
6	GND	GND
7	GND	GND
8	GND	GND
9	GND	GND
10	GND	GND
11	GND	GND
12	GND	GND
13	D0	Display data signal Data 00h displays black. D0: LSB D5: MSB Gamma correction is done inside the driver.
14	D1	
15	D2	
16	D3	
17	D4	
18	D5	
19	GND	GND
20	GND	GND
21	GND	GND
22	GND	GND
23	GND	GND
24	GND	GND
25	GND	GND
26	GND	GND
27	ENAB	Input data enable (Hi-active)
28	VDD	Power +3.3V (3.0V ≤ VDD ≤ 3.6V)
29	VDD	Power +3.3V (3.0V ≤ VDD ≤ 3.6V)
30	RL_UD	Horizontally and Vertically Flipped signal Lo: Normal, Hi: Reverse
31	NC1	NC
32	NC2	NC
33	GND	GND

Note

The recommended connector is a 04-6240-033-023-846+ from Kyocera elco.

7.2 Connection Examples

The information in this section provides connection examples for the S1D13513 and S1D13748 display controllers. For the S1D13513 and S1D13748, the display controller is available in two packages. The connection information differs for each package and is listed separately.

In addition to the pin connections for the selected display controller, the COM57T5M71 requires the following power supplies.

VDD +3.3V (3.0V ≤ VDD ≤ 3.6V)

VL +5.6V (VBL ≤ 6.4V)

For VDD, select a voltage within the supportable range of the Display Controller.

For further details on the COM57T5M71, such as power consumption and absolute maximum ratings, please contact your Ortustech representative.

7.2.1 Connecting the COM57T5M71 to the S1D13513

The following diagram shows an example implementation of the COM57T5M71 panel connected to the S1D13513.

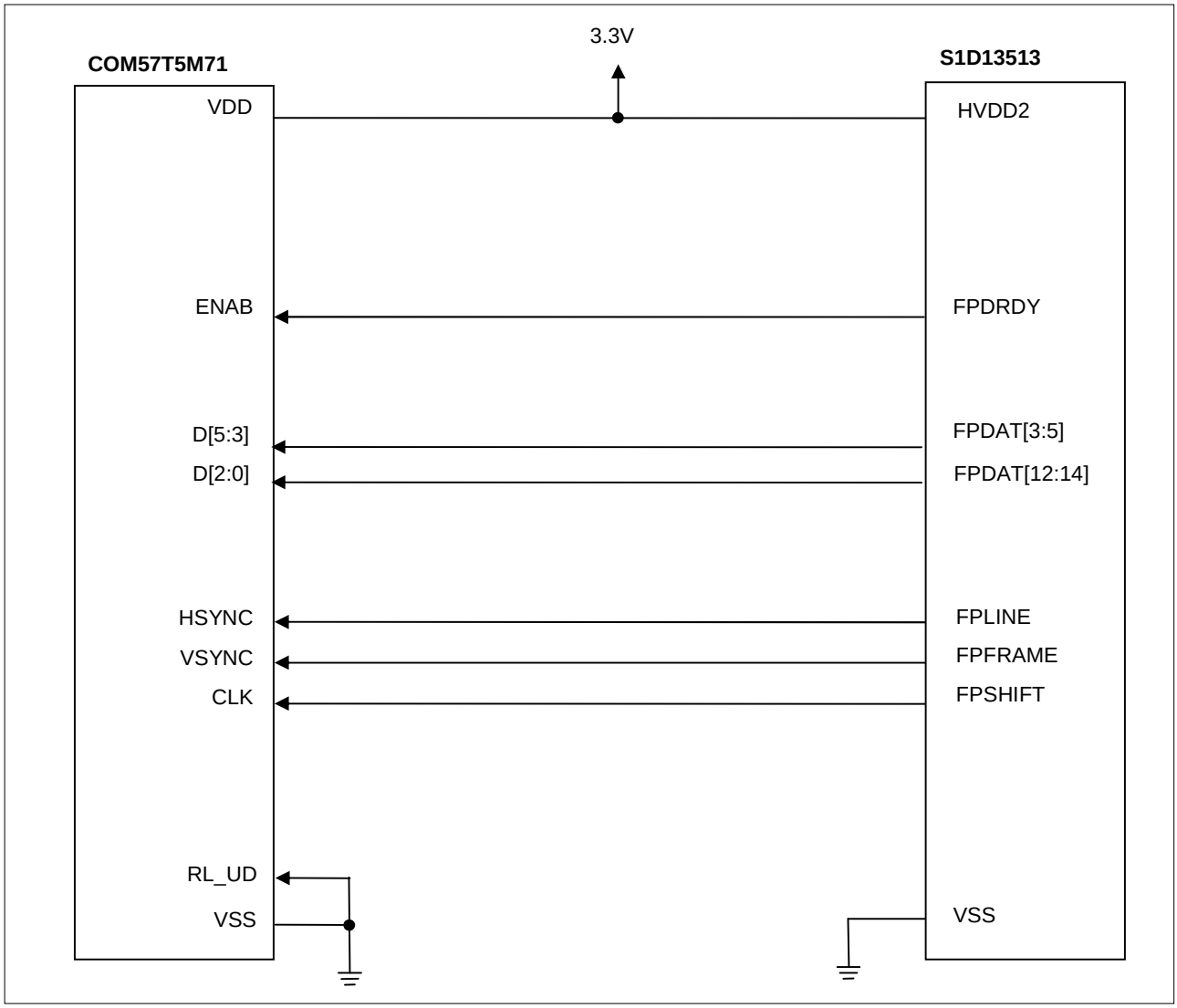

Figure 7-1 Connecting the COM57T5M71 to the S1D13513

The following table provides a detailed pin listing for the required connections between the COM57T5M71 and the S1D13513. Pin mappings are shown for both S1D13513 package types.

Table 7-2 Connecting the COM57T5M71 to the S1D13513

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
1	GND	GND	Note	Note	VSS
2	CLK	Dot clock (Capture at the falling edge)	77	P8	FPSHIFT
3	HSYNC	Horizontal synchronous signal (Negative)	79	R8	FPLINE
4	VSYNC	Vertical synchronous signal (Negative)	78	T8	FPFRAME
5	GND	GND	Note	Note	VSS
6	GND	GND	Note	Note	VSS
7	GND	GND	Note	Note	VSS
8	GND	GND	Note	Note	VSS
9	GND	GND	Note	Note	VSS
10	GND	GND	Note	Note	VSS
11	GND	GND	Note	Note	VSS
12	GND	GND	Note	Note	VSS
13	D0	Display data signal Data 00h displays black. D0: LSB D5: MSB Gamma correction is done inside the driver.	56	R4	FPDAT14
14	D1		59	T4	FPDAT13
15	D2		60	T5	FPDAT12
16	D3		69	L7	FPDAT5
17	D4		70	P7	FPDAT4
18	D5		71	R7	FPDAT3
19	GND	GND	Note	Note	VSS
20	GND	GND	Note	Note	VSS
21	GND	GND	Note	Note	VSS
22	GND	GND	Note	Note	VSS
23	GND	GND	Note	Note	VSS
24	GND	GND	Note	Note	VSS
25	GND	GND	Note	Note	VSS
26	GND	GND	Note	Note	VSS
27	ENAB	Input data enable (Hi-active)	78	G7	FPDRDY
28	VDD	Power +3.3V	57,65,75	L5,L8,T6	HVDD2
29	VDD	Power +3.3V	57,65,75	L5,L8,T6	HVDD2
30	RL_UD	Horizontally and Vertically Flipped signal Lo: Normal, Hi: Reverse	Note	Note	VSS
31	NC1	NC	—	—	—
32	NC2	NC	—	—	—
33	GND	GND	Note	Note	VSS

S1D13513 HVDD2 and COM57T5M71 VDD must be configured between +3.0V to +3.6V.

Note

Allocation of VSS pin for each packages are as follows.
QFP: 10, 20, 38, 58, 66, 76, 92, 99, 106, 120, 133, 139, 151, 163, 169, 175, 184, 197
BGA: A1, A16, D4, D8, D13, G7-G10, G13, H7-H10, J1, J7-J10, K2, K7-K10, K13, N3, N6, N9, N13, T1, T16

7.2.2 Connecting the COM57T5M71 to the S1D13748

The following diagram shows an example implementation of the COM57T5M71 panel connected to the S1D13748.

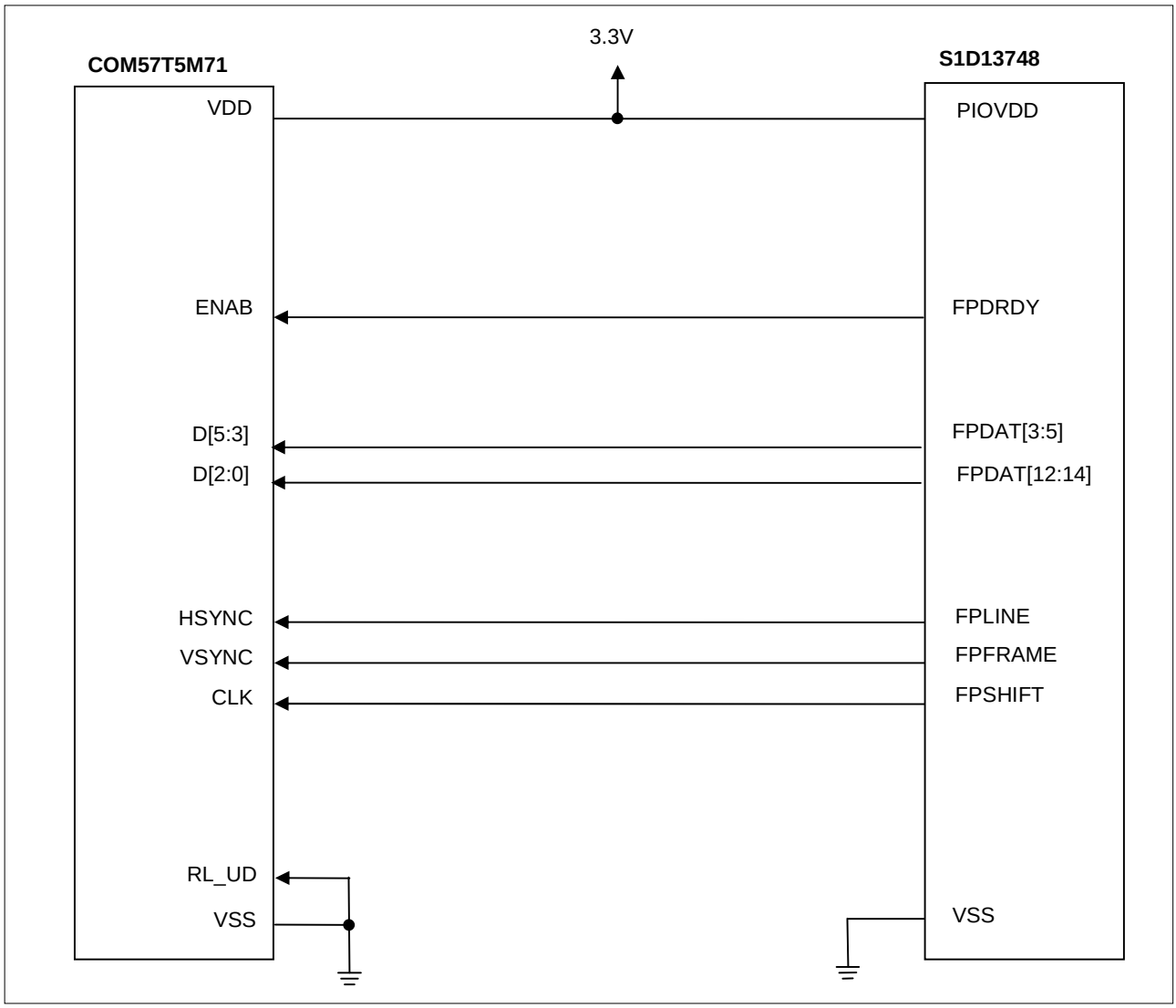

Figure 7-2 Connecting the COM57T5M71 to the S1D13748

The following table provides a detailed pin listing for the required connections between the COM57T5M71 and the S1D13748. Pin mappings are shown for both S1D13748 package types.

Table 7-3 Connecting the COM57T5M71 to the S1D13748

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
1	GND	GND	Note	Note	VSS
2	CLK	Dot clock (Capture at the falling edge)	75	J11	FPSHIFT
3	HSYNC	Horizontal synchronous signal (Negative)	77	H10	FPLINE

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
4	VSYNC	Vertical synchronous signal (Negative)	76	J10	FPFRAME
5	GND	GND	Note	Note	VSS
6	GND	GND	Note	Note	VSS
7	GND	GND	Note	Note	VSS
8	GND	GND	Note	Note	VSS
9	GND	GND	Note	Note	VSS
10	GND	GND	Note	Note	VSS
11	GND	GND	Note	Note	VSS
12	GND	GND	Note	Note	VSS
13	G0	Display data signal Data 00h displays black. D0: LSB D5: MSB Gamma correction is done inside the driver.	69	H8	FPDAT14
14	G1		68	K9	FPDAT13
15	G2		64	L9	FPDAT12
16	G3		54	L6	FPDAT5
17	G4		53	J6	FPDAT4
18	G5		52	H6	FPDAT3
19	GND	GND	Note	Note	VSS
20	GND	GND	Note	Note	VSS
21	GND	GND	Note	Note	VSS
22	GND	GND	Note	Note	VSS
23	GND	GND	Note	Note	VSS
24	GND	GND	Note	Note	VSS
25	GND	GND	Note	Note	VSS
26	GND	GND	Note	Note	VSS
27	ENAB	Input data enable (Hi-active)	78	G7	FPDRDY
28	VDD	Power +3.3V	19, 26, 35, 40, 46, 55, 67, 73, 83, 87	E8, F4, H7, J4	PIOVDD
29	VDD	Power +3.3V	19, 26, 35, 40, 46, 55, 67, 73, 83, 87	E8, F4, H7, J4	PIOVDD
30	RL_UD	Horizontally and Vertically Flipped signal Lo: Normal, Hi: Reverse	Note	Note	VSS
31	NC1	NC	—	—	—
32	NC2	NC	—	—	—
33	GND	GND	Note	Note	VSS

S1D13748 PIOVDD and COM57T5M71 VDD must be configured between +3.0V to +3.6V.

Note
Allocation of VSS pin for each packages are as follows.
QFP: 6, 13, 20, 31, 36, 39, 47, 56, 66, 74, 82, 91, 97, 102, 108, 115, 129, 138, 144
PFBGA: B1, C4, C8, D10, E6, F2, F8, G4, K6, K11

7.3 Example Register Settings

In addition to the pin connections, the S1D13513/S1D13748 internal registers must be configured appropriately for the COM57T5M71 LCD panel. The following tables provide example settings for each display controller. However, these values are for reference only and may differ according to each specific implementation.

Also included in the table is an example clock configuration designed to achieve a 50Hz or greater LCD refresh.

Table 7-4 Example Register Settings for the S1D13513

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0800h] LCD Panel Type Select Register	0280h	—
REG[0802h] LCD Horizontal Total Register	01ACh	429
REG[0804h] LCD Horizontal Display Period Register	009Fh	320
REG[0806h] LCD Horizontal Display Period Start Position Register	0029h	42
REG[0808h] LCD Horizontal Pulse Width	000Ah	11
REG[080Ah] LCD Horizontal Pulse Start Position	0000h	0
REG[080Ch] LCD Vertical Total Register	0105h	262
REG[080Eh] LCD Vertical Display Period Resister	00EFh	240
REG[0810h] LCD Vertical Display Period Start Position Register	0006h	6
REG[0812h] LCD Vertical Pulse Width	0002h	3
REG[0814h] LCD Vertical Pulse Start Position	0000h	0
PLL2 output frequency in MHz	—	80
REG[0446h] LCD Clock Control Register	000Bh	12
FPSHIFT in MHz	—	6.67
LCD Refresh in Hz	—	59.3

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13513 register values, see the *S1D13513 Hardware Functional Specification*, document number X78B-A-001-xx.

Table 7-5 Example Register Settings for the S1D13748

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0040h] LCD1 Horizontal Total Register	53	429
REG[0042h] LCD1 Horizontal Display Period Register	159	320
REG[0044h] LCD1 Horizontal Display Period Start Position Register	33	42
REG[0046h] LCD1 Horizontal Pulse Register	10	11
REG[0048h] LCD1 Horizontal Pulse Start Position Register	0	1
REG[004Ah] LCD1 Vertical Total Register	261	262
REG[004Ch] LCD1 Vertical Display Period Resister	239	240
REG[004Eh] LCD1 Vertical Display Period Start Position Register	6	6
REG[0050h] LCD1 Vertical Pulse Register	2	3
REG[0052h] LCD1 Vertical Pulse Start Position Register	0	1
REG[0246h] Main1 Window Image Horizontal Size Register	319	320
REG[0248h] Main1 Window Image Vertical Size Register	279	280
PLL output frequency in MHz	—	54
REG[0030h] LCD Interface Clock Setting Register	0506h	8
FPSHIFT in MHz	—	6.75
LCD Refresh in Hz	—	60.1

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13748 register values, see the *S1D13748 Hardware Functional Specification*, document number X80A-A-001-xx.

8 Connecting to the Ortustech COM57T5140

The Ortustech COM57T5140 TFT panel is compatible with the S1D13A05 display controller. The following sections will provide connector details, pin mappings, and example register settings for these combinations.

8.1 COM57T5140 Pin Mapping

The COM57T5140 TFT panel uses a 61-pin connector with the following pin mapping.

Table 8-1 COM57T5140 Pin Mapping (LCD Module)

Connector Pin#	Pin Name	Pin Description
1	NC	OPEN
2	NC	OPEN
3	NC	OPEN
4	NC	OPEN
5	VGL	Gate Driver Drive Negative Power
6	C5M	Charge Pump capacitor
7	C5P	Charge Pump capacitor
8	VGH	Gate Driver Drive Positive Power
9	VVCOM	Output for COMOUT
10	C4P	Charge Pump capacitor
11	C4M	Charge Pump capacitor
12	C3P	Charge Pump capacitor
13	C3M	Charge Pump capacitor
14	VSS	GND
15	VSS	GND
16	VDD2	Internal Power
17	COMOUT	Clock Out
18	VDD	Power +3.3V (3.0V ≤ VDD ≤ 3.6V)
19	C2P	Charge Pump capacitor
20	C2M	Charge Pump capacitor
21	C1M	Charge Pump capacitor
22	C1P	Charge Pump capacitor
23	VSREF	Internal DAC Ref Voltage
24	COMDC	DC Output
25	RVDD	Internal Power
26	POCB	Power On Clear Input
27	MODE	Input mode select, Lo: 24bit, Hi: 18bit
28	VSS	GND
29	VSS	GND
30	CLK	Clock In (Capture at the falling edge)
31	HSYNC	Horizontal synchronous signal (Negative)

Connector Pin#	Pin Name	Pin Description
32	VSYNC	Vertical synchronous signal (Negative)
33	SCK/REV	24bit mode: Serial clock 18bit mode: Vertical and Horizontal reverse control signal input (Lo: Normal, Hi: Reverse)
34	DI/DE	24bit mode: Serial data input 18bit mode: DATA ENABLE (Hi-active)
35	CS/STBY	24bit mode: Serial chip select (Lo-active) 18bit mode: Standby control signal input (Lo: Normal, Hi: Standby)
36	BLON	24bit mode: Signal for external backlight control circuit. 18bit mode: Open
37	D00	24bit mode: RED data signal (LSB) 18bit mode: Connect to VSS
38	D01	24bit mode: RED data signal 18bit mode: Connect to VSS
39	D02	24bit mode: RED data signal 18bit mode: RED data signal (LSB)
40	D03	RED data signal
41	D04	RED data signal
42	D05	RED data signal
43	D06	RED data signal
44	D07	RED data signal (MSB)
45	D10	24bit mode: GREEN data signal (LSB) 18bit mode: Connect to VSS
46	D11	24bit mode: GREEN data signal 18bit mode: Connect to VSS
47	D12	24bit mode: GREEN data signal 18bit mode: GREEN data signal (LSB)
48	D13	GREEN data signal
49	D14	GREEN data signal
50	D15	GREEN data signal
51	D16	GREEN data signal
52	D17	GREEN data signal (MSB)
53	D20	24bit mode: BLUE data signal (LSB) 18bit mode: Connect to VSS
54	D21	24bit mode: BLUE data signal 18bit mode: Connect to VSS
55	D22	24bit mode: BLUE data signal 18bit mode: BLUE data signal (LSB)
56	D23	BLUE data signal
57	D24	BLUE data signal
58	D25	BLUE data signal
59	D26	BLUE data signal
60	D27	BLUE data signal (MSB)
61	VCOM	Common driver signal

Note

The recommended connector is a FH26-61S-0.3SHW(05) from Hirose Electric Co., Ltd.

Table 8-2 COM57T5140 Pin Mapping (Backlight Module)

Connector Pin#	Pin Name	Pin Description
1	BLH1	LED driver power 1 (anode side)
2	BLH2	LED driver power 2 (anode side)
3	BLL2	LED driver power 2 (cathode side)
4	BLL1	LED driver power 1 (cathode side)

Note
The recommended connector is a 04 6277 004 001 883+ from Kyocera elco.

8.2 Connection Examples

The information in this section provides connection examples for the S1D13A05 display controller. For the S1D13A05, the display controller is available in two packages. The connection information differs for each package and is listed separately.

In addition to the pin connections for the selected display controller, the COM57T5140 requires the following power supplies.

VDD +3.3V (3.0V ≤ VDD ≤ 3.6V)

VL +27V (VL ≤ 29.7V)

For VDD, select a voltage within the supportable range of the Display Controller.

For further details on the COM57T5140, such as power consumption and absolute maximum ratings, please contact your Ortustech representative.

8.2.1 Connecting the COM57T5140 to the S1D13A05

The following diagram shows an example implementation of the COM57T5140 panel connected to the S1D13A05. This example is for the setting of 18-bit panel mode (MODE="VDD") on COM57T5140

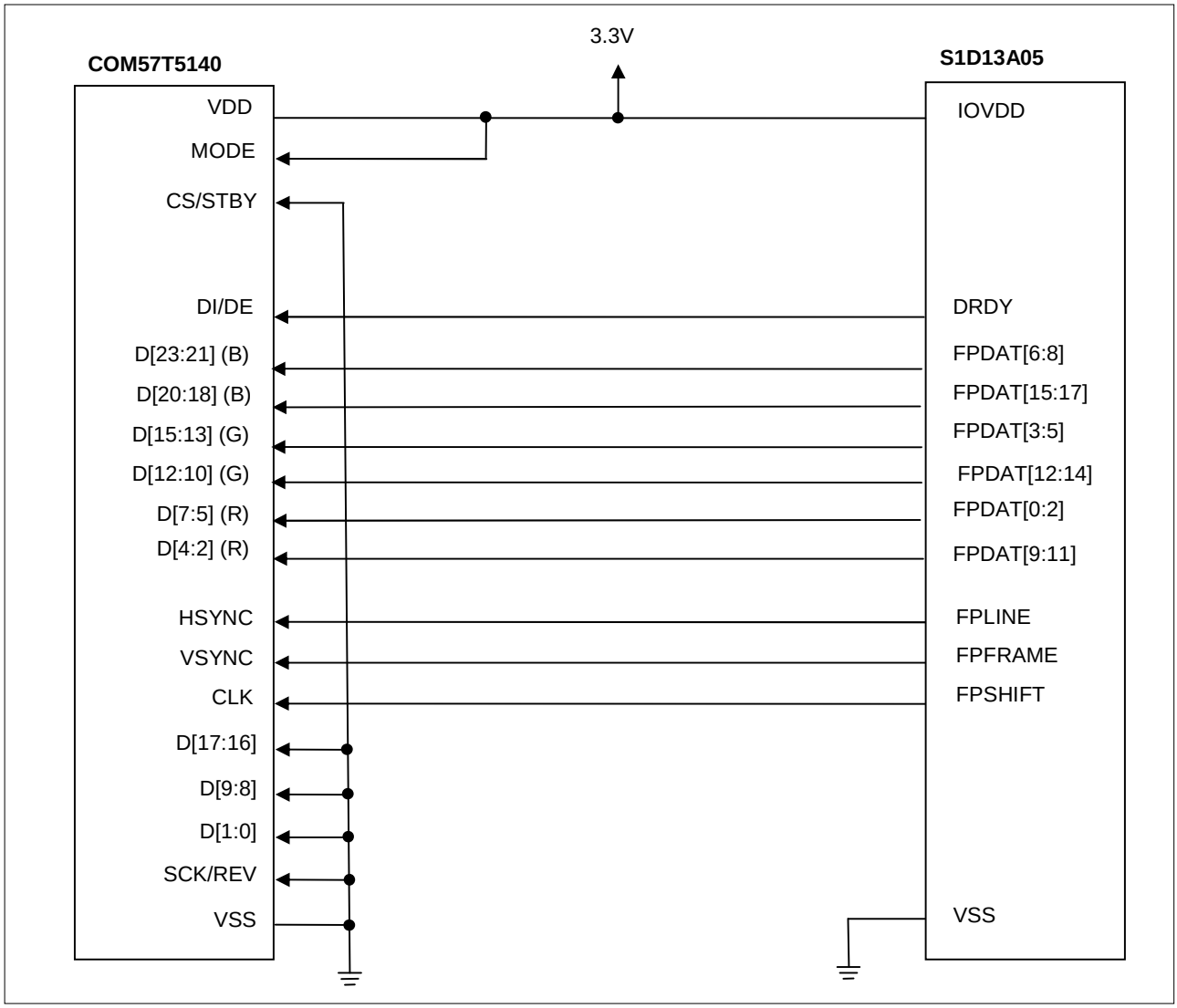

Figure 8-1 Connecting the COM57T5140 to the S1D13A05 (18-bit Panel Mode, MODE = "VDD")

The following table provides a detailed pin listing for the required connections between the COM57T5140 and the S1D13A05. This table is for the setting of 18-bit panel mode (MODE="VDD") on COM57T5140. Pin mappings are shown for both S1D13A05 package types.

Table 8-3 Connecting the COM57T5140 to the S1D13A05 (18-bit Panel Mode, MODE = "VDD")

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13A05 QFP Pin#	S1D13A05 PFBGA Ball#	S1D13A05 Pin Name
1	NC	OPEN	—	—	—
2	NC	OPEN	—	—	—
3	NC	OPEN	—	—	—
4	NC	OPEN	—	—	—
5	VGL	Gate Driver Drive Negative Power	—	—	—
6	C5M	Charge Pump capacitor	—	—	—
7	C5P	Charge Pump capacitor	—	—	—
8	VGH	Gate Driver Drive Positive Power	—	—	—
9	VVCOM	Output for COMOUT	—	—	—
10	C4P	Charge Pump capacitor	—	—	—
11	C4M	Charge Pump capacitor	—	—	—
12	C3P	Charge Pump capacitor	—	—	—
13	C3M	Charge Pump capacitor	—	—	—
14	VSS	GND	Note	Note	VSS
15	VSS	GND	Note	Note	VSS
16	VDD2	Internal Power	—	—	—
17	COMOUT	Clock Out	—	—	—
18	VDD	Power +3.3V			
19	C2P	Charge Pump capacitor	—	—	—
20	C2M	Charge Pump capacitor	—	—	—
21	C1M	Charge Pump capacitor	—	—	—
22	C1P	Charge Pump capacitor	—	—	—
23	VSREF	Internal DAC Ref Voltage	—	—	—
24	COMDC	DC Output	—	—	—
25	RVDD	Internal Power	—	—	—
26	POCB	Power On Clear Input			
27	MODE	Input mode select, Lo: 24bit Hi: 18bit	Note	Note	VSS
28	VSS	GND	Note	Note	VSS
29	VSS	GND	Note	Note	VSS
30	CLK	Clock In (Capture at the falling edge)	43	H10	FPSHIFT
31	HSYNC	Horizontal synchronous signal (Negative)	42	H9	FPLINE
32	VSYNC	Vertical synchronous signal (Negative)	40	J9	FPFRAME
33	SCK/REV	24bit mode: Serial clock 18bit mode: Vertical and Horizontal reverse control signal input (Lo: Normal, Hi: Reverse)	Note	Note	VSS
34	DI/DE	24bit mode: Serial data input 18bit mode: DATA ENABLE (Hi-active)	34	K9	DRDY

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13A05 QFP Pin#	S1D13A05 PFBGA Ball#	S1D13A05 Pin Name
35	CS/STBY	24bit mode: Serial chip select (Lo-active) 18bit mode: Standby control signal input (Lo: Normal, Hi: Standby)	Note	Note	VSS
36	BLON	24bit mode: Signal for external backlight control circuit. 18bit mode: Open	—	—	—
37	D00	24bit mode: RED data signal (LSB) 18bit mode: Connect to VSS	Note	Note	VSS
38	D01	24bit mode: RED data signal 18bit mode: Connect to VSS	Note	Note	VSS
39	D02	24bit mode: RED data signal 18bit mode: RED data signal (LSB)	55	E10	FPDAT11
40	D03	RED data signal	56	E11	FPDAT10
41	D04	RED data signal	57	E8	FPDAT9
42	D05	RED data signal	46	G9	FPDAT2
43	D06	RED data signal	45	G8	FPDAT1
44	D07	RED data signal (MSB)	44	H11	FPDAT0
45	D10	24bit mode: GREEN data signal (LSB) 18bit mode: Connect to VSS	Note	Note	VSS
46	D11	24bit mode: GREEN data signal 18bit mode: Connect to VSS	Note	Note	VSS
47	D12	24bit mode: GREEN data signal 18bit mode: GREEN data signal (LSB)	60	D11	FPDAT14
48	D13	GREEN data signal	72	D8	FPDAT13
49	D14	GREEN data signal	54	E9	FPDAT12
50	D15	GREEN data signal	29	G7	FPDAT5
51	D16	GREEN data signal	48	G11	FPDAT4
52	D17	GREEN data signal (MSB)	47	G10	FPDAT3
53	D20	24bit mode: BLUE data signal (LSB) 18bit mode: Connect to VSS	Note	Note	VSS
54	D21	24bit mode: BLUE data signal 18bit mode: Connect to VSS	Note	Note	VSS
55	D22	24bit mode: BLUE data signal 18bit mode: BLUE data signal (LSB)	63	C10	FPDAT17
56	D23	BLUE data signal	61	D9	FPDAT16
57	D24	BLUE data signal	59	D10	FPDAT15
58	D25	BLUE data signal	53	F7	FPDAT8
59	D26	BLUE data signal	51	F10	FPDAT7
60	D27	BLUE data signal (MSB)	49	F8	FPDAT6
61	VCOM	Common driver signal	—	—	—

Note

Allocation of VSS pin for each packages are as follows.
QFP: 1, 13, 35, 50, 65, 101, 114
BGA: B2, F2, K2, G5, F9, B10, K10

8.3 Example Register Settings

In addition to the pin connections, the S1D13A05 internal registers must be configured appropriately for the COM57T5140 LCD panel. The following tables provide example settings for S1D13A05 display controller. However, these values are for reference only and may differ according to each specific implementation.

Also included in the table is an example clock configuration designed to achieve a 60Hz or greater LCD refresh.

Table 8-4 Example Register Settings for the S1D13A05

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[000Ch] Panel Type & MOD Rate Register	00000061h	—
REG[0020h] Horizontal Total Register	(432/8-1)	432
REG[0024h] Horizontal Display Period Register	(320/8-1)	320
REG[0028h] Horizontal Display Period Start Position Register	(42-5)	42
REG[002Ch] FPLINE Register	00070000h	Pulse Width 8 Start Position 1
REG[0030h] Vertical Total Register	261	262
REG[0034h] Vertical Display Period Resister	239	240
REG[0038h] Vertical Display Period Start Position Register	6	6
REG[003Ch] FPFRAME Register	00020000h	Pulse Width 3 Start Position 0
CLKI2 frequency in MHz	—	27
REG[0008h] Pixel Clock Configuration Register	00000032h	CLKI to FPSHIFT ratio 4
FPSHIFT in MHz	—	6.75
LCD Refresh in Hz	—	59.6

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13A05 register values, see the *S1D13A05 Hardware Functional Specification*, document number X40A-A-001-xx.

9 Connecting to the Ortustech COM37H3M77

The Ortustech COM37H3M77 TFT panel is compatible with the S1D13513, S1D13517 and S1D13781 display controllers. The following sections will provide connector details, pin mappings, and example register settings for these combinations.

9.1 COM37H3M77Pin Mapping

The COM37H3M77 TFT panel uses a 39-pin connector with the following pin mapping.

Table 9-1 COM37H3M77Pin Mapping

Connector Pin#	Pin Name	Pin Description
1	VSS	GND
2	VSS	GND
3	VDD	Power +3.0V (2.7V ≤ VDD ≤ 3.6V)
4	VDD	Power +3.0V (2.7V ≤ VDD ≤ 3.6V)
5	MODE	Input mode select, Lo: QVGA mode, Hi: VGA mode (Note: Mode switching is not valid during Power ON)
6	RESETB	Power on clear input (Lo-active). For valid reset, a 1ms delay is required after VDD power on (90% of the peak) to the rising edge of the POCB.
7	HSYNC	Horizontal synchronous signal (Negative)
8	VSYNC	Vertical synchronous signal (Negative)
9	CLK	Dot clock (Capture at the falling edge)
10	VSS	GND
11	D00	BLUE data signal (LSB)
12	D01	BLUE data signal
13	D02	BLUE data signal
14	D03	BLUE data signal
15	D04	BLUE data signal
16	D05	BLUE data signal (MSB)
17	D10	GREEN data signal (LSB)
18	D11	GREEN data signal
19	D12	GREEN data signal
20	D13	GREEN data signal
21	D14	GREEN data signal
22	D15	GREEN data signal (MSB)
23	D20	RED data signal (LSB)
24	D21	RED data signal
25	D22	RED data signal
26	D23	RED data signal
27	D24	RED data signal
28	D25	RED data signal (MSB)
29	VSS	GND
30	DE	Input data enable (Hi-active)

Connector Pin#	Pin Name	Pin Description
31	STBYB	Standby control signal input; Lo: Standby, Hi: Normal
32	TEST	This pin should be connected to GND.
33	NC	OPEN
34	NC	OPEN
35	NC	OPEN
36	NC	OPEN
37	REV	Horizontal and vertical reverse display control, Lo: Normal, Hi: Reverse (Note: Switching is not valid during Power ON)
38	BLH	LED drive power (anode)
39	BLL	LED drive power (cathode)

Note
The recommended connector is a FH23-39S-0.3SHW(0.5) from Hirose Electric Co., Ltd. The connector is a 0.3mm pitch 39-pin FPC connector (12mm x 0.2mm gold plate).

9.2 Connection Examples

The information in this section provides connection examples for the S1D13513, S1D13517 and S1D13781 display controllers. Some display controllers are available in two packages. The connection information differs for each package and is listed separately.

In addition to the pin connections for the selected display controller, the COM37H3M77 requires the following power supply.

VDD +3.0V (2.7V ≤ VDD ≤ 3.6V)

VL +16.8V (VL ≤ 17.4V)

For VDD, select a voltage within the supportable range of the Display Controller.

For further details on the COM37H3M77, such as power consumption and absolute maximum ratings, please contact your Ortustech representative.

9.2.1 Connecting the COM37H3M77 to the S1D13513

The following diagram shows an example implementation of the COM37H3M77 panel connected to the S1D13513.

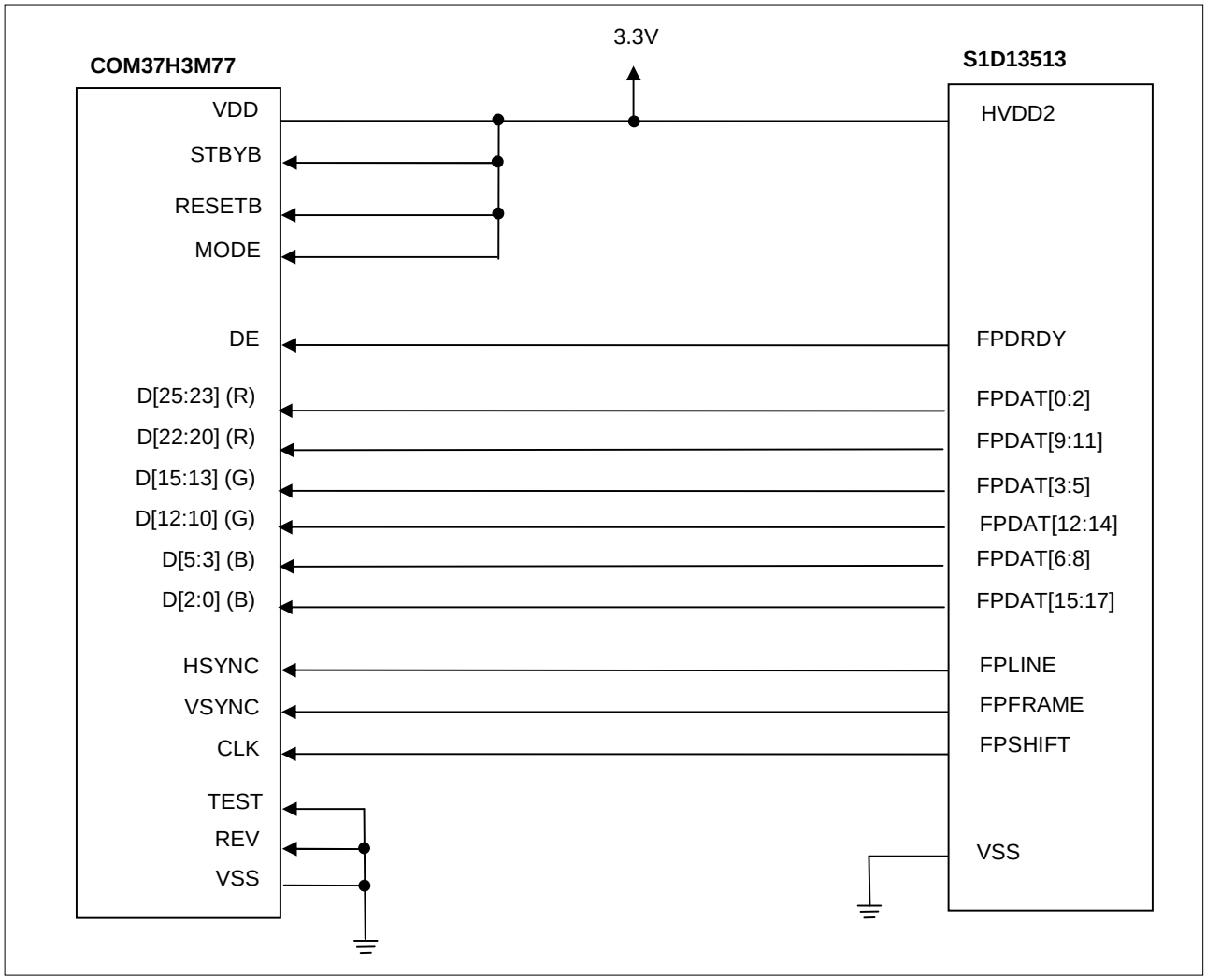

Figure 9-1 Connecting the COM37H3M77 to the S1D13513

The following table provides a detailed pin listing for the required connections between the COM37H3M77 and the S1D13513. Pin mappings are shown for both S1D13513 package types.

Table 9-2 Connecting the COM37H3M77 to the S1D13513

LCD Panel Connector Pin#.	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
1	VSS	GND	Note	Note	VSS
2	VSS	GND	Note	Note	VSS
3	VDD	Power +3.3V	57,65,75	L5,L8,T6	HVDD2
4	VDD	Power +3.3V	57,65,75	L5,L8,T6	HVDD2
5	MODE	Input mode select, Lo: QVGA mode, Hi: VGA mode (Note: Mode switching is not valid during Power ON)	57, 65, 75 or Note	L5, L8, T6 or Note	HVDD2 or VSS
6	RESETB	Power on clear input (Lo-active). For valid reset, a 1ms delay is required after VDD power on (90% of the peak) to the rising edge of the POCB.	57, 65, 75	L5, L8, T6	HVDD2
7	HSYNC	Horizontal synchronous signal (Negative)	79	R8	FPLINE
8	VSYNC	Vertical synchronous signal (Negative)	78	T8	FPFRAME
9	CLK	Dot clock (Capture at the falling edge)	77	P8	FPSHIFT
10	VSS	GND	Note	Note	VSS
11	D00	BLUE data signal (LSB)	53	N4	FPDAT17
12	D01	BLUE data signal	54	P4	FPDAT16
13	D02	BLUE data signal	55	T2	FPDAT15
14	D03	BLUE data signal	64	R6	FPDAT8
15	D04	BLUE data signal	67	K6	FPDAT7
16	D05	BLUE data signal (MSB)	68	M6	FPDAT6
17	D10	GREEN data signal (LSB)	56	R4	FPDAT14
18	D11	GREEN data signal	59	T4	FPDAT13
19	D12	GREEN data signal	60	T5	FPDAT12
20	D13	GREEN data signal	69	L7	FPDAT5
21	D14	GREEN data signal	70	P7	FPDAT4
22	D15	GREEN data signal (MSB)	71	R7	FPDAT3
23	D20	RED data signal (LSB)	61	N5	FPDAT11
24	D21	RED data signal	62	M5	FPDAT10
25	D22	RED data signal	63	P6	FPDAT9
26	D23	RED data signal	72	T7	FPDAT2
27	D24	RED data signal	73	N7	FPDAT1
28	D25	RED data signal (MSB)	74	M7	FPDAT0
29	VSS	GND	Note	Note	VSS
30	DE	Input data enable (Hi-active)	80	M8	FPDRDY
31	STBYB	Standby control signal input, Lo: Standby, Hi: Normal	57, 65, 75	L5, L8, T6	HVDD2
32	TEST	This pin should be connected to GND.	Note	Note	VSS

LCD Panel Connector Pin#.	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
33	NC	OPEN	—	—	—
34	NC	OPEN	—	—	—
35	NC	OPEN	—	—	—
36	NC	OPEN	—	—	—
37	REV	Horizontal and vertical reverse display control, Lo: Normal, Hi: Reverse (Note: Switching is not valid during Power ON)	Note	Note	VSS
38	BLH	LED drive power (anode)	—	—	—
39	BLL	LED drive power (cathode)	—	—	—

Note
Allocation of VSS pin for each packages are as follows.
QFP: 10, 20, 38, 58, 66, 76, 92, 99, 106, 120, 133, 139, 151, 163, 169, 175, 184, 197
BGA: A1, A16, D4, D8, D13, G7-G10, G13, H7-H10, J1, J7-J10, K2, K7-K10, K13, N3, N6, N9, N13, T1, T16

9.2.2 Connecting the COM37H3M77 to the S1D13517

The following diagram shows an example implementation of the COM37H3M77 panel connected to the S1D13517.

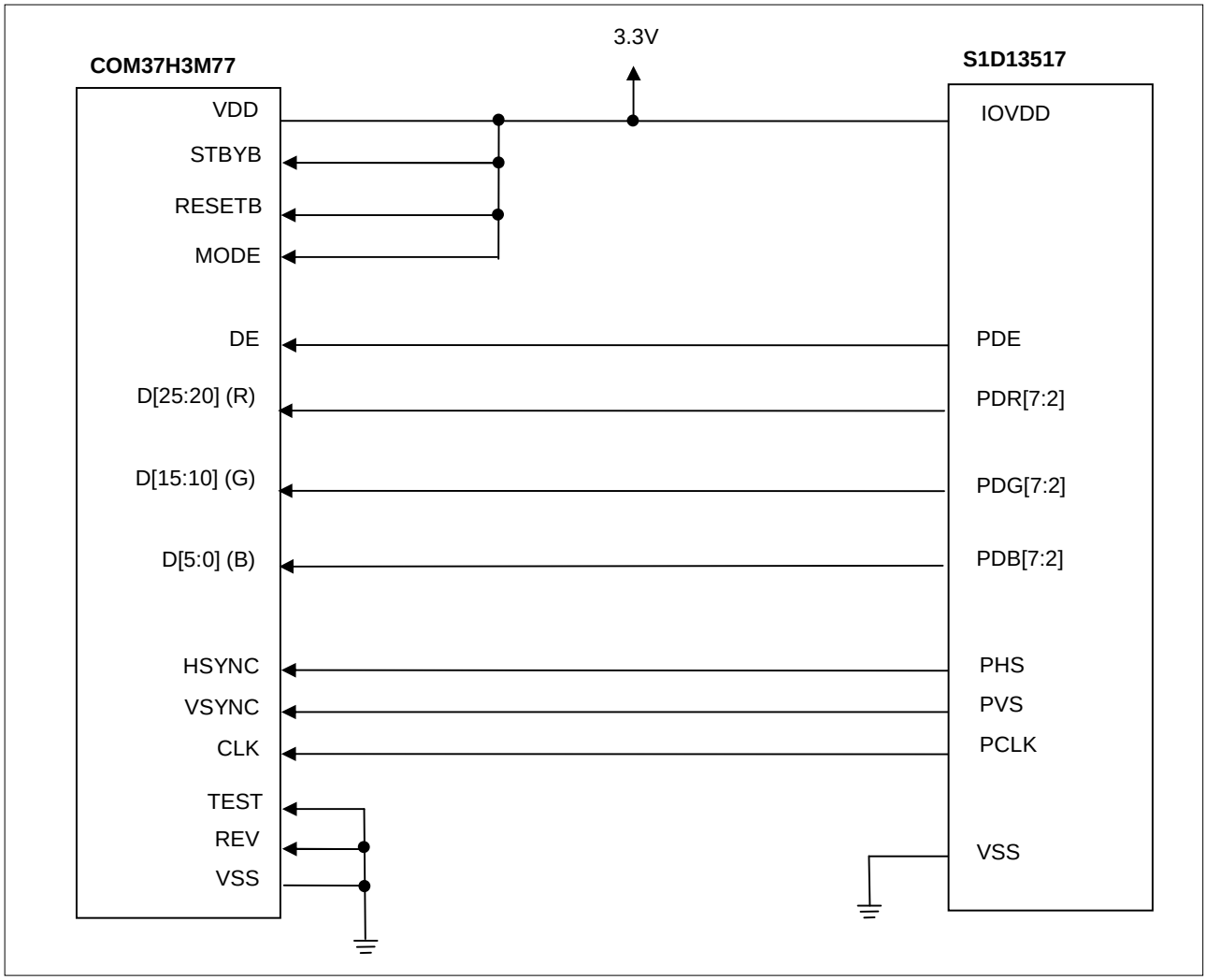

Figure 9-2 Connecting the COM37H3M77 to the S1D13517

The following table provides a detailed pin listing for the required connections between the COM37H3M77 and the S1D13517.

Table 9-3 Connecting the COM37H3M77 to the S1D13517

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13517 QFP Pin#	S1D13517 Pin Name
1	VSS	GND	Note1	VSS
2	VSS	GND	Note1	VSS
3	VDD	Power +3.3V	Note2	IOVDD
4	VDD	Power +3.3V	Note2	IOVDD
5	MODE	Input mode select, Lo: QVGA mode, Hi: VGA mode (Note: Mode switching is not valid during Power ON)	Note2	IOVDD
6	RESETB	Power on clear input (Lo-active). For valid reset, a 1ms delay is required after VDD power on (90% of the peak) to the rising edge of the POCB.	Note2	IOVDD
7	HSYNC	Horizontal synchronous signal (Negative)	83	PHS
8	VSYNC	Vertical synchronous signal (Negative)	82	PVS
9	CLK	Dot clock (Capture at the falling edge)	110	PCLK
10	VSS	GND	Note1	VSS
11	D00	BLUE data signal (LSB)	89	PDB2
12	D01	BLUE data signal	88	PDB3
13	D02	BLUE data signal	87	PDB4
14	D03	BLUE data signal	86	PDB5
15	D04	BLUE data signal	85	PDB6
16	D05	BLUE data signal (MSB)	84	PDB7
17	D10	GREEN data signal (LSB)	99	PDG2
18	D11	GREEN data signal	98	PDG3
19	D12	GREEN data signal	95	PDG4
20	D13	GREEN data signal	94	PDG5
21	D14	GREEN data signal	93	PDG6
22	D15	GREEN data signal (MSB)	92	PDG7
23	D20	RED data signal (LSB)	107	PDR2
24	D21	RED data signal	106	PDR3
25	D22	RED data signal	105	PDR4
26	D23	RED data signal	104	PDR5
27	D24	RED data signal	103	PDR6
28	D25	RED data signal (MSB)	102	PDR7
29	VSS	GND	Note1	VSS
30	DE	Input data enable (Hi-active)	81	PDE
31	STBYB	Standby control signal input, Lo: Standby, Hi: Normal	Note2	IOVDD
32	TEST	This pin should be connected to GND.	Note1	VSS
33	NC	OPEN	—	—
34	NC	OPEN	—	—
35	NC	OPEN	—	—

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13517 QFP Pin#	S1D13517 Pin Name
36	NC	OPEN	—	—
37	REV	Horizontal and vertical reverse display control, Lo: Normal, Hi: Reverse (Note: Switching is not valid during Power ON)	Note1	VSS
38	BLH	LED drive power (anode)	—	—
39	BLL	LED drive power (cathode)	—	—

Note1
Allocation of VSS pin for each packages are as follows.
QFP: 1, 17, 24, 32, 48, 54, 65, 80, 97, 114

Note2
Allocation of IOVDD pin for each packages are as follows.
QFP: 16, 31, 47, 64, 79, 96, 113, 128

9.2.3 Connecting the COM37H3M77 to the S1D13781

The following diagram shows an example implementation of the COM37H3M77 panel connected to the S1D13781.

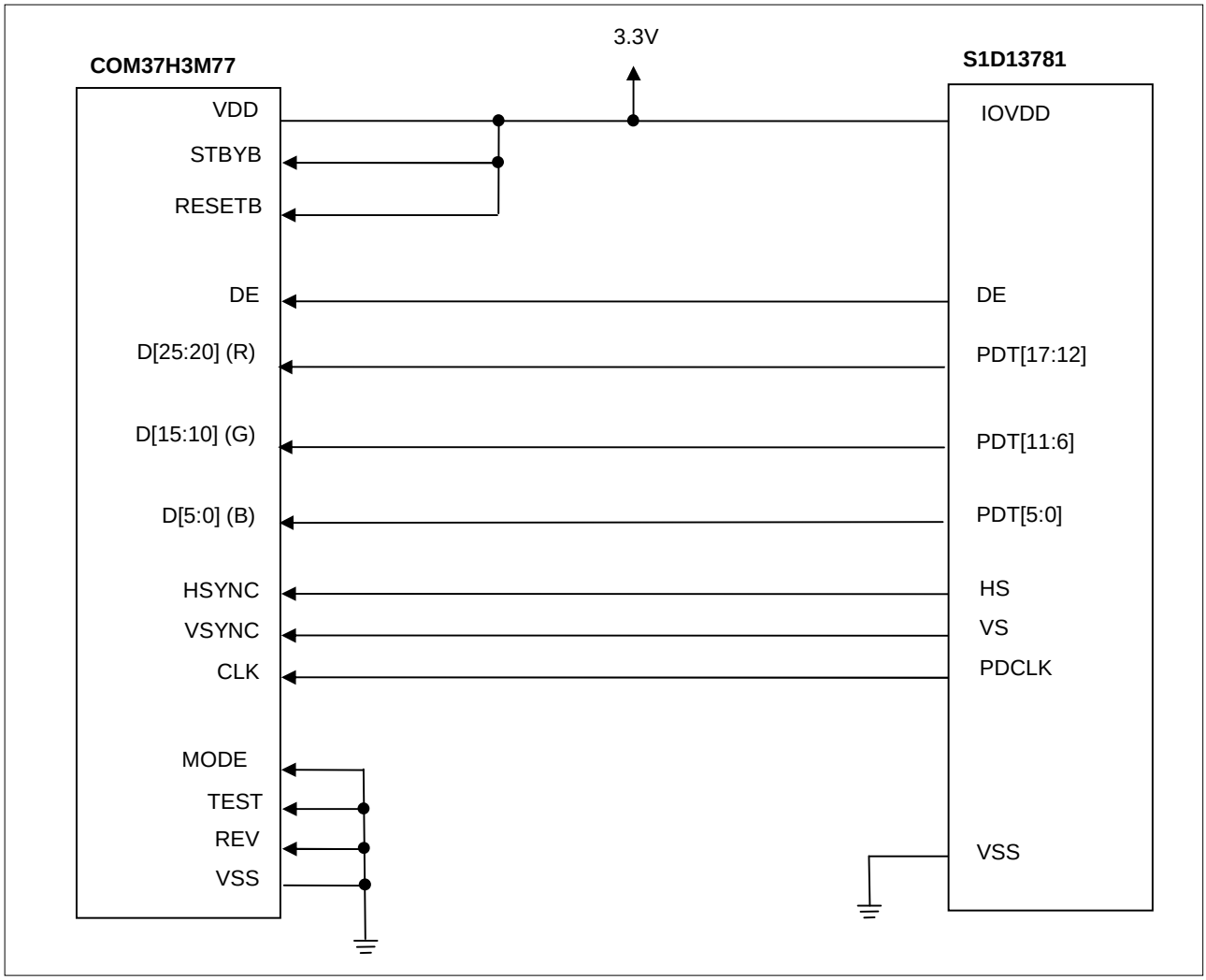

Figure 9-3 Connecting the COM37H3M77 to the S1D13781

The following table provides a detailed pin listing for the required connections between the COM37H3M77 and the S1D13781.

Table 9-4 Connecting the COM37H3M77 to the S1D13781

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13781 QFP Pin#	S1D13781 Pin Name
1	VSS	GND	Note1	GND
2	VSS	GND	Note1	GND
3	VDD	Power +3.3V	Note2	PIOVDD
4	VDD	Power +3.3V	Note2	PIOVDD
5	MODE	Input mode setting (Lo: QVGA, Hi: VGA) No mode change allowed during power on.	Note1	GND
6	RESETB	RESET(Lo-active)	Note2	PIOVDD
7	HSYNC	Horizontal synchronous signal (Negative)	55	HS
8	VSYNC	Vertical synchronous signal (Negative)	54	VS
9	CLK	Dot clock (Capture at the falling edge)	59	PDCLK
10	VSS	GND	Note1	GND
11	D00	BLUE data signal (LSB)	61	PDT0
12	D01	BLUE data signal	62	PDT1
13	D02	BLUE data signal	63	PDT2
14	D03	BLUE data signal	64	PDT3
15	D04	BLUE data signal	65	PDT4
16	D05	BLUE data signal (MSB)	66	PDT5
17	D10	GREEN data signal (LSB)	68	PDT6
18	D11	GREEN data signal	69	PDT7
19	D12	GREEN data signal	70	PDT8
20	D13	GREEN data signal	71	PDT9
21	D14	GREEN data signal	72	PDT10
22	D15	GREEN data signal (MSB)	74	PDT11
23	D20	RED data signal (LSB)	75	PDT12
24	D21	RED data signal	76	PDT13
25	D22	RED data signal	77	PDT14
26	D23	RED data signal	78	PDT15
27	D24	RED data signal	81	PDT16
28	D25	RED data signal (MSB)	82	PDT17
29	VSS	GND	Note1	GND
30	DE	Input data enable (Hi-active)	56	DE
31	STBYB	Display control signal Lo: Standby, Hi: Normal	Note2	PIOVDD
32	TEST	Connect to GND	Note1	GND
33	NC	OPEN	—	—
34	NC	OPEN	—	—
35	NC	OPEN	—	—
36	NC	OPEN	—	—

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13781 QFP Pin#	S1D13781 Pin Name
37	REV	Vertical and Horizontal reverse control signal input (Lo: Normal, Hi: Reverse) No mode change allowed during power on.	Note1	GND
38	BLH	Power supply for back light LED(anode)	—	—
39	BLL	Power supply for back light LED(cathode)	—	—

Note 1
Allocation of VSS pin for each packages are as follows.
QFP: 12, 23, 38, 48, 57, 67, 80, 90

Note 2
Allocation of IOVDD pin for each packages are as follows.
QFP: 60, 73, 89

9.3 Example Register Settings

In addition to the pin connections, the S1D13513/S1D13517/S1D13781 internal registers must be configured appropriately for the COM37H3M77 LCD panel. The following tables provide example settings for each display controller. However, these values are for reference only and may differ according to each specific implementation.

Also included in the table is an example clock configuration designed to achieve a typical LCD refresh.

Table 9-5 Example Register Settings for the S1D13513 (VGA mode)

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0800h] LCD Panel Type Select Register	0280h	—
REG[0802h] LCD Horizontal Total Register	0239h	570
REG[0804h] LCD Horizontal Display Period Register	00EFh	480
REG[0806h] LCD Horizontal Display Period Start Position Register	0008h	9
REG[0808h] LCD Horizontal Pulse Width	0001h	2
REG[080Ah] LCD Horizontal Pulse Start Position	0051h	81
REG[080Ch] LCD Vertical Total Register	0289h	650
REG[080Eh] LCD Vertical Display Period Resister	027Fh	640
REG[0810h] LCD Vertical Display Period Start Position Register	0003h	3
REG[0812h] LCD Vertical Pulse Width	0000h	1
REG[0814h] LCD Vertical Pulse Start Position	0000h	0
REG[0C1Eh] GPIOH Pin Function Register	0555h	Set GPIO pins for 24bpp mode configuration
PLL2 output frequency in MHz	—	90
REG[0446h] LCD Clock Control Register	0003h	4
FPSHIFT in MHz	—	22.5
LCD Refresh in Hz	—	60.73

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13513 register values, see the *S1D13513 Hardware Functional Specification*, document number X78B-A-001-xx.

Table 9-6 Example Register Settings for the S1D13513 (QVGA mode)

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0800h] LCD Panel Type Select Register	0280h	—
REG[0802h] LCD Horizontal Total Register	011Eh	287
REG[0804h] LCD Horizontal Display Period Register	0077h	240
REG[0806h] LCD Horizontal Display Period Start Position Register	0008h	9
REG[0808h] LCD Horizontal Pulse Width	0001h	2
REG[080Ah] LCD Horizontal Pulse Start Position	0026h	38
REG[080Ch] LCD Vertical Total Register	0144h	325
REG[080Eh] LCD Vertical Display Period Resister	013Fh	320
REG[0810h] LCD Vertical Display Period Start Position Register	0041h	65
REG[0812h] LCD Vertical Pulse Width	0000h	1
REG[0814h] LCD Vertical Pulse Start Position	0000h	0
REG[0C1Eh] GPIOH Pin Function Register	—	110
PLL2 output frequency in MHz	0013h	20
REG[0446h] LCD Clock Control Register	—	5.5
FPSHIFT in MHz	—	58.97
LCD Refresh in Hz	0026h	38

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13513 register values, see the *S1D13513 Hardware Functional Specification*, document number X78B-A-001-xx.

Table 9-7 Example Register Settings for the S1D13517 (VGA mode)

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[14h] LCD Panel Type Register	01h	24bpp mode1, 18-bit
REG[16h] Horizontal Display Width Register (HDISP)	3Bh	480
REG[18h] Horizontal Non-Display Period Register (HNDP)	2Ch	90
REG[1Ah] Vertical Display Height Register 0 (VDISP)	7Fh	640
REG[1Ch] Vertical Display Height Register 1 (VDISP)	02h	—
REG[1Eh] Vertical Non-Display Period Register (VNDP)	04h	10
REG[20h] PHS Pulse Width Register (HSW)	01h	2
REG[22h] PHS Pulse Start Position Register (HPS)	51h	81
REG[24h] PVS Pulse Width Register (VSW)	00h	1
REG[26h] PVS Pulse Start Position Register (VPS)	07h	7
REG[28h] PCLK Polarity Register	00h	PCLK polarity is rising edge.
REG[04h] PLL D-Divider Register	97h	PLL D-div is 1:24. Input 24MHz -> Output 1MHz
REG[06h] PLL Setting Register 0	01h	PLL output = 90MHz
REG[08h] PLL Setting Register 1	01h	PLL clock Divide ratio = 1/2. (45MHz)
REG[0Ch] PLL N-Divider Register	2Ch	PLL N-counter 45MHz
REG[0Eh] SS Control Register 0	3Fh	SS disabled
REG[12h] Clock Source Select Register	90h	SYSCLK = ½ (45MHz/2 = 22.5MHz)
REG[8Ch] SDRAM Refresh Counter Register 0	5Bh	Refresh counter 1/22.5MHz x 347 = 15.42us
REG[8Eh] SDRAM Refresh Counter Register 1	01h	—
FPSHIFT in MHz	—	22.5
LCD Refresh in Hz	—	60.73

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13517 register values, see the *S1D13517 Hardware Functional Specification*, document number X92A-G-001-xx.

Table 9-8 Example Register Settings for the S1D13781 (QVGA mode)

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[20h] Panel Setting Register	004Dh	DE: High active PCLK Polarity: rising edge PanelType: Color TFT 18-bit
REG[24h] Horizontal Display Width Register	001Eh	240
REG[26h] Horizontal Non-Display Period Register	002Fh	47
REG[28h] Vertical Display Height Register	0140h	320

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[2Ah] Vertical Non-Display Period Register	0005h	5
REG[2Ch] HS Pulse Width Register	0002h	2
REG[2Eh] HS Pulse Start Position Register	0026h	38
REG[30h] VS Pulse Width Register	0001h	1
REG[32h] VS Pulse Start Position Register	0002h	2
REG[12h] PLL Setting Register 1	0011h	MM=18
REG[14h] PLL Setting Register 2	0029h	LL=42
REG[16h] Internal Clock Configuration Register	0009h	fPLL_REF_CLK = fCLKI /10
CLKI in MHz	—	24
PCLK in MHz	—	5.6
LCD refresh in Hz	—	60.4

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13781 register values, see the *S1D13781 Hardware Functional Specification*, document number X92A-G-001-xx.

10 Connecting to the Ortustech COM43H4M71

The Ortustech COM43H4M71 TFT panel is compatible with the S1D13513, S1D13517 and S1D13781 display controllers. The following sections will provide connector details, pin mappings, and example register settings for these combinations.

10.1 COM43H4M71 Pin Mapping

The COM43H4M71 TFT panel uses a 45-pin connector with the following pin mapping.

Table 10-1 COM43H4M71Pin Mapping

Connector Pin#	Pin Name	Pin Description
1	VSS	GND
2	VSS	GND
3	VDD	Power +3.3V (3.0V ≤ VDD ≤ 3.6V)
4	VDD	Power +3.3V (3.0V ≤ VDD ≤ 3.6V)
5	D00	RED data signal (LSB)
6	D01	RED data signal
7	D02	RED data signal
8	D03	RED data signal
9	D04	RED data signal
10	D05	RED data signal
11	D06	RED data signal
12	D07	RED data signal (MSB)
13	D10	GREEN data signal (LSB)
14	D11	GREEN data signal
15	D12	GREEN data signal
16	D13	GREEN data signal
17	D14	GREEN data signal
18	D15	GREEN data signal
19	D16	GREEN data signal
20	D17	GREEN data signal (MSB)
21	D20	BLUE data signal (LSB)
22	D21	BLUE data signal
23	D22	BLUE data signal
24	D23	BLUE data signal
25	D24	BLUE data signal
26	D25	BLUE data signal
27	D26	BLUE data signal
28	D27	BLUE data signal (MSB)
29	VSS	GND
30	CLK	Dot clock (Capture at the falling edge)
31	STBYB	Standby Control signal Lo: Standby, Hi: Normal operation

Connector Pin#	Pin Name	Pin Description
32	HSYNC	Horizontal synchronous signal (Negative)
33	VSYNC	Vertical synchronous signal (Negative)
34	DE	Input data enable (Hi-active)
35	NC	OPEN
36	VSS	GND
37	NC	OPEN
38	NC	OPEN
39	NC	OPEN
40	NC	OPEN
41	VSS	GND
42	BLL	LED drive power (cathode)
43	BLH	LED drive power (anode)
44	NC	OPEN
45	NC	OPEN

Note
The recommended connector is a FH12A-45S-0.5SH(55) from Hirose Electric Co., Ltd. The connector is a 0.5mm pitch 45-pin FPC connector.

10.2 Connection Examples

The information in this section provides connection examples for the S1D13513, S1D13517 and S1D13781 display controllers. Some display controllers are available in two packages. The connection information differs for each package and is listed separately.

In addition to the pin connections for the selected display controller, the COM43H4M71 requires the following power supply.

VDD +3.3V (3.0V ≤ VDD ≤ 3.6V)

VL +14.25V (VL ≤ 16.25V)

For VDD, select a voltage within the supportable range of the Display Controller.

For further details on the COM43H4M71, such as power consumption and absolute maximum ratings, please contact your Ortustech representative.

10.2.1 Connecting the COM43H4M71 to the S1D13513

The following diagram shows an example implementation of the COM43H4M71 panel connected to the S1D13513.

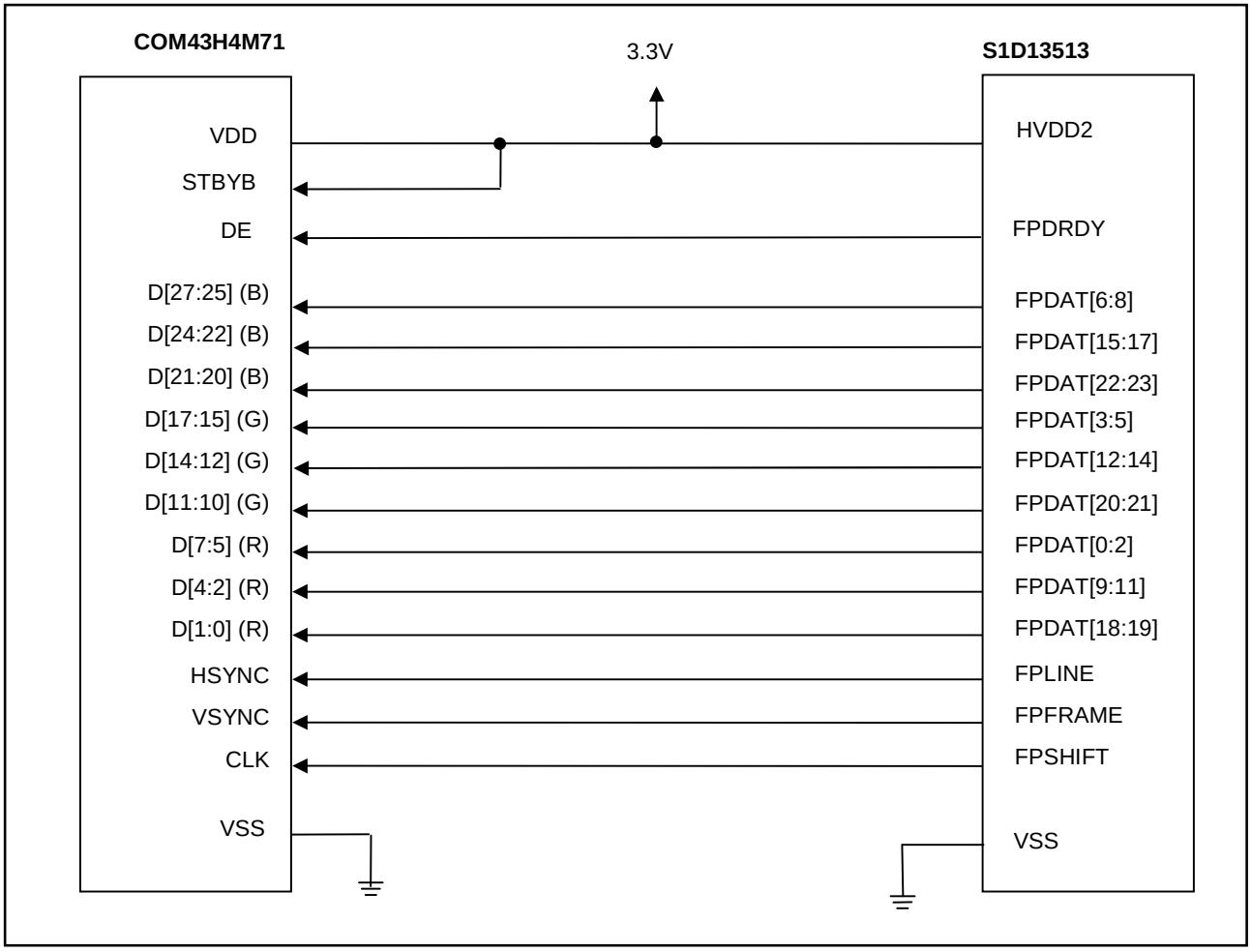

Figure 10-1 Connecting the COM43H4M71 to the S1D13513

The following table provides a detailed pin listing for the required connections between the COM43H4M71 and the S1D13513. Pin mappings are shown for both S1D13513 package types.

Table 10-2 Connecting the COM43H4M71 to the S1D13513

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
1	VSS	GND	Note1	Note1	VSS
2	VSS	GND	Note1	Note1	VSS
3	VDD	Power +3.3V	57, 65, 75	L5, L8, T6	HVDD2
4	VDD	Power +3.3V	57, 65, 75	L5, L8, T6	HVDD2
5	D00	RED data signal (LSB)	Note2	K5	FPDAT19
6	D01	RED data signal	Note2	R5	FPDAT18

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
7	D02	RED data signal	61	N5	FPDAT11
8	D03	RED data signal	62	M5	FPDAT10
9	D04	RED data signal	63	P6	FPDAT9
10	D05	RED data signal	72	T7	FPDAT2
11	D06	RED data signal	73	N7	FPDAT1
12	D07	RED data signal (MSB)	74	M7	FPDAT0
13	D10	GREEN data signal (LSB)	Note2	T3	FPDAT21
14	D11	GREEN data signal	Note2	P5	FPDAT20
15	D12	GREEN data signal	56	R4	FPDAT14
16	D13	GREEN data signal	59	T4	FPDAT13
17	D14	GREEN data signal	60	T5	FPDAT12
18	D15	GREEN data signal	69	L7	FPDAT5
19	D16	GREEN data signal	70	P7	FPDAT4
20	D17	GREEN data signal (MSB)	71	R7	FPDAT3
21	D20	BLUE data signal (LSB)	Note2	K4	FPDAT23
22	D21	BLUE data signal	Note2	R3	FPDAT22
23	D22	BLUE data signal	53	N4	FPDAT17
24	D23	BLUE data signal	54	P4	FPDAT16
25	D24	BLUE data signal	55	T2	FPDAT15
26	D25	BLUE data signal	64	R6	FPDAT8
27	D26	BLUE data signal	67	K6	FPDAT7
28	D27	BLUE data signal (MSB)	68	M6	FPDAT6
29	VSS	GND	Note1	Note1	VSS
30	CLK	Dot clock (Capture at the falling edge)	77	P8	FPSHIFT
31	STBYB	Standby Control signal Lo: Standby, Hi: Normal operation	57, 65, 75	L5, L8, T6	HVDD2
32	HSYNC	Horizontal synchronous signal (Negative)	79	R8	FPLINE
33	VSYNC	Vertical synchronous signal (Negative)	77	T8	FPFRAME
34	DE	Input data enable (Hi-active)	80	M8	FPDRDY
35	NC	OPEN	—	—	—
36	VSS	GND	Note1	Note1	VSS
37	NC	OPEN	—	—	—
38	NC	OPEN	—	—	—
39	NC	OPEN	—	—	—
40	NC	OPEN	—	—	—
41	VSS	GND	Note1	Note1	VSS
42	BLL	LED drive power (cathode)	—	—	—
43	BLH	LED drive power (anode)	—	—	—
44	NC	OPEN	—	—	—
45	NC	OPEN	—	—	—

S1D13513 HVDD2 and COM43H4M71 VDD must be configured between +3.0V to +3.6V.

Note 1
Allocation of VSS pin for each packages are as follows.
QFP: 10, 20, 38, 58, 66, 76, 92, 99, 106, 120, 133, 139, 151, 163, 169, 175, 184, 197
BGA: A1, A16, D4, D8, D13, G7-G10, G13, H7-H10, J1, J7-J10, K2, K7-K10, K13, N3, N6, N9, N13, T1, T16

Note 2
Connect to VSS pin for QFP package.

10.2.2 Connecting the COM43H4M71 to the S1D13517

The following diagram shows an example implementation of the COM43H4M71 panel connected to the S1D13517.

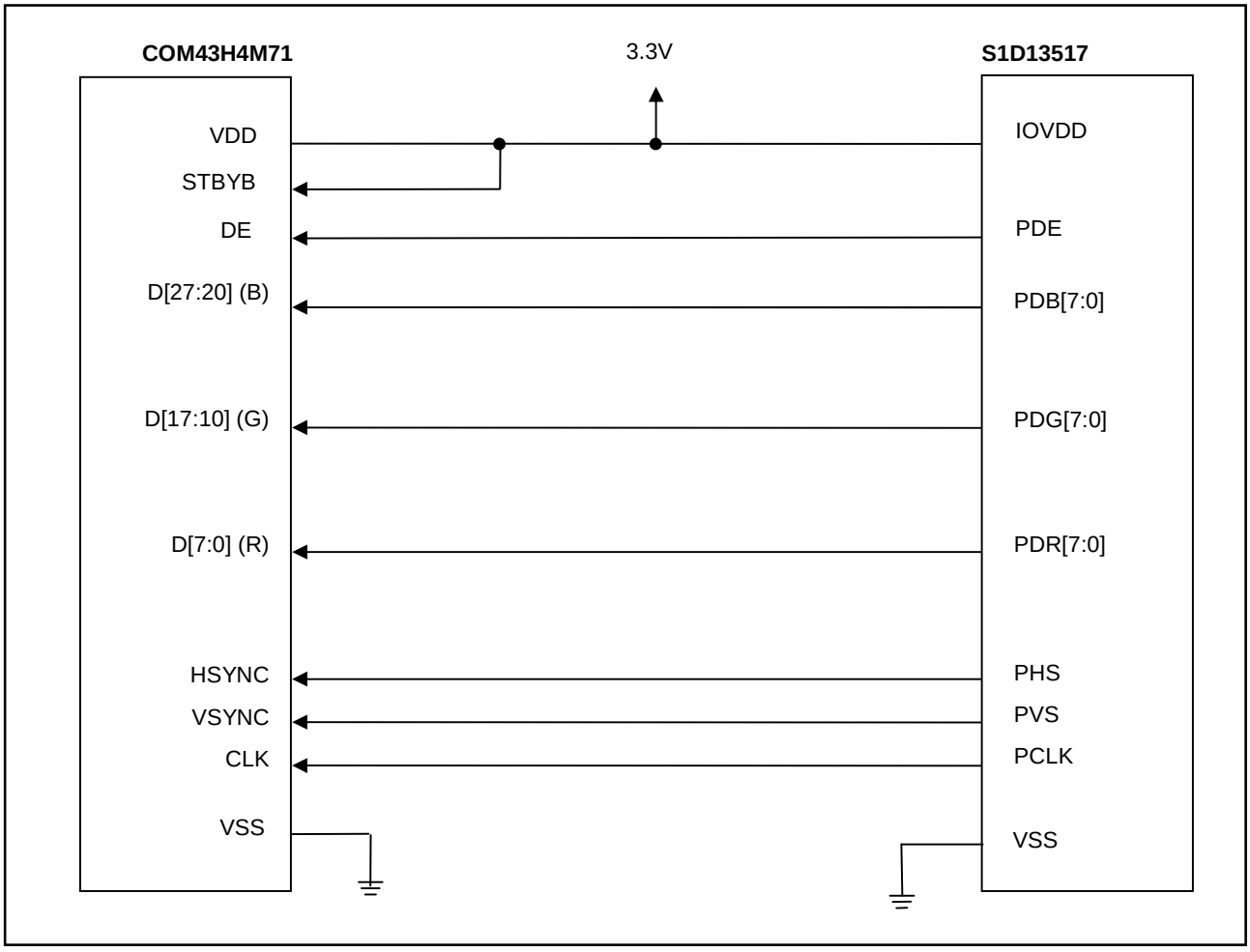

Figure 10-2 Connecting the COM43H4M71 to the S1D13517

The following table provides a detailed pin listing for the required connections between the COM43H4M71 and the S1D13517.

Table 10-3 Connecting the COM43H4M71 to the S1D13517

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13517 QFP Pin#	S1D13517 Pin Name
1	VSS	GND	Note1	VSS
2	VSS	GND	Note1	VSS
3	VDD	Power +3.3V	Note2	IOVDD
4	VDD	Power +3.3V	Note2	IOVDD
5	D00	RED data signal (LSB)	109	PDR0
6	D01	RED data signal	108	PDR1
7	D02	RED data signal	107	PDR2
8	D03	RED data signal	106	PDR3
9	D04	RED data signal	105	PDR4
10	D05	RED data signal	104	PDR5
11	D06	RED data signal	103	PDR6
12	D07	RED data signal (MSB)	102	PDR7
13	D10	GREEN data signal (LSB)	101	PDG0
14	D11	GREEN data signal	100	PDG1
15	D12	GREEN data signal	99	PDG2
16	D13	GREEN data signal	98	PDG3
17	D14	GREEN data signal	95	PDG4
18	D15	GREEN data signal	94	PDG5
19	D16	GREEN data signal	93	PDG6
20	D17	GREEN data signal (MSB)	92	PDG7
21	D20	BLUE data signal (LSB)	91	PDB0
22	D21	BLUE data signal	90	PDB1
23	D22	BLUE data signal	89	PDB2
24	D23	BLUE data signal	88	PDB3
25	D24	BLUE data signal	87	PDB4
26	D25	BLUE data signal	86	PDB5
27	D26	BLUE data signal	85	PDB6
28	D27	BLUE data signal (MSB)	84	PDB7
29	VSS	GND	Note1	VSS
30	CLK	Dot clock (Capture at the falling edge)	110	PCLK
31	STBYB	Standby Control signal; Lo: Standby, Hi: Normal operation	Note2	IOVDD
32	HSYNC	Horizontal synchronous signal (Negative)	83	PHS
33	VSYNC	Vertical synchronous signal (Negative)	82	PVS
34	DE	Input data enable (Hi-active)	81	PDE
35	NC	OPEN	—	—
36	VSS	GND	Note1	VSS
37	NC	OPEN	—	—

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13517 QFP Pin#	S1D13517 Pin Name
38	NC	OPEN	—	—
39	NC	OPEN	—	—
40	NC	OPEN	—	—
41	VSS	GND	Note1	VSS
42	BLL	LED drive power (cathode)	—	—
43	BLH	LED drive power (anode)	—	—
44	NC	OPEN	—	—
45	NC	OPEN	—	—

Note 1
Allocation of VSS pin for each package are as follows.
QFP: 1, 17, 24, 32, 48, 54, 65, 80, 97, 114

Note 2
Allocation of IOVDD pin for each package are as follows.
QFP: 16, 31, 47, 64, 79, 96, 113, 128

10.2.3 Connecting the COM43H4M71 to the S1D13781

The following diagram shows an example implementation of the COM43H4M71 panel connected to the S1D13781.

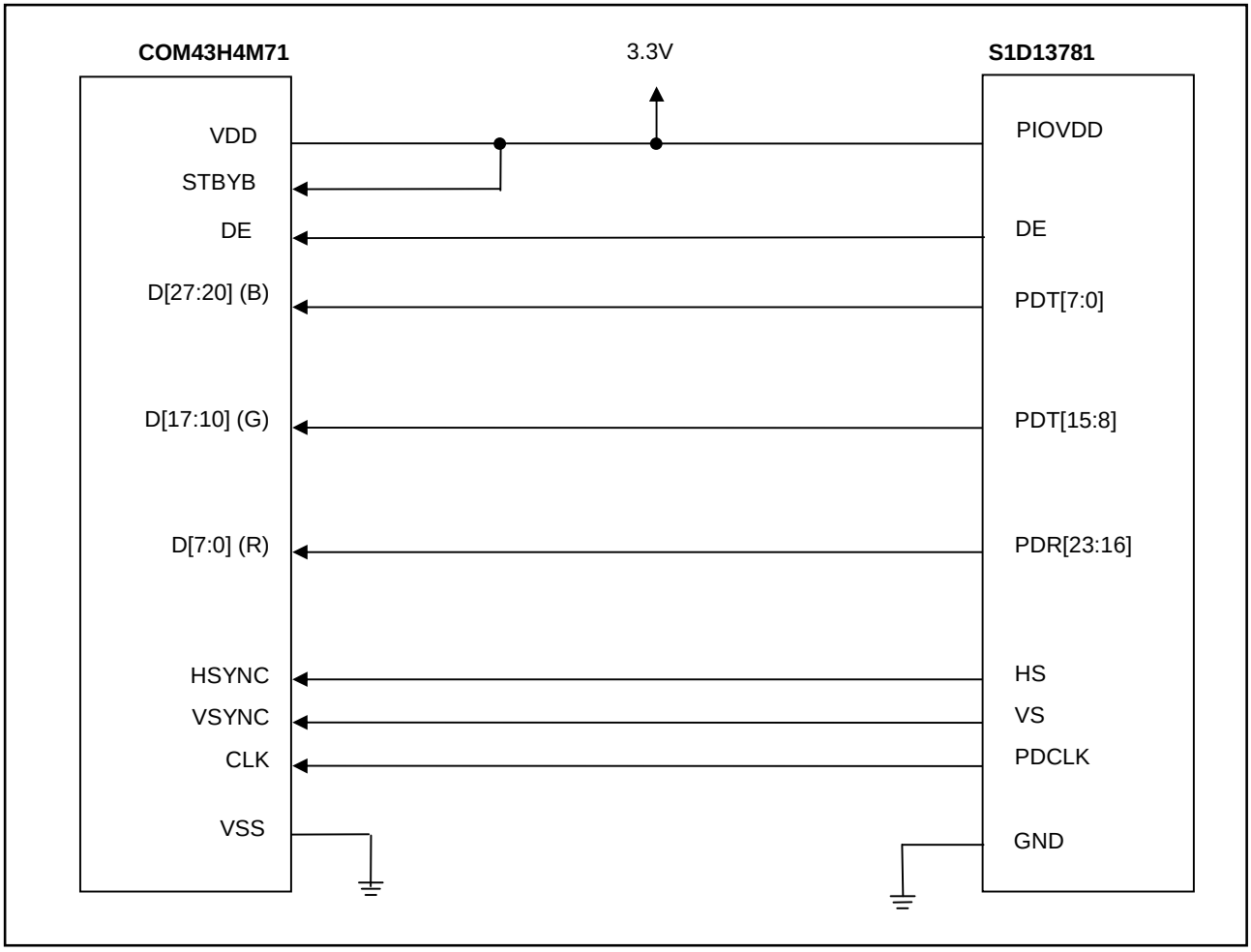

Figure 10-3 Connecting the COM43H4M71 to the S1D13781

The following table provides a detailed pin listing for the required connections between the COM43H4M71 and the S1D13781.

Table 10-4 Connecting the COM43H4M71 to the S1D13781

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13781 QFP Pin#	S1D13781 Pin Name
1	VSS	GND	Note1	GND
2	VSS	GND	Note1	GND
3	VDD	Power +3.3V	Note2	PIOVDD
4	VDD	Power +3.3V	Note2	PIOVDD
5	D00	RED data signal (LSB)	81	PDT16
6	D01	RED data signal	82	PDT17
7	D02	RED data signal	83	PDT18
8	D03	RED data signal	84	PDT19
9	D04	RED data signal	85	PDT20
10	D05	RED data signal	86	PDT21
11	D06	RED data signal	87	PDT22
12	D07	RED data signal (MSB)	88	PDT23
13	D10	GREEN data signal (LSB)	70	PDT8
14	D11	GREEN data signal	71	PDT9
15	D12	GREEN data signal	72	PDT10
16	D13	GREEN data signal	74	PDT11
17	D14	GREEN data signal	75	PDT12
18	D15	GREEN data signal	76	PDT13
19	D16	GREEN data signal	77	PDT14
20	D17	GREEN data signal (MSB)	78	PDT15
21	D20	BLUE data signal (LSB)	61	PDT0
22	D21	BLUE data signal	62	PDT1
23	D22	BLUE data signal	63	PDT2
24	D23	BLUE data signal	64	PDT3
25	D24	BLUE data signal	65	PDT4
26	D25	BLUE data signal	66	PDT5
27	D26	BLUE data signal	68	PDT6
28	D27	BLUE data signal (MSB)	69	PDT7
29	VSS	GND	Note1	GND
30	CLK	Dot clock (Capture at the falling edge)	59	PDCLK
31	STBYB	Standby Control signal; Lo: Standby, Hi: Normal operation	Note2	PIOVDD
32	HSYNC	Horizontal synchronous signal (Negative)	55	HS
33	VSYNC	Vertical synchronous signal (Negative)	54	VS
34	DE	Input data enable (Hi-active)	56	DE
35	NC	OPEN	—	—
36	VSS	GND	Note1	GND
37	NC	OPEN	—	—

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13781 QFP Pin#	S1D13781 Pin Name
38	NC	OPEN	—	—
39	NC	OPEN	—	—
40	NC	OPEN	—	—
41	VSS	GND	Note1	GND
42	BLL	LED drive power (cathode)	—	—
43	BLH	LED drive power (anode)	—	—
44	NC	OPEN	—	—
45	NC	OPEN	—	—

Note 1
Allocation of VSS pin for each packages are as follows.
QFP: 12, 23, 38, 48, 57, 67, 80, 90

Note 2
Allocation of IOVDD pin for each packages are as follows.
QFP: 60, 73, 89

10.3 Example Register Settings

In addition to the pin connections, the S1D13513/S1D13517/S1D13781 internal registers must be configured appropriately for the COM43H4M71 LCD panel. The following tables provide example settings for each display controller. However, these values are for reference only and may differ according to each specific implementation.

Also included in the table is an example clock configuration designed to achieve a typical LCD refresh.

Table 10-5 Example Register Settings for the S1D13513

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0800h] LCD Panel Type Select Register	0380h	—
REG[0802h] LCD Horizontal Total Register	020Ch	525
REG[0804h] LCD Horizontal Display Period Register	00EFh	480
REG[0806h] LCD Horizontal Display Period Start Position Register	0027h	40
REG[0808h] LCD Horizontal Pulse Width	0000h	1
REG[080Ah] LCD Horizontal Pulse Start Position	0005h	5
REG[080Ch] LCD Vertical Total Register	011Fh	288
REG[080Eh] LCD Vertical Display Period Resister	010Fh	272
REG[0810h] LCD Vertical Display Period Start Position Register	0008h	8
REG[0812h] LCD Vertical Pulse Width	0000h	1
REG[0814h] LCD Vertical Pulse Start Position	0000h	0
REG[0C1Eh] GPIOH Pin Function Register	0555h	Set GPIO pins for 24bpp mode configuration
PLL2 output frequency in MHz	—	90

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0446h] LCD Clock Control Register	0009h	10
FPSHIFT in MHz	—	9
LCD Refresh in Hz	—	59.52

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13513 register values, see the *S1D13513 Hardware Functional Specification*, document number X78B-A-001-xx.

Table 10-6 Example Register Settings for the S1D13517

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[14h] LCD Panel Type Register	00h	24bpp mode1, 24-bit
REG[16h] Horizontal Display Width Register (HDISP)	3Bh	480
REG[18h] Horizontal Non-Display Period Register (HNDP)	16h	46
REG[1Ah] Vertical Display Height Register 0 (VDISP)	0Fh	272
REG[1Ch] Vertical Display Height Register 1 (VDISP)	01h	—
REG[1Eh] Vertical Non-Display Period Register (VNDP)	07h	16
REG[20h] PHS Pulse Width Register (HSW)	01h	2
REG[22h] PHS Pulse Start Position Register (HPS)	05h	5
REG[24h] PVS Pulse Width Register (VSW)	00h	1
REG[26h] PVS Pulse Start Position Register (VPS)	08h	8
REG[28h] PCLK Polarity Register	00h	PCLK polarity is rising edge.
REG[04h] PLL D-Divider Register	97h	PLL D-div is 1:24. Input 24MHz -> Output 1MHz
REG[06h] PLL Setting Register 0	01h	PLL output = 54MHz
REG[08h] PLL Setting Register 1	01h	PLL clock Divide ratio = 1/2. (27MHz)
REG[0Ch] PLL N-Divider Register	1Ah	PLL N-counter 54MHz
REG[0Eh] SS Control Register 0	3Fh	SS disabled
REG[12h] Clock Source Select Register	80h	SYSCLK = 1/3 (27MHz/3 = 9MHz)
REG[8Ch] SDRAM Refresh Counter Register 0	A2h	Refresh counter 1/27MHz x 418 = 15.48us
REG[8Eh] SDRAM Refresh Counter Register 1	01h	—
FPSHIFT in MHz	—	9
LCD Refresh in Hz	—	59.41

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13517 register values, see the *S1D13517 Hardware Functional Specification*, document number X92A-G-001-xx.

Table 10-7 Example Register Settings for the S1D13781

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[20h] Panel Setting Register	004Fh	DE:High active PCLK Polarity: rising edge PanelType: Color TFT 24-bit
REG[24h] Horizontal Display Width Register	003Ch	480
REG[26h] Horizontal Non-Display Period Register	002Dh	45
REG[28h] Vertical Display Height Register	0110h	272
REG[2Ah] Vertical Non-Display Period Register	0010h	16
REG[2Ch] HS Pulse Width Register	0001h	1
REG[2Eh] HS Pulse Start Position Register	0005h	5
REG[30h] VS Pulse Width Register	0001h	1
REG[32h] VS Pulse Start Position Register	0008h	8
REG[12h] PLL Setting Register 1	000Fh	MM=16
REG[14h] PLL Setting Register 2	0029h	LL=42
REG[16h] Internal Clock Configuration Register	0006h	fPLL_REF_CLK = fCLKI /7
CLKI in MHz	—	24
PCLK in MHz	—	9
LCD refresh in Hz	—	59.52

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13781 register values, see the *S1D13781 Hardware Functional Specification*, document number X92A-G-001-xx.

11 Connecting to the Ortustech COM57T5M54

The Ortustech COM57T5M54 TFT panel is compatible with the S1D13513, S1D13742 and S1D13748 display controllers. The following sections will provide connector details, pin mappings, and example register settings for these combinations.

11.1 COM57T5M54 Pin Mapping

The COM57T5M54 TFT panel uses a 33-pin connector with the following pin mapping.

Table 11-1 COM57T5M54 Pin Mapping

Connector Pin#	Pin Name	Pin Description
1	GND	GND
2	CLK	Dot clock (Capture at the falling edge)
3	HSYNC	Horizontal synchronous signal (Negative)
4	VSYNC	Vertical synchronous signal (Negative)
5	GND	GND
6	R0	RED data signal Data 00h displays black. R0: LSB R5: MSB Gamma correction is done inside the driver.
7	R1	
8	R2	
9	R3	
10	R4	
11	R5	
12	GND	GND
13	G0	GREEN data signal Data 00h displays black. G0: LSB G5: MSB Gamma correction is done inside the driver.
14	G1	
15	G2	
16	G3	
17	G4	
18	G5	
19	GND	GND
20	B0	BLUE data signal Data 00h displays black. B0: LSB B5: MSB Gamma correction is done inside the driver.
21	B1	
22	B2	
23	B3	
24	B4	
25	B5	
26	GND	GND
27	ENAB	Input data enable (Hi-active)
28	VDD	Power +3.3V (3.0V ≤ VDD ≤ 3.6V)
29	VDD	Power +3.3V (3.0V ≤ VDD ≤ 3.6V)
30	RL	Horizontally Flipped (right/left) signal Lo: Flipped, Hi: Normal
31	UD	Vertically Flipped (up/down) display control Lo: Normal, Hi: Flipped
32	DISP	Display control signal (Lo: Display off, Hi: Display on)
33	GND	GND

Note
The recommended connector is a 04-6240-033-023-846+ from Kyocera elco.

11.2 Connection Examples

The information in this section provides connection examples for the S1D13513, S1D13742 and S1D13748 display controllers. Some display controllers are available in two packages. The connection information differs for each package and is listed separately.

In addition to the pin connections for the selected display controller, the COM57T5M54 requires the following power supply.

VDD +3.3V (3.0V ≤ VDD ≤ 3.6V)

VL +15V (VL ≤ 17V)

For VDD, select a voltage within the supportable range of the Display Controller.

For further details on the COM57T5M54, such as power consumption and absolute maximum ratings, please contact your Ortustech representative.

11.2.1 Connecting the COM57T5M54 to the S1D13513

The following diagram shows an example implementation of the COM57T5M54 panel connected to the S1D13513.

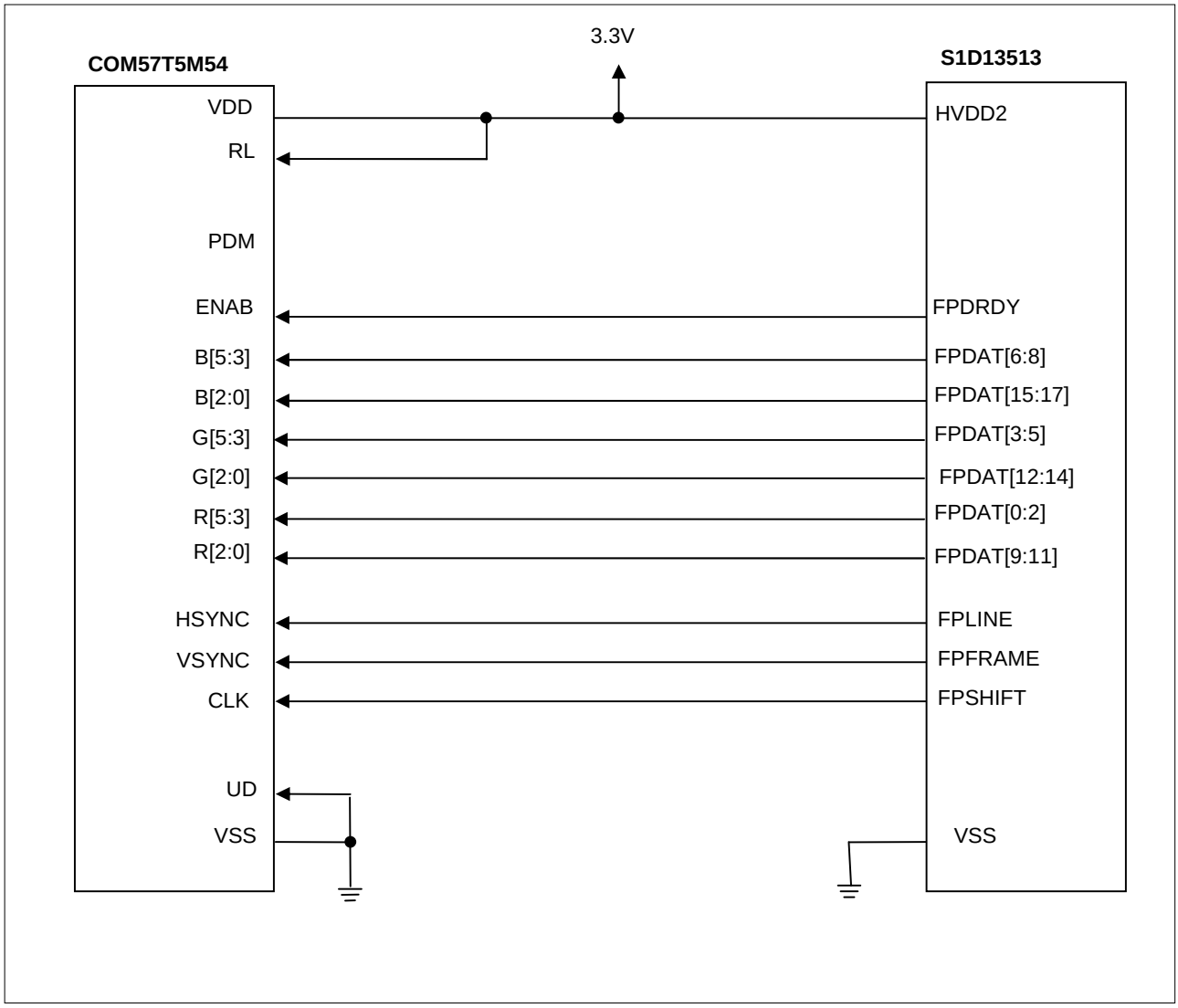

Figure 11-1 Connecting the COM57T5M54 to the S1D13513

The following table provides a detailed pin listing for the required connections between the COM57T5M54 and the S1D13513. Pin mappings are shown for both S1D13513 package types.

Table 11-2 Connecting the COM57T5M54 to the S1D13513

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
1	GND	GND	Note	Note	VSS
2	CLK	Dot clock (Capture at the falling edge)	77	P8	FPSHIFT
3	HSYNC	Horizontal synchronous signal (Negative)	79	R8	FPLINE
4	VSYNC	Vertical synchronous signal (Negative)	78	T8	FPFRAME
5	GND	GND	Note	Note	VSS
6	R0	RED data signal Data 00h displays black. R0: LSB R5: MSB Gamma correction is done inside the driver.	61	N5	FPDAT11
7	R1		62	M5	FPDAT10
8	R2		63	P6	FPDAT9
9	R3		72	T7	FPDAT2
10	R4		73	N7	FPDAT1
11	R5		74	M7	FPDAT0
12	GND	GND	Note	Note	VSS
13	G0	GREEN data signal Data 00h displays black. G0: LSB G5: MSB Gamma correction is done inside the driver.	56	R4	FPDAT14
14	G1		59	T4	FPDAT13
15	G2		60	T5	FPDAT12
16	G3		69	L7	FPDAT5
17	G4		70	P7	FPDAT4
18	G5		71	R7	FPDAT3
19	GND	GND	Note	Note	VSS
20	B0	BLUE data signal Data 00h displays black. B0: LSB B5: MSB Gamma correction is done inside the driver.	53	N4	FPDAT17
21	B1		54	P4	FPDAT16
22	B2		55	T2	FPDAT15
23	B3		64	R6	FPDAT8
24	B4		67	K6	FPDAT7
25	B5		68	M6	FPDAT6
26	GND	GND	Note	Note	VSS
27	ENAB	Input data enable (Hi-active)	78	G7	FPDRDY
28	VDD	Power +3.3V	57,65,75	L5,L8,T6	HVDD2
29	VDD	Power +3.3V	57,65,75	L5,L8,T6	HVDD2
30	RL	Horizontally Flipped (right/left) signal Lo: Flipped, Hi: Normal	57,65,75	L5,L8,T6	HVDD2
31	UD	Vertically Flipped (up/down) display control Lo: Normal, Hi: Flipped	Note	Note	VSS
32	DISP	Display control signal (Lo: Display off, Hi: Display on)	57,65,75	L5,L8,T6	HVDD2
33	GND	GND	Note	Note	VSS

Note

Allocation of VSS pin for each packages are as follows.

QFP: 10, 20, 38, 58, 66, 76, 92, 99, 106, 120, 133, 139, 151, 163, 169, 175, 184, 197

BGA: A1, A16, D4, D8, D13, G7-G10, G13, H7-H10, J1, J7-J10, K2, K7-K10, K13, N3, N6, N9, N13, T1, T16

11.2.2 Connecting the COM57T5M54 to the S1D13742

The following diagram shows an example implementation of the COM57T5M54 panel connected to the S1D13742.

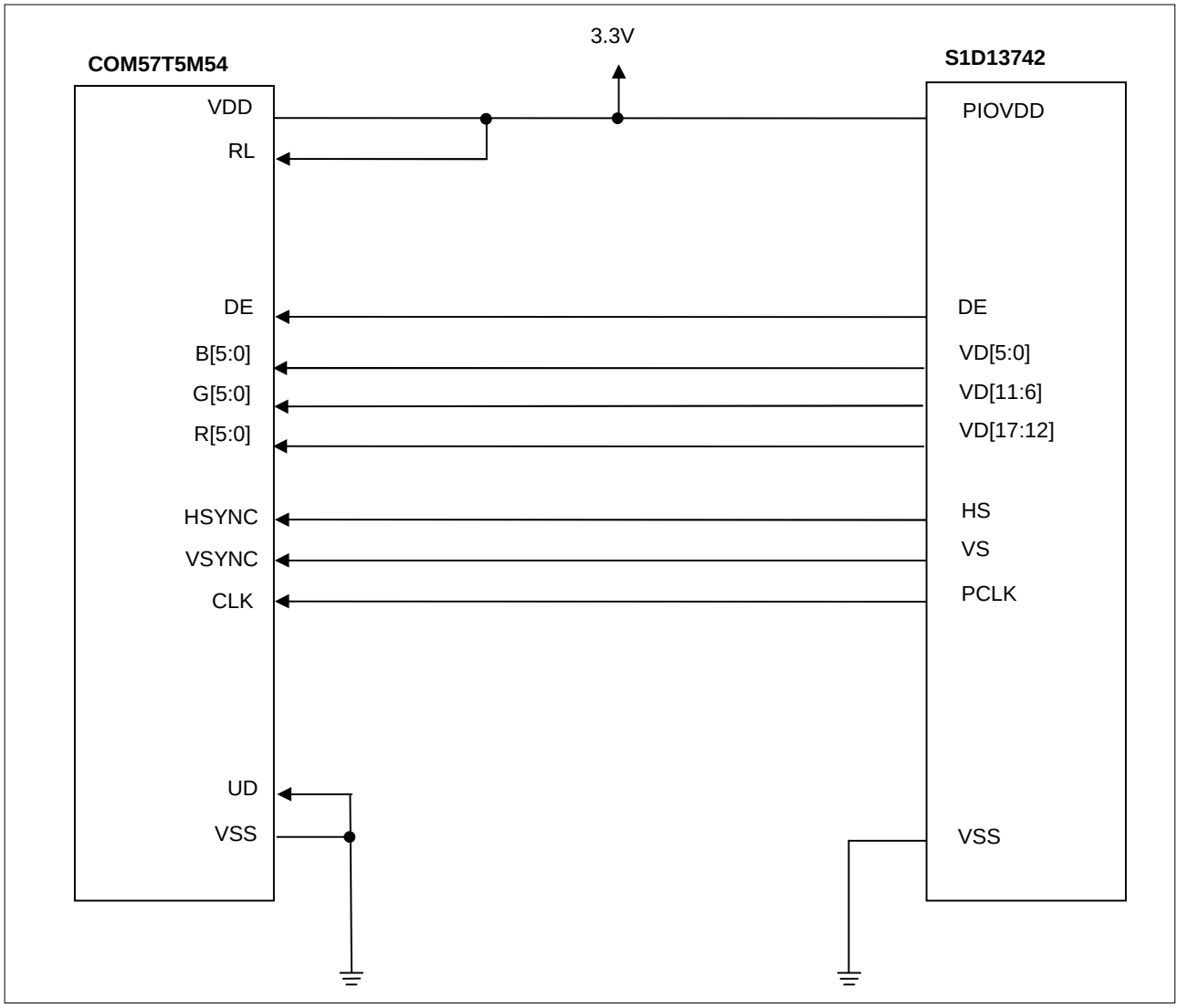

Figure 11-2 Connecting the COM57T5M54 to the S1D13742

The following table provides a detailed pin listing for the required connections between the COM57T5M54 and the S1D13742.

Table 11-3 Connecting the COM57T5M54 to the S1D13742

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13742 QFP Pin#	S1D13742 Pin Name
1	GND	GND	Note	VSS
2	CLK	Dot clock (Capture at the falling edge)	11	PCLK
3	HSYNC	Horizontal synchronous signal (Negative)	9	HS
4	VSYNC	Vertical synchronous signal (Negative)	10	VS
5	GND	GND	Note	VSS
6	R0	RED data signal Data 00h displays black. R0: LSB R5: MSB Gamma correction is done inside the driver.	61	VD12
7	R1		64	VD13
8	R2		30	VD14
9	R3		29	VD15
10	R4		43	VD16
11	R5		47	VD17
12	GND	GND	Note	VSS
13	G0	GREEN data signal Data 00h displays black. G0: LSB G5: MSB Gamma correction is done inside the driver.	66	VD6
14	G1		42	VD7
15	G2		44	VD8
16	G3		48	VD9
17	G4		51	VD10
18	G5		58	VD11
19	GND	GND	Note	VSS
20	B0	BLUE data signal Data 00h displays black. B0: SB B5: MSB Gamma correction is done inside the driver.	45	VD0
21	B1		49	VD1
22	B2		54	VD2
23	B3		59	VD3
24	B4		62	VD4
25	B5		65	VD5
26	GND	GND	Note	VSS
27	ENAB	Input data enable (Hi-active)	8	DE
28	VDD	Power +3.3V	4,17,20, 33,38,52,55,69	PIOVDD
29	VDD	Power +3.3V	4,17,20, 33,38,52,55,69	PIOVDD
30	RL	Horizontally Flipped (right/left) signal Lo: Flipped, Hi: Normal	4,17,20, 33,38,52,55,69	PIOVDD
31	UD	Vertically Flipped (up/down) display control Lo: Normal, Hi: Flipped	Note	VSS
32	DISP	Display control signal (Lo: Display off, Hi: Display on)	4,17,20, 33,38,52,55,69	PIOVDD
33	GND	GND	Note	VSS

Note

Allocation of VSS pin for each packages are as follows.

QFP: 5, 7, 18, 21, 32, 34, 39, 41, 53, 56, 68, 70, 78, 90, 103, 105, 112, 116, 119, 129, 135, 144

11.2.3 Connecting the COM57T5M54 to the S1D13748

The following diagram shows an example implementation of the COM57T5M54 panel connected to the S1D13748.

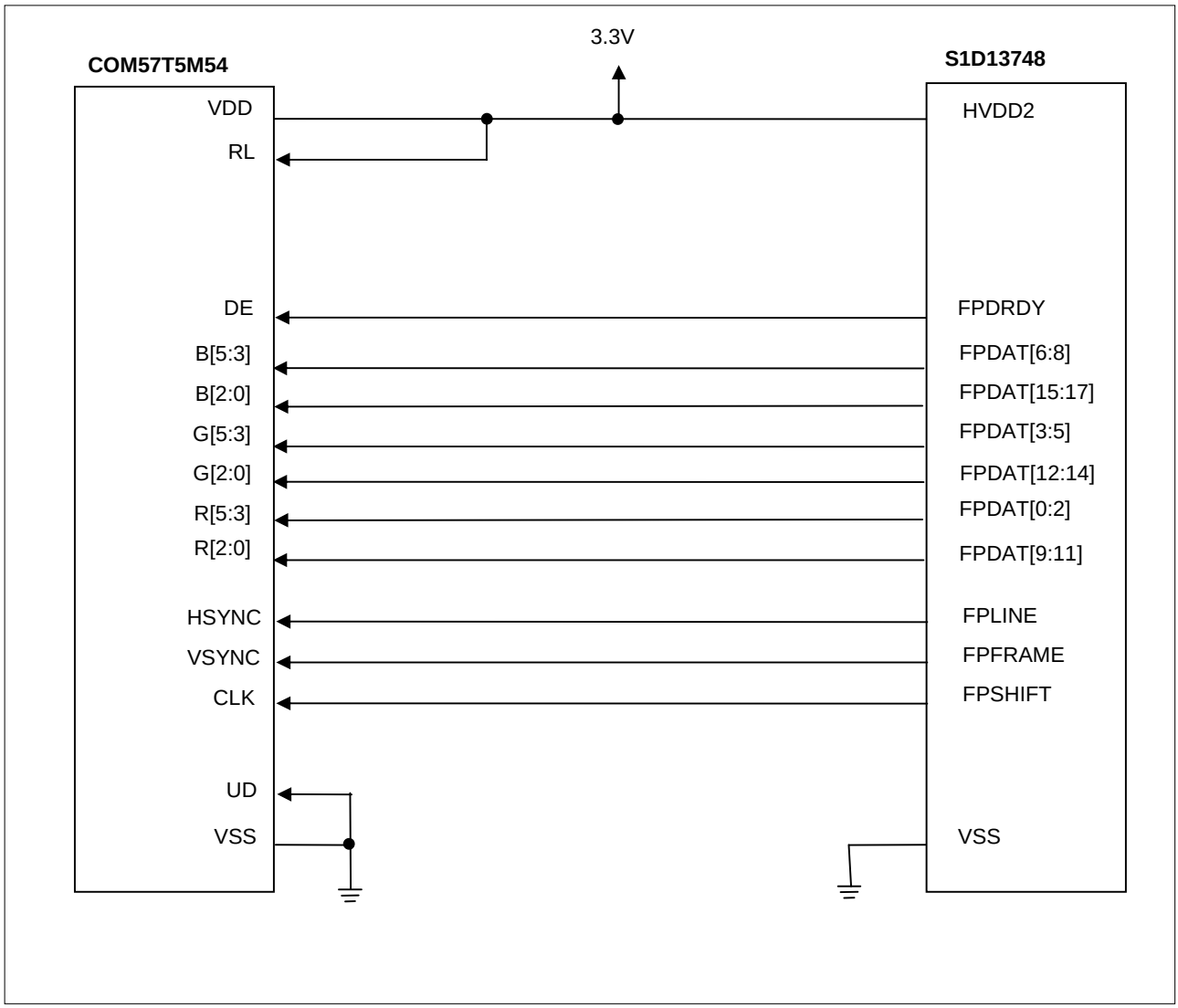

Figure 11-3 Connecting the COM57T5M54 to the S1D13748

The following table provides a detailed pin listing for the required connections between the COM57T5M54 and the S1D13748.

Table 11-4 Connecting the COM57T5M54 to the S1D13748

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
1	GND	GND	Note	Note	VSS
2	CLK	Dot clock (Capture at the falling edge)	75	J11	FPSHIFT
3	HSYNC	Horizontal synchronous signal (Negative)	77	H10	FPLINE
4	VSYNC	Vertical synchronous signal (Negative)	76	J10	FPFRAME
5	GND	GND	Note	Note	VSS
6	R0	RED data signal Data 00h displays black. R0: LSB R5: MSB Gamma correction is done inside the driver.	63	L8	FPDAT11
7	R1		62	J8	FPDAT10
8	R2		61	K8	FPDAT9
9	R3		51	K5	FPDAT2
10	R4		50	L5	FPDAT1
11	R5		49	J5	FPDAT0
12	GND	GND	Note	Note	VSS
13	G0	GREEN data signal Data 00h displays black. G0: LSB G5: MSB Gamma correction is done inside the driver.	69	H8	FPDAT14
14	G1		68	K9	FPDAT13
15	G2		64	L9	FPDAT12
16	G3		54	L6	FPDAT5
17	G4		53	J6	FPDAT4
18	G5		52	H6	FPDAT3
19	GND	GND	Note	Note	VSS
20	B0	BLUE data signal Data 00h displays black. B0: LSB B5: MSB Gamma correction is done inside the driver.	72	J9	FPDAT17
21	B1		71	K10	FPDAT16
22	B2		70	L10	FPDAT15
23	B3		60	K7	FPDAT8
24	B4		59	J7	FPDAT7
25	B5		58	L7	FPDAT6
26	GND	GND	Note	Note	VSS
27	ENAB	Input data enable (Hi-active)	78	G7	FPDRDY
28	VDD	Power +3.3V	19, 26, 35, 40, 46, 55, 67, 73, 83, 87	E8, F4, H7, J4	PIOVDD
29	VDD	Power +3.3V	19, 26, 35, 40, 46, 55, 67, 73, 83, 87	E8, F4, H7, J4	PIOVDD
30	RL	Horizontally Flipped (right/left) signal Lo: Flipped, Hi: Normal	19, 26, 35, 40, 46, 55, 67, 73, 83, 87	E8, F4, H7, J4	PIOVDD
31	UD	Vertically Flipped (up/down) display control Lo: Normal, Hi: Flipped	Note	Note	VSS
32	DISP	Display control signal (Lo: Display off, Hi: Display on)	19, 26, 35, 40, 46, 55, 67, 73, 83, 87	E8, F4, H7, J4	PIOVDD
33	GND	GND	Note	Note	VSS

Note
Allocation of VSS pin for each packages are as follows.
PFBGA: B1, C4, C8, D10, E6, F2, F8, G4, K6, K11
QFP: 6, 13, 20, 31, 36, 39, 47, 56, 66, 74, 82, 91, 97, 102, 108, 115, 129, 138, 144

11.3 Example Register Settings

In addition to the pin connections, the S1D13513/S1D13742/S1D13748 internal registers must be configured appropriately for the COM57T5M54 LCD panel. The following tables provide example settings for each display controller. However, these values are for reference only and may differ according to each specific implementation.

Also included in the table is an example clock configuration designed to achieve a typical LCD refresh.

Table 11-5 Example Register Settings for the S1D13513

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0800h] LCD Panel Type Select Register	0200h	—
REG[0802h] LCD Horizontal Total Register	031Fh	800
REG[0804h] LCD Horizontal Display Period Register	013Fh	640
REG[0806h] LCD Horizontal Display Period Start Position Register	008Fh	144
REG[0808h] LCD Horizontal Pulse Width	001Dh	30
REG[080Ah] LCD Horizontal Pulse Start Position	0000h	0
REG[080Ch] LCD Vertical Total Register	020Ch	525
REG[080Eh] LCD Vertical Display Period Resister	01DFh	480
REG[0810h] LCD Vertical Display Period Start Position Register	0023h	35
REG[0812h] LCD Vertical Pulse Width	0002h	3
REG[0814h] LCD Vertical Pulse Start Position	0000h	0
PLL2 output frequency in MHz	—	100
REG[0446h] LCD Clock Control Register	0003h	4
FPSHIFT in MHz	—	25.0
LCD Refresh in Hz	—	59.5

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13513 register values, see the *S1D13513 Hardware Functional Specification*, document number X78B-A-001-xx.

Table 11-6 Example Register Settings for the S1D13742

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[14h] Panel Type Register	00h	—
REG[16h] Horizontal Display Width Register	80	640
REG[18h] Horizontal Non-Display Period Register	240	240
REG[1Ah][1Ch] Vertical Display Height Registers	480	480
REG[1Eh] Vertical Non-Display Period Register	45	45
REG[20h] HS Pulse Width Register	30	30
REG[22h] HS Pulse Start Position Register 0	30	30
REG[24h] VS Pulse Width Register	3	3
REG[26h] VS Pulse Start Position Register 0	10	10
PLL frequency in MHz	—	50
REG[12h] Pixel Clock Configuration Register	09h	2
FPSHIFT in MHz	—	25
LCD Refresh in Hz	—	54.1

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13742 register values, see the *S1D13742 Hardware Functional Specification*, document number X63A-A-001-xx.

Table 11-7 Example Register Settings for the S1D13748

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0040h] LCD1 Horizontal Total Register	99	800
REG[0042h] LCD1 Horizontal Display Period Register	319	640
REG[0044h] LCD1 Horizontal Display Period Start Position Register	135	144
REG[0046h] LCD1 Horizontal Pulse Register	29	30
REG[0048h] LCD1 Horizontal Pulse Start Position Register	0	1
REG[004Ah] LCD1 Vertical Total Register	524	525
REG[004Ch] LCD1 Vertical Display Period Resister	479	480
REG[004Eh] LCD1 Vertical Display Period Start Position Register	35	35
REG[0050h] LCD1 Vertical Pulse Register	2	3
REG[0052h] LCD1 Vertical Pulse Start Position Register	0	1
REG[0246h] Main1 Window Image Horizontal Size Register	639	640
REG[0248h] Main1 Window Image Vertical Size Register	479	480
PLL output frequency in MHz	—	50
REG[0030h] LCD Interface Clock Setting Register	0500h	2
FPSHIFT in MHz	—	25
LCD Refresh in Hz	—	59.5

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13748 register values, see the *S1D13748 Hardware Functional Specification*, document number X80A-A-001-xx.

12 Connecting to the Ortustech COM65T6111

The Ortustech COM65T6111 TFT panel is compatible with the S1D13513, S1D13742 and S1D13748 display controllers. The following sections will provide connector details, pin mappings, and example register settings for these combinations.

12.1 COM65T6111 Pin Mapping

The COM65T6111 TFT panel uses a 45-pin connector with the following pin mapping.

Table 12-1 COM65T6111 Pin Mapping

Connector Pin#	Pin Name	Pin Description
1	VSS	GND
2	CLK	Dot clock
3	VSS	GND
4	HSYNC	Horizontal synchronous signal (Negative)
5	VSYNC	Vertical synchronous signal (Negative)
6	VSS	GND
7	TEST1	Connect to VSS
8	TEST2	Connect to VSS
9	D20	BLUE data signal (LSB)
10	D21	BLUE data signal
11	D22	BLUE data signal
12	D23	BLUE data signal
13	D24	BLUE data signal
14	D25	BLUE data signal (MSB)
15	VSS	GND
16	TEST3	Connect to VSS
17	TEST4	Connect to VSS
18	D10	GREEN data signal (LSB)
19	D11	GREEN data signal
20	D12	GREEN data signal
21	D13	GREEN data signal
22	D14	GREEN data signal
23	D15	GREEN data signal (MSB)
24	VSS	GND
25	TEST5	Connect to VSS
26	TEST6	Connect to VSS
27	D00	RED data signal (LSB)
28	D01	RED data signal
29	D02	RED data signal
30	D03	RED data signal
31	D04	RED data signal

Connector Pin#	Pin Name	Pin Description
32	D05	RED data signal (MSB)
33	VSS	GND
34	RL	Horizontal reverse display control (Lo: Reverse, Hi: Normal)
35	VDD	Power supply for logic +3.3V (3.0V≦VDD≦3.6V)
36	VDD	Power supply for logic +3.3V (3.0V≦VDD≦3.6V)
37	DISP	Display control signal Lo: OFF, Hi: ON
38	DE	Input data enable (Hi-active)
39	UD	Vertical reverse display control (Lo: Normal, Hi: Reverse)
40	VSS	GND
41	VBL	Power supply for back light +12V (10.8V≦VBL≦13.2V)
42	VBL	Power supply for back light +12V (10.8V≦VBL≦13.2V)
43	PDM	Back light dimmer control pulse input (Lo: 0% (Back light off), Hi: 100%)
44	VSS	GND
45	VSS	GND

Note
The recommended connector is a 04-6240-045-023-846+ from Kyocera elco.

12.2 Connection Examples

The information in this section provides connection examples for the S1D13513, S1D13742 and S1D13748 display controllers. Some display controllers are available in two packages. The connection information differs for each package and is listed separately.

In addition to the pin connections for the selected display controller, the COM65T6111 requires the following power supply.

VDD +3.3V (3.0V ≤ VDD ≤ 3.6V)

VBL +12V (10.8V ≤ VBL ≤ 13.2V)

For VDD, select a voltage within the supportable range of the Display Controller.

For further details on the COM65T6111, such as power consumption and absolute maximum ratings, please contact your Ortustech representative.

12.2.1 Connecting the COM65T6111 to the S1D13513

The following diagram shows an example implementation of the COM65T6111 panel connected to the S1D13513.

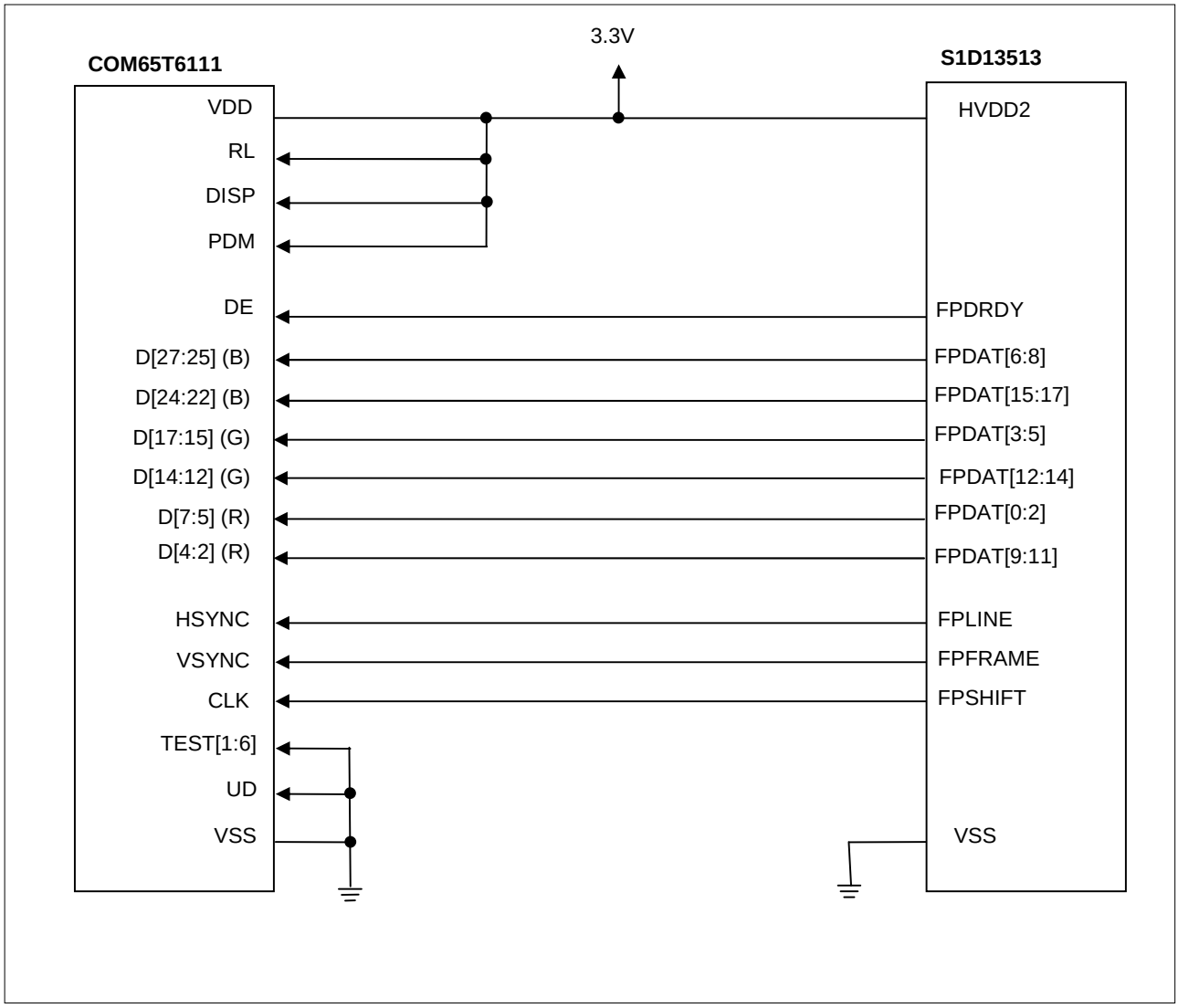

Figure 12-1 Connecting the COM65T6111 to the S1D13513

The following table provides a detailed pin listing for the required connections between the COM65T6111 and the S1D13513. Pin mappings are shown for both S1D13513 package types.

Table 12-2 Connecting the COM65T6111 to the S1D13513

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
1	VSS	GND	Note	Note	VSS
2	CLK	Dot clock	77	P8	FPSHIFT
3	VSS	GND	Note	Note	VSS
4	HSYNC	Horizontal synchronous signal (Negative)	79	R8	FPLINE
5	VSYNC	Vertical synchronous signal (Negative)	78	T8	FPFRAME
6	VSS	GND	Note	Note	VSS
7	TEST1	Connect to VSS	Note	Note	VSS
8	TEST2	Connect to VSS	Note	Note	VSS
9	D20	BLUE data signal (LSB)	53	N4	FPDAT17
10	D21	BLUE data signal	54	P4	FPDAT16
11	D22	BLUE data signal	55	T2	FPDAT15
12	D23	BLUE data signal	64	R6	FPDAT8
13	D24	BLUE data signal	67	K6	FPDAT7
14	D25	BLUE data signal (MSB)	68	M6	FPDAT6
15	VSS	GND	Note	Note	VSS
16	TEST3	Connect to VSS	Note	Note	VSS
17	TEST4	Connect to VSS	Note	Note	VSS
18	D10	GREEN data signal (LSB)	56	R4	FPDAT14
19	D11	GREEN data signal	59	T4	FPDAT13
20	D12	GREEN data signal	60	T5	FPDAT12
21	D13	GREEN data signal	69	L7	FPDAT5
22	D14	GREEN data signal	70	P7	FPDAT4
23	D15	GREEN data signal (MSB)	71	R7	FPDAT3
24	VSS	GND	Note	Note	VSS
25	TEST5	Connect to VSS	Note	Note	VSS
26	TEST6	Connect to VSS	Note	Note	VSS
27	D00	RED data signal (LSB)	61	N5	FPDAT11
28	D01	RED data signal	62	M5	FPDAT10
29	D02	RED data signal	63	P6	FPDAT9
30	D03	RED data signal	72	T7	FPDAT2
31	D04	RED data signal	73	N7	FPDAT1
32	D05	RED data signal (MSB)	74	M7	FPDAT0
33	VSS	GND	Note	Note	VSS
34	RL	Horizontal reverse display control (Lo: Reverse, Hi: Normal)	57, 65, 75	L5, L8, T6	HVDD2
35	VDD	Power supply for logic +3.3V	57, 65, 75	L5, L8, T6	HVDD2
36	VDD	Power supply for logic +3.3V	57, 65, 75	L5, L8, T6	HVDD2

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
37	DISP	Display control signal Lo:OFF, Hi:ON	57,65,75	L5,L8,T6	HVDD2
38	DE	Input data enable (Hi-active)	80	M8	FPDRDY
39	UD	Vertical reverse display control (Lo: Normal, Hi: Reverse)	Note	Note	VSS
40	VSS	GND	Note	Note	VSS
41	VBL	Power supply for back light +12V	—	—	—
42	VBL	Power supply for back light +12V	—	—	—
43	PDM	Back light dimmer control pulse input (Lo: 0%(Back light off), Hi:100%)	57, 65, 75	L5, L8, T6	HVDD2
44	VSS	GND	Note	Note	VSS
45	VSS	GND	Note	Note	VSS

Note
Allocation of VSS pin for each packages are as follows.
QFP: 10, 20, 38, 58, 66, 76, 92, 99, 106, 120, 133, 139, 151, 163, 169, 175, 184, 197
BGA: A1, A16, D4, D8, D13, G7-G10, G13, H7-H10, J1, J7-J10, K2, K7-K10, K13, N3, N6, N9, N13, T1, T16

12.2.2 Connecting the COM65T6111 to the S1D13742

The following diagram shows an example implementation of the COM65T6111 panel connected to the S1D13742.

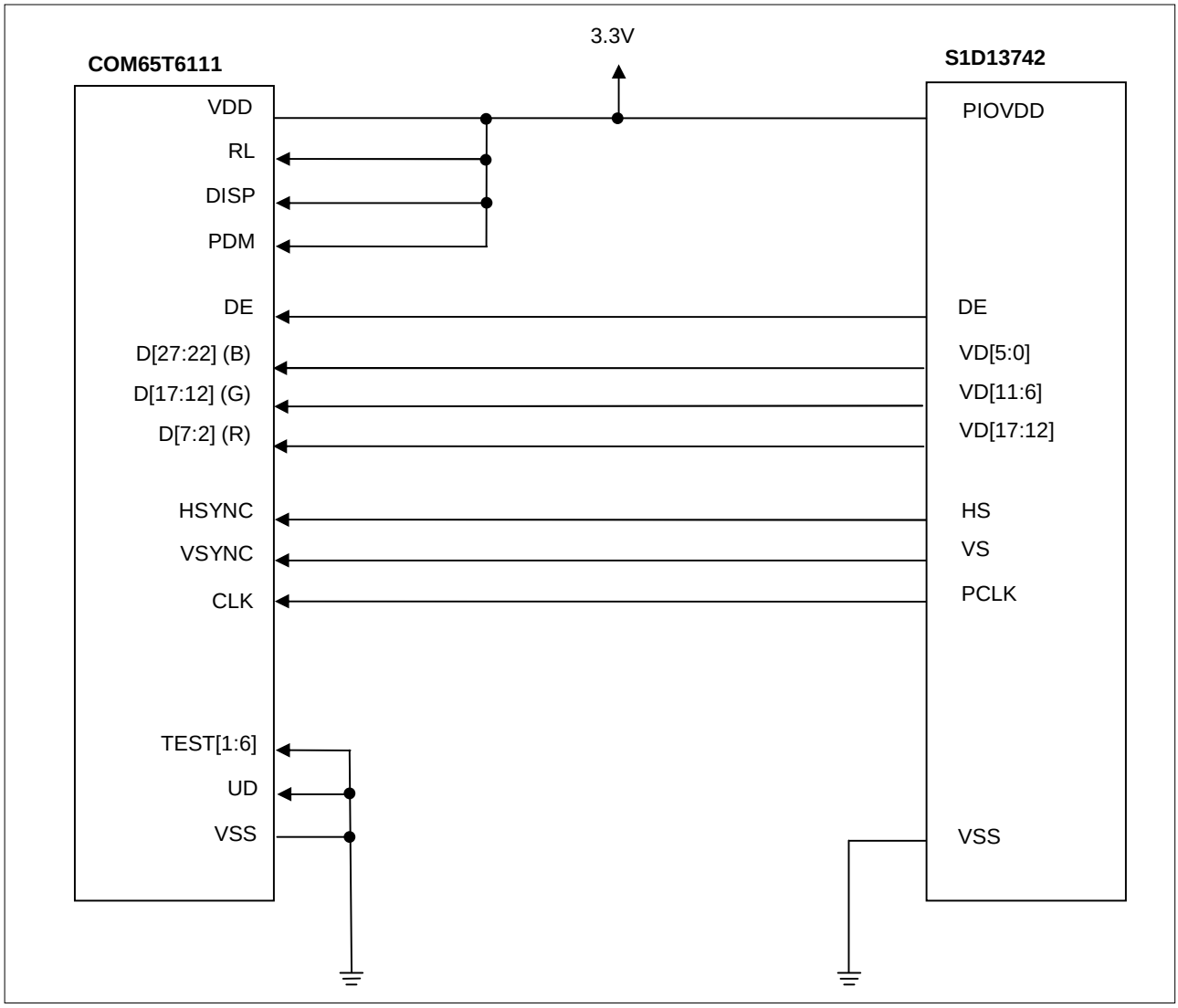

Figure 12-2 Connecting the COM65T6111 to the S1D13742

The following table provides a detailed pin listing for the required connections between the COM65T6111 and the S1D13742.

Table 12-3 Connecting the COM65T6111 to the S1D13742

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13742 QFP Pin#	S1D13742 Pin Name
1	VSS	GND	Note	VSS
2	CLK	Dot clock	11	PCLK
3	VSS	GND	Note	VSS
4	HSYNC	Horizontal synchronous signal (Negative)	9	HS
5	VSYNC	Vertical synchronous signal (Negative)	10	VS
6	VSS	GND	Note	VSS
7	TEST1	Connect to VSS	Note	VSS
8	TEST2	Connect to VSS	Note	VSS
9	D20	BLUE data signal (LSB)	45	VD0
10	D21	BLUE data signal	49	VD1
11	D22	BLUE data signal	54	VD2
12	D23	BLUE data signal	59	VD3
13	D24	BLUE data signal	62	VD4
14	D25	BLUE data signal (MSB)	65	VD5
15	VSS	GND	Note	VSS
16	TEST3	Connect to VSS	Note	VSS
17	TEST4	Connect to VSS	Note	VSS
18	D10	GREEN data signal (LSB)	66	VD6
19	D11	GREEN data signal	42	VD7
20	D12	GREEN data signal	44	VD8
21	D13	GREEN data signal	48	VD9
22	D14	GREEN data signal	51	VD10
23	D15	GREEN data signal (MSB)	58	VD11
24	VSS	GND	Note	VSS
25	TEST5	Connect to VSS	Note	VSS
26	TEST6	Connect to VSS	Note	VSS
27	D00	RED data signal (LSB)	61	VD12
28	D01	RED data signal	64	VD13
29	D02	RED data signal	30	VD14
30	D03	RED data signal	29	VD15
31	D04	RED data signal	43	VD16
32	D05	RED data signal (MSB)	47	VD17
33	VSS	GND	Note	VSS
34	RL	Horizontal reverse display control (Lo: Reverse, Hi: Normal)	4, 17, 20, 33, 38, 52, 55, 69	PIOVDD

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13742 QFP Pin#	S1D13742 Pin Name
35	VDD	Power supply for logic +3.3V	4, 17, 20, 33, 38, 52, 55, 69	PIOVDD
36	VDD	Power supply for logic +3.3V	4, 17, 20, 33, 38, 52, 55, 69	PIOVDD
37	DISP	Display control signal Lo: OFF, Hi: ON	4, 17, 20, 33, 38, 52, 55, 69	PIOVDD
38	DE	Input data enable (Hi-active)	8	DE
39	UD	Vertical reverse display control (Lo: Normal, Hi: Reverse)	Note	VSS
40	VSS	GND	Note	VSS
41	VBL	Power supply for back light +12V	—	—
42	VBL	Power supply for back light +12V	—	—
43	PDM	Back light dimmer control pulse input (Lo: 0% (Back light off), Hi: 100%)	4, 17, 20, 33, 38, 52, 55, 69	PIOVDD
44	VSS	GND	Note	VSS
45	VSS	GND	Note	VSS

Note
Allocation of VSS pin for each packages are as follows.
QFP: 5, 7, 18, 21, 32, 34, 39, 41, 53, 56, 68, 70, 78, 90, 103, 105, 112, 116, 119, 129, 135, 144

Connecting the COM65T6111 to the S1D13748

The following diagram shows an example implementation of the COM65T6111 panel connected to the S1D13748.

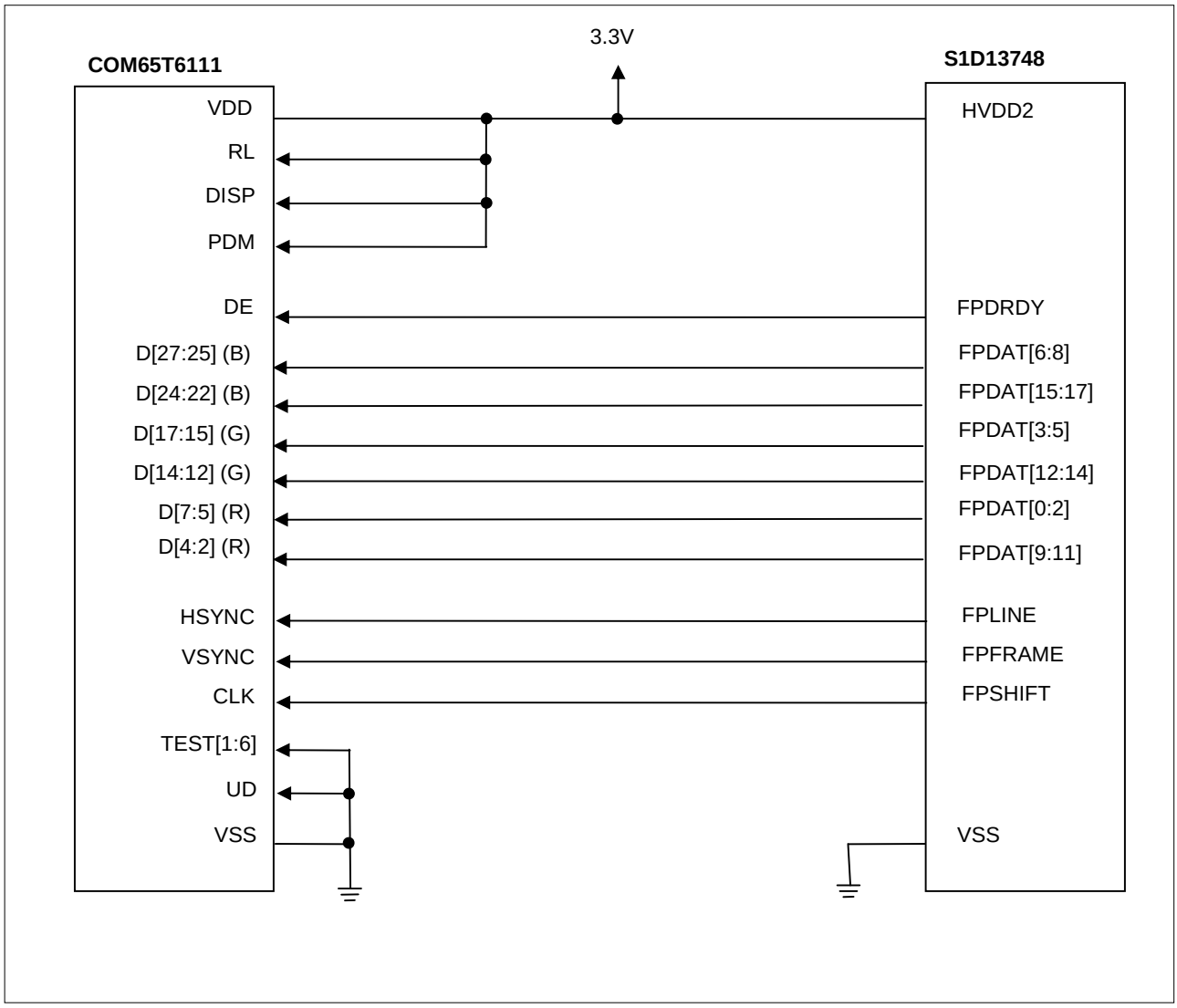

Figure 12-3 Connecting the COM65T6111 to the S1D13748

The following table provides a detailed pin listing for the required connections between the COM65T6111 and the S1D13748.

Table 12-4 Connecting the COM65T6111 to the S1D13748

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
1	VSS	GND	Note	Note	VSS
2	CLK	Dot clock	75	J11	FPSHIFT
3	VSS	GND	Note	Note	VSS
4	HSYNC	Horizontal synchronous signal (Negative)	77	H10	FPLINE
5	VSYNC	Vertical synchronous signal (Negative)	76	J10	FPFRAME
6	VSS	GND	Note	Note	VSS
7	TEST1	Connect to VSS	Note	Note	VSS
8	TEST2	Connect to VSS	Note	Note	VSS
9	D20	BLUE data signal (LSB)	72	J9	FPDAT17
10	D21	BLUE data signal	71	K10	FPDAT16
11	D22	BLUE data signal	70	L10	FPDAT15
12	D23	BLUE data signal	60	K7	FPDAT8
13	D24	BLUE data signal	59	J7	FPDAT7
14	D25	BLUE data signal (MSB)	58	L7	FPDAT6
15	VSS	GND	Note	Note	VSS
16	TEST3	Connect to VSS	Note	Note	VSS
17	TEST4	Connect to VSS	Note	Note	VSS
18	D10	GREEN data signal (LSB)	69	H8	FPDAT14
19	D11	GREEN data signal	68	K9	FPDAT13
20	D12	GREEN data signal	64	L9	FPDAT12
21	D13	GREEN data signal	54	L6	FPDAT5
22	D14	GREEN data signal	53	J6	FPDAT4
23	D15	GREEN data signal (MSB)	52	H6	FPDAT3
24	VSS	GND	Note	Note	VSS
25	TEST5	Connect to VSS	Note	Note	VSS
26	TEST6	Connect to VSS	Note	Note	VSS
27	D00	RED data signal (LSB)	63	L8	FPDAT11
28	D01	RED data signal	62	J8	FPDAT10
29	D02	RED data signal	61	K8	FPDAT9
30	D03	RED data signal	51	K5	FPDAT2
31	D04	RED data signal	50	L5	FPDAT1
32	D05	RED data signal (MSB)	49	J5	FPDAT0
33	VSS	GND	Note	Note	VSS
34	RL	Horizontal reverse display control (Lo: Reverse, Hi: Normal)	19, 26, 35, 40, 46, 55, 67, 73, 83, 87	E8, F4, H7, J4	PIOVDD

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
35	VDD	Power supply for logic +3.3V	19, 26, 35, 40, 46, 55, 67, 73, 83, 87	E8, F4, H7, J4	PIOVDD
36	VDD	Power supply for logic +3.3V	19, 26, 35, 40, 46, 55, 67, 73, 83, 87	E8, F4, H7, J4	PIOVDD
37	DISP	Display control signal; Lo: OFF, Hi: ON	19, 26, 35, 40, 46, 55, 67, 73, 83, 87	E8, F4, H7, J4	PIOVDD
38	DE	Input data enable (Hi-active)	78	G7	FPDRDY
39	UD	Vertical reverse display control (Lo: Normal, Hi: Reverse)	Note	Note	VSS
40	VSS	GND	Note	Note	VSS
41	VBL	Power supply for back light +12V	—	—	—
42	VBL	Power supply for back light +12V	—	—	—
43	PDM	Back light dimmer control pulse input (Lo: 0% (Back light off), Hi: 100%)	19, 26, 35, 40, 46, 55, 67, 73, 83, 87	E8, F4, H7, J4	PIOVDD
44	VSS	GND	Note	Note	VSS
45	VSS	GND	Note	Note	VSS

Note
Allocation of VSS pin for each packages are as follows.
PFBGA: B1, C4, C8, D10, E6, F2, F8, G4, K6, K11
QFP: 6, 13, 20, 31, 36, 39, 47, 56, 66, 74, 82, 91, 97, 102, 108, 115, 129, 138, 144

12.3 Example Register Settings

In addition to the pin connections, the S1D13513/S1D13742/S1D13748 internal registers must be configured appropriately for the COM65T6111 LCD panel. The following tables provide example settings for each display controller. However, these values are for reference only and may differ according to each specific implementation.

Also included in the table is an example clock configuration designed to achieve a typical LCD refresh.

Table 12-5 Example Register Settings for the S1D13513

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0800h] LCD Panel Type Select Register	0200h	—
REG[0802h] LCD Horizontal Total Register	031Fh	800
REG[0804h] LCD Horizontal Display Period Register	013Fh	640
REG[0806h] LCD Horizontal Display Period Start Position Register	008Fh	144
REG[0808h] LCD Horizontal Pulse Width	001Dh	30
REG[080Ah] LCD Horizontal Pulse Start Position	0000h	0
REG[080Ch] LCD Vertical Total Register	020Ch	525
REG[080Eh] LCD Vertical Display Period Resister	01DFh	480
REG[0810h] LCD Vertical Display Period Start Position Register	0023h	35
REG[0812h] LCD Vertical Pulse Width	0002h	3
REG[0814h] LCD Vertical Pulse Start Position	0000h	0
PLL2 output frequency in MHz	—	100
REG[0446h] LCD Clock Control Register	0003h	4
FPSHIFT in MHz	—	25.0
LCD Refresh in Hz	—	59.5

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13513 register values, see the *S1D13513 Hardware Functional Specification*, document number X78B-A-001-xx.

Table 12-6 Example Register Settings for the S1D13742

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[14h] Panel Type Register	00h	—
REG[16h] Horizontal Display Width Register	80	640
REG[18h] Horizontal Non-Display Period Register	240	240
REG[1Ah][1Ch] Vertical Display Height Registers	480	480
REG[1Eh] Vertical Non-Display Period Register	45	45
REG[20h] HS Pulse Width Register	30	30
REG[22h] HS Pulse Start Position Register 0	30	30
REG[24h] VS Pulse Width Register	3	3
REG[26h] VS Pulse Start Position Register 0	10	10
PLL frequency in MHz	—	50
REG[12h] Pixel Clock Configuration Register	09h	2
FPSHIFT in MHz	—	25
LCD Refresh in Hz	—	54.1

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13742 register values, see the *S1D13742 Hardware Functional Specification*, document number X63A-A-001-xx.

Table 12-7 Example Register Settings for the S1D13748

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0040h] LCD1 Horizontal Total Register	99	800
REG[0042h] LCD1 Horizontal Display Period Register	319	640
REG[0044h] LCD1 Horizontal Display Period Start Position Register	135	144
REG[0046h] LCD1 Horizontal Pulse Register	29	30
REG[0048h] LCD1 Horizontal Pulse Start Position Register	0	1
REG[004Ah] LCD1 Vertical Total Register	524	525
REG[004Ch] LCD1 Vertical Display Period Resister	479	480
REG[004Eh] LCD1 Vertical Display Period Start Position Register	35	35
REG[0050h] LCD1 Vertical Pulse Register	2	3
REG[0052h] LCD1 Vertical Pulse Start Position Register	0	1
REG[0246h] Main1 Window Image Horizontal Size Register	639	640
REG[0248h] Main1 Window Image Vertical Size Register	479	480
PLL output frequency in MHz	—	50
REG[0030h] LCD Interface Clock Setting Register	0500h	2
FPSHIFT in MHz	—	25
LCD Refresh in Hz	—	59.5

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13748 register values, see the *S1D13748 Hardware Functional Specification*, document number X80A-A-001-xx.

13 Connecting to the Ortustech COM65T6112

The Ortustech COM65T6112 TFT panel is compatible with the S1D13513, S1D13742 and S1D13748 display controllers. The following sections will provide connector details, pin mappings, and example register settings for these combinations.

13.1 COM65T6112 Pin Mapping

The COM65T6112 TFT panel uses a 45-pin connector with the following pin mapping.

Table 13-1 COM65T6112 Pin Mapping

Connector Pin#	Pin Name	Pin Description
1	VSS	GND
2	VGL	Gate driver power(-)
3	VDD	Power supply for logic +3.3V (3.0V ≤ VDD ≤ 3.6V)
4	VGH	Gate driver power(+)
5	AVDD	Power supply for analog +12V (11V ≤ AVDD ≤ 13V)
6	V10	Gamma generation reference for negative side
7	V6	Gamma generation reference for negative side
8	V5	Gamma generation reference for positive side
9	V1	Gamma generation reference for positive side
10	POCB	Power on clear input (Lo-active)
11	DISP	Display control signal (Hi: display on, Lo: display off)
12	RL	Horizontal reverse control signal input (Hi: Normal, Lo: Reverse)
13	UD	Vertical reverse control signal input (Hi: Reverse, Lo: Normal)
14	VSS	GND
15	VDD	Power supply for logic +3.3V (3.0V ≤ VDD ≤ 3.6V)
16	DE	Input data enable (Hi-active)
17	HSYNC	Horizontal synchronous signal (Negative)
18	VSYNC	Vertical synchronous signal (Negative)
19	CLK	Dot clock (Capture at the rising edge)
20	TEST5	GND
21	TEST6	GND
22	D00	RED data signal (LSB)
23	D01	RED data signal
24	D02	RED data signal
25	D03	RED data signal
26	D04	RED data signal
27	D05	RED data signal (MSB)
28	TEST3	GND
29	TEST4	GND

Connector Pin#	Pin Name	Pin Description
30	D10	GREEN data signal (LSB)
31	D11	GREEN data signal
32	D12	GREEN data signal
33	D13	GREEN data signal
34	D14	GREEN data signal
35	D15	GREEN data signal (MSB)
36	TEST1	GND
37	TEST2	GND
38	D20	BLUE data signal (LSB)
39	D21	BLUE data signal
40	D22	BLUE data signal
41	D23	BLUE data signal
42	D24	BLUE data signal
43	D25	BLUE data signal (MSB)
44	VCOM	Comon driver signal input
45	VSS	GND

Note
The recommended connector is a 04-6240-045-023-846+ from Kyocera elco.

13.2 Connection Examples

The information in this section provides connection examples for the S1D13513, S1D13742 and S1D13748 display controllers. Some display controllers are available in two packages. The connection information differs for each package and is listed separately.

In addition to the pin connections for the selected display controller, the COM65T6112 requires the following power supply.

VDD +3.3V (3.0V ≤ VDD ≤ 3.6V)

AVDD +12V (11V ≤ AVDD ≤ 13V)

VGH +21V (20V ≤ VGH ≤ 22V)

VGL -7V (-8V ≤ VGL ≤ -6V)

VCOM +4.7V (4.2V ≤ VCOM ≤ 5.2V)

V1 +10.6V (10.3V ≤ V1 ≤ 10.9V)

V5 +6.9V (6.6V ≤ V5 ≤ 7.2V)

V6 +5.7V (5.4V ≤ V6 ≤ 6.0V)

V10 +0.8V (0.7V ≤ V10 ≤ 0.9V)

VL +28.8V (VL ≤ 31.5V)

For VDD, select a voltage within the supportable range of the Display Controller.

For further details on the COM65T6112, such as power consumption and absolute maximum ratings, please contact your Ortustech representative.

13.2.1 Connecting the COM65T6112 to the S1D13513

The following diagram shows an example implementation of the COM65T6112 panel connected to the S1D13513.

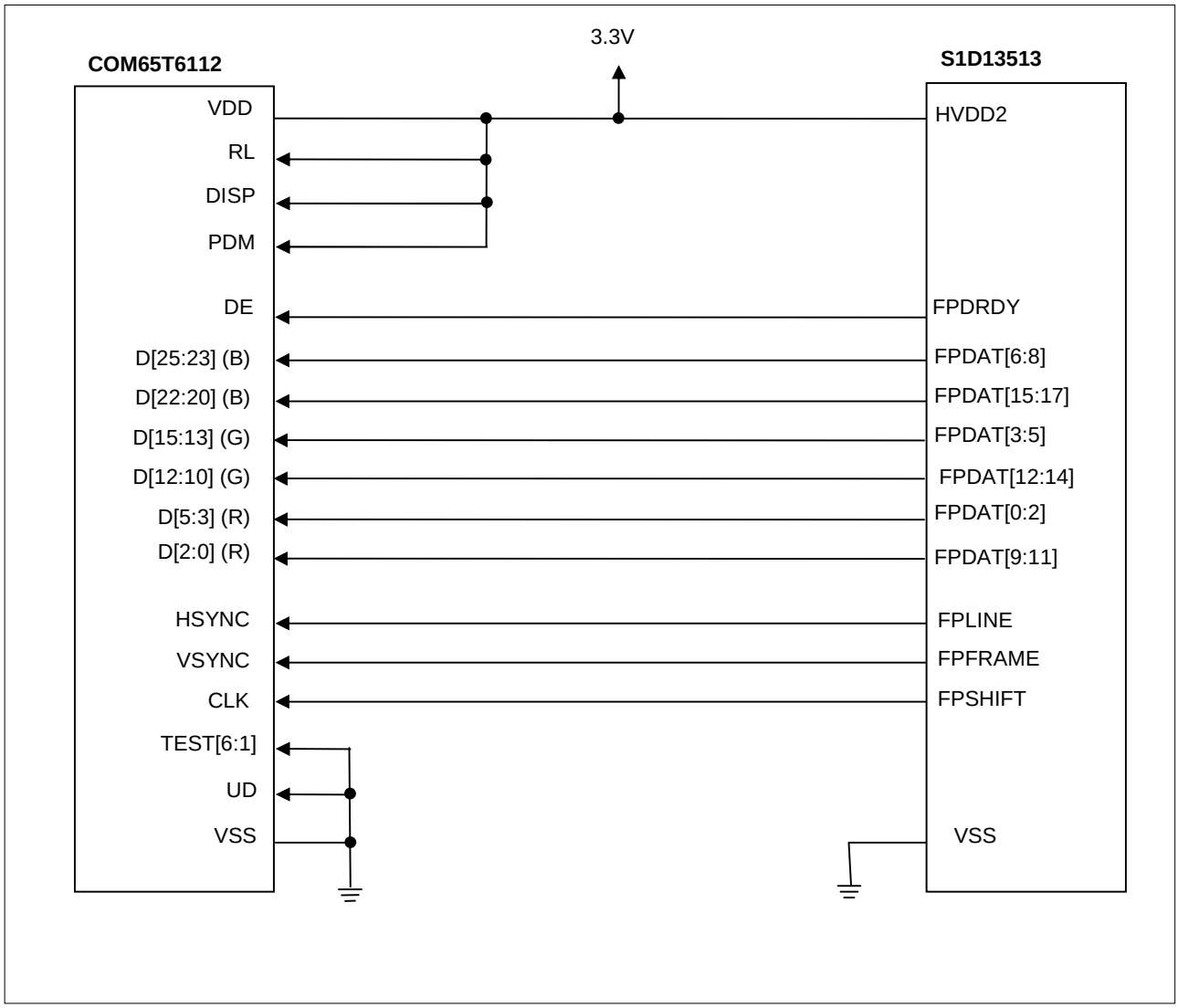

Figure 13-1 Connecting the COM65T6112 to the S1D13513

The following table provides a detailed pin listing for the required connections between the COM65T6112 and the S1D13513. Pin mappings are shown for both S1D13513 package types.

Table 13-2 Connecting the COM65T6112 to the S1D13513

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
1	VSS	GND	Note	Note	VSS
2	VGL	Gate driver power (-)	—	—	—
3	VDD	Power supply for logic +3.3V	57,65,75	L5,L8,T6	HVDD2
4	VGH	Gate driver power (+)	—	—	—
5	AVDD	Power supply for analog +12V	—	—	—
6	V10	Gamma generation reference for negative side	—	—	—
7	V6	Gamma generation reference for negative side	—	—	—
8	V5	Gamma generation reference for positive side	—	—	—
9	V1	Gamma generation reference for positive side	—	—	—
10	POCB	Power on clear input (Lo-active)	—	—	—
11	DISP	Display control signal (Hi: display on, Lo: display off)	57, 65, 75	L5, L8, T6	HVDD2
12	RL	Horizontal reverse control signal input (Hi: Normal, Lo: Reverse)	57, 65, 75	L5, L8, T6	HVDD2
13	UD	Vertical reverse control signal input (Hi: Reverse, Lo: Normal)	Note	Note	VSS
14	VSS	GND	Note	Note	VSS
15	VDD	Power supply for logic +3.3V	57, 65, 75	L5, L8, T6	HVDD2
16	DE	Input data enable (Hi-active)	80	M8	FPDRDY
17	HSYNC	Horizontal synchronous signal (Negative)	79	R8	FPLINE
18	VSYNC	Vertical synchronous signal (Negative)	78	T8	FPFRAME
19	CLK	Dot clock (Capture at the rising edge)	77	P8	FPSHIFT
20	TEST5	GND	Note	Note	VSS
21	TEST6	GND	Note	Note	VSS
22	D00	RED data signal (LSB)	61	N5	FPDAT11
23	D01	RED data signal	62	M5	FPDAT10
24	D02	RED data signal	63	P6	FPDAT9
25	D03	RED data signal	72	T7	FPDAT2
26	D04	RED data signal	73	N7	FPDAT1
27	D05	RED data signal (MSB)	74	M7	FPDAT0
28	TEST3	GND	Note	Note	VSS
29	TEST4	GND	Note	Note	VSS
30	D10	GREEN data signal (LSB)	56	R4	FPDAT14
31	D11	GREEN data signal	59	T4	FPDAT13
32	D12	GREEN data signal	60	T5	FPDAT12
33	D13	GREEN data signal	69	L7	FPDAT5
34	D14	GREEN data signal	70	P7	FPDAT4
35	D15	GREEN data signal (MSB)	71	R7	FPDAT3

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
36	TEST1	GND	Note	Note	VSS
37	TEST2	GND	Note	Note	VSS
38	D20	BLUE data signal (LSB)	53	N4	FPDAT17
39	D21	BLUE data signal	54	P4	FPDAT16
40	D22	BLUE data signal	55	T2	FPDAT15
41	D23	BLUE data signal	64	R6	FPDAT8
42	D24	BLUE data signal	67	K6	FPDAT7
43	D25	BLUE data signal (MSB)	68	M6	FPDAT6
44	VCOM	Common driver signal input	—	—	—
45	VSS	GND	Note	Note	VSS

Note
Allocation of VSS pin for each packages are as follows.
QFP: 10, 20, 38, 58, 66, 76, 92, 99, 106, 120, 133, 139, 151, 163, 169, 175, 184, 197
BGA: A1, A16, D4, D8, D13, G7-G10, G13, H7-H10, J1, J7-J10, K2, K7-K10, K13, N3, N6, N9, N13, T1, T16

13.2.2 Connecting the COM65T6112 to the S1D13742

The following diagram shows an example implementation of the COM65T6112 panel connected to the S1D13742.

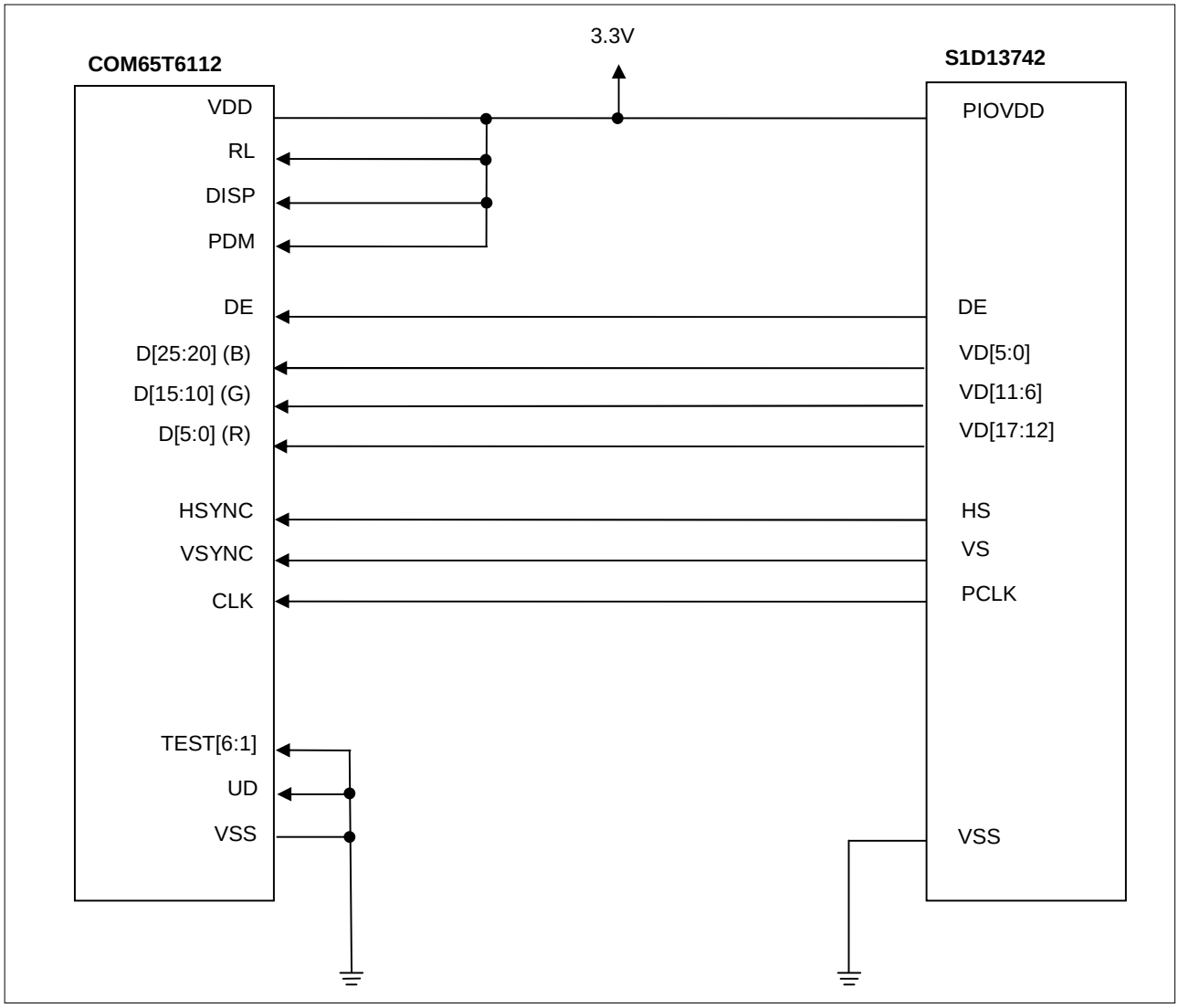

Figure 13-2 Connecting the COM65T6112 to the S1D13742

The following table provides a detailed pin listing for the required connections between the COM65T6112 and the S1D13742.

Table 13-3 Connecting the COM65T6112 to the S1D13742

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13742 QFP Pin#	S1D13742 Pin Name
1	VSS	GND	Note	VSS
2	VGL	Gate driver power (-)	—	—
3	VDD	Power supply for logic +3.3V	4, 17, 20, 33, 38, 52, 55, 69	PIOVDD
4	VGH	Gate driver power (+)	—	—
5	AVDD	Power supply for analog +12V	—	—
6	V10	Gamma generation reference for negative side	—	—
7	V6	Gamma generation reference for negative side	—	—
8	V5	Gamma generation reference for positive side	—	—
9	V1	Gamma generation reference for positive side	—	—
10	POCB	Power on clear input (Lo-active)	—	—
11	DISP	Display control signal (Hi: display on, Lo: display off)	4, 17, 20, 33, 38, 52, 55, 9	PIOVDD
12	RL	Horizontal reverse control signal input (Hi: Normal, Lo: Reverse)	4, 17, 20, 33, 38, 52, 55, 69	PIOVDD
13	UD	Vertical reverse control signal input (Hi: Reverse, Lo: Normal)	Note	VSS
14	VSS	GND	Note	VSS
15	VDD	Power supply for logic +3.3V	4, 17, 20, 33, 38, 52, 55, 69	PIOVDD
16	DE	Input data enable (Hi-active)	8	DE
17	HSYNC	Horizontal synchronous signal (Negative)	9	HS
18	VSYNC	Vertical synchronous signal (Negative)	10	VS
19	CLK	Dot clock (Capture at the rising edge)	11	PCLK
20	TEST5	GND	Note	VSS
21	TEST6	GND	Note	VSS
22	D00	RED data signal (LSB)	61	VD12
23	D01	RED data signal	64	VD13
24	D02	RED data signal	30	VD14
25	D03	RED data signal	29	VD15
26	D04	RED data signal	43	VD16
27	D05	RED data signal (MSB)	47	VD17
28	TEST3	GND	Note	VSS
29	TEST4	GND	Note	VSS
30	D10	GREEN data signal (LSB)	66	VD6

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13742 QFP Pin#	S1D13742 Pin Name
31	D11	GREEN data signal	42	VD7
32	D12	GREEN data signal	44	VD8
33	D13	GREEN data signal	48	VD9
34	D14	GREEN data signal	51	VD10
35	D15	GREEN data signal (MSB)	58	VD11
36	TEST1	GND	Note	VSS
37	TEST2	GND	Note	VSS
38	D20	BLUE data signal (LSB)	45	VD0
39	D21	BLUE data signal	49	VD1
40	D22	BLUE data signal	54	VD2
41	D23	BLUE data signal	59	VD3
42	D24	BLUE data signal	62	VD4
43	D25	BLUE data signal (MSB)	65	VD5
44	VCOM	Common driver signal input	—	—
45	VSS	GND	Note	VSS

Note

Allocation of VSS pin for each packages are as follows.

QFP: 5, 7, 18, 21, 32, 34, 39, 41, 53, 56, 68, 70, 78, 90, 103, 105, 112, 116, 119, 129, 135, 144

13.2.3 Connecting the COM65T6112 to the S1D13748

The following diagram shows an example implementation of the COM65T6112 panel connected to the S1D13748.

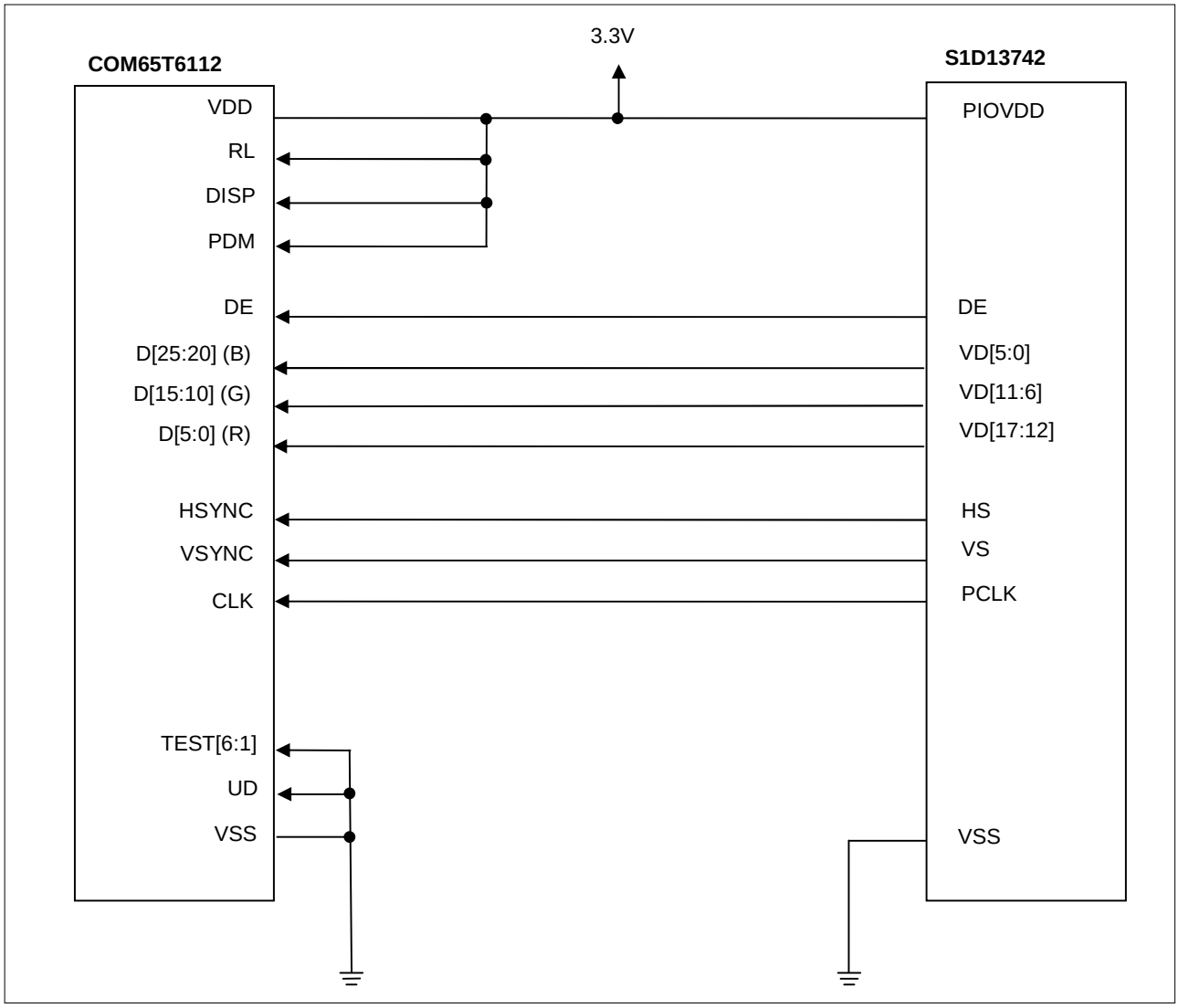

Figure 13-3 Connecting the COM65T6112 to the S1D13748

The following table provides a detailed pin listing for the required connections between the COM65T6112 and the S1D13748.

Table 13-4 Connecting the COM65T6112 to the S1D13748

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
1	VSS	GND	Note	Note	VSS
2	VGL	Gate driver power (-)	—	—	—
3	VDD	Power supply for logic +3.3V	19, 26, 35, 40, 46, 55, 67, 73, 83, 87	E8, F4, H7, J4	PIOVDD
4	VGH	Gate driver power (+)	—	—	—
5	AVDD	Power supply for analog +12V	—	—	—
6	V10	Gamma generation reference for negative side	—	—	—
7	V6	Gamma generation reference for negative side	—	—	—
8	V5	Gamma generation reference for positive side	—	—	—
9	V1	Gamma generation reference for positive side	—	—	—
10	POCB	Power on clear input (Lo-active)	—	—	—
11	DISP	Display control signal (Hi: display on, Lo: display off)	19, 26, 35, 40, 46, 55, 67, 73, 83, 87	E8, F4, H7, J4	PIOVDD
12	RL	Horizontal reverse control signal input (Hi: Normal, Lo: Reverse)	19, 26, 35, 40, 46, 55, 67, 73, 83, 87	E8, F4, H7, J4	PIOVDD
13	UD	Vertical reverse control signal input (Hi: Reverse, Lo: Normal)	Note	Note	VSS
14	VSS	GND	Note	Note	VSS
15	VDD	Power supply for logic +3.3V	19, 26, 35, 40, 46, 55, 67, 73, 83, 87	E8, F4, H7, J4	PIOVDD
16	DE	Input data enable (Hi-active)	78	G7	FPDRDY
17	HSYNC	Horizontal synchronous signal (Negative)	77	H10	FPLINE
18	VSYNC	Vertical synchronous signal (Negative)	76	J10	FPFRAME
19	CLK	Dot clock (Capture at the rising edge)	75	J11	FPSHIFT
20	TEST5	GND	Note	Note	VSS
21	TEST6	GND	Note	Note	VSS
22	D00	RED data signal (LSB)	63	L8	FPDAT11
23	D01	RED data signal	62	J8	FPDAT10
24	D02	RED data signal	61	K8	FPDAT9
25	D03	RED data signal	51	K5	FPDAT2
26	D04	RED data signal	50	L5	FPDAT1
27	D05	RED data signal (MSB)	49	J5	FPDAT0
28	TEST3	GND	Note	Note	VSS

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
29	TEST4	GND	Note	Note	VSS
30	D10	GREEN data signal (LSB)	69	H8	FPDAT14
31	D11	GREEN data signal	68	K9	FPDAT13
32	D12	GREEN data signal	64	L9	FPDAT12
33	D13	GREEN data signal	54	L6	FPDAT5
34	D14	GREEN data signal	53	J6	FPDAT4
35	D15	GREEN data signal (MSB)	52	H6	FPDAT3
36	TEST1	GND	Note	Note	VSS
37	TEST2	GND	Note	Note	VSS
38	D20	BLUE data signal (LSB)	72	J9	FPDAT17
39	D21	BLUE data signal	71	K10	FPDAT16
40	D22	BLUE data signal	70	L10	FPDAT15
41	D23	BLUE data signal	60	K7	FPDAT8
42	D24	BLUE data signal	59	J7	FPDAT7
43	D25	BLUE data signal (MSB)	58	L7	FPDAT6
44	VCOM	Common driver signal input	—	—	—
45	VSS	GND	Note	Note	VSS

Note
Allocation of VSS pin for each packages are as follows.
QFP: 6, 13, 20, 31, 36, 39, 47, 56, 66, 74, 82, 91, 97, 102, 108, 115, 129, 138, 144
PFBGA: B1, C4, C8, D10, E6, F2, F8, G4, K6, K11

13.3 Example Register Settings

In addition to the pin connections, the S1D13513/S1D13742/S1D13748 internal registers must be configured appropriately for the COM65T6112 LCD panel. The following tables provide example settings for each display controller. However, these values are for reference only and may differ according to each specific implementation.

Also included in the table is an example clock configuration designed to achieve a typical LCD refresh.

Table 13-5 Example Register Settings for the S1D13513

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0800h] LCD Panel Type Select Register	0200h	—
REG[0802h] LCD Horizontal Total Register	031Fh	800
REG[0804h] LCD Horizontal Display Period Register	013Fh	640
REG[0806h] LCD Horizontal Display Period Start Position Register	008Fh	144
REG[0808h] LCD Horizontal Pulse Width	001Dh	30
REG[080Ah] LCD Horizontal Pulse Start Position	0000h	0
REG[080Ch] LCD Vertical Total Register	020Ch	525
REG[080Eh] LCD Vertical Display Period Resister	01DFh	480
REG[0810h] LCD Vertical Display Period Start Position Register	0023h	35
REG[0812h] LCD Vertical Pulse Width	0002h	3
REG[0814h] LCD Vertical Pulse Start Position	0000h	0
PLL2 output frequency in MHz	—	100
REG[0446h] LCD Clock Control Register	0003h	4
FPSHIFT in MHz	—	25.0
LCD Refresh in Hz	—	59.5

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13513 register values, see the *S1D13513 Hardware Functional Specification*, document number X78B-A-001-xx.

Table 13-6 Example Register Settings for the S1D13742

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[14h] Panel Type Register	00h	—
REG[16h] Horizontal Display Width Register	80	640
REG[18h] Horizontal Non-Display Period Register	240	240
REG[1Ah][1Ch] Vertical Display Height Registers	480	480
REG[1Eh] Vertical Non-Display Period Register	45	45
REG[20h] HS Pulse Width Register	30	30
REG[22h] HS Pulse Start Position Register 0	30	30
REG[24h] VS Pulse Width Register	3	3
REG[26h] VS Pulse Start Position Register 0	10	10
PLL frequency in MHz	—	50
REG[12h] Pixel Clock Configuration Register	09h	2
FPSHIFT in MHz	—	25
LCD Refresh in Hz	—	54.1

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13742 register values, see the *S1D13742 Hardware Functional Specification*, document number X63A-A-001-xx.

Table 13-7 Example Register Settings for the S1D13748

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0040h] LCD1 Horizontal Total Register	99	800
REG[0042h] LCD1 Horizontal Display Period Register	319	640
REG[0044h] LCD1 Horizontal Display Period Start Position Register	135	144
REG[0046h] LCD1 Horizontal Pulse Register	29	30
REG[0048h] LCD1 Horizontal Pulse Start Position Register	0	1
REG[004Ah] LCD1 Vertical Total Register	524	525
REG[004Ch] LCD1 Vertical Display Period Resister	479	480
REG[004Eh] LCD1 Vertical Display Period Start Position Register	35	35
REG[0050h] LCD1 Vertical Pulse Register	2	3
REG[0052h] LCD1 Vertical Pulse Start Position Register	0	1
REG[0246h] Main1 Window Image Horizontal Size Register	639	640
REG[0248h] Main1 Window Image Vertical Size Register	479	480
PLL output frequency in MHz	—	50
REG[0030h] LCD Interface Clock Setting Register	0500h	2
FPSHIFT in MHz	—	25
LCD Refresh in Hz	—	59.5

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13748 register values, see the *S1D13748 Hardware Functional Specification*, document number X80A-A-001-xx.

14 Connecting to the Ortustech COM43H4M85

The Ortustech COM43H4M85 TFT panel is compatible with the S1D13513, S1D13517 and S1D13748 display controllers. The following sections will provide connector details, pin mappings, and example register settings for these combinations.

14.1 COM43H4M85 Pin Mapping

The COM43H4M85 TFT panel uses a 39-pin connector with the following pin mapping.

Table 14-1 COM43H4M85 Pin Mapping

Connector Pin#	Pin Name	Pin Description
1	VSS	GND
2	VSS	GND
3	VDD	Power +3.3V (2.7V ≤ VDD ≤ 3.6V)
4	VCCIO	Power +3.3V (1.7V ≤ VCCIO ≤ VDD)
5	VSS	GND
6	RESETB	Power on clear input (Lo-active).
7	HSYNC	Horizontal synchronous signal (Negative)
8	VSYNC	Vertical synchronous signal (Negative)
9	CLK	Dot clock (Capture at the falling edge)
10	VSS	GND
11	D00	BLUE data signal (LSB)
12	D01	BLUE data signal
13	D02	BLUE data signal
14	D03	BLUE data signal
15	D04	BLUE data signal
16	D05	BLUE data signal (MSB)
17	D10	GREEN data signal (LSB)
18	D11	GREEN data signal
19	D12	GREEN data signal
20	D13	GREEN data signal
21	D14	GREEN data signal
22	D15	GREEN data signal (MSB)
23	D20	RED data signal (LSB)
24	D21	RED data signal
25	D22	RED data signal
26	D23	RED data signal
27	D24	RED data signal
28	D25	RED data signal (MSB)
29	VSS	GND
30	DE	Input data enable (Hi-active)
31	STBYB	Standby control signal input, Lo: Standby, Hi: Normal
32	TEST1	This pin should be connected to GND.
33	NC	OPEN
34	NC	OPEN
35	NC	OPEN
36	NC	OPEN
37	TEST2	This pin should be connected to GND.
38	BLH	LED drive power (anode)
39	BLL	LED drive power (cathode)

Note
The recommended connector is a FH23-39S-0.3SHW(0.5) from Hirose Electric Co., Ltd. The connector is a 0.3mm pitch 39-pin FPC connector (12.0mm x 0.2mm gold plate).

14.2 Connection Examples

The information in this section provides connection examples for the S1D13513, S1D13517 and S1D13748 display controllers. Some display controllers are available in two packages. The connection information differs for each package and is listed separately.

In addition to the pin connections for the selected display controller, the COM43H4M85 requires the following power supply.

VDD +3.3V (2.7V ≤ VDD ≤ 3.6V)

VCCIO +3.3V (1.7V ≤ VCCIO ≤ VDD)

VL +19.6V (VL ≤ 20.3V)

For VDD, select a voltage within the supportable range of the Display Controller.

For further details on the COM43H4M85, such as power consumption and absolute maximum ratings, please contact your Ortustech representative.

14.2.1 Connecting the COM43H4M85 to the S1D13513

The following diagram shows an example implementation of the COM43H4M85 panel connected to the S1D13513.

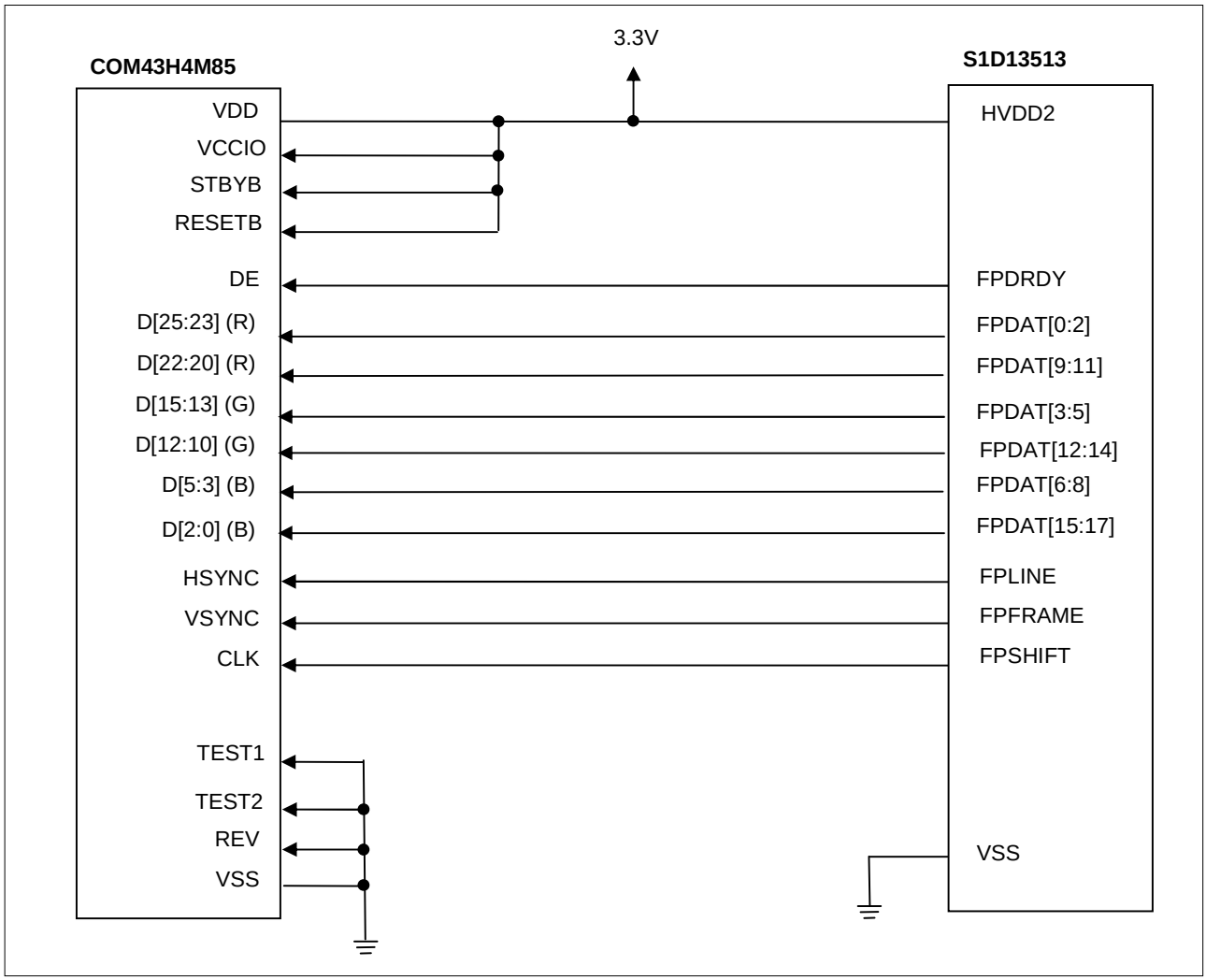

Figure 14-1 Connecting the COM43H4M85 to the S1D13513

The following table provides a detailed pin listing for the required connections between the COM43H4M85 and the S1D13513. Pin mappings are shown for both S1D13513 package types.

Table 14-2 Connecting the COM43H4M85 to the S1D13513

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
1	VSS	GND	Note	Note	VSS
2	VSS	GND	Note	Note	VSS
3	VDD	Power +3.3V	57,65,75	L5,L8,T6	HVDD2
4	VCCIO	Power +3.3V	57,65,75	L5,L8,T6	HVDD2
1	VSS	GND	Note	Note	VSS
6	RESETB	Power on clear input (Lo-active).	57,65,75	L5,L8,T6	HVDD2
7	HSYNC	Horizontal synchronous signal (Negative)	79	R8	FPLINE
8	VSYNC	Vertical synchronous signal (Negative)	78	T8	FPFRAME
9	CLK	Dot clock (Capture at the falling edge)	77	P8	FPSHIFT
10	VSS	GND	Note	Note	VSS
11	D00	BLUE data signal (LSB)	53	N4	FPDAT17
12	D01	BLUE data signal	54	P4	FPDAT16
13	D02	BLUE data signal	55	T2	FPDAT15
14	D03	BLUE data signal	64	R6	FPDAT8
15	D04	BLUE data signal	67	K6	FPDAT7
16	D05	BLUE data signal (MSB)	68	M6	FPDAT6
17	D10	GREEN data signal (LSB)	56	R4	FPDAT14
18	D11	GREEN data signal	59	T4	FPDAT13
19	D12	GREEN data signal	60	T5	FPDAT12
20	D13	GREEN data signal	69	L7	FPDAT5
21	D14	GREEN data signal	70	P7	FPDAT4
22	D15	GREEN data signal (MSB)	71	R7	FPDAT3
23	D20	RED data signal (LSB)	61	N5	FPDAT11
24	D21	RED data signal	62	M5	FPDAT10
25	D22	RED data signal	63	P6	FPDAT9
26	D23	RED data signal	72	T7	FPDAT2
27	D24	RED data signal	73	N7	FPDAT1
28	D25	RED data signal (MSB)	74	M7	FPDAT0
29	VSS	GND	Note	Note	VSS
30	DE	Input data enable (Hi-active)	80	M8	FPDRDY
31	STBYB	Standby control signal input, Lo: Standby, Hi: Normal	57,65,75	L5,L8,T6	HVDD2
32	TEST1	This pin should be connected to GND.	Note	Note	VSS
33	NC	OPEN	—	—	—
34	NC	OPEN	—	—	—
35	NC	OPEN	—	—	—
36	NC	OPEN	—	—	—
37	TEST2	This pin should be connected to GND.	Note	Note	VSS
38	BLH	LED drive power (anode)	—	—	—
39	BLL	LED drive power (cathode)	—	—	—

Note
Allocation of VSS pin for each packages are as follows.
QFP: 10, 20, 38, 58, 66, 76, 92, 99, 106, 120, 133, 139, 151, 163, 169, 175, 184, 197
BGA: A1, A16, D4, D8, D13, G7-G10, G13, H7-H10, J1, J7-J10, K2, K7-K10, K13, N3, N6, N9, N13, T1, T16

14.2.2 Connecting the COM43H4M85 to the S1D13517

The following diagram shows an example implementation of the COM43H4M85 panel connected to the S1D13517.

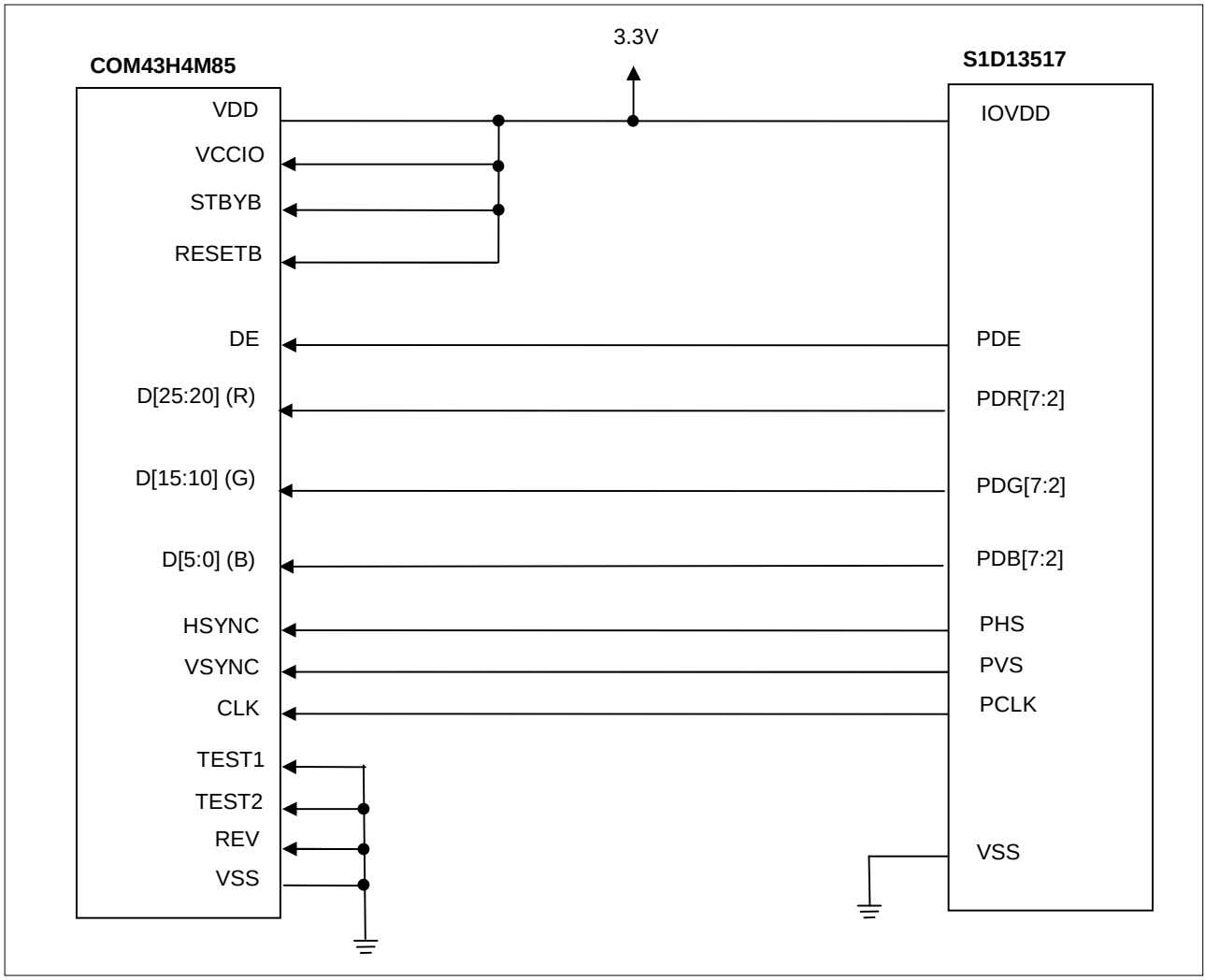

Figure 14-2 Connecting the COM43H4M85 to the S1D13517

The following table provides a detailed pin listing for the required connections between the COM43H4M85 and the S1D13517.

Table 14-3 Connecting the COM43H4M85 to the S1D13517

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13517 QFP Pin#	S1D13517 Pin Name
1	VSS	GND	Note1	VSS
2	VSS	GND	Note1	VSS
3	VDD	Power +3.3V	Note2	IOVDD
4	VCCIO	Power +3.3V	Note2	IOVDD
1	VSS	GND	Note1	VSS
6	RESETB	Power on clear input (Lo-active).	Note2	IOVDD
7	HSYNC	Horizontal synchronous signal (Negative)	83	PHS
8	VSYNC	Vertical synchronous signal (Negative)	82	PVS
9	CLK	Dot clock (Capture at the falling edge)	110	PCLK
10	VSS	GND	Note1	VSS
11	D00	BLUE data signal (LSB)	89	PDB2
12	D01	BLUE data signal	88	PDB3
13	D02	BLUE data signal	87	PDB4
14	D03	BLUE data signal	86	PDB5
15	D04	BLUE data signal	85	PDB6
16	D05	BLUE data signal (MSB)	84	PDB7
17	D10	GREEN data signal (LSB)	99	PDG2
18	D11	GREEN data signal	98	PDG3
19	D12	GREEN data signal	95	PDG4
20	D13	GREEN data signal	94	PDG5
21	D14	GREEN data signal	93	PDG6
22	D15	GREEN data signal (MSB)	92	PDG7
23	D20	RED data signal (LSB)	107	PDR2
24	D21	RED data signal	106	PDR3
25	D22	RED data signal	105	PDR4
26	D23	RED data signal	104	PDR5
27	D24	RED data signal	103	PDR6
28	D25	RED data signal (MSB)	102	PDR7
29	VSS	GND	Note1	VSS
30	DE	Input data enable (Hi-active)	81	PDE
31	STBYB	Standby control signal input, Lo: Standby, Hi: Normal	Note2	IOVDD
32	TEST1	This pin should be connected to GND.	Note1	VSS
33	NC	OPEN	—	—
34	NC	OPEN	—	—
35	NC	OPEN	—	—
36	NC	OPEN	—	—
37	TEST2	This pin should be connected to GND.	Note1	VSS
38	BLH	LED drive power (anode)	—	—
39	BLL	LED drive power (cathode)	—	—

Note 1
Allocation of VSS pin for each packages are as follows.
QFP: 1, 17, 24, 32, 48, 54, 65, 80, 97, 114

Note 2
Allocation of IOVDD pin for each packages are as follows.
QFP: 16, 31, 47, 64, 79, 96, 113, 128

14.2.3 Connecting the COM43H4M85 to the S1D13748

The following diagram shows an example implementation of the COM43H4M85 panel connected to the S1D13748.

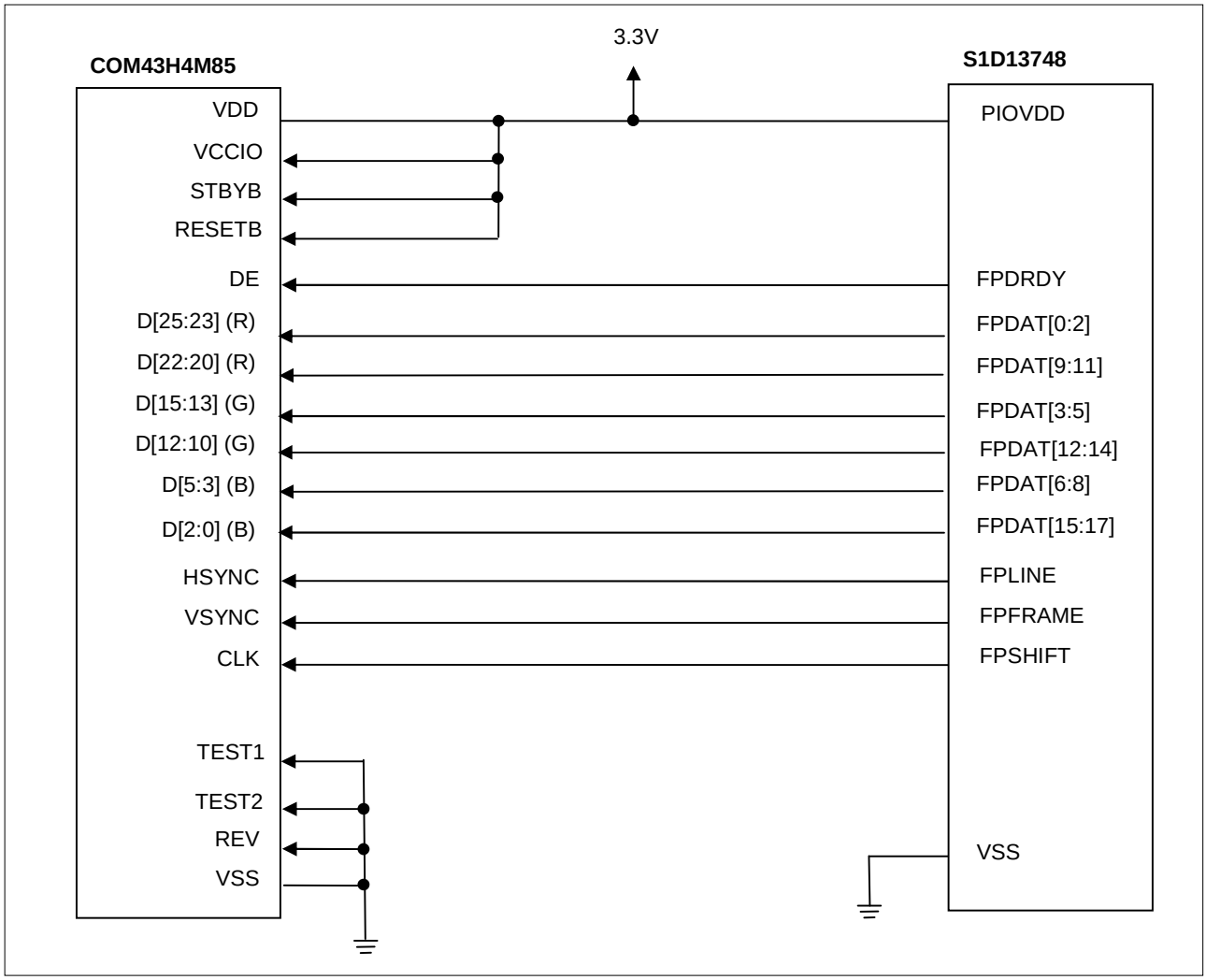

Figure 14-3 Connecting the COM43H4M85 to the S1D13748

The following table provides a detailed pin listing for the required connections between the COM43H4M85 and the S1D13748.

Table 14-4 Connecting the COM43H4M85 to the S1D13748

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
1	VSS	GND	Note	Note	VSS
2	VSS	GND	Note	Note	VSS
3	VDD	Power +3.3V	19, 26, 35, 40, 46, 55, 67, 73, 83, 87	E8, F4, H7, J4	PIOVDD
4	VCCIO	Power +3.3V	19, 26, 35, 40, 46, 55, 67, 73, 83, 87	E8, F4, H7, J4	PIOVDD
1	VSS	GND	Note	Note	VSS
6	RESETB	Power on clear input (Lo-active).	19, 26, 35, 40, 46, 55, 67, 73, 83, 87	E8, F4, H7, J4	PIOVDD
7	HSYNC	Horizontal synchronous signal (Negative)	77	H10	FPLINE
8	VSYNC	Vertical synchronous signal (Negative)	76	J10	FPFRAME
9	CLK	Dot clock (Capture at the falling edge)	75	J11	FPSHIFT
10	VSS	GND	Note	Note	VSS
11	D00	BLUE data signal (LSB)	72	J9	FPDAT17
12	D01	BLUE data signal	71	K10	FPDAT16
13	D02	BLUE data signal	70	L10	FPDAT15
14	D03	BLUE data signal	60	K7	FPDAT8
15	D04	BLUE data signal	59	J7	FPDAT7
16	D05	BLUE data signal (MSB)	58	L7	FPDAT6
17	D10	GREEN data signal (LSB)	69	H8	FPDAT14
18	D11	GREEN data signal	68	K9	FPDAT13
19	D12	GREEN data signal	64	L9	FPDAT12
20	D13	GREEN data signal	54	L6	FPDAT5
21	D14	GREEN data signal	53	J6	FPDAT4
22	D15	GREEN data signal (MSB)	52	H6	FPDAT3
23	D20	RED data signal (LSB)	63	L8	FPDAT11
24	D21	RED data signal	62	J8	FPDAT10
25	D22	RED data signal	61	K8	FPDAT9
26	D23	RED data signal	51	K5	FPDAT2
27	D24	RED data signal	50	L5	FPDAT1
28	D25	RED data signal (MSB)	49	J5	FPDAT0
29	VSS	GND	Note	Note	VSS
30	DE	Input data enable (Hi-active)	78	G7	FPDRDY
31	STBYB	Standby control signal input, Lo: Standby, Hi: Normal	19, 26, 35, 40, 46, 55, 67, 73, 83, 87	E8, F4, H7, J4	PIOVDD
32	TEST1	This pin should be connected to GND.	Note	Note	VSS
33	NC	OPEN	—	—	—
34	NC	OPEN	—	—	—
35	NC	OPEN	—	—	—

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
36	NC	OPEN	—	—	—
37	TEST2	This pin should be connected to GND.	Note	Note	VSS
38	BLH	LED drive power (anode)	—	—	—
39	BLL	LED drive power (cathode)	—	—	—

Note

Allocation of VSS pin for each packages are as follows.
QFP: 6, 13, 20, 31, 36, 39, 47, 56, 66, 74, 82, 91, 97, 102, 108, 115, 129, 138, 144
PFBGA: B1, C4, C8, D10, E6, F2, F8, G4, K6, K11

14.3 Example Register Settings

In addition to the pin connections, the S1D13513/S1D13517/S1D13748 internal registers must be configured appropriately for the COM43H4M85 LCD panel. The following tables provide example settings for each display controller. However, these values are for reference only and may differ according to each specific implementation.

Also included in the table is an example clock configuration designed to achieve a typical LCD refresh.

Table 14-5 Example Register Settings for the S1D13513

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0800h] LCD Panel Type Select Register	0280h	18bpp mode, FPSHIFT polarity is rising edge.
REG[0802h] LCD Horizontal Total Register	0201h	514
REG[0804h] LCD Horizontal Display Period Register	0076h	239
REG[0806h] LCD Horizontal Display Period Start Position Register	0017h	24
REG[0808h] LCD Horizontal Pulse Width	0008h	9
REG[080Ah] LCD Horizontal Pulse Start Position	0000h	0
REG[080Ch] LCD Vertical Total Register	0327h	808
REG[080Eh] LCD Vertical Display Period Resister	031Eh	799
REG[0810h] LCD Vertical Display Period Start Position Register	0006h	6
REG[0812h] LCD Vertical Pulse Width	0001h	2
REG[0814h] LCD Vertical Pulse Start Position	0000h	0
PLL2 output frequency in MHz	—	100
REG[0446h] LCD Clock Control Register	0003h	4
FPSHIFT in MHz	—	25
LCD Refresh in Hz	—	60.20

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13513 register values, see the *S1D13513 Hardware Functional Specification*, document number X78B-A-001-xx.

Table 14-6 Example Register Settings for the S1D13517

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[14h] LCD Panel Type Register	01h	24bpp mode1(packed), 18-bit
REG[16h] Horizontal Display Width Register (HDISP)	3Bh	480
REG[18h] Horizontal Non-Display Period Register (HNDP)	10h	34
REG[1Ah] Vertical Display Height Register 0 (VDISP)	1Fh	800
REG[1Ch] Vertical Display Height Register 1 (VDISP)	03h	—
REG[1Eh] Vertical Non-Display Period Register (VNDP)	3h	8
REG[20h] PHS Pulse Width Register (HSW)	8h	9
REG[22h] PHS Pulse Start Position Register (HPS)	0h	0
REG[24h] PVS Pulse Width Register (VSW)	1h	2
REG[26h] PVS Pulse Start Position Register (VPS)	3h	3
REG[28h] PCLK Polarity Register	00h	PCLK polarity is rising edge.
REG[04h] PLL D-Divider Register	97h	PLL D-div is 1:24. Input 24MHz -> Output 1MHz: Bit-5-0=17h PLL enable: Bit-7=1b
REG[06h] PLL Setting Register 0	51h	PLL output = 150MHz
REG[08h] PLL Setting Register 1	01h	PLL clock Divide ratio = 1/2. (150MHz /2)
REG[0Ch] PLL N-Divider Register	4Ah	PLL N-counter 75MHz
REG[0Eh] SS Control Register 0	3Fh	SS disabled
REG[12h] Clock Source Select Register	80h	SYSCLK = 1/3 (75MHz/3 = 25MHz)
REG[8Ch] SDRAM Refresh Counter Register 0	92h	Refresh counter 64msec/4096=15.63us (IS42S16800E-7TLI) should be bigger than this setting. 1/75MHz x 1170 =15.6us
REG[8Eh] SDRAM Refresh Counter Register 1	04h	—
FPSHIFT in MHz	—	25
LCD Refresh in Hz	—	60.20

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13517 register values, see the *S1D13517 Hardware Functional Specification*, document number X63A-A-001-xx.

Table 14-7 Example Register Settings for the S1D13748

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0040h] LCD1 Horizontal Total Register	3Fh	512
REG[0042h] LCD1 Horizontal Display Period Register	EFh	480
REG[0044h] LCD1 Horizontal Display Period Start Position Register	Fh	24
REG[0046h] LCD1 Horizontal Pulse Register	88h	9
REG[0048h] LCD1 Horizontal Pulse Start Position Register	0h	1
REG[004Ah] LCD1 Vertical Total Register	327h	808
REG[004Ch] LCD1 Vertical Display Period Resister	31Fh	800
REG[004Eh] LCD1 Vertical Display Period Start Position Register	6h	6
REG[0050h] LCD1 Vertical Pulse Register	1h	2
REG[0052h] LCD1 Vertical Pulse Start Position Register	0h	0
REG[0246h] Main1 Window Image Horizontal Size Register	1DFh	480
REG[0248h] Main1 Window Image Vertical Size Register	31Fh	800
PLL output frequency in MHz	—	50
REG[0030h] LCD Interface Clock Setting Register	0500h	2
FPSHIFT in MHz	—	25
LCD Refresh in Hz	—	60.4

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13748 register values, see the *S1D13748 Hardware Functional Specification*, document number X80A-A-001-xx.

15 Change Record

X00A-G-008-01 Revision 1.4 - Issued: June 24, 2013

- Changed and changed connective LCD panels

X00A-G-008-01 Revision 1.0 - Issued: April 20, 2012

- Re-format and edit document for release

EPSON

International Sales Operations

AMERICA

EPSON ELECTRONICS AMERICA, INC.

214 Devcon Drive,
San Jose, CA 95112, USA
Phone: +1-800-228-3964 FAX: +1-408-922-0238

EUROPE

EPSON EUROPE ELECTRONICS GmbH

Riesstrasse 15, 80992 Munich,
GERMANY
Phone: +49-89-14005-0 FAX: +49-89-14005-110

ASIA

EPSON (CHINA) CO., LTD.

7F, Jinbao Bldg., No.89 Jinbao St.,
Dongcheng District,
Beijing 100005, CHINA
Phone: +86-10-8522-1199 FAX: +86-10-8522-1125

SHANGHAI BRANCH

7F, Block B, Hi-Tech Bldg., 900 Yishan Road,
Shanghai 200233, CHINA
Phone: +86-21-5423-5577 FAX: +86-21-5423-4677

SHENZHEN BRANCH

12F, Dawning Mansion, Keji South 12th Road,
Hi-Tech Park, Shenzhen 518057, CHINA
Phone: +86-755-2699-3828 FAX: +86-755-2699-3838

EPSON HONG KONG LTD.

Unit 715-723, 7/F Trade Square, 681 Cheung Sha Wan Road,
Kowloon, Hong Kong.
Phone: +852-2585-4600 FAX: +852-2827-4346

EPSON TAIWAN TECHNOLOGY & TRADING LTD.

14F, No. 7, Song Ren Road,
Taipei 110, TAIWAN
Phone: +886-2-8786-6688 FAX: +886-2-8786-6660

EPSON SINGAPORE PTE., LTD.

1 HarbourFront Place,
#03-02 HarbourFront Tower One, Singapore 098633
Phone: +65-6586-5500 FAX: +65-6271-3182

SEIKO EPSON CORP.
KOREA OFFICE

5F, KLI 63 Bldg., 60 Yoido-dong,
Youngdeungpo-Ku, Seoul 150-763, KOREA
Phone: +82-2-784-6027 FAX: +82-2-767-3677

SEIKO EPSON CORP.
MICRODEVICES OPERATIONS DIVISION

IC Sales & Marketing Department

421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-42-587-5814 FAX: +81-42-587-5117

Document Code: X94A-G-008-01
First Issue April 2012
Revised June 2013 in JAPAN