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Connecting EPSON Display Controllers to Kyocera LCD Panels

Document Number: X00A-G-007-01

Issue Date: 2012/04/18

SEIKO EPSON CORPORATION

Rev. 1.0

NOTICE

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1 Introduction

This document provides connection information enabling EPSON Display Controllers to control a variety of Kyocera Corp. LCD panels. This document includes connector details, pin mappings, and example register settings.

For detailed technical information on EPSON Display Controllers or Kyocera LCD panels, please refer to the specification or technical manual for each product.

This document is updated as appropriate. Please check for the latest revision of this document before beginning any development. The latest revision can be downloaded at www.erd.epson.com.

2 Display Controller Compatibility

This document discusses the following Kyocera LCD panels.

- KCG057QV1DB-G70 (5.7 inch、QVGA)
- KG057QV1CA-G05 (5.7 inch、QVGA)
- TCG057QV1AC-G10 (5.7 inch、QVGA)
- TCG057VG1AC-G00 (5.7 inch、VGA)
- KCG062HV1AA-A21 (6.2 inch、HVGA)
- KCG062HV1AE-G03 (6.2 inch、HVGA)
- TCG062HV1AE-G00 (6.2 inch、HVGA)
- KCG075VG2BE-G00 (7.5 inch、VGA)
- TCG075VG2AC-G00 (7.5 inch、VGA)
- TCG085WV1AB-G00 (8.5 inch、WVGA)
- TCG104VG2AA-G00 (10.4 inch、VGA)

Each Kyocera LCD panel is compatible with one or more of the following EPSON display controllers.

- S1D13513 (QFP 208-pin or PBGA 256-pin)
- S1D13700 (TQFP 64-pin)
- S1D13706 (TQFP 100-pin)
- S1D13A05 (PFBGA 121-pin or QFP 128-pin)
- S1D13719 (PFBGA 180-pin or QFP 208-pin)
- S1D13742 (FCBGA 121-pin or QFP 144-pin)
- S1D13743 (FCBGA 121-pin or QFP 144-pin)
- S1D13748 (PFBGA 121-pin or QFP 144-pin)

The following table summarizes which EPSON display controllers are compatible with each Kyocera LCD panels.

Kyocera Panel	S1D13513	S1D13700	S1D13706	S1D13A05	S1D13719	S1D13742	S1D13743	S1D13748
KCG057QV1DB-G70	√	—	√	√	—	—	—	—
KG057QV1CA-G05	√	√	√	√	—	—	—	—
TCG057QV1AC-G10	√	—	—	—	√	√	√	√
TCG057VG1AC-G00	√	—	—	—	—	—	—	—
KCG062HV1AA-A21	√	—	—	—	—	—	—	—
KCG062HV1AE-G03	√	—	—	—	—	—	—	—
TCG062HV1AE-G00	√	—	—	—	—	√	√	√
KCG075VG2BE-G00	√	—	—	—	—	—	—	—
TCG075VG2AC-G00	√	—	—	—	—	—	—	√
TCG085WV1AB-G00	√	—	—	—	—	√	—	√
TCG104VG2AA-G00	√	—	—	—	—	—	—	—

3 Connecting to the Kyocera KCG057QV1DB-G70

The Kyocera KCG057QV1DB-G70 LCD panel is compatible with the S1D13513, S1D13706, and S1D13A05 display controllers. The following sections will provide connector details, pin mappings, and example register settings for these combinations.

3.1 KCG057QV1DB-G70 Pin Mapping

The KCG057QV1DB-G70 LCD panel uses a 20-pin connector with the following pin mapping.

Table 3-1 KCG057QV1DB-G70 Pin Mapping

Connector Pin#	Pin Name	Pin Description
1	FRM	Synchronous signal for drive scanning line
2	LOAD	Data signal latch clock
3	CP	Data signal shift clock
4	DISP	Display control signal
5	VDD	Power supply for logic (+5V)
6	VSS	GND
7	VCONT	LCD adjust voltage (+1.3V ≤ VCONT ≤ +2.3V)
8	D7	Data signal (MSB)
9	D6	Data signal
10	D5	Data signal
11	D4	Data signal
12	D3	Data signal
13	D2	Data signal
14	D1	Data signal
15	D0	Data signal (LSB)
16	VDD	Power supply for logic (+5V)
17	VDD	Power supply for logic (+5V)
18	VSS	GND
19	VSS	GND
20	VSS	GND

Note
The recommended mounting connector is a Kyocera 08-6210-020-340-800+. The connector is a 0.5mm pitch 20-pin FPC connector (10.5mm x 0.3mm gold plate).

3.2 Connection Examples

The information in this section provides connection examples for the S1D13513, S1D13706, and S1D13A05 display controllers. For the S1D13513 and S1D13A05, the display controller is available in two packages. The connection information differs for each package and is listed separately.

In addition to the pin connections for the selected display controller, the KCG057QV1DB-G70 requires the following power supplies.

VDD	+5.0V (±0.25V)
VCONT (liquid crystal drive power supply)	+1.8V (±0.5V)

For further details on the KCG057QV1DB-G70, such as power consumption and absolute maximum ratings, please contact your Kyocera representative.

3.2.1 Connecting the KCG057QV1DB-G70 Panel to the S1D13513

The following diagram shows an example implementation of the KCG057QV1DB-G70 panel connected to the S1D13513.

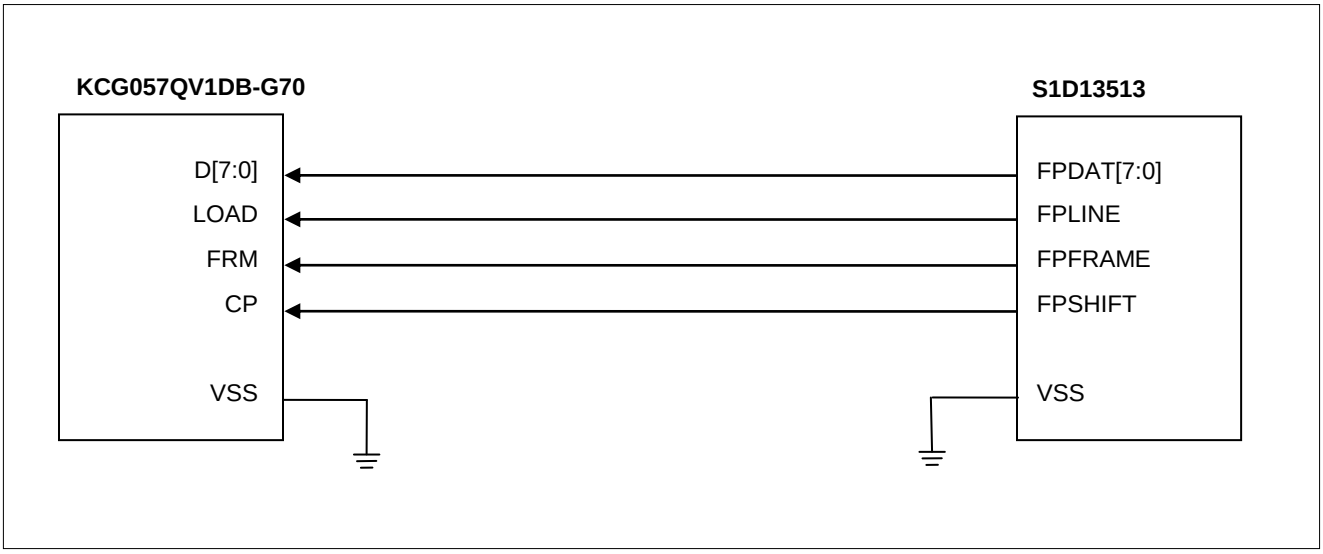

Figure 3-1 Connecting the KCG057QV1DB-G70 Panel to the S1D13513

The following table provides a detailed pin listing for the required connections between the KCG057QV1DB-G70 and the S1D13513. Pin mappings are shown for both S1D13513 package types.

Table 3-2 Connecting the KCG057QV1DB-G70 Panel to the S1D13513

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
1	FRM	Synchronous signal for drive scanning line	78	T8	FPFRAME
2	LOAD	Data signal latch clock	79	R8	FPLINE
3	CP	Data signal shift clock	77	P8	FPSHIFT
4	DISP	Display control signal	—	—	—
5	VDD	Power supply for logic (+5V)	—	—	—
6	VSS	GND	—	—	VSS
7	VCONT	LCD adjust voltage (+1.3V ≤ VCONT ≤ +2.3V)	—	—	—
8	D7	Data signal (MSB)	67	K6	FPDAT7
9	D6	Data signal	68	M6	FPDAT6
10	D5	Data signal	69	L7	FPDAT5
11	D4	Data signal	70	P7	FPDAT4
12	D3	Data signal	71	R7	FPDAT3
13	D2	Data signal	72	T7	FPDAT2
14	D1	Data signal	73	N7	FPDAT1
15	D0	Data signal (LSB)	74	M7	FPDAT0
16	VDD	Power supply for logic (+5V)	—	—	—
17	VDD	Power supply for logic (+5V)	—	—	—
18	VSS	GND	—	—	VSS
19	VSS	GND	—	—	VSS
20	VSS	GND	—	—	VSS

3.2.2 Connecting the KCG057QV1DB-G70 to the S1D13706

The following diagram shows an example implementation of the KCG057QV1DB-G70 panel connected to the S1D13706.

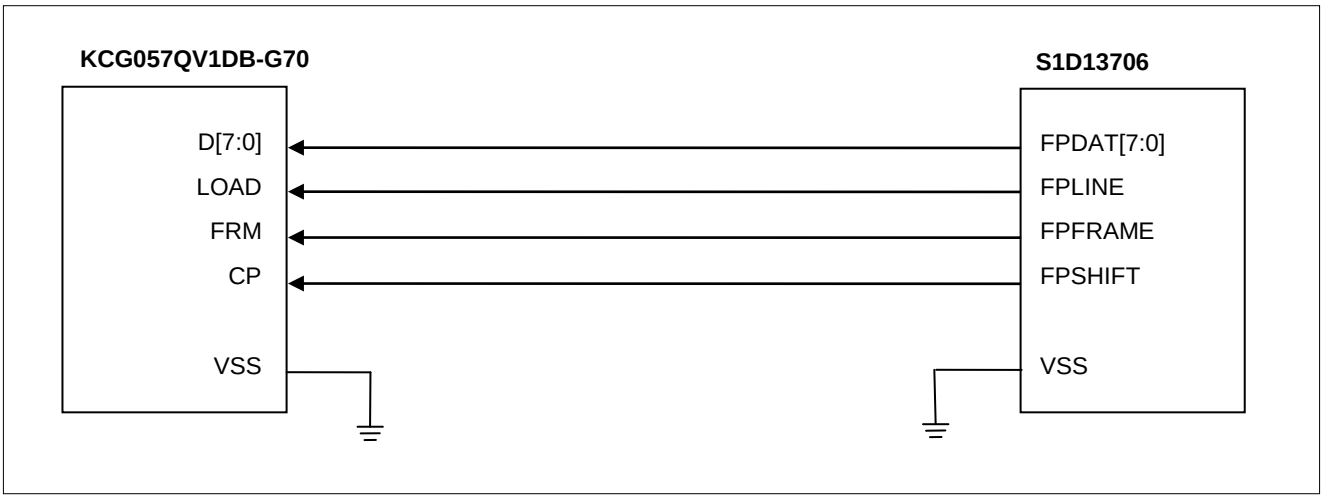

Figure 3-2 Connecting the KCG057QV1DB-G70 to the S1D13706

The following table provides a detailed pin listing for the required connections between the KCG057QV1DB-G70 and the S1D13706.

Table 3-3 Connecting the KCG057QV1DB-G70 to the S1D13706

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13706 TQFP Pin#	S1D13706 Pin Name
1	FRM	Synchronous signal for drive scanning line	52	FPFRAME
2	LOAD	Data signal latch clock	53	FPLINE
3	CP	Data signal shift clock	54	FPSHIFT
4	DISP	Display control signal	—	—
5	VDD	Power supply for logic (+5V)	—	—
6	VSS	GND	—	VSS
7	VCONT	LCD adjust voltage (+1.3V ≤ VCONT ≤ +2.3V)	—	—
8	D7	Data signal(MSB)	64	FPDAT7
9	D6	Data signal	61	FPDAT6
10	D5	Data signal	60	FPDAT5
11	D4	Data signal	59	FPDAT4
12	D3	Data signal	58	FPDAT3
13	D2	Data signal	57	FPDAT2
14	D1	Data signal	56	FPDAT1
15	D0	Data signal (LSB)	55	FPDAT0
16	VDD	Power supply for logic (+5V)	—	—
17	VDD	Power supply for logic (+5V)	—	—
18	VSS	GND	—	VSS
19	VSS	GND	—	VSS
20	VSS	GND	—	VSS

3.2.3 Connecting the KCG057QV1DB-G70 to the S1D13A05

The following diagram shows an example implementation of the KCG057QV1DB-G70 panel connected to the S1D13A05.

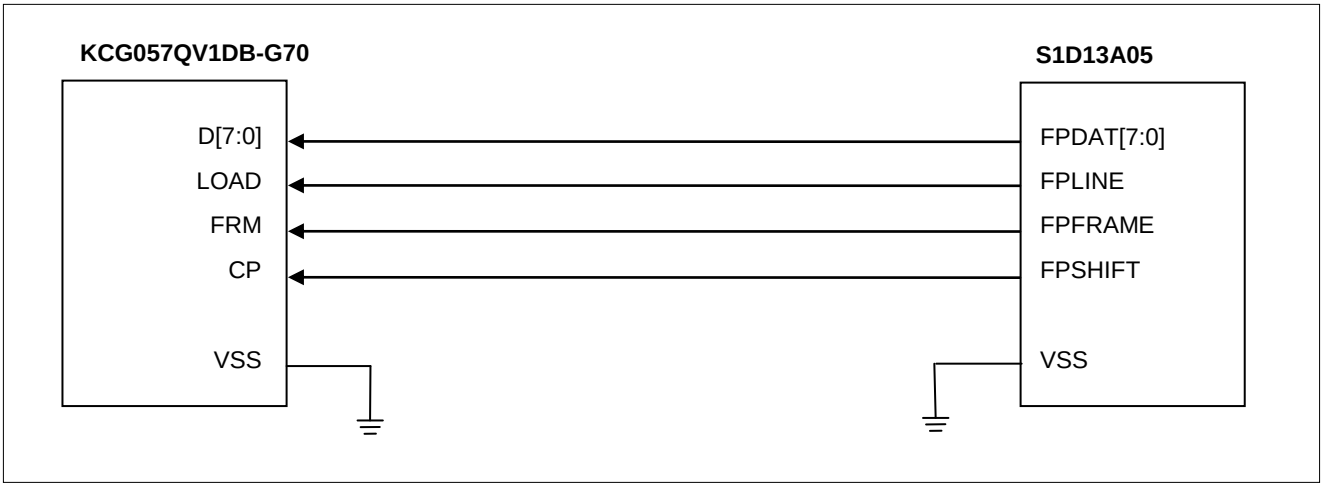

Figure 3-3 Connecting the KCG057QV1DB-G70 to the S1D13A05

The following table provides a detailed pin listing for the required connections between the KCG057QV1DB-G70 and the S1D13A05. Pin mappings are shown for both S1D13A05 package types.

Table 3-4 Connecting the KCG057QV1DB-G70 to the S1D13A05

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13A05 QFP Pin#	S1D13A05 PFBGA Ball#	S1D13A05 Pin Name
1	FRM	Synchronous signal for drive scanning line	40	J9	FPFRAME
2	LOAD	Data signal latch clock	42	H9	FPLINE
3	CP	Data signal shift clock	43	H10	FPSHIFT
4	DISP	Display control signal	—	—	—
5	VDD	Power supply for logic （+5V）	—	—	—
6	VSS	GND	—	—	VSS
7	VCONT	LCD adjust voltage (+1.3V ≤ VCONT ≤ +2.3V)	—	—	—
8	D7	Data signal (MSB)	51	F10	FPDAT7
9	D6	Data signal	49	F8	FPDAT6
10	D5	Data signal	29	G7	FPDAT5
11	D4	Data signal	48	G11	FPDAT4
12	D3	Data signal	47	G10	FPDAT3
13	D2	Data signal	46	G9	FPDAT2
14	D1	Data signal	45	G8	FPDAT1
15	D0	Data signal (LSB)	44	H11	FPDAT0
16	VDD	Power supply for logic (+5V)	—	—	—
17	VDD	Power supply for logic (+5V)	—	—	—
18	VSS	GND	—	—	VSS
19	VSS	GND	—	—	VSS
20	VSS	GND	—	—	VSS

3.3 Example Register Settings

In addition to the pin connections, the S1D13513/S1D13706/S1D13A05 internal registers must be configured appropriately for the KCG057QV1DB-G70 LCD panel. The following tables provide example settings for each display controller. However, these values are for reference only and may differ according to each specific implementation. For details on configuring the S1D13513 register values, see the S1D13513 Hardware Functional Specification, document number X78B-A-001-xx. For details on configuring the S1D13706 register values, see the S1D13706 Hardware Functional Specification, document number X31B-A-001-xx. For details on configuring the S1D13A05 register values, see the S1D13A05 Hardware Functional Specification, document number X40A-A-001-xx.

Also included in the table is an example clock configuration designed to achieve a typical LCD refresh.

Table 3-5 Example Register Settings for the S1D13513

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0800h] LCD Panel Type Select Register	5100h	—
REG[0802h] LCD Horizontal Total Register	(320×3/8×4-1+30)	510
REG[0804h] LCD Horizontal Display Period Register	159	320
REG[0806h] LCD Horizontal Display Period Start Position Register	20	20
REG[0808h] LCD Horizontal Pulse Width	8000h+16	17
REG[080Ah] LCD Horizontal Pulse Start Position	0	0
REG[080Ch] LCD Vertical Total Register	249	250
REG[080Eh] LCD Vertical Display Period Resister	239	240
REG[0810h] LCD Vertical Display Period Start Position Register	9	9
REG[0812h] LCD Vertical Pulse Width	8000h+0	1
REG[0814h] LCD Vertical Pulse Start Position	10	10
PLL2 output frequency in MHz	—	90
REG[0446h] LCD Clock Control Register	9	10
FPSHIFT in MHz	—	2.25
LCD Refresh in Hz	—	70.6

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13513 register values, see the *S1D13513 Hardware Functional Specification*, document number X78B-A-001-xx.

Table 3-6 Example Register Settings for the S1D13706

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0010h] PANEL Type Register	D0h	—
REG[0012h] Horizontal Total Register	2Bh	352
REG[0014h] Horizontal Display Period Register	27h	320
REG[0016h] Horizontal Display Period Start Position Register 0	0h	0
REG[0020h] FPLINE Pulse Width Register	80h+3	4
REG[0022h] FPLINE Pulse Start Pos Register 0	0	1
REG[0018h] Vertical Total Register 0	F9h	250
REG[001Ch] Vertical Display Period Resister 0	EFh	240
REG[001Eh] Vertical Display Period Start Position Register 0	0h	0
REG[0024]h Vertical Sync Pulse Width Register	80h+0	1
REG[0026h] Vertical Sync Pulse Start Pos Register 0	1	1
CLKI2 frequency in MHz	—	50
REG[0005h] Pixel Clock Configuration Register	33h	4
FPSHIFT in MHz	—	3.125
LCD Refresh in Hz	—	71

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13706 register values, see the *S1D13706 Hardware Functional Specification*, document number X31B-A-001-xx.

Table 3-7 Example Register Settings for the S1D13A05

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[000Ch] Panel Type & MOD Rate Register	D0h	—
REG[0020h] Horizontal Total Register	2Bh	352
REG[0024h] Horizontal Display Period Register	27h	320
REG[0028h] Horizontal Display Period Start Position Register	0h	0
REG[002Ch] FPLINE Register	00870156h	Pulse Width 8, Start Position 87
REG[0030h] Vertical Total Register	F9h	250
REG[0034h] Vertical Display Period Resister	EFh	240
REG[0038h] Vertical Display Period Start Position Register	0h	0
REG[003Ch] FPFRAME Register	00800000h	Pulse Width 1, Start Position 0
CLKI2 frequency in MHz	—	50
REG[0008h] Pixel Clock Configuration Register	33h	4
FPSHIFT in MHz	—	3.125
LCD Refresh in Hz	—	71

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13A05 register values, see the *S1D13A05 Hardware Functional Specification*, document number X40A-A-001-xx.

4 Connecting to the Kyocera KG057QV1CA-G05

The Kyocera KG057QV1CA-G05 LCD panel is compatible with the S1D13513, S1D13700, S1D13706, and S1D13A05 display controllers. The following sections will provide connector details, pin mappings, and example register settings for these combinations.

4.1 KG057QV1CA-G05 Pin Mapping

The KG057QV1CA-G05 LCD panel uses a 20-pin connector with the following pin mapping.

Table 4-1 KG057QV1CA-G05 Pin Mapping

Connector Pin#	Pin Name	Pin Description
1	FRM	Synchronous signal for drive scanning line
2	LOAD	Data signal latch clock
3	CP	Data signal shift clock
4	DISP	Display control signal
5	VDD	Power supply for logic (+3.3V)
6	VSS	GND
7	VCONT	LCD adjust voltage (+1.3V ≤ VCONT ≤ +2.3V)
8	D7	Data signal (MSB)
9	D6	Data signal
10	D5	Data signal
11	D4	Data signal
12	D3	Data signal
13	D2	Data signal
14	D1	Data signal
15	D0	Data signal (LSB)
16	VDD	Power supply for logic (+3.3V)
17	VDD	Power supply for logic (+3.3V)
18	VSS	GND
19	VSS	GND
20	VSS	GND

Note
The recommended mounting connector is a Kyocera 08-6210-020-340-800+. The connector is a 0.5mm pitch 20-pin FPC connector (10.5mm x 0.3mm gold plate).

4.2 Connection Examples

The information in this section provides connection examples for the S1D13700, S1D13706, and S1D13A05 display controllers. For the S1D13A05, the display controller is available in two packages. The connection information differs for each package and is listed separately.

In addition to the pin connections for the selected display controller, the KG057QV1CA-G05 requires the following power supplies.

VDD	+3.3V (±0.3V)
VCONT (liquid crystal drive power supply)	+1.95V (±0.5V)

For further details on the KG057QV1CA-G05, such as power consumption and absolute maximum ratings, please contact your Kyocera representative.

4.2.1 Connecting the KG057QV1CA-G05 to the S1D13700

The following diagram shows an example implementation of the KG057QV1CA-G05 panel connected to the S1D13700.

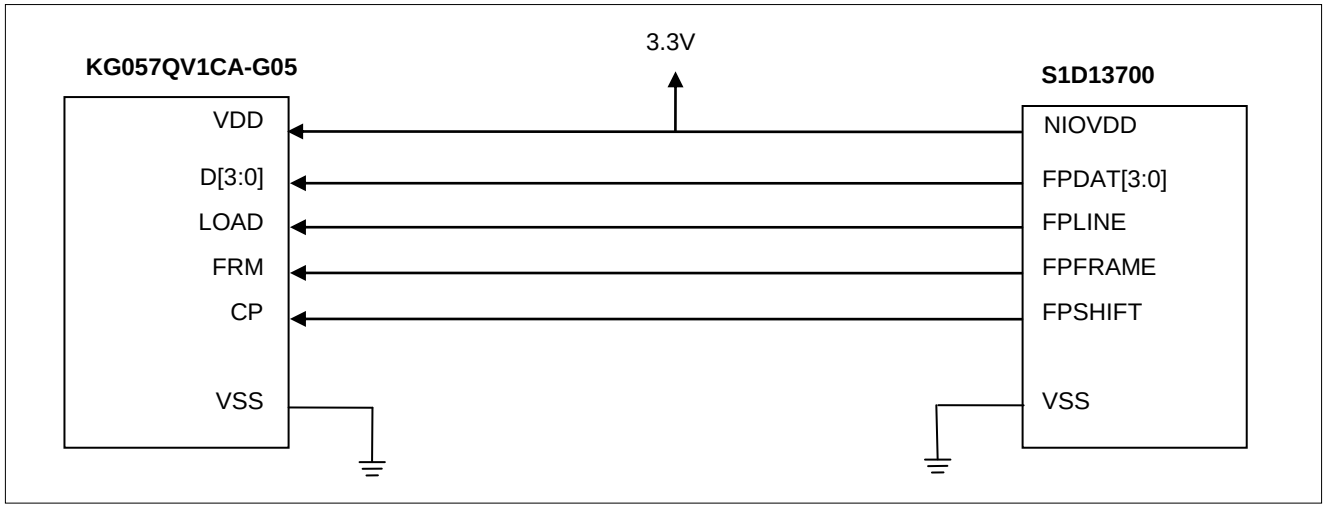

Figure 4-1 Connecting the KG057QV1CA-G05 to the S1D13700

The following table provides a detailed pin listing for the required connections between the KG057QV1CA-G05 and the S1D13700.

Table 4-2 Connecting the KG057QV1CA-G05 to the S1D13700

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13700 TQFP Pin#	S1D13700 Pin Name
1	FRM	Synchronous signal for drive scanning line	30	FPFRAME
2	LOAD	Data signal latch clock	26	FPLINE
3	CP	Data signal shift clock	23	FPSHIFT
4	DISP	Display control signal	—	—
5	VDD	Power supply for logic (+3.3V±0.3V)	—	NIOVDD
6	VSS	GND	—	VSS
7	VCONT	LCD adjust voltage (+1.45V ≤ VCONT ≤ +2.45V)	—	—
8	NC	not connected	—	—
9	NC	not connected	—	—
10	NC	not connected	—	—
11	NC	not connected	—	—
12	D3	Data signal (MSB)	18	FPDAT3
13	D2	Data signal	19	FPDAT2
14	D1	Data signal	20	FPDAT1
15	D0	Data signal(LSB)	21	FPDAT0
16	VDD	Power supply for logic (+3.3V±0.3V)	—	NIOVDD
17	VDD	Power supply for logic (+3.3V±0.3V)	—	NIOVDD
18	VSS	GND	—	VSS
19	VSS	GND	—	VSS
20	VSS	GND	—	VSS

4.2.2 Connecting the KG057QV1CA-G05 to the S1D13706

The following diagram shows an example implementation of the KG057QV1CA-G05 panel connected to the S1D13706.

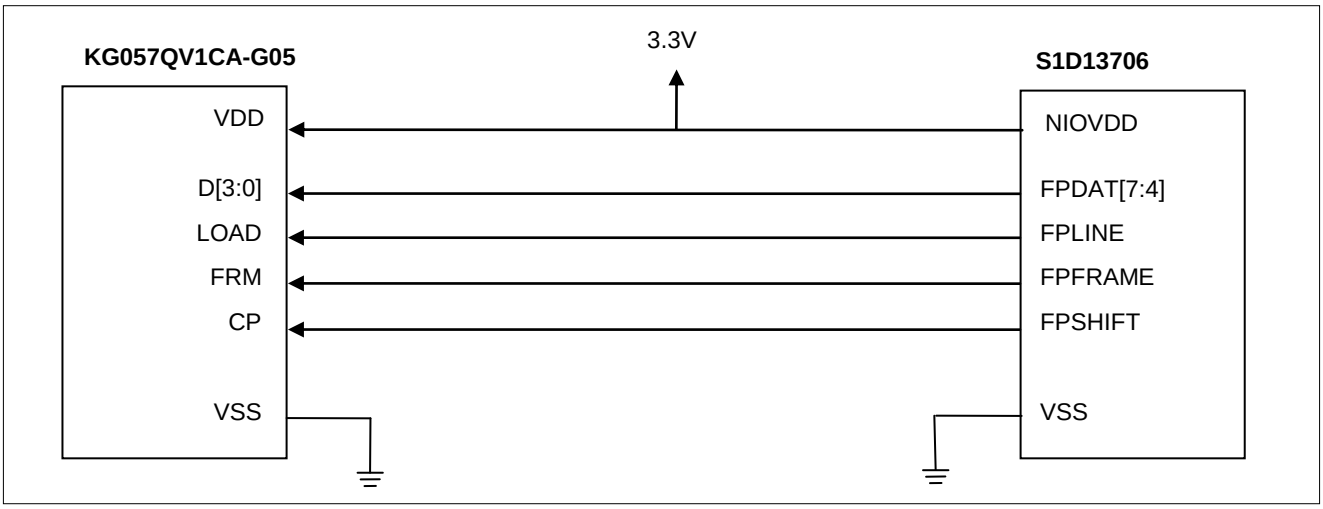

Figure 4-2 Connecting the KG057QV1CA-G05 to the S1D13706

The following table provides a detailed pin listing for the required connections between the KG057QV1CA-G05 and the S1D13706.

Table 4-3 Connecting the KG057QV1CA-G05 to the S1D13706

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13706 TQFP Pin#	S1D13706 Pin Name
1	FRM	Synchronous signal for drive scanning line	52	FPFRAME
2	LOAD	Data signal latch clock	53	FPLINE
3	CP	Data signal shift clock	54	FPSHIFT
4	DISP	Display control signal	—	—
5	VDD	Power supply for logic (+3.3V±0.3V)	—	NIOVDD
6	VSS	GND	—	VSS
7	VCONT	LCD adjust voltage (+1.45V ≤ VCONT ≤ +2.45V)	—	—
8	NC	not connected	—	—
9	NC	not connected	—	—
10	NC	not connected	—	—
11	NC	not connected	—	—
12	D3	Data signal (MSB)	58	FPDAT7
13	D2	Data signal	57	FPDAT6
14	D1	Data signal	56	FPDAT5
15	D0	Data signal (LSB)	55	FPDAT4
16	VDD	Power supply for logic (+3.3V±0.3V)	—	NIOVDD
17	VDD	Power supply for logic (+3.3V±0.3V)	—	NIOVDD
18	VSS	GND	—	VSS
19	VSS	GND	—	VSS
20	VSS	GND	—	VSS

4.2.3 Connecting the KG057QV1CA-G05 to the S1D13A05

The following diagram shows an example implementation of the KG057QV1CA-G05 panel connected to the S1D13A05.

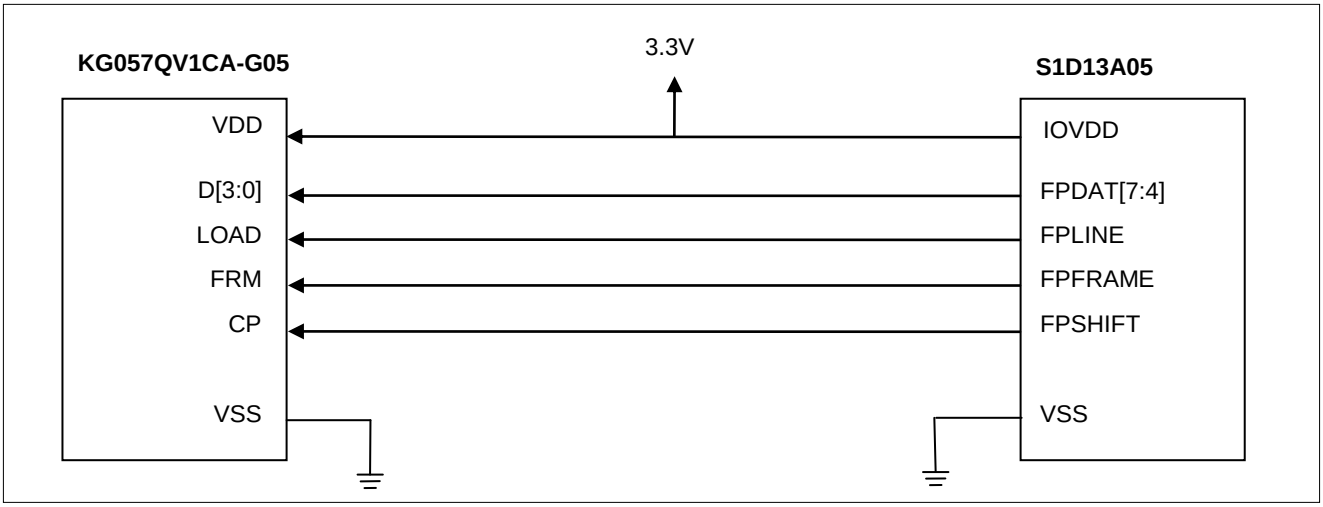

Figure 4-3 Connecting the KG057QV1CA-G05 to the S1D13A05

The following table provides a detailed pin listing for the required connections between the KG057QV1CA-G05 and the S1D13A05. Pin mappings are shown for both S1D13A05 package types.

Table 4-4 Connecting the KG057QV1CA-G05 to the S1D13A05

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13A05 QFP Pin#	S1D13A05 PFBGA Ball#	S1D13A05 Pin Name
1	FRM	Synchronous signal for drive scanning line	40	J9	FPFRAME
2	LOAD	Data signal latch clock	42	H9	FPLINE
3	CP	Data signal shift clock	43	H10	FPSHIFT
4	DISP	Display control signal	—	—	—
5	VDD	Power supply for logic (+3.3V ±0.3V)	—	—	IOVDD
6	VSS	GND	—	—	VSS
7	VCONT	LCD adjust voltage (+1.45V ≤ VCONT ≤ +2.45V)	—	—	—
8	NC	not connected	—	—	—
9	NC	not connected	—	—	—
10	NC	not connected	—	—	—
11	NC	not connected	—	—	—
12	D3	Data signal (MSB)	51	F10	FPDAT7
13	D2	Data signal	49	F8	FPDAT6
14	D1	Data signal	29	G7	FPDAT5
15	D0	Data signal (LSB)	48	G11	FPDAT4
16	VDD	Power supply for logic (+3.3V±0.3V)	—	—	IOVDD
17	VDD	Power supply for logic (+3.3V±0.3V)	—	—	IOVDD
18	VSS	GND	—	—	VSS
19	VSS	GND	—	—	VSS
20	VSS	GND	—	—	VSS

4.3 Example Register Settings

In addition to the pin connections, the S1D13700/S1D13706/S1D13A05 internal registers must be configured appropriately for the KG057QV1CA-G05 LCD panel. The following tables provide example settings for each display controller. However, these values are for reference only and may differ according to each specific implementation. For details on configuring the S1D13700 register values, see the S1D13700 Hardware Functional Specification, document number X42D-A-001-xx. For details on configuring the S1D13706 register values, see the S1D13706 Hardware Functional Specification, document number X31B-A-001-xx. For details on configuring the S1D13A05 register values, see the S1D13A05 Hardware Functional Specification, document number X40A-A-001-xx.

Also included in the table is an example clock configuration designed to achieve a typical LCD refresh.

Example Register Settings for the S1D13700

The LCD timing parameters are fixed for the S1D13700 and there are no register settings required to configure the S1D13700 for use with the KG057QV1CA-G05. However, the FPSHIFT frequency must be set appropriately using the CNF[1:0] pins (1/4, 1/8, or 1/16 of CLKI).

For details on configuring the S1D13700, see the S1D13700 Hardware Functional Specification, document number X42D-A-001-xx

Example Register Settings for the S1D13706

Table 4-5 Example Register Settings for the S1D13706

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0010h] PANEL Type Register	00h	—
REG[0012h] Horizontal Total Register	2Bh	352
REG[0014h] Horizontal Display Period Register	27h	320
REG[0016h] Horizontal Display Period Start Position Register 0	0h	0
REG[0020h] FPLINE Pulse Width Register	80h+3	4
REG[0022h] FPLINE Pulse Start Pos Register 0	0	0
REG[0018h] Vertical Total Register 0	F9h	250
REG[001Ch] Vertical Display Period Resister 0	EFh	240
REG[001Eh] Vertical Display Period Start Position Register 0	0h	0
REG[0024]h Vertical Sync Pulse Width Register	80h+0	1
REG[0026h] Vertical Sync Pulse Start Pos Register 0	1	1
CLKI2 frequency in MHz	—	50
REG[0005h] Pixel Clock Configuration Register	33	4
FPSHIFT in MHz	—	1.56
LCD Refresh in Hz	—	71

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13706 register values, see the S1D13706 Hardware Functional Specification, document number X31B-A-001-xx.

Example Register Settings for the S1D13A05

Table 4-6 Example Register Settings for the S1D13A05

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[000Ch] Panel Type & MOD Rate Register	00h	—
REG[0020h] Horizontal Total Register	2Bh	352
REG[0024h] Horizontal Display Period Register	27h	320
REG[0028h] Horizontal Display Period Start Position Register	0h	0
REG[002Ch] FPLINE Register	00870156h	Pulse Width 8 Start Position 87
REG[0030h] Vertical Total Register	F9h	250
REG[0034h] Vertical Display Period Resister	EFh	240
REG[0038h] Vertical Display Period Start Position Register	0h	0
REG[003Ch] FPFRAME Register	00800000h	Pulse Width 1 Start Position 0

CLKI2 frequency in MHz	—	50
REG[0008h] Pixel Clock Configuration Register	33h	4
FPSHIFT in MHz	—	1.56
LCD Refresh in Hz	—	71

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13A05 register values, see the S1D13A05 Hardware Functional Specification, document number X40A-A-001-xx.

5 Connecting to the Kyocera TCG057QV1AC-G10

The Kyocera TCG057QV1AC-G10 LCD panel is compatible with the S1D13513, S1D13719, S1D13742, S1D13743, and S1D13748 display controllers. The following sections will provide connector details, pin mappings, and example register settings.

5.1 TCG057QV1AC-G10 Pin Mapping

The TCG057QV1AC-G10 LCD panel uses a 33-pin connector with the following pin mapping.

Table 5-1 TCG057QV1AC-G10 Pin Mapping

Connector Pin#	Pin Name	Pin Description
1	GND	GND
2	CK	Clock signal for sampling each data signal
3	Hsync	Horizontal synchronous signal (negative)
4	Vsync	Vertical synchronous signal (negative)
5	GND	GND
6	R0	RED data signal (LSB)
7	R1	RED data signal
8	R2	RED data signal
9	R3	RED data signal
10	R4	RED data signal
11	R5	RED data signal (MSB)
12	GND	GND
13	G0	GREEN data signal (LSB)
14	G1	GREEN data signal
15	G2	GREEN data signal
16	G3	GREEN data signal
17	G4	GREEN data signal
18	G5	GREEN data signal (MSB)
19	GND	GND
20	B0	BLUE data signal (LSB)
21	B1	BLUE data signal
22	B2	BLUE data signal
23	B3	BLUE data signal
24	B4	BLUE data signal
25	B5	BLUE data signal (MSB)
26	GND	GND
27	ENAB	Signal to settle the horizontal display position (positive)
28	VDD	3.3V power supply
29	VDD	3.3V power supply
30	R/L	Horizontal display mode select signal Low: Normal , High: Left/Right reverse mode

Connector Pin#	Pin Name	Pin Description
31	U/D	Vertical display mode select signal High: Normal , Low: Up/Down reverse mode
32	V/Q	Resolution mode select signal High: VGA , Low: QVGA
33	GND	GND

Note
The recommended mounting connector is a Kyocera 08-6210-020-340-800+. The connector is a 0.5mm pitch 33-pin FPC connector (17mm x 0.3mm gold plate).

5.2 Connection Examples

The information in this section provides connection examples for the S1D13513, S1D13719, S1D13742, S1D13743, and S1D13748 display controllers. Some display controllers are available in two packages. The connection information differs for each package and is listed separately.

In addition to the pin connections for the selected display controller, the TCG057QV1AC-G10 requires the following power supply.

VDD +3.3V (±0.3V)

Note
For the S1D13719, the panel VDD and S1D13719 PIOVDD should be set to 3.0V instead of 3.3V.

For further details on the TCG057QV1AC-G10, such as power consumption and absolute maximum ratings, please contact your Kyocera representative.

5.2.1 Connecting the TCG057QV1AC-G10 to the S1D13513

The following diagram shows an example implementation of the TCG057QV1AC-G10 panel connected to the S1D13513.

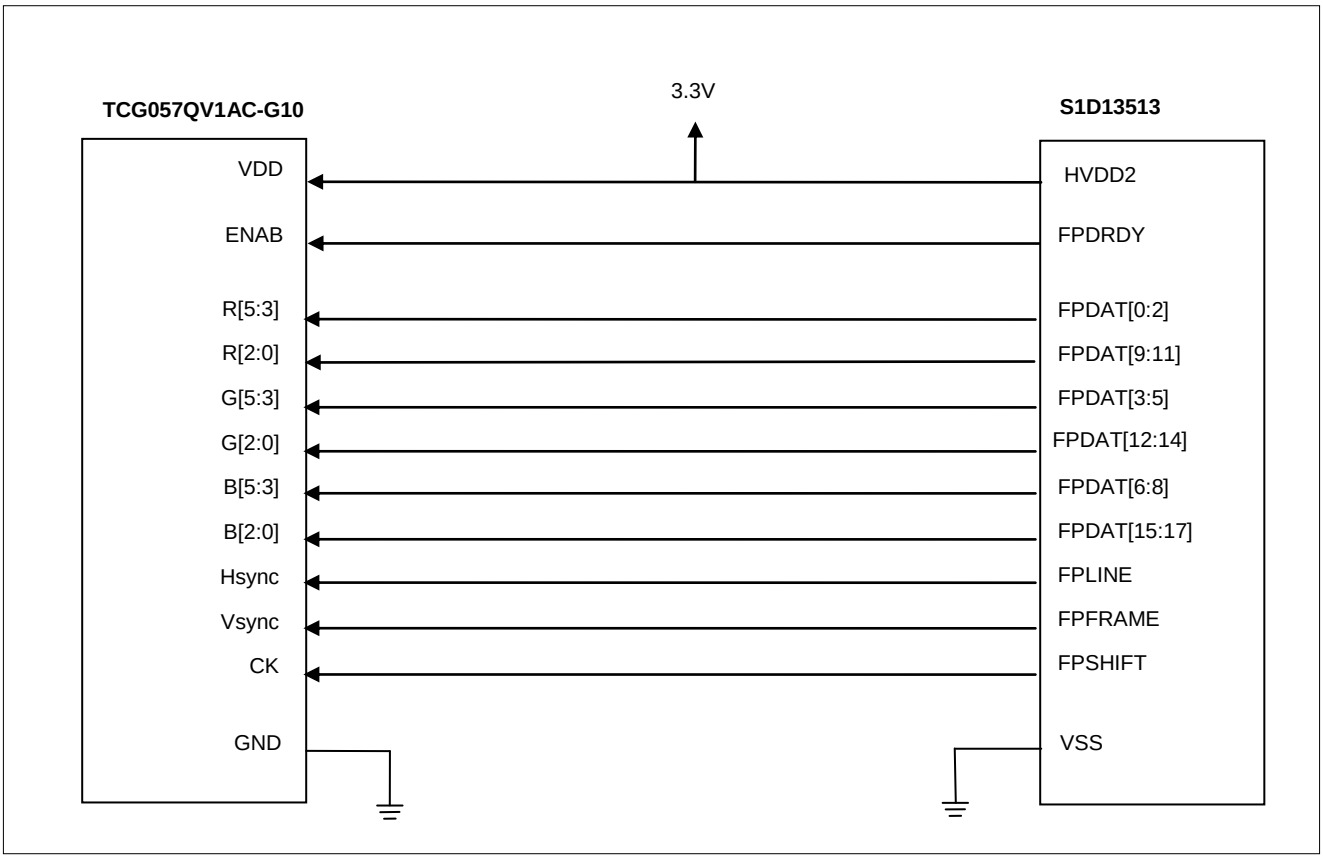

Figure 5-1 Connecting the TCG057QV1AC-G10 to the S1D13513

The following table provides a detailed pin listing for the required connections between the TCG057QV1AC-G10 and the S1D13513. Pin mappings are shown for both S1D13513 package types.

Table 5-2 Connecting the TCG057QV1AC-G10 to the S1D13513

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
1	GND	GND	—	—	VSS
2	CK	Clock signal for sampling each data signal	77	P8	FPSHIFT
3	Hsync	Horizontal synchronous signal (negative)	79	R8	FPLINE
4	Vsync	Vertical synchronous signal (negative)	78	T8	FPFRAME
5	GND	GND	—	—	VSS
6	R0	RED data signal (LSB)	61	N5	FPDAT11
7	R1	RED data signal	62	M5	FPDAT10
8	R2	RED data signal	63	P6	FPDAT9
9	R3	RED data signal	72	T7	FPDAT2
10	R4	RED data signal	73	N7	FPDAT1

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
11	R5	RED data signal (MSB)	74	M7	FPDAT0
12	GND	GND	—	—	VSS
13	G0	GREEN data signal (LSB)	56	R4	FPDAT14
14	G1	GREEN data signal	59	T4	FPDAT13
15	G2	GREEN data signal	60	T5	FPDAT12
16	G3	GREEN data signal	69	L7	FPDAT5
17	G4	GREEN data signal	70	P7	FPDAT4
18	G5	GREEN data signal (MSB)	71	R7	FPDAT3
19	GND	GND	—	—	VSS
20	B0	BLUE data signal (LSB)	53	N4	FPDAT17
21	B1	BLUE data signal	54	P4	FPDAT16
22	B2	BLUE data signal	55	T2	FPDAT15
23	B3	BLUE data signal	64	R6	FPDAT8
24	B4	BLUE data signal	67	K6	FPDAT7
25	B5	BLUE data signal (MSB)	68	M6	FPDAT6
26	GND	GND	-	-	VSS
27	ENAB	Signal to settle the horizontal display position (positive)	80	M8	FPDRDY
28	VDD	3.3V power supply	—	—	HVDD2
29	VDD	3.3V power supply	—	—	HVDD2
30	R/L	Horizontal display mode select signal Low: Normal, High: Left/Right reverse mode	—	—	—
31	U/D	Vertical display mode select signal High: Normal, Low: Up/Down reverse mode	—	—	—
32	V/Q	Resolution mode select signal High: VGA, Low: QVGA	—	—	—
33	GND	GND	—	—	VSS

5.2.2 Connecting the TCG057QV1AC-G10 to the S1D13719

The following diagram shows an example implementation of the TCG057QV1AC-G10 panel connected to the S1D13719.

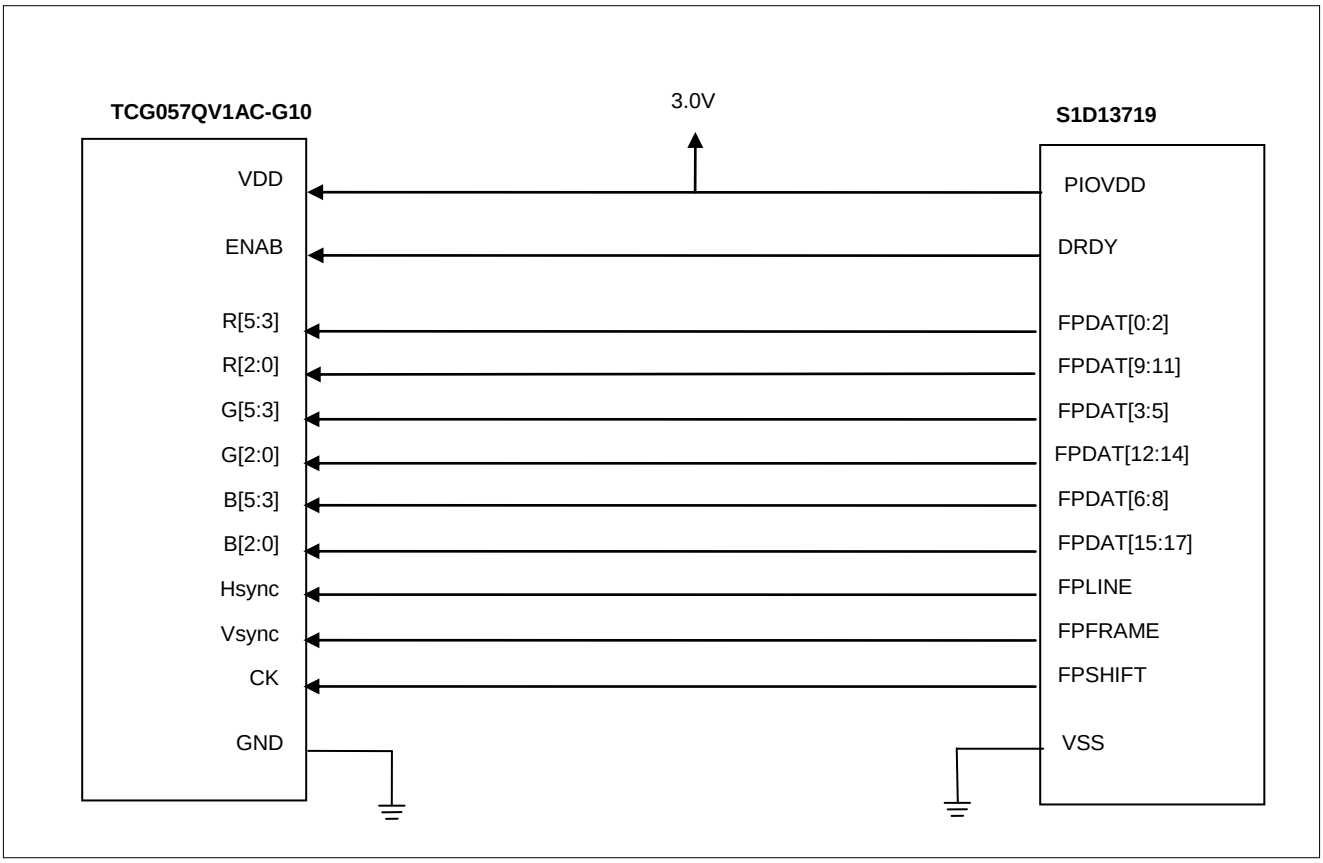

Figure 5-2 Connecting the TCG057QV1AC-G10 to the S1D13719

Note
For the S1D13719, the panel VDD and S1D13719 PIOVDD should be set to 3.0V instead of 3.3V.

The following table provides a detailed pin listing for the required connections between the TCG057QV1AC-G10 and the S1D13719. Pin mappings are shown for both S1D13719 package types.

Table 5-3 Connecting the TCG057QV1AC-G10 to the S1D13719

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13719 PFBGA Pin#	S1D13719 FCBGA Ball#	S1D13719 QFP Pin#	S1D13719 Pin Name
1	GND	GND	—	—	—	VSS
2	CK	Clock signal for sampling each data signal	P5	F17	66	FPSHIFT
3	Hsync	Horizontal synchronous signal (negative)	P4	E17	58	FPLINE
4	Vsync	Vertical synchronous signal (negative)	P3	D17	57	FPFRAME
5	GND	GND	—	—	—	VSS

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13719 PFBGA Pin#	S1D13719 FCBGA Ball#	S1D13719 QFP Pin#	S1D13719 Pin Name
6	R0	RED data signal (LSB)	L8	K16	82	FPDAT11
7	R1	RED data signal	M8	K14	83	FPDAT10
8	R2	RED data signal	M6	H15	72	FPDAT9
9	R3	RED data signal	K4	A15	49	FPDAT2
10	R4	RED data signal	N1	C14	48	FPDAT1
11	R5	RED data signal (MSB)	L3	B15	47	FPDAT0
12	GND	GND	—	—	—	VSS
13	G0	GREEN data signal (LSB)	M7	J17	79	FPDAT14
14	G1	GREEN data signal	N8	K17	80	FPDAT13
15	G2	GREEN data signal	P8	K15	81	FPDAT12
16	G3	GREEN data signal	N3	D16	55	FPDAT5
17	G4	GREEN data signal	N2	C17	54	FPDAT4
18	G5	GREEN data signal (MSB)	P2	C16	53	FPDAT3
19	GND	GND	—	—	—	VSS
20	B0	BLUE data signal (LSB)	N6	H17	73	FPDAT17
21	B1	BLUE data signal	L7	J15	74	FPDAT16
22	B2	BLUE data signal	M4	F16	60	FPDAT15
23	B3	BLUE data signal	L2	B14	45	FPDAT8
24	B4	BLUE data signal	L6	G15	68	FPDAT7
25	B5	BLUE data signal (MSB)	M3	D15	56	FPDAT6
26	GND	GND	—	—	—	VSS
27	ENAB	Signal to settle the horizontal display position (positive)	M1	C13	44	DRDY
28	VDD	3.0V power supply	—	—	—	PIOVDD
29	VDD	3.0V power supply	—	—	—	PIOVDD
30	R/L	Horizontal display mode select signal Low: Normal, High: Left/Right reverse mode	—	—	—	—
31	U/D	Vertical display mode select signal High: Normal, Low: Up/Down reverse mode	—	—	—	—
32	V/Q	Resolution mode select signal High: VGA, Low: QVGA	—	—	—	—
33	GND	GND	—	—	—	VSS

5.2.3 Connecting the TCG057QV1AC-G10 to the S1D13742

The following diagram shows an example implementation of the TCG057QV1AC-G10 panel connected to the S1D13742.

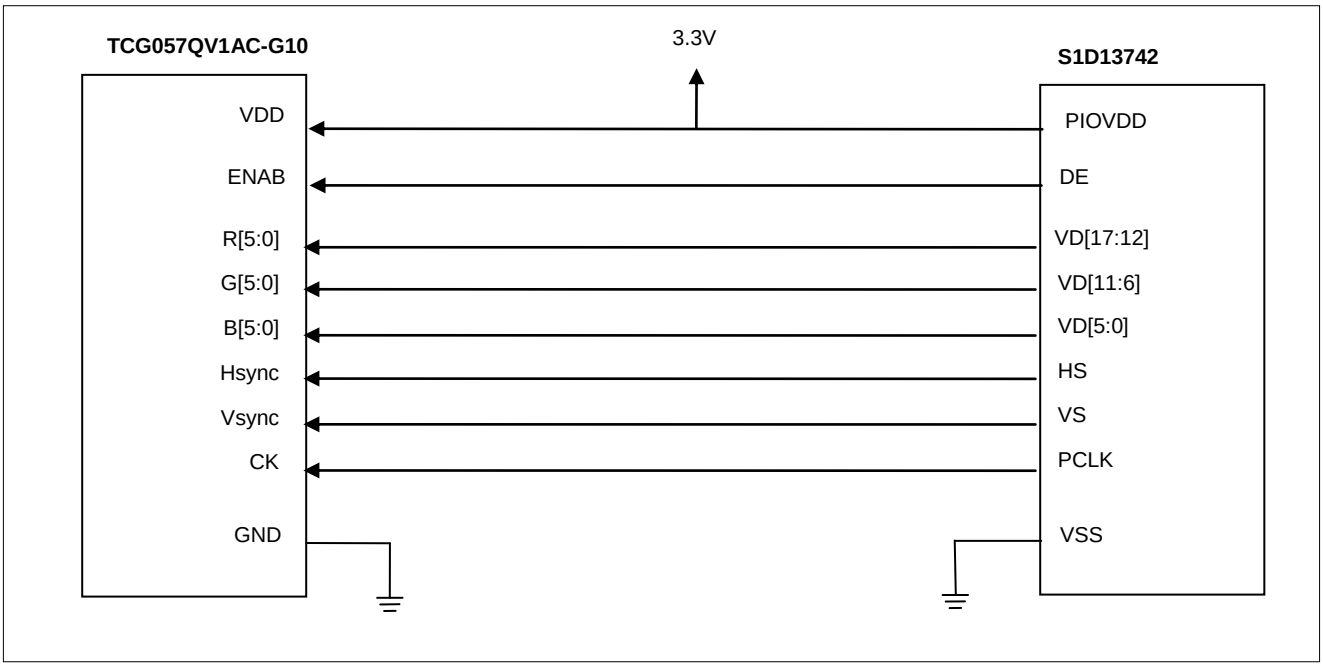

Figure 5-3 Connecting the TCG057QV1AC-G10 to the S1D13742

The following table provides a detailed pin listing for the required connections between the TCG057QV1AC-G10 and the S1D13742. Pin mappings are shown for both S1D13742 package types.

Table 5-4 Connecting the TCG057QV1AC-G10 to the S1D13742

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13742 QFP Pin#	S1D13742 FCBGA Ball#	S1D13742 Pin Name
1	GND	GND	—	—	VSS
2	CK	Clock signal for sampling each data signal	11	D11	PCLK
3	Hsync	Horizontal synchronous signal (negative)	9	D9	HS
4	Vsync	Vertical synchronous signal (negative)	10	D10	VS
5	GND	GND	—	—	VSS
6	R0	RED data signal (LSB)	61	K5	VD12
7	R1	RED data signal	64	K4	VD13
8	R2	RED data signal	30	J11	VD14
9	R3	RED data signal	29	J10	VD15
10	R4	RED data signal	43	J9	VD16
11	R5	RED data signal (MSB)	47	J8	VD17
12	GND	GND	—	—	VSS
13	G0	GREEN data signal (LSB)	66	L3	VD6
14	G1	GREEN data signal	42	K10	VD7

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13742 QFP Pin#	S1D13742 FCBGA Ball#	S1D13742 Pin Name
15	G2	GREEN data signal	44	K9	VD8
16	G3	GREEN data signal	48	K8	VD9
17	G4	GREEN data signal	51	K7	VD10
18	G5	GREEN data signal (MSB)	58	K6	VD11
19	GND	GND	—	—	VSS
20	B0	BLUE data signal (LSB)	45	L9	VD0
21	B1	BLUE data signal	49	L8	VD1
22	B2	BLUE data signal	54	L7	VD2
23	B3	BLUE data signal	59	L6	VD3
24	B4	BLUE data signal	62	L5	VD4
25	B5	BLUE data signal (MSB)	65	L4	VD5
26	GND	GND	—	—	VSS
27	ENAB	Signal to settle the horizontal display position (positive)	8	C11	DE
28	VDD	3.3V power supply	—	—	PIOVDD
29	VDD	3.3V power supply	—	—	PIOVDD
30	R/L	Horizontal display mode select signal Low: Normal, High: Left/Right reverse mode	—	—	—
31	U/D	Vertical display mode select signal High: Normal, Low: Up/Down reverse mode	—	—	—
32	V/Q	Resolution mode select signal High: VGA, Low: QVGA	—	—	—
33	GND	GND	—	—	VSS

5.2.4 Connecting the TCG057QV1AC-G10 to the S1D13743

The following diagram shows an example implementation of the TCG057QV1AC-G10 panel connected to the S1D13743.

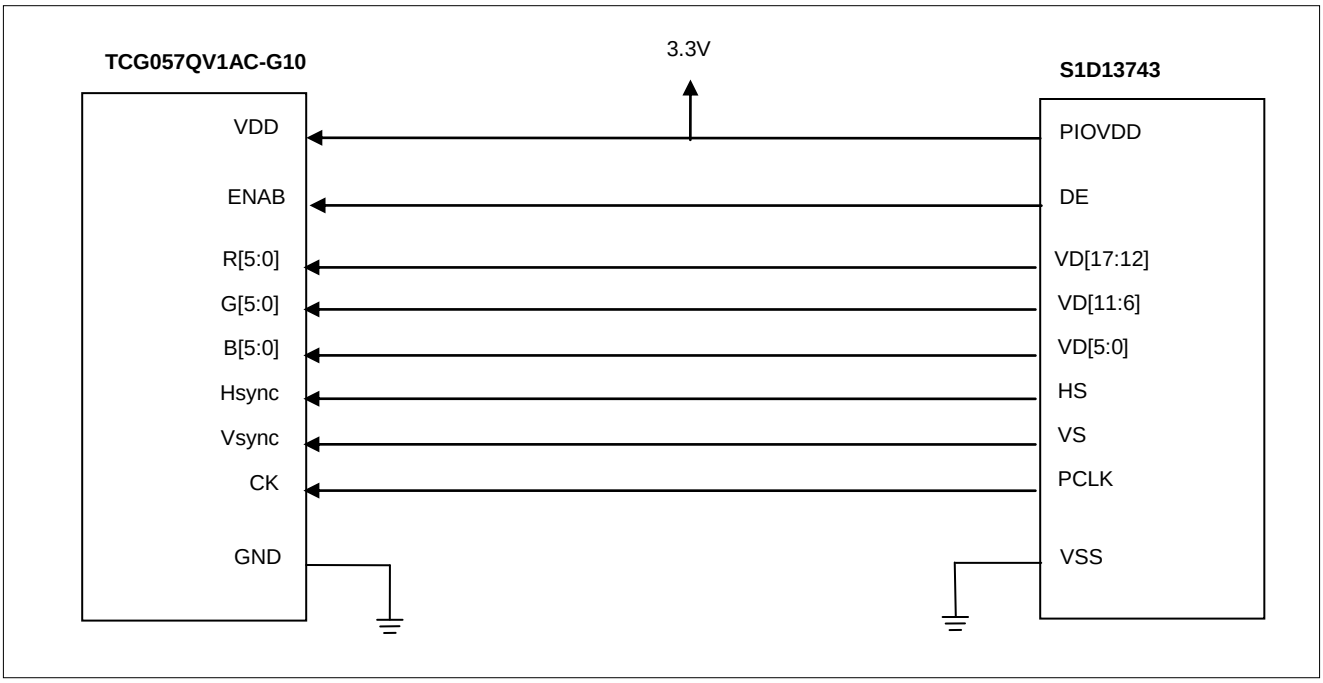

Figure 5-4 Connecting the TCG057QV1AC-G10 to the S1D13743

The following table provides a detailed pin listing for the required connections between the TCG057QV1AC-G10 and the S1D13743. Pin mappings are shown for both S1D13743 package types.

Table 5-5 Connecting the TCG057QV1AC-G10 to the S1D13743

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13743 QFP Pin#	S1D13743 FCBGA Ball#	S1D13743 Pin Name
1	GND	GND	—	—	VSS
2	CK	Clock signal for sampling each data signal	8	D11	PCLK
3	Hsync	Horizontal synchronous signal (negative)	4	D9	HS
4	Vsync	Vertical synchronous signal (negative)	5	D10	VS
5	GND	GND	—	—	VSS
6	R0	RED data signal (LSB)	56	K5	VD12
7	R1	RED data signal	61	K4	VD13
8	R2	RED data signal	15	J11	VD14
9	R3	RED data signal	14	J10	VD15
10	R4	RED data signal	20	J9	VD16
11	R5	RED data signal (MSB)	40	J8	VD17
12	GND	GND	—	—	VSS
13	G0	GREEN data signal (LSB)	63	L3	VD6

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13743 QFP Pin#	S1D13743 FCBGA Ball#	S1D13743 Pin Name
14	G1	GREEN data signal	21	K10	VD7
15	G2	GREEN data signal	38	K9	VD8
16	G3	GREEN data signal	44	K8	VD9
17	G4	GREEN data signal	48	K7	VD10
18	G5	GREEN data signal (MSB)	51	K6	VD11
19	GND	GND	—	—	VSS
20	B0	BLUE data signal (LSB)	39	L9	VD0
21	B1	BLUE data signal	43	L8	VD1
22	B2	BLUE data signal	49	L7	VD2
23	B3	BLUE data signal	54	L6	VD3
24	B4	BLUE data signal	57	L5	VD4
25	B5	BLUE data signal (MSB)	62	L4	VD5
26	GND	GND	—	—	VSS
27	ENAB	Signal to settle the horizontal display position (positive)	3	C11	DE
28	VDD	3.3V power supply	—	—	PIOVDD
29	VDD	3.3V power supply	—	—	PIOVDD
30	R/L	Horizontal display mode select signal Low: Normal, High: Left/Right reverse mode	—	—	—
31	U/D	Vertical display mode select signal High: Normal, Low: Up/Down reverse mode	—	—	—
32	V/Q	Resolution mode select signal High: VGA, Low: QVGA	—	—	—
33	GND	GND	—	—	VSS

5.2.5 Connecting the TCG057QV1AC-G10 to the S1D13748

The following diagram shows an example implementation of the TCG057QV1AC-G10 panel connected to the S1D13748.

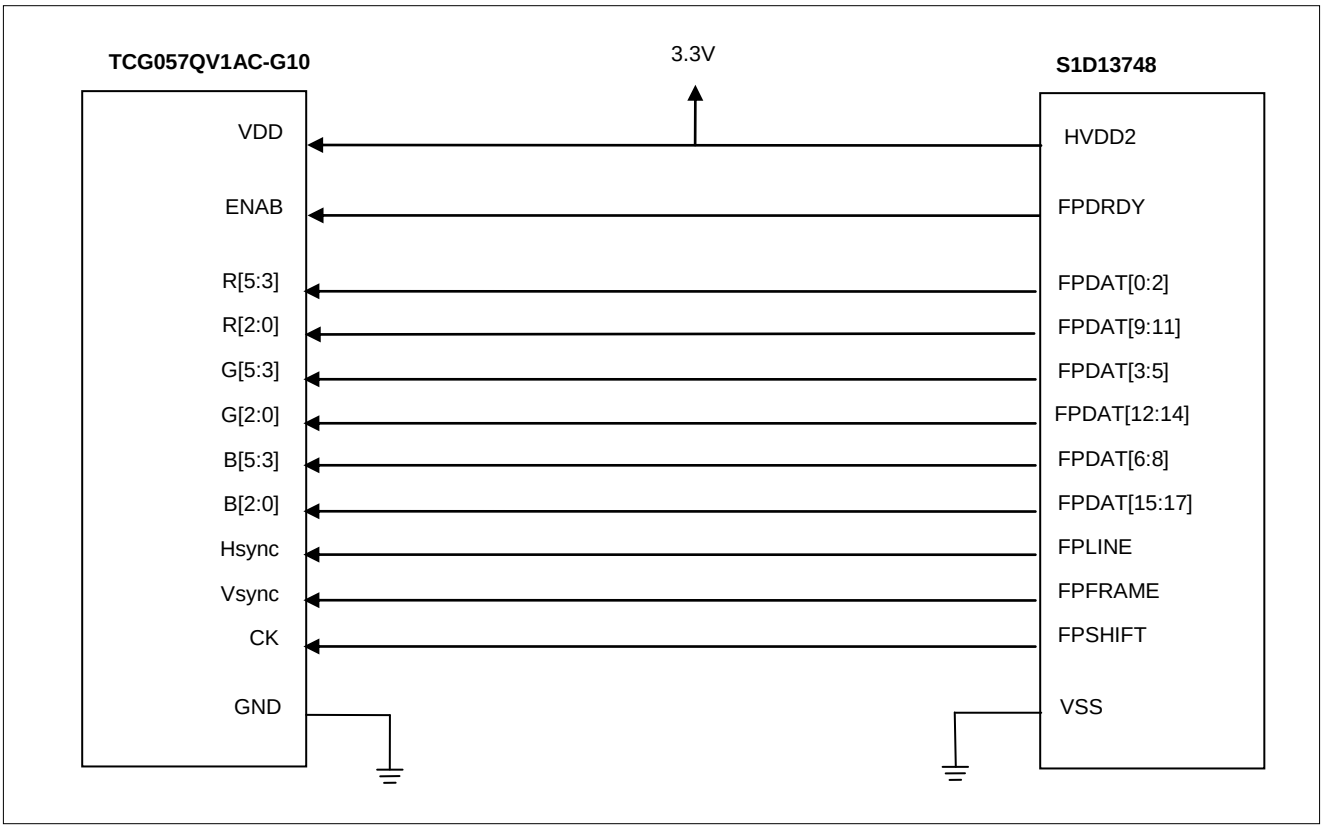

Figure 5-5 Connecting the TCG057QV1AC-G10 to the S1D13748

The following table provides a detailed pin listing for the required connections between the TCG057QV1AC-G10 and the S1D13748. Pin mappings are shown for both S1D13748 package types.

Table 5-6 Connecting the TCG057QV1AC-G10 to the S1D13748

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
1	GND	GND	—	—	VSS
2	CK	Clock signal for sampling each data signal	75	J11	FPSHIFT
3	Hsync	Horizontal synchronous signal (negative)	77	H10	FPLINE
4	Vsync	Vertical synchronous signal (negative)	76	J10	FPFRAME
5	GND	GND	—	—	VSS
6	R0	RED data signal (LSB)	63	L8	FPDAT11
7	R1	RED data signal	62	J8	FPDAT10
8	R2	RED data signal	61	K8	FPDAT9
9	R3	RED data signal	51	K5	FPDAT2
10	R4	RED data signal	50	L5	FPDAT1

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
11	R5	RED data signal (MSB)	49	J5	FPDAT0
12	GND	GND	—	—	VSS
13	G0	GREEN data signal (LSB)	69	H8	FPDAT14
14	G1	GREEN data signal	68	K9	FPDAT13
15	G2	GREEN data signal	64	L9	FPDAT12
16	G3	GREEN data signal	54	L6	FPDAT5
17	G4	GREEN data signal	53	J6	FPDAT4
18	G5	GREEN data signal (MSB)	52	H6	FPDAT3
19	GND	GND	—	—	VSS
20	B0	BLUE data signal (LSB)	72	J9	FPDAT17
21	B1	BLUE data signal	71	K10	FPDAT16
22	B2	BLUE data signal	70	L10	FPDAT15
23	B3	BLUE data signal	60	K7	FPDAT8
24	B4	BLUE data signal	59	J7	FPDAT7
25	B5	BLUE data signal (MSB)	58	L7	FPDAT6
26	GND	GND	—	—	VSS
27	ENAB	Signal to settle the horizontal display position (positive)	78	G7	FPDRDY
28	VDD	3.3V power supply	—	—	PIOVDD
29	VDD	3.3V power supply	—	—	PIOVDD
30	R/L	Horizontal display mode select signal Low: Normal, High: Left/Right reverse mode	—	—	—
31	U/D	Vertical display mode select signal High: Normal, Low: Up/Down reverse mode	—	—	—
32	V/Q	Resolution mode select signal High: VGA, Low: QVGA	—	—	—
33	GND	GND	—	—	VSS

5.2.6 Example Register Settings

In addition to the pin connections, the S1D13513/S1D13719/S1D13742/S1D13743/S1D13748 internal registers must be configured appropriately for the TCG057QV1AC-G10 LCD panel. The following tables provide example settings for each display controller. However, these values are for reference only and may differ according to each specific implementation.

Also included in the table is an example clock configuration designed to achieve a typical LCD refresh.

Table 5-7 Example Register Settings for the S1D13513

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0800h] LCD Panel Type Select Register	0280h	—
REG[0802h] LCD Horizontal Total Register	399	400
REG[0804h] LCD Horizontal Display Period Register	159	320
REG[0806h] LCD Horizontal Display Period Start Position Register	61	61
REG[0808h] LCD Horizontal Pulse Width	16	17
REG[080Ah] LCD Horizontal Pulse Start Position	0	0
REG[080Ch] LCD Vertical Total Register	261	262
REG[080Eh] LCD Vertical Display Period Resister	239	240
REG[0810h] LCD Vertical Display Period Start Position Register	7	7
REG[0812h] LCD Vertical Pulse Width	2	3
REG[0814h] LCD Vertical Pulse Start Position	0	0
PLL2 output frequency in MHz	-	60
REG[0446h] LCD Clock Control Register	9	10
FPSHIFT in MHz	—	6
LCD Refresh in Hz	—	57.3

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13513 register values, see the *S1D13513 Hardware Functional Specification*, document number X78B-A-001-xx.

Table 5-8 Example Register Settings for the S1D13719

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0040h] LCD1 Horizontal Total Register	49	400
REG[0042h] LCD1 Horizontal Display Period Register	159	320
REG[0044h] LCD1 Horizontal Display Period Start Position Register	53	62
REG[0046h] LCD1 FPLINE Register	16	17
REG[0048h] LCD1 FPLINE Pulse Position Register	31	32
REG[004Ah] LCD1 Vertical Total Register	319	320
REG[004Ch] LCD1 Vertical Display Period Resister	239	240
REG[004Eh] LCD1 Vertical Display Period Start Position Register	22	22
REG[0050h] LCD1 FPFRAME Register	7	8
REG[0052h] LCD1 FPFRAME Pulse Position Register	15	15
PLL output frequency in MHz	—	54
REG[0030h] LCD Interface Clock Control Register	503h	8
FPSHIFT in MHz	—	6.75
LCD Refresh in Hz	—	52.7

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13719 register values, see the S1D13719 Hardware Functional Specification, document number X59A-A-001-xx.

Table 5-9 Example Register Settings for the S1D13742

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[14h] Panel Type Register	00h	—
REG[16h] Horizontal Display Width Register	40	320
REG[18h] Horizontal Non-Display Period Register	102	102
REG[1Ah]~[1Ch] Vertical Display Height Registers	240	240
REG[1Eh] Vertical Non-Display Period Register	10	10
REG[20h] HS Pulse Width Register	16	16
REG[22h] HS Pulse Start Position Register 0	90	90
REG[24h] VS Pulse Width Register	2	2
REG[26h] VS Pulse Start Position Register 0	0	0
PLL output frequency in MHz	—	66
REG[12h] Pixel Clock Configuration Register	49h	10
FPSHIFT in MHz	—	6.6
LCD Refresh in Hz	—	62.6

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13742 register values, see the S1D13742 Hardware Functional Specification, document number X63A-A-001-xx.

Table 5-10 Example Register Settings for the S1D13743

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[14h] Panel Type Register	00h	—
REG[16h] Horizontal Display Width Register	40	320
REG[18h] Horizontal Non－Display Period Register	102	102
REG[1Ah]~[1Ch] Vertical Display Height Register0,1	240	240
REG[1Eh] Vertical Non－Display Period Register	10	2
REG[20h] HS Pulse Width Register	16	16
REG[22h] HS Pulse Start Position Resister	90	91
REG[24h] VS Pulse Width Register	2	2
REG[26h] VS Pulse Start Position Resister	0	0
PLL output frequency in MHz	—	66
REG[12h] Clock Source Select Register	49h	10
FPSHIFT in MHz	—	6.6
LCD Refresh in Hz	—	62.6

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13743 register values, see the S1D13743 Hardware Functional Specification, document number X70A-A-001-xx.

Table 5-11 Example Register Settings for the S1D13748

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0040h] LCD1 Horizontal Total Register	53	432
REG[0042h] LCD1 Horizontal Display Period Register	159	320
REG[0044h] LCD1 Horizontal Display Period Start Position Register	53	53
REG[0046h] LCD1 Horizontal Pulse Register	15	16
REG[0048h] LCD1 Horizontal Pulse Start Position Register	0	1
REG[004Ah] LCD1 Vertical Total Register	249	250
REG[004Ch] LCD1 Vertical Display Period Resister	239	240
REG[0050h] LCD1 Vertical Pulse Register	0	1
REG[0052h] LCD1 Vertical Pulse Start Position Register	0	1
REG[0246h] Main1 Window Image Horizontal Size Register	319	320
REG[0248h] Main1 Window Image Vertical Size Register	239	240
REG[004Eh] LCD1 Vertical Display Period Start Position Register	9	9
PLL output frequency in MHz	—	12.8
REG[0030h] LCD Interface Clock Setting Register	0500h	2
FPSHIFT in MHz	—	6. 4
LCD Refresh in Hz	—	59.3

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13748 register values, see the S1D13748 Hardware Functional Specification, document number X80A-A-001-xx.

6 Connecting to the Kyocera TCG057VG1AC-G00

The Kyocera TCG057VG1AC-G00 LCD panel is compatible with the S1D13513 display controller. The following sections will provide connector details, pin mappings, and example register settings.

6.1 TCG057VG1AC-G00 Pin Mapping

The TCG057VG1AC-G00 LCD panel uses a 33-pin connector with the following pin mapping.

Table 6-1 TCG057VG1AC-G00 Pin Mapping

Connector Pin#	Pin Name	Pin Description
1	GND	GND
2	CK	Clock signal for sampling each data signal
3	Hsync	Horizontal synchronous signal (negative)
4	Vsync	Vertical synchronous signal (negative)
5	GND	GND
6	R0	RED data signal (LSB)
7	R1	RED data signal
8	R2	RED data signal
9	R3	RED data signal
10	R4	RED data signal
11	R5	RED data signal (MSB)
12	GND	GND
13	G0	GREEN data signal (LSB)
14	G1	GREEN data signal
15	G2	GREEN data signal
16	G3	GREEN data signal
17	G4	GREEN data signal
18	G5	GREEN data signal (MSB)
19	GND	GND
20	B0	BLUE data signal (LSB)
21	B1	BLUE data signal
22	B2	BLUE data signal
23	B3	BLUE data signal
24	B4	BLUE data signal
25	B5	BLUE data signal (MSB)
26	GND	GND
27	ENAB	Signal to settle the horizontal display position (positive)
28	VDD	3.3V power supply
29	VDD	3.3V power supply
30	R/L	Horizontal display mode select signal; Low: Normal, High: Left/Right reverse mode
31	U/D	Vertical display mode select signal; High: Normal, Low: Up/Down reverse mode
32	V/Q	Resolution mode select signal; High: VGA, Low: QVGA
33	GND	GND

Note
The recommended mounting connector is a Kyocera 08-6210-020-340-800+. The connector is a 0.5mm pitch 33-pin FPC connector (17mm x 0.3mm gold plate).

6.2 Connection Examples

The information in this section provides a connection example for the S1D13513 display controller. The S1D13513 display controller is available in two packages. The connection information differs for each package and is listed separately.

In addition to the pin connections for the selected display controller, the TCG057VG1AC-G00 requires the following power supply.

VDD +3.3V (±0.3V)

For further details on the TCG057VG1AC-G00, such as power consumption and absolute maximum ratings, please contact your Kyocera representative.

6.2.1 Connecting the TCG057VG1AC-G00 to the S1D13513

The following diagram shows an example implementation of the TCG057VG1AC-G00 panel connected to the S1D13513.

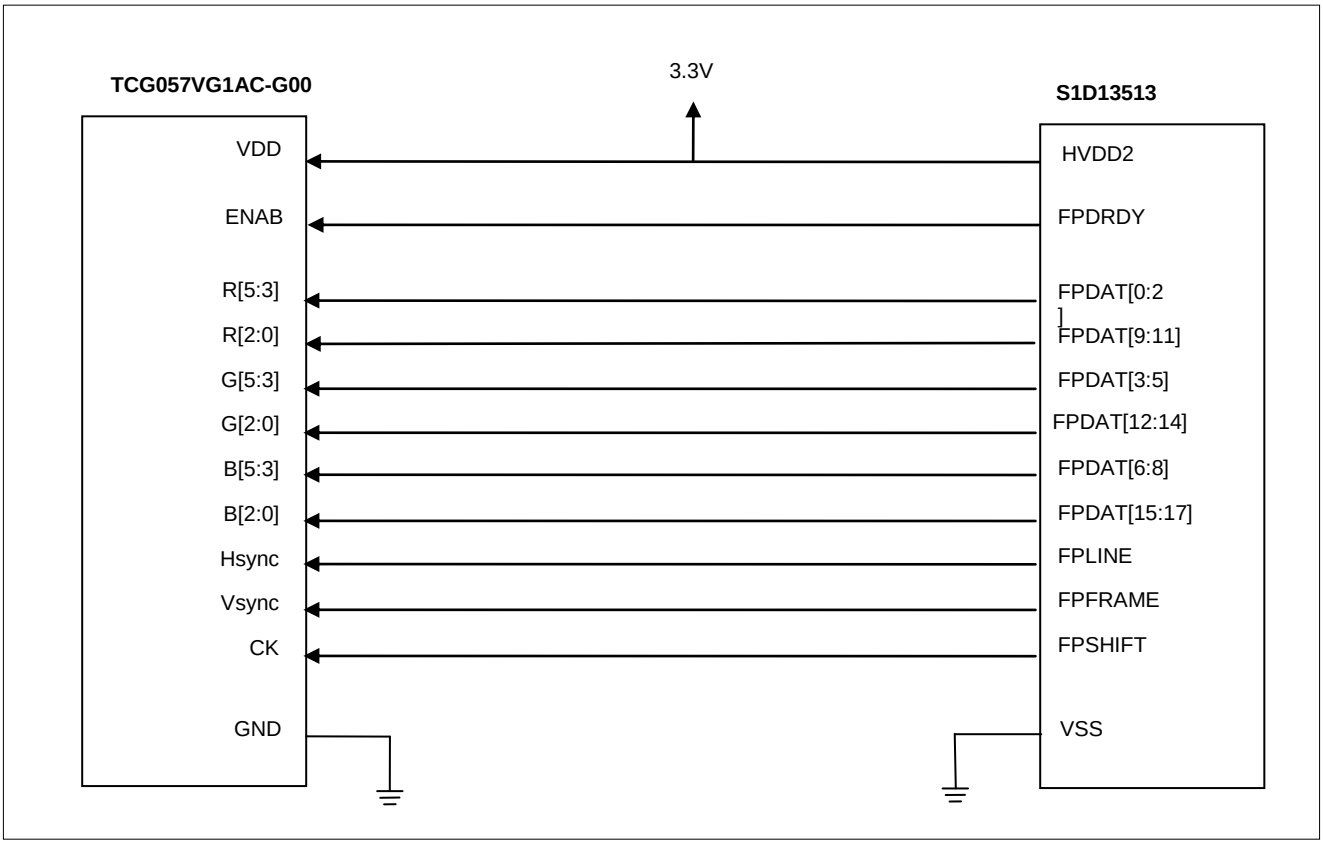

Figure 6-1 Connecting the TCG057VG1AC-G00 to the S1D13513

The following table provides a detailed pin listing for the required connections between the TCG057VG1AC-G00 and the S1D13513. Pin mappings are shown for both S1D13513 package types.

Table 6-2 Connecting the TCG057VG1AC-G00 to the S1D13513

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
1	GND	GND	—	—	VSS
2	CK	Clock signal for sampling each data signal	77	P8	FPSHIFT
3	Hsync	Horizontal synchronous signal (negative)	79	R8	FPLINE
4	Vsync	Vertical synchronous signal (negative)	78	T8	FPFRAME
5	GND	GND	—	—	VSS
6	R0	RED data signal (LSB)	61	N5	FPDAT11
7	R1	RED data signal	62	M5	FPDAT10
8	R2	RED data signal	63	P6	FPDAT9
9	R3	RED data signal	72	T7	FPDAT2
10	R4	RED data signal	73	N7	FPDAT1
11	R5	RED data signal (MSB)	74	M7	FPDAT0
12	GND	GND	—	—	VSS
13	G0	GREEN data signal (LSB)	56	R4	FPDAT14
14	G1	GREEN data signal	59	T4	FPDAT13
15	G2	GREEN data signal	60	T5	FPDAT12
16	G3	GREEN data signal	69	L7	FPDAT5
17	G4	GREEN data signal	70	P7	FPDAT4
18	G5	GREEN data signal (MSB)	71	R7	FPDAT3
19	GND	GND	—	—	VSS
20	B0	BLUE data signal (LSB)	53	N4	FPDAT17
21	B1	BLUE data signal	54	P4	FPDAT16
22	B2	BLUE data signal	55	T2	FPDAT15
23	B3	BLUE data signal	64	R6	FPDAT8
24	B4	BLUE data signal	67	K6	FPDAT7
25	B5	BLUE data signal (MSB)	68	M6	FPDAT6
26	GND	GND	—	—	VSS
27	ENAB	Signal to settle the horizontal display position (positive)	80	M8	FPDRDY
28	VDD	3.3V power supply	—	—	HVDD2
29	VDD	3.3V power supply	—	—	HVDD2
30	R/L	Horizontal display mode select signal Low: Normal, High: Left/Right reverse mode	—	—	—
31	U/D	Vertical display mode select signal High: Normal, Low: Up/Down reverse mode	—	—	—
32	V/Q	Resolution mode select signal High: VGA, Low: QVGA	—	—	—
33	GND	GND	—	—	VSS

6.3 Example Register Settings

In addition to the pin connections, the S1D13513 internal registers must be configured appropriately for the TCG057VG1AC-G00 LCD panel. The following table provides example settings. However, these values are for reference only and may differ according to each specific implementation.

Also included in the table is an example clock configuration designed to achieve a typical LCD refresh.

Example Register Settings for the S1D13513

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0800h] LCD Panel Type Select Register	0280h	—
REG[0802h] LCD Horizontal Total Register	799	800
REG[0804h] LCD Horizontal Display Period Register	319	640
REG[0806h] LCD Horizontal Display Period Start Position Register	61	61
REG[0808h] LCD Horizontal Pulse Width	16	17
REG[080Ah] LCD Horizontal Pulse Start Position	0	0
REG[080Ch] LCD Vertical Total Register	524	525
REG[080Eh] LCD Vertical Display Period Resister	479	480
REG[0810h] LCD Vertical Display Period Start Position Register	34	34
REG[0812h] LCD Vertical Pulse Width	2	3
REG[0814h] LCD Vertical Pulse Start Position	0	0
PLL2 output frequency in MHz	—	100
REG[0446h] LCD Clock Control Register	3	4
FPSHIFT in MHz	—	25
LCD Refresh in Hz	—	59.5

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13513 register values, see the *S1D13513 Hardware Functional Specification*, document number X78B-A-001-xx.

7 Connecting to the Kyocera KCG062HV1AA-A21

The Kyocera KCG062HV1AA-A21 LCD panel is compatible with the S1D13513 display controller. The following sections will provide connector details, pin mappings, and example register settings.

7.1 KCG062HV1AA-A21 Pin Mapping

The KCG062HV1AA-A21 LCD panel uses a 20-pin connector with the following pin mapping.

Table 7-1 KCG062HV1AA-A21 Pin Mapping

Connector Pin#	Pin Name	Pin Description
1	FRM	Synchronous signal for drive scanning line
2	LOAD	Data signal latch clock
3	CP	Data signal shift clock
4	DISP	Display control signal
5	VDD	Power supply for logic (+3.3V±0.3V)
6	VSS	GND
7	VCONT	LCD adjust voltage (+1.3V ≤ VCONT ≤ +2.3V)
8	D7	Data signal (MSB)
9	D6	Data signal
10	D5	Data signal
11	D4	Data signal
12	D3	Data signal
13	D2	Data signal
14	D1	Data signal
15	D0	Data signal (LSB)
16	VDD	Power supply for logic (+3.3V±0.3V)
17	VDD	Power supply for logic (+3.3V±0.3V)
18	VSS	GND
19	VSS	GND
20	VSS	GND

Note
The recommended mounting connector is a Kyocera 08-6210-020-340-800+. The connector is a 0.5mm pitch 20-pin FPC connector (10.5mm x 0.3mm gold plate).

7.2 Connection Examples

The information in this section provides a connection example for the S1D13513 display controller. The S1D13513 display controller is available in two packages. The connection information differs for each package and is listed separately.

In addition to the pin connections for the selected display controller, the KCG062HV1AA-A21 requires the following power supply.

VDD	+3.3V (±0.3V)
VCONT (liquid crystal drive power supply)	+1.8V (±0.5V)

For further details on the KCG062HV1AA-A21, such as power consumption and absolute maximum ratings, please contact your Kyocera representative.

7.2.1 Connecting the KCG062HV1AA-A21 to the S1D13513

The following diagram shows an example implementation of the KCG062HV1AA-A21 panel connected to the S1D13513.

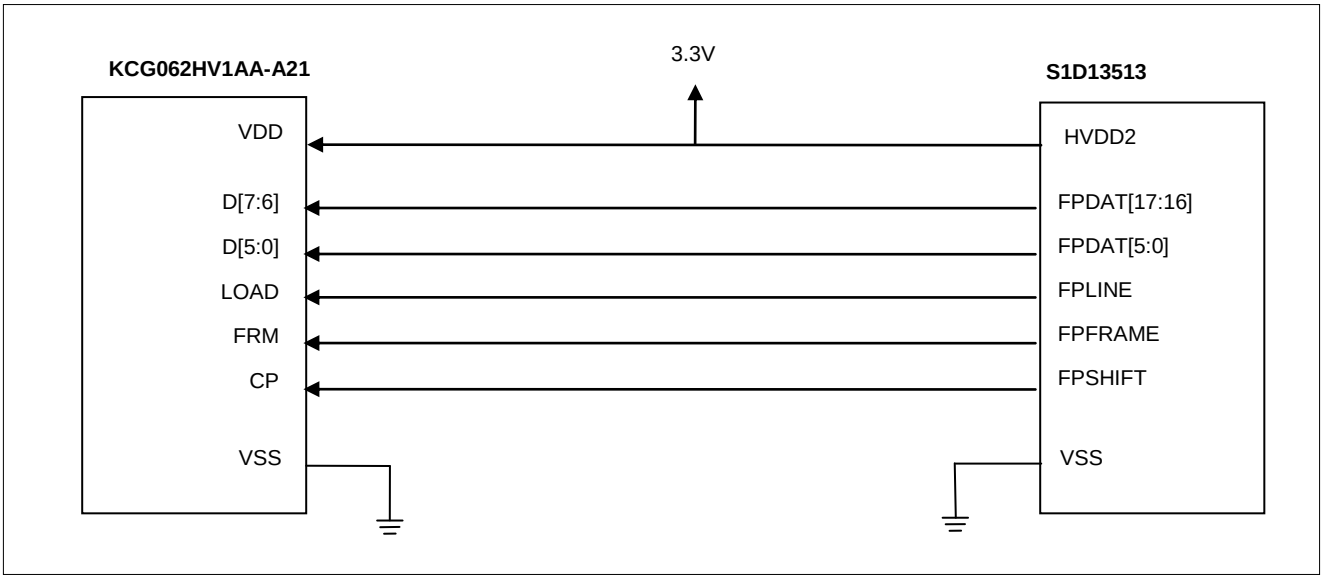

Figure 7-1 Connecting the KCG062HV1AA-A21 to the S1D13513

The following table provides a detailed pin listing for the required connections between the KCG062HV1AA-A21 and the S1D13513. Pin mappings are shown for both S1D13513 package types.

Table 7-2 Connecting the KCG062HV1AA-A21 to the S1D13513

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
1	FRM	Synchronous signal for drive scanning line	78	T8	FPFRAME
2	LOAD	Data signal latch clock	79	R8	FPLINE
3	CP	Data signal shift clock	77	P8	FPSHIFT
4	DISP	Display control signal	—	—	—
5	VDD	Power supply for logic (+3.3V±0.3V)	—	—	HVDD2
6	VSS	GND	—	—	VSS
7	VCONT	LCD adjust voltage (+1.3V ≤ VCONT ≤ +2.3V)	—	—	—
8	D7	Data signal (MSB)	53	N4	FPDAT17
9	D6	Data signal	54	P4	FPDAT16
10	D5	Data signal	69	L7	FPDAT5
11	D4	Data signal	70	P7	FPDAT4
12	D3	Data signal	71	R7	FPDAT3
13	D2	Data signal	72	T7	FPDAT2
14	D1	Data signal	73	N7	FPDAT1
15	D0	Data signal (LSB)	74	M7	FPDAT0
16	VDD	Power supply for logic (+3.3V±0.3V)	—	—	HVDD2
17	VDD	Power supply for logic (+3.3V±0.3V)	—	—	HVDD2
18	VSS	GND	—	—	VSS
19	VSS	GND	—	—	VSS
20	VSS	GND	—	—	VSS

7.3 Example Register Settings

In addition to the pin connections, the S1D13513 internal registers must be configured appropriately for the KCG062HV1AA-A21 LCD panel. The following table provides example settings. However, these values are for reference only and may differ according to each specific implementation.

Also included in the table is an example clock configuration designed to achieve a typical LCD refresh.

Table 7-3 Example Register Settings for the S1D13513

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0800h] LCD Panel Type Select Register	5100h	—
REG[0802h] LCD Horizontal Total Register	640t×3/8×4-1+20	980
REG[0804h] LCD Horizontal Display Period Register	319	640
REG[0806h] LCD Horizontal Display Period Start Position Register	20	20
REG[0808h] LCD Horizontal Pulse Width	8000h+16	17
REG[080Ah] LCD Horizontal Pulse Start Position	0	0
REG[080Ch] LCD Vertical Total Register	249	250
REG[080Eh] LCD Vertical Display Period Resister	239	240
REG[0810h] LCD Vertical Display Period Start Position Register	9	9
REG[0812h] LCD Vertical Pulse Width	8000h+0	1
REG[0814h] LCD Vertical Pulse Start Position	10	10
PLL2 output frequency in MHz	—	70
REG[0446h] LCD Clock Control Register	3	4
FPSHIFT in MHz	—	4.38
LCD Refresh in Hz	—	71.4

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13513 register values, see the *S1D13513 Hardware Functional Specification*, document number X78B-A-001-xx.

8 Connecting to the Kyocera KCG062HV1AE-G03

The Kyocera KCG062HV1AE-G03 LCD panel is compatible with the S1D13513 display controller. The following sections will provide connector details, pin mappings, and example register settings.

8.1 KCG062HV1AE-G03 Pin Mapping

The KCG062HV1AE-G03 LCD panel uses a 20-pin connector with the following pin mapping.

Table 8-1 KCG062HV1AE-G03 Pin Mapping

Connector Pin#	Pin Name	Pin Description
1	FRM	Synchronous signal for drive scanning line
2	LOAD	Data signal latch clock
3	CP	Data signal shift clock
4	DISP	Display control signal
5	VDD	Power supply for logic (+3.3V±0.3V)
6	VSS	GND
7	VCONT	LCD adjust voltage (+1.3V ≤ VCONT ≤ +2.3V)
8	D7	Data signal (MSB)
9	D6	Data signal
10	D5	Data signal
11	D4	Data signal
12	D3	Data signal
13	D2	Data signal
14	D1	Data signal
15	D0	Data signal (LSB)
16	VDD	Power supply for logic (+3.3V±0.3V)
17	VDD	Power supply for logic (+3.3V±0.3V)
18	VSS	GND
19	VSS	GND
20	VSS	GND

Note
The recommended mounting connector is a Kyocera 08-6210-020-340-800+. The connector is a 0.5mm pitch 20-pin FPC connector (10.5mm x 0.3mm gold plate).

8.2 Connection Examples

The information in this section provides a connection example for the S1D13513 display controller. The S1D13513 display controller is available in two packages. The connection information differs for each package and is listed separately.

In addition to the pin connections for the selected display controller, the KCG062HV1AE-G03 requires the following power supply.

VDD	+3.3V (±0.3V)
VCONT (liquid crystal drive power supply)	+1.8V (±0.5V)

For further details on the KCG062HV1AE-G03, such as power consumption and absolute maximum ratings, please contact your Kyocera representative.

8.2.1 Connecting the KCG062HV1AE-G03 to the S1D13513

The following diagram shows an example implementation of the KCG062HV1AE-G03 panel connected to the S1D13513.

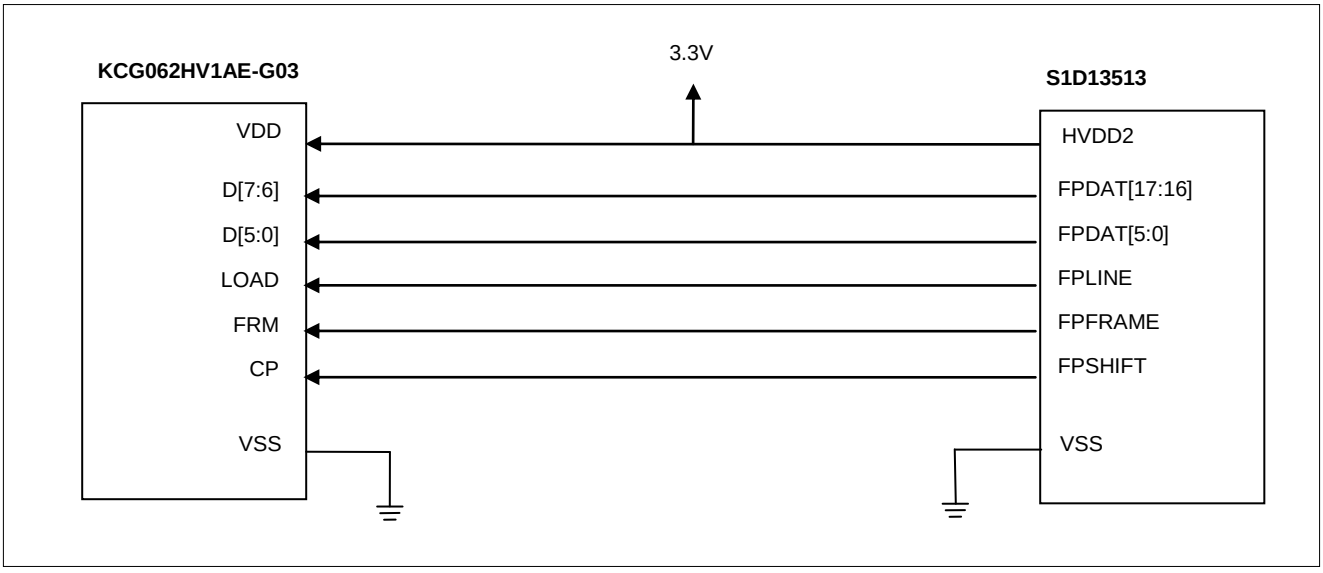

Figure 8-1 Connecting the KCG062HV1AE-G03 to the S1D13513

The following table provides a detailed pin listing for the required connections between the KCG062HV1AE-G03 and the S1D13513. Pin mappings are shown for both S1D13513 package types.

Table 8-2 Connecting the KCG062HV1AE-G03 to the S1D13513

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
1	FRM	Synchronous signal for drive scanning line	78	T8	FPFRAME
2	LOAD	Data signal latch clock	79	R8	FPLINE
3	CP	Data signal shift clock	77	P8	FPSHIFT
4	DISP	Display control signal	—	—	—
5	VDD	Power supply for logic (+3.3V±0.3V)	—	—	HVDD2
6	VSS	GND	—	—	VSS
7	VCONT	LCD adjust voltage (+1.3V ≤ VCONT ≤ +2.3V)	—	—	—
8	D7	Data signal (MSB)	53	N4	FPDAT17
9	D6	Data signal	54	P4	FPDAT16
10	D5	Data signal	69	L7	FPDAT5
11	D4	Data signal	70	P7	FPDAT4
12	D3	Data signal	71	R7	FPDAT3
13	D2	Data signal	72	T7	FPDAT2
14	D1	Data signal	73	N7	FPDAT1
15	D0	Data signal (LSB)	74	M7	FPDAT0
16	VDD	Power supply for logic (+3.3V±0.3V)	—	—	HVDD2
17	VDD	Power supply for logic (+3.3V±0.3V)	—	—	HVDD2
18	VSS	GND	—	—	VSS
19	VSS	GND	—	—	VSS
20	VSS	GND	—	—	VSS

8.3 Example Register Settings

In addition to the pin connections, the S1D13513 internal registers must be configured appropriately for the KCG062HV1AE-G03 LCD panel. The following table provides example settings. However, these values are for reference only and may differ according to each specific implementation.

Also included in the table is an example clock configuration designed to achieve a typical LCD refresh.

Example Register Settings for the S1D13513

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0800h] LCD Panel Type Select Register	5100h	—
REG[0802h] LCD Horizontal Total Register	640t×3/8×4-1+20	980
REG[0804h] LCD Horizontal Display Period Register	319	640
REG[0806h] LCD Horizontal Display Period Start Position Register	20	20
REG[0808h] LCD Horizontal Pulse Width	8000h+16	17
REG[080Ah] LCD Horizontal Pulse Start Position	0	0
REG[080Ch] LCD Vertical Total Register	249	250
REG[080Eh] LCD Vertical Display Period Resister	239	240
REG[0810h] LCD Vertical Display Period Start Position Register	9	9
REG[0812h] LCD Vertical Pulse Width	8000h+0	1
REG[0814h] LCD Vertical Pulse Start Position	10	10

PLL2 output frequency in MHz	—	70
REG[0446h] LCD Clock Control Register	3	4
FPSHIFT in MHz	—	4.38
LCD Refresh in Hz	—	71.4

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13513 register values, see the *S1D13513 Hardware Functional Specification*, document number X78B-A-001-xx.

9 Connecting to the Kyocera TCG062HV1AE-G00

The Kyocera TCG062HV1AE-G00 LCD panel is compatible with the S1D13513, S1D13742, S1D13743, and S1D13748 display controllers. The following sections will provide connector details, pin mappings, and example register settings.

9.1 TCG062HV1AE-G00 Pin Mapping

The TCG062HV1AE-G00 LCD panel uses a 33-pin connector with the following pin mapping.

Table 9-1 TCG062HV1AE-G00 Pin Mapping

Connector Pin#	Pin Name	Pin Description
1	GND	GND
2	CK	Clock signal for sampling each data signal
3	Hsync	Horizontal synchronous signal (negative)
4	Vsync	Vertical synchronous signal (negative)
5	GND	GND
6	R0	RED data signal (LSB)
7	R1	RED data signal
8	R2	RED data signal
9	R3	RED data signal
10	R4	RED data signal
11	R5	RED data signal (MSB)
12	GND	GND
13	G0	GREEN data signal (LSB)
14	G1	GREEN data signal
15	G2	GREEN data signal
16	G3	GREEN data signal
17	G4	GREEN data signal
18	G5	GREEN data signal (MSB)
19	GND	GND
20	B0	BLUE data signal (LSB)
21	B1	BLUE data signal
22	B2	BLUE data signal
23	B3	BLUE data signal
24	B4	BLUE data signal
25	B5	BLUE data signal (MSB)
26	GND	GND
27	ENAB	Signal to settle the horizontal display position (positive)
28	VDD	3.3V power supply
29	VDD	3.3V power supply
30	R/L	Horizontal display mode select signal Low: Normal, High: Left/Right reverse mode

Connector Pin#	Pin Name	Pin Description
31	U/D	Vertical display mode select signal High: Normal, Low: Up/Down reverse mode
32	NC	not connected
33	GND	GND

Note
The recommended mounting connector is a Kyocera 08-6210-020-340-800+. The connector is a 0.5mm pitch 33-pin FPC connector (17mm x 0.3mm gold plate).

9.2 Connection Examples

The information in this section provides connection examples for the S1D13513, S1D13742, S1D13743, and S1D13748 display controllers. Some display controllers are available in two packages. The connection information differs for each package and is listed separately.

In addition to the pin connections for the selected display controller, the TCG062HV1AE-G00 requires the following power supply.

VDD	+3.3V (±0.3V)
VCONT (liquid crystal drive power supply)	+1.8V (±0.5V)

For further details on the TCG062HV1AE-G00, such as power consumption and absolute maximum ratings, please contact your Kyocera representative.

9.2.1 Connecting the TCG062HV1AE-G00 to the S1D13513

The following diagram shows an example implementation of the TCG062HV1AE-G00 panel connected to the S1D13513.

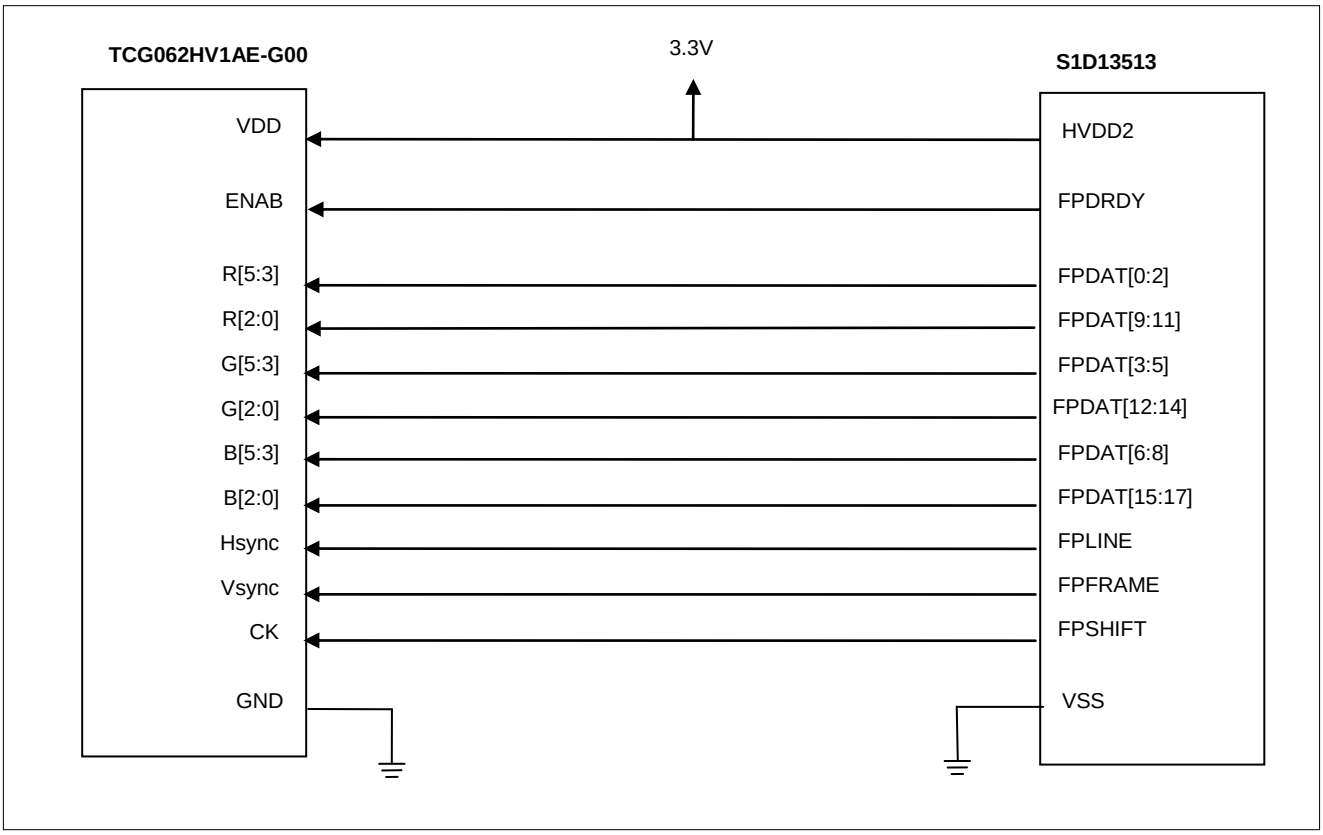

Figure 9-1 Connecting the TCG062HV1AE-G00 to the S1D13513

The following table provides a detailed pin listing for the required connections between the TCG062HV1AE-G00 and the S1D13513. Pin mappings are shown for both S1D13513 package types.

Table 9-2 Connecting the TCG062HV1AE-G00 to the S1D13513

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
1	GND	GND	—	—	VSS
2	CK	Clock signal for sampling each data signal	77	P8	FPSHIFT
3	Hsync	Horizontal synchronous signal (negative)	79	R8	FPLINE
4	Vsync	Vertical synchronous signal (negative)	78	T8	FPFRAME
5	GND	GND	—	—	VSS
6	R0	RED data signal (LSB)	61	N5	FPDAT11
7	R1	RED data signal	62	M5	FPDAT10
8	R2	RED data signal	63	P6	FPDAT9
9	R3	RED data signal	72	T7	FPDAT2
10	R4	RED data signal	73	N7	FPDAT1

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
11	R5	RED data signal (MSB)	74	M7	FPDAT0
12	GND	GND	—	—	VSS
13	G0	GREEN data signal (LSB)	56	R4	FPDAT14
14	G1	GREEN data signal	59	T4	FPDAT13
15	G2	GREEN data signal	60	T5	FPDAT12
16	G3	GREEN data signal	69	L7	FPDAT5
17	G4	GREEN data signal	70	P7	FPDAT4
18	G5	GREEN data signal (MSB)	71	R7	FPDAT3
19	GND	GND	—	—	VSS
20	B0	BLUE data signal (LSB)	53	N4	FPDAT17
21	B1	BLUE data signal	54	P4	FPDAT16
22	B2	BLUE data signal	55	T2	FPDAT15
23	B3	BLUE data signal	64	R6	FPDAT8
24	B4	BLUE data signal	67	K6	FPDAT7
25	B5	BLUE data signal (MSB)	68	M6	FPDAT6
26	GND	GND	—	—	VSS
27	ENAB	Signal to settle the horizontal display position (positive)	80	M8	FPDRDY
28	VDD	3.3V power supply	—	—	HVDD2
29	VDD	3.3V power supply	—	—	HVDD2
30	R/L	Horizontal display mode select signal Low: Normal, High: Left/Right reverse mode	—	—	—
31	U/D	Vertical display mode select signal High: Normal, Low: Up/Down reverse mode	—	—	—
32	NC	not connected	—	—	—
33	GND	GND	—	—	VSS

9.2.2 Connecting the TCG062HV1AE-G00 to the S1D13742

The following diagram shows an example implementation of the TCG062HV1AE-G00 panel connected to the S1D13742.

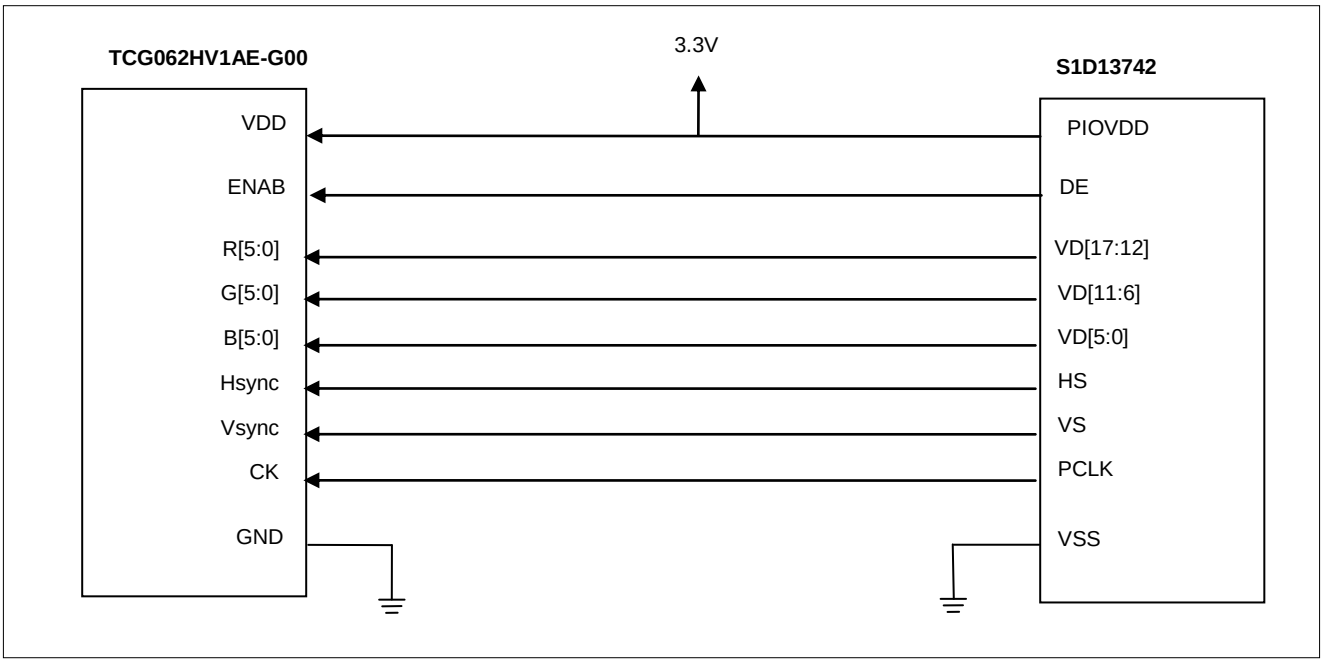

Figure 9-2 Connecting the TCG062HV1AE-G00 to the S1D13742

The following table provides a detailed pin listing for the required connections between the TCG062HV1AE-G00 and the S1D13742. Pin mappings are shown for both S1D13742 package types.

Table 9-3 Connecting the TCG062HV1AE-G00 to the S1D13742

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13742 QFP Pin#	S1D13742 FCBGA Ball#	S1D13742 Pin Name
1	GND	GND	—	—	VSS
2	CK	Clock signal for sampling each data signal	11	D11	PCLK
3	Hsync	Horizontal synchronous signal (negative)	9	D9	HS
4	Vsync	Vertical synchronous signal (negative)	10	D10	VS
5	GND	GND	—	—	VSS
6	R0	RED data signal (LSB)	61	K5	VD12
7	R1	RED data signal	64	K4	VD13
8	R2	RED data signal	30	J11	VD14
9	R3	RED data signal	29	J10	VD15
10	R4	RED data signal	43	J9	VD16
11	R5	RED data signal (MSB)	47	J8	VD17
12	GND	GND	—	—	VSS
13	G0	GREEN data signal (LSB)	66	L3	VD6
14	G1	GREEN data signal	42	K10	VD7

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13742 QFP Pin#	S1D13742 FCBGA Ball#	S1D13742 Pin Name
15	G2	GREEN data signal	44	K9	VD8
16	G3	GREEN data signal	48	K8	VD9
17	G4	GREEN data signal	51	K7	VD10
18	G5	GREEN data signal (MSB)	58	K6	VD11
19	GND	GND	—	—	VSS
20	B0	BLUE data signal (LSB)	45	L9	VD0
21	B1	BLUE data signal	49	L8	VD1
22	B2	BLUE data signal	54	L7	VD2
23	B3	BLUE data signal	59	L6	VD3
24	B4	BLUE data signal	62	L5	VD4
25	B5	BLUE data signal (MSB)	65	L4	VD5
26	GND	GND	—	—	VSS
27	ENAB	Signal to settle the horizontal display position (positive)	8	C11	DE
28	VDD	3.3V power supply	—	—	PIOVDD
29	VDD	3.3V power supply	—	—	PIOVDD
30	R/L	Horizontal display mode select signal Low: Normal, High: Left/Right reverse mode	—	—	—
31	U/D	Vertical display mode select signal High: Normal, Low: Up/Down reverse mode	—	—	—
32	V/Q	Resolution mode select signal High: VGA, Low: QVGA	—	—	—
33	GND	GND	—	—	VSS

9.2.3 Connecting the TCG062HV1AE-G00 to the S1D13743

The following diagram shows an example implementation of the TCG062HV1AE-G00 panel connected to the S1D13743.

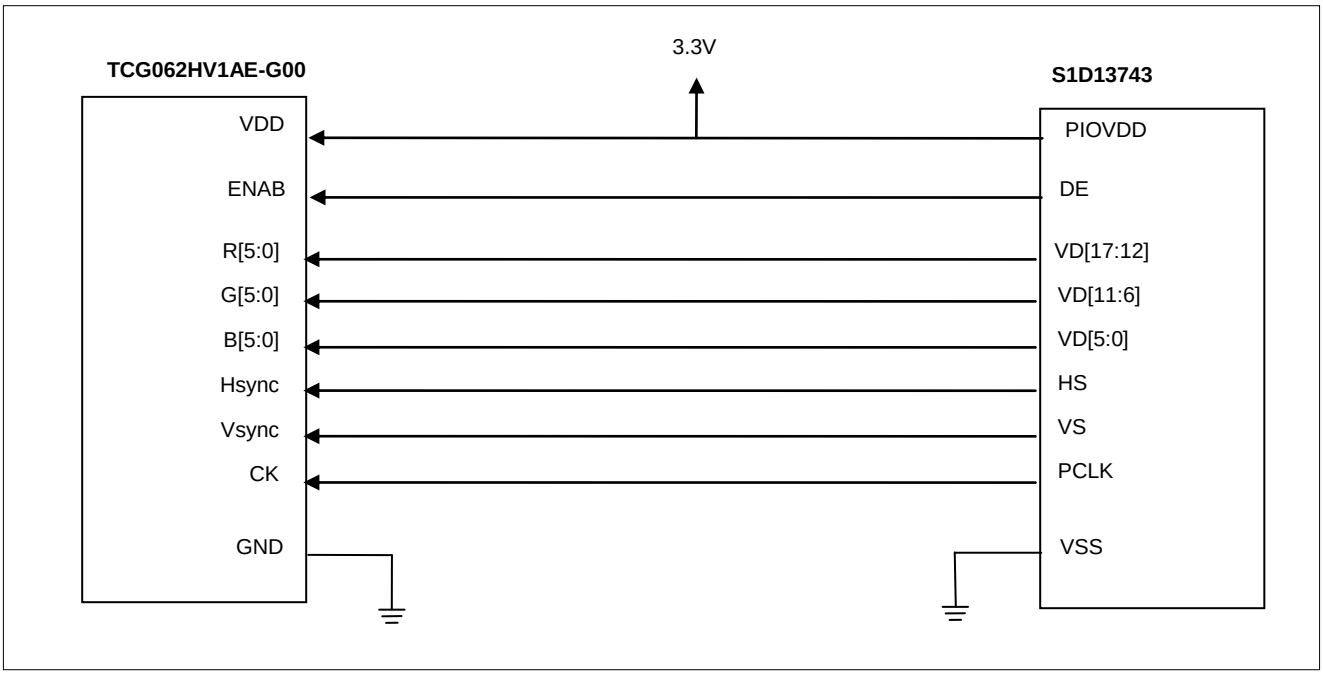

Figure 9-3 Connecting the TCG062HV1AE-G00 to the S1D13743

The following table provides a detailed pin listing for the required connections between the TCG062HV1AE-G00 and the S1D13743. Pin mappings are shown for both S1D13743 package types.

Table 9-4 Connecting the TCG062HV1AE-G00 to the S1D13743

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13743 QFP Pin#	S1D13743 FCBGA Ball#	S1D13743 Pin Name
1	GND	GND	—	—	VSS
2	CK	Clock signal for sampling each data signal	8	D11	PCLK
3	Hsync	Horizontal synchronous signal (negative)	4	D9	HS
4	Vsync	Vertical synchronous signal (negative)	5	D10	VS
5	GND	GND	—	—	VSS
6	R0	RED data signal (LSB)	56	K5	VD12
7	R1	RED data signal	61	K4	VD13
8	R2	RED data signal	15	J11	VD14
9	R3	RED data signal	14	J10	VD15
10	R4	RED data signal	20	J9	VD16
11	R5	RED data signal (MSB)	40	J8	VD17
12	GND	GND	—	—	VSS
13	G0	GREEN data signal (LSB)	63	L3	VD6
14	G1	GREEN data signal	21	K10	VD7

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13743 QFP Pin#	S1D13743 FCBGA Ball#	S1D13743 Pin Name
15	G2	GREEN data signal	38	K9	VD8
16	G3	GREEN data signal	44	K8	VD9
17	G4	GREEN data signal	48	K7	VD10
18	G5	GREEN data signal (MSB)	51	K6	VD11
19	GND	GND	—	—	VSS
20	B0	BLUE data signal (LSB)	39	L9	VD0
21	B1	BLUE data signal	43	L8	VD1
22	B2	BLUE data signal	49	L7	VD2
23	B3	BLUE data signal	54	L6	VD3
24	B4	BLUE data signal	57	L5	VD4
25	B5	BLUE data signal (MSB)	62	L4	VD5
26	GND	GND	—	—	VSS
27	ENAB	Signal to settle the horizontal display position (positive)	3	C11	DE
28	VDD	3.3V power supply	—	—	PIOVDD
29	VDD	3.3V power supply	—	—	PIOVDD
30	R/L	Horizontal display mode select signal Low: Normal, High: Left/Right reverse mode	—	—	—
31	U/D	Vertical display mode select signal High: Normal, Low: Up/Down reverse mode	—	—	—
32	V/Q	Resolution mode select signal High: VGA, Low: QVGA	—	—	—
33	GND	GND	—	—	VSS

9.2.4 Connecting the TCG062HV1AE-G00 to the S1D13748

The following diagram shows an example implementation of the TCG062HV1AE-G00 panel connected to the S1D13748.

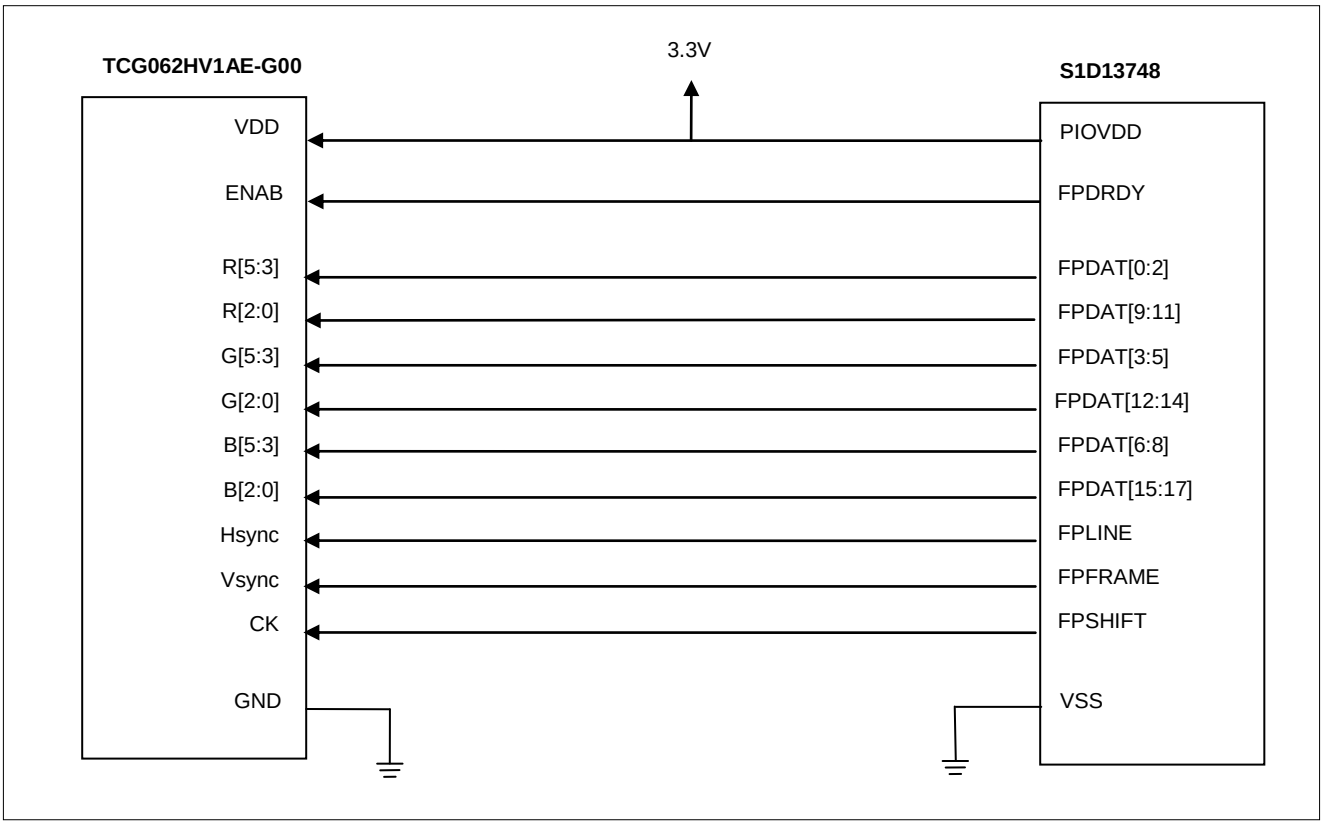

Figure 9-4 Connecting the TCG062HV1AE-G00 to the S1D13748

The following table provides a detailed pin listing for the required connections between the TCG062HV1AE-G00 and the S1D13748. Pin mappings are shown for both S1D13748 package types.

Table 9-5 Connecting the TCG062HV1AE-G00 to the S1D13748

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
1	GND	GND	—	—	VSS
2	CK	Clock signal for sampling each data signal	75	J11	FPSHIFT
3	Hsync	Horizontal synchronous signal (negative)	77	H10	FPLINE
4	Vsync	Vertical synchronous signal (negative)	76	J10	FPFRAME
5	GND	GND	—	—	VSS
6	R0	RED data signal (LSB)	63	L8	FPDAT11
7	R1	RED data signal	62	J8	FPDAT10
8	R2	RED data signal	61	K8	FPDAT9
9	R3	RED data signal	51	K5	FPDAT2
10	R4	RED data signal	50	L5	FPDAT1

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
11	R5	RED data signal (MSB)	49	J5	FPDAT0
12	GND	GND	—	—	VSS
13	G0	GREEN data signal (LSB)	69	H8	FPDAT14
14	G1	GREEN data signal	68	K9	FPDAT13
15	G2	GREEN data signal	64	L9	FPDAT12
16	G3	GREEN data signal	54	L6	FPDAT5
17	G4	GREEN data signal	53	J6	FPDAT4
18	G5	GREEN data signal (MSB)	52	H6	FPDAT3
19	GND	GND	—	—	VSS
20	B0	BLUE data signal (LSB)	72	J9	FPDAT17
21	B1	BLUE data signal	71	K10	FPDAT16
22	B2	BLUE data signal	70	L10	FPDAT15
23	B3	BLUE data signal	60	K7	FPDAT8
24	B4	BLUE data signal	59	J7	FPDAT7
25	B5	BLUE data signal (MSB)	58	L7	FPDAT6
26	GND	GND	—	—	VSS
27	ENAB	Signal to settle the horizontal display position (positive)	78	G7	FPDRDY
28	VDD	3.3V power supply	—	—	PIOVDD
29	VDD	3.3V power supply	—	—	PIOVDD
30	R/L	Horizontal display mode select signal Low: Normal, High: Left/Right reverse mode	—	—	—
31	U/D	Vertical display mode select signal High: Normal, Low: Up/Down reverse mode	—	—	—
32	V/Q	Resolution mode select signal High: VGA, Low: QVGA	—	—	—
33	GND	GND	—	—	VSS

9.3 Example Register Settings

In addition to the pin connections, the S1D13513/S1D13742/S1D13743/S1D13748 internal registers must be configured appropriately for the TCG062HV1AE-G00 LCD panel. The following tables provide example settings for each display controller. However, these values are for reference only and may differ according to each specific implementation.

Also included in the table is an example clock configuration designed to achieve a typical LCD refresh.

Table 9-6 Example Register Settings for the S1D13513

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0800h] LCD Panel Type Select Register	0280h	—
REG[0802h] LCD Horizontal Total Register	799	800
REG[0804h] LCD Horizontal Display Period Register	319	640
REG[0806h] LCD Horizontal Display Period Start Position Register	61	61
REG[0808h] LCD Horizontal Pulse Width	16	17
REG[080Ah] LCD Horizontal Pulse Start Position	0	0
REG[080Ch] LCD Vertical Total Register	524	525
REG[080Eh] LCD Vertical Display Period Resister	239	240
REG[0810h] LCD Vertical Display Period Start Position Register	34	34
REG[0812h] LCD Vertical Pulse Width	2	3
REG[0814h] LCD Vertical Pulse Start Position	0	0
PLL2 output frequency in MHz	—	100
REG[0446h] LCD Clock Control Register	3	4
FPSHIFT in MHz	—	25
LCD Refresh in Hz	—	59.5

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13513 register values, see the *S1D13513 Hardware Functional Specification*, document number X78B-A-001-xx.

Table 9-7 Example Register Settings for the S1D13742

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[14h] Panel Type Register	00h	—
REG[16h] Horizontal Display Width Register	80	640
REG[18h] Horizontal Non-Display Period Register	127	127
REG[1Ah]~[1Ch] Vertical Display Height Registers	240	240
REG[1Eh] Vertical Non-Display Period Register	150	150
REG[20h] HS Pulse Width Register	16	16
REG[22h] HS Pulse Start Position Register 0	0	0
REG[24h] VS Pulse Width Register	2	2
REG[26h] VS Pulse Start Position Register 0	117	117
PLL output frequency in MHz	—	66
REG[12h] Pixel Clock Configuration Register	11h	3
FPSHIFT in MHz	—	22
LCD Refresh in Hz	—	45.5

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13742 register values, see the *S1D13742 Hardware Functional Specification*, document number X63A-A-001-xx.

Table 9-8 Example Register Settings for the S1D13743

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[14h] Panel Type Register	00h	—
REG[16h] Horizontal Display Width Register	80	640
REG[18h] Horizontal Non－Display Period Register	127	127
REG[1Ah]~[1Ch] Vertical Display Height Register0,1	240	240
REG[1Eh] Vertical Non－Display Period Register	150	150
REG[20h] HS Pulse Width Register	16	16
REG[22h] HS Pulse Start Position Resister	0	0
REG[24h] VS Pulse Width Register	2	2
REG[26h] VS Pulse Start Position Resister	112	112
PLL output frequency in MHz	—	66
REG[12h] Clock Source Select Register	19h	4
FPSHIFT in MHz	—	16.5
LCD Refresh in Hz	—	55.2

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13743 register values, see the *S1D13743 Hardware Functional Specification*, document number X70A-A-001-xx.

Table 9-9 Example Register Settings for the S1D13748

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0040h] LCD1 Horizontal Total Register	99	800
REG[0042h] LCD1 Horizontal Display Period Register	319	640
REG[0044h] LCD1 Horizontal Display Period Start Position Register	53	53
REG[0046h] LCD1 Horizontal Pulse Register	15	16
REG[0048h] LCD1 Horizontal Pulse Start Position Register	0	1
REG[004Ah] LCD1 Vertical Total Register	524	525
REG[004Ch] LCD1 Vertical Display Period Resister	239	240
REG[0050h] LCD1 Vertical Pulse Register	9	34
REG[0052h] LCD1 Vertical Pulse Start Position Register	0	1
REG[0246h] Main1 Window Image Horizontal Size Register	0	1
REG[0248h] Main1 Window Image Vertical Size Register	639	640
REG[004Eh] LCD1 Vertical Display Period Start Position Register	239	240
PLL output frequency in MHz	—	50
REG[0030h] LCD Interface Clock Setting Register	0500h	2
FPSHIFT in MHz	—	25
LCD Refresh in Hz	—	59.5

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13748 register values, see the *S1D13748 Hardware Functional Specification*, document number X80A-A-001-xx.

10 Connecting to the Kyocera KCG075VG2BE-G00

The Kyocera KCG075VG2BE-G00 LCD panel is compatible with the S1D13513 display controller. The following sections will provide connector details, pin mappings, and example register settings.

10.1 KCG075VG2BE-G00 Pin Mapping

The KCG075VG2BE-G00 LCD panel uses a 20-pin connector with the following pin mapping.

Table 10-1 KCG075VG2BE-G00 Pin Mapping

Connector Pin#	Pin Name	Pin Description
1	FRM	Synchronous signal for drive scanning line
2	LOAD	Data signal latch clock
3	CP	Data signal shift clock
4	DISP	Display control signal
5	VDD	Power supply for logic (+3.3V±0.3V)
6	VSS	GND
7	VCONT	LCD adjust voltage (+1.45V ≤ VCONT ≤ +2.45V)
8	D7	Data signal (MSB)
9	D6	Data signal
10	D5	Data signal
11	D4	Data signal
12	D3	Data signal
13	D2	Data signal
14	D1	Data signal
15	D0	Data signal (LSB)
16	VDD	Power supply for logic (+3.3V±0.3V)
17	VDD	Power supply for logic (+3.3V±0.3V)
18	VSS	GND
19	VSS	GND
20	VSS	GND

Note
The recommended mounting connector is a Kyocera 08-6210-020-340-800+. The connector is a 0.5mm pitch 20-pin FPC connector (10.5mm x 0.3mm gold plate).

10.2 Connection Examples

The information in this section provides a connection example for the S1D13513 display controller. The S1D13513 display controller is available in two packages. The connection information differs for each package and is listed separately.

In addition to the pin connections for the selected display controller, the KCG075VG2BE-G00 requires the following power supply.

VDD	+3.3V (±0.3V)
VCONT (liquid crystal drive power supply)	+1.95V (±0.5V)

For further details on the KCG075VG2BE-G00, such as power consumption and absolute maximum ratings, please contact your Kyocera representative.

10.2.1 Connecting the KCG075VG2BE-G00 to the S1D13513

The following diagram shows an example implementation of the KCG075VG2BE-G00 panel connected to the S1D13513.

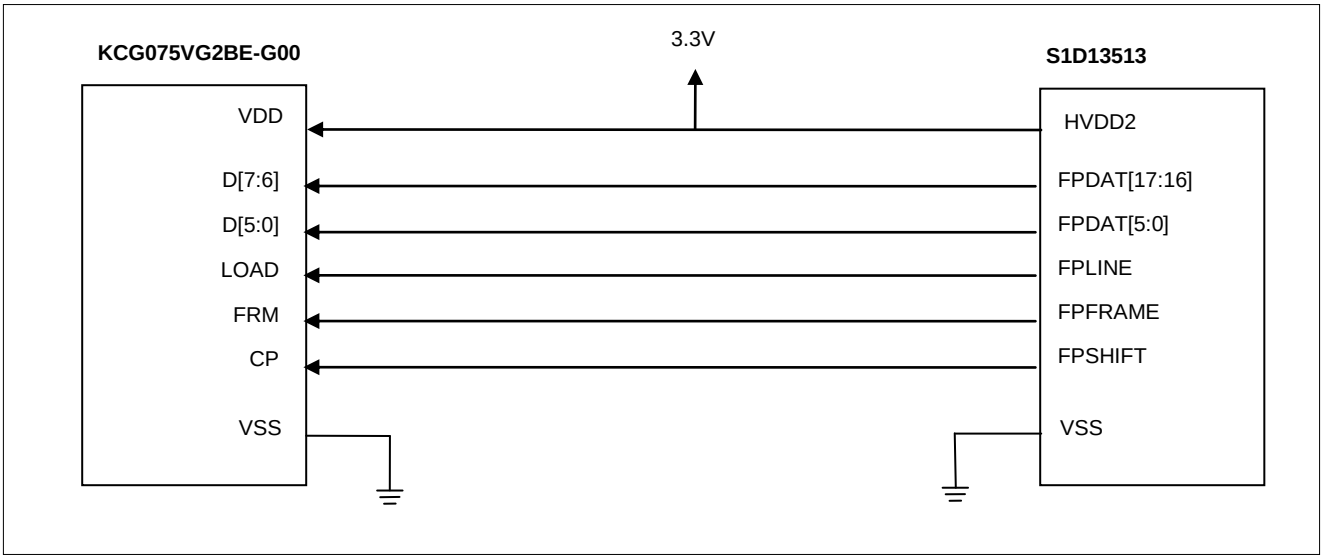

Figure 10-1 Connecting the KCG075VG2BE-G00 to the S1D13513

The following table provides a detailed pin listing for the required connections between the KCG075VG2BE-G00 and the S1D13513. Pin mappings are shown for both S1D13513 package types.

Table 10-2 Connecting the KCG075VG2BE-G00 to the S1D13513

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
1	FRM	Synchronous signal for drive scanning line	78	T8	FPFRAME
2	LOAD	Data signal latch clock	79	R8	FPLINE
3	CP	Data signal shift clock	77	P8	FPSHIFT
4	DISP	Display control signal	—	—	—
5	VDD	Power supply for logic (+3.3V±0.3V)	—	—	HVDD2
6	VSS	GND	—	—	VSS
7	VCONT	LCD adjust voltage (+1.45V ≤ VCONT ≤ +2.45V)	—	—	—
8	D7	Data signal (MSB)	53	N4	FPDAT17
9	D6	Data signal	54	P4	FPDAT16
10	D5	Data signal	69	L7	FPDAT5
11	D4	Data signal	70	P7	FPDAT4
12	D3	Data signal	71	R7	FPDAT3
13	D2	Data signal	72	T7	FPDAT2
14	D1	Data signal	73	N7	FPDAT1
15	D0	Data signal (LSB)	74	M7	FPDAT0
16	VDD	Power supply for logic (+3.3V±0.3V)	—	—	HVDD2
17	VDD	Power supply for logic (+3.3V±0.3V)	—	—	HVDD2
18	VSS	GND	—	—	VSS
19	VSS	GND	—	—	VSS
20	VSS	GND	—	—	VSS

10.3 Example Register Settings

In addition to the pin connections, the S1D13513 internal registers must be configured appropriately for the KCG075VG2BE-G00 LCD panel. The following table provides example settings. However, these values are for reference only and may differ according to each specific implementation.

Also included in the table is an example clock configuration designed to achieve a typical LCD refresh.

Table 10-3 Example Register Settings for the S1D13513

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0800h] LCD Panel Type Select Register	5100h	—
REG[0802h] LCD Horizontal Total Register	640×3/8×4-1+30	990
REG[0804h] LCD Horizontal Display Period Register	319	640
REG[0806h] LCD Horizontal Display Period Start Position Register	20	20
REG[0808h] LCD Horizontal Pulse Width	8000h+16	17
REG[080Ah] LCD Horizontal Pulse Start Position	0	0
REG[080Ch] LCD Vertical Total Register	489	490
REG[080Eh] LCD Vertical Display Period Resister	479	480
REG[0810h] LCD Vertical Display Period Start Position Register	9	9
REG[0812h] LCD Vertical Pulse Width	8000h+0	1
REG[0814h] LCD Vertical Pulse Start Position	10	10
PLL2 output frequency in MHz	—	70
REG[0446h] LCD Clock Control Register	3	2
FPSHIFT in MHz	—	8.75
LCD Refresh in Hz	—	72.2

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13513 register values, see the *S1D13513 Hardware Functional Specification*, document number X78B-A-001-xx.

11 Connecting to the Kyocera TCG075VG2AC-G00

The Kyocera TCG075VG2AC-G00 LCD panel is compatible with the S1D13513 and S1D13748 display controllers. The following sections will provide connector details, pin mappings, and example register settings.

11.1 TCG075VG2AC-G00 Pin Mapping

The TCG075VG2AC-G00 LCD panel uses a 33-pin connector with the following pin mapping.

Table 11-1 TCG075VG2AC-G00 Pin Mapping

Connector Pin#	Pin Name	Pin Description
1	GND	GND
2	CK	Clock signal for sampling each data signal
3	Hsync	Horizontal synchronous signal (negative)
4	Vsync	Vertical synchronous signal (negative)
5	GND	GND
6	R0	RED data signal (LSB)
7	R1	RED data signal
8	R2	RED data signal
9	R3	RED data signal
10	R4	RED data signal
11	R5	RED data signal (MSB)
12	GND	GND
13	G0	GREEN data signal (LSB)
14	G1	GREEN data signal
15	G2	GREEN data signal
16	G3	GREEN data signal
17	G4	GREEN data signal
18	G5	GREEN data signal (MSB)
19	GND	GND
20	B0	BLUE data signal (LSB)
21	B1	BLUE data signal
22	B2	BLUE data signal
23	B3	BLUE data signal
24	B4	BLUE data signal
25	B5	BLUE data signal (MSB)
26	GND	GND
27	ENAB	Signal to settle the horizontal display position (positive)
28	VDD	3.3V power supply
29	VDD	3.3V power supply
30	R/L	Horizontal display mode select signal; Low: Normal, High: Left/Right reverse mode
31	U/D	Vertical display mode select signal; High: Normal, Low: Up/Down reverse mode

Connector Pin#	Pin Name	Pin Description
32	NC	not connected
33	GND	GND

Note
The recommended mounting connector is a Kyocera 08-6210-020-340-800+. The connector is a 0.5mm pitch 33-pin FPC connector (17mm x 0.3mm gold plate).

11.2 Connection Examples

The information in this section provides connection examples for the S1D13513 and S1D13748 display controllers. Some display controllers are available in two packages. The connection information differs for each package and is listed separately.

In addition to the pin connections for the selected display controller, the TCG075VG2AC-G00 requires the following power supply.

VDD +3.3V (±0.3V)

For further details on the TCG075VG2AC-G00, such as power consumption and absolute maximum ratings, please contact your Kyocera representative.

11.2.1 Connecting the TCG075VG2AC-G00 to the S1D13513

The following diagram shows an example implementation of the TCG075VG2AC-G00 panel connected to the S1D13513.

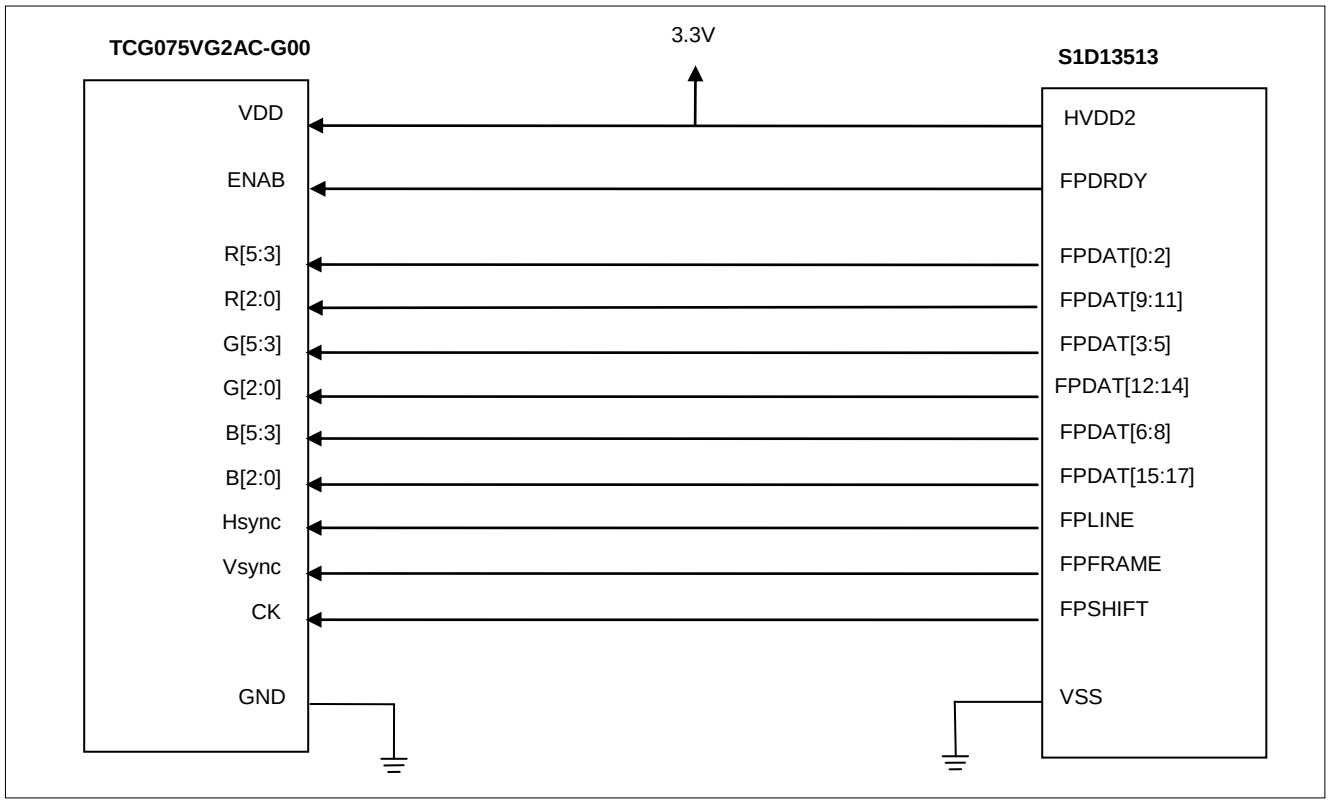

Figure 11-1 Connecting the TCG075VG2AC-G00 to the S1D13513

The following table provides a detailed pin listing for the required connections between the TCG075VG2AC-G00 and the S1D13513. Pin mappings are shown for both S1D13513 package types.

Table 11-2 Connecting the TCG075VG2AC-G00 to the S1D13513

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
1	GND	GND	—	—	VSS
2	CK	Clock signal for sampling each data signal	77	P8	FPSHIFT
3	Hsync	Horizontal synchronous signal (negative)	79	R8	FPLINE
4	Vsync	Vertical synchronous signal (negative)	78	T8	FPFRAME
5	GND	GND	—	—	VSS
6	R0	RED data signal (LSB)	61	N5	FPDAT11
7	R1	RED data signal	62	M5	FPDAT10
8	R2	RED data signal	63	P6	FPDAT9
9	R3	RED data signal	72	T7	FPDAT2
10	R4	RED data signal	73	N7	FPDAT1
11	R5	RED data signal (MSB)	74	M7	FPDAT0
12	GND	GND	—	—	VSS
13	G0	GREEN data signal (LSB)	56	R4	FPDAT14
14	G1	GREEN data signal	59	T4	FPDAT13
15	G2	GREEN data signal	60	T5	FPDAT12
16	G3	GREEN data signal	69	L7	FPDAT5
17	G4	GREEN data signal	70	P7	FPDAT4
18	G5	GREEN data signal (MSB)	71	R7	FPDAT3
19	GND	GND	—	—	VSS
20	B0	BLUE data signal (LSB)	53	N4	FPDAT17
21	B1	BLUE data signal	54	P4	FPDAT16
22	B2	BLUE data signal	55	T2	FPDAT15
23	B3	BLUE data signal	64	R6	FPDAT8
24	B4	BLUE data signal	67	K6	FPDAT7
25	B5	BLUE data signal (MSB)	68	M6	FPDAT6
26	GND	GND	—	—	VSS
27	ENAB	Signal to settle the horizontal display position (positive)	80	M8	FPDRDY
28	VDD	3.3V power supply	—	—	HVDD2
29	VDD	3.3V power supply	—	—	HVDD2
30	R/L	Horizontal display mode select signal Low: Normal, High: Left/Right reverse mode	—	—	—
31	U/D	Vertical display mode select signal High: Normal, Low: Up/Down reverse mode	—	—	—
32	NC	not connected	—	—	—
33	GND	GND	—	—	VSS

11.2.2 Connecting the TCG075VG2AC-G00 to the S1D13748

The following diagram shows an example implementation of the TCG075VG2AC-G00 panel connected to the S1D13748.

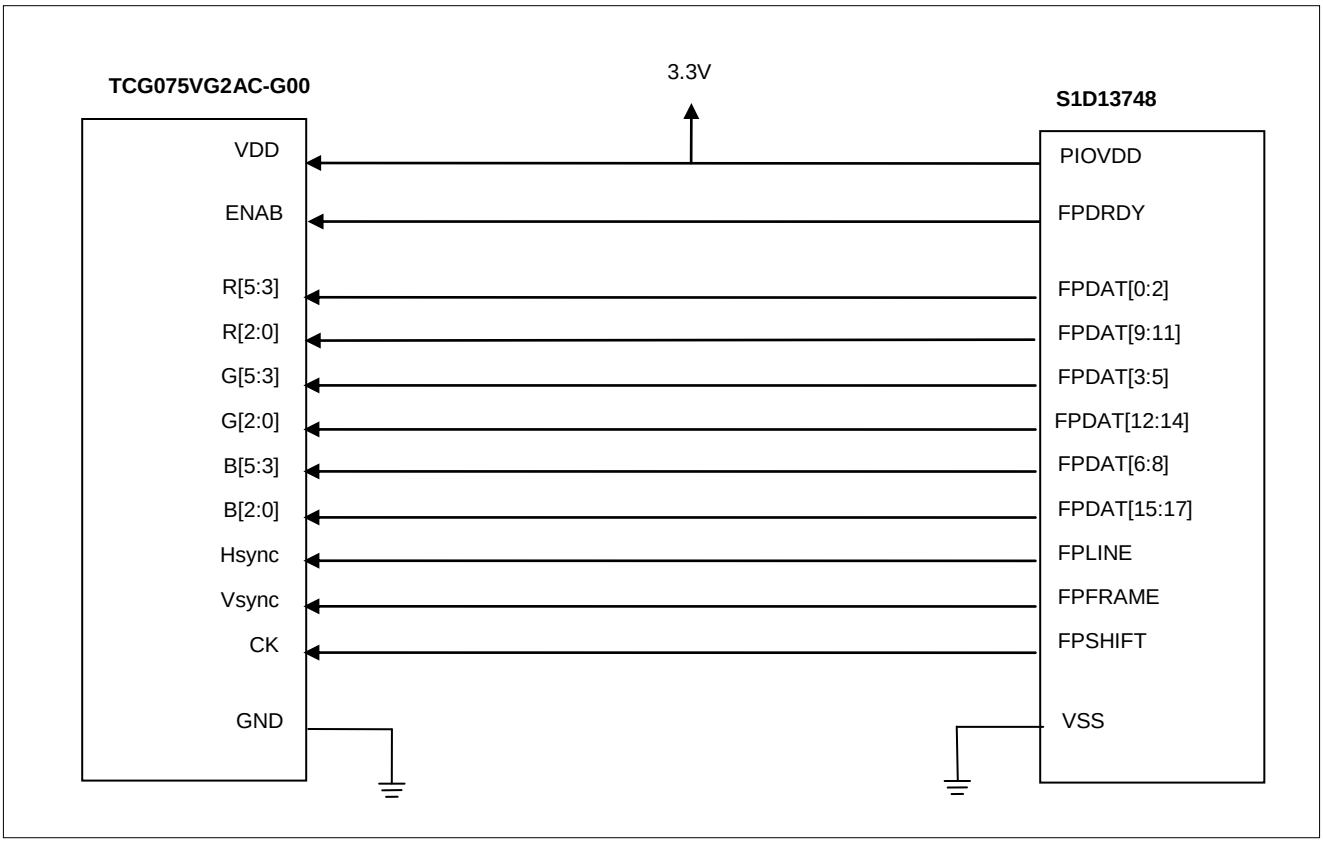

Figure 11-2 Connecting the TCG075VG2AC-G00 to the S1D13748

The following table provides a detailed pin listing for the required connections between the TCG075VG2AC-G00 and the S1D13748. Pin mappings are shown for both S1D13748 package types.

Table 11-3 Connecting the TCG075VG2AC-G00 to the S1D13748

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
1	GND	GND	—	—	VSS
2	CK	Clock signal for sampling each data signal	75	J11	FPSHIFT
3	Hsync	Horizontal synchronous signal (negative)	77	H10	FPLINE
4	Vsync	Vertical synchronous signal (negative)	76	J10	FPFRAME
5	GND	GND	—	—	VSS
6	R0	RED data signal (LSB)	63	L8	FPDAT11
7	R1	RED data signal	62	J8	FPDAT10
8	R2	RED data signal	61	K8	FPDAT9
9	R3	RED data signal	51	K5	FPDAT2
10	R4	RED data signal	50	L5	FPDAT1

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
11	R5	RED data signal (MSB)	49	J5	FPDAT0
12	GND	GND	—	—	VSS
13	G0	GREEN data signal (LSB)	69	H8	FPDAT14
14	G1	GREEN data signal	68	K9	FPDAT13
15	G2	GREEN data signal	64	L9	FPDAT12
16	G3	GREEN data signal	54	L6	FPDAT5
17	G4	GREEN data signal	53	J6	FPDAT4
18	G5	GREEN data signal (MSB)	52	H6	FPDAT3
19	GND	GND	—	—	VSS
20	B0	BLUE data signal (LSB)	72	J9	FPDAT17
21	B1	BLUE data signal	71	K10	FPDAT16
22	B2	BLUE data signal	70	L10	FPDAT15
23	B3	BLUE data signal	60	K7	FPDAT8
24	B4	BLUE data signal	59	J7	FPDAT7
25	B5	BLUE data signal (MSB)	58	L7	FPDAT6
26	GND	GND	—	—	VSS
27	ENAB	Signal to settle the horizontal display position (positive)	78	G7	FPDRDY
28	VDD	3.3V power supply	—	—	PIOVDD
29	VDD	3.3V power supply	—	—	PIOVDD
30	R/L	Horizontal display mode select signal Low: Normal, High: Left/Right reverse mode	—	—	—
31	U/D	Vertical display mode select signal High: Normal, Low: Up/Down reverse mode	—	—	—
32	NC	not connected	—	—	—
33	GND	GND	—	—	VSS

11.3 Example Register Settings

In addition to the pin connections, the S1D13513/S1D13748 internal registers must be configured appropriately for the TCG075VG2AC-G00 LCD panel. The following tables provide example settings for each display controller. However, these values are for reference only and may differ according to each specific implementation.

Also included in the table is an example clock configuration designed to achieve a typical LCD refresh.

Table 11-4 Example Register Settings for the S1D13513

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0800h] LCD Panel Type Select Register	0280h	—
REG[0802h] LCD Horizontal Total Register	799	800
REG[0804h] LCD Horizontal Display Period Register	319	640
REG[0806h] LCD Horizontal Display Period Start Position Register	61	61
REG[0808h] LCD Horizontal Pulse Width	16	17
REG[080Ah] LCD Horizontal Pulse Start Position	0	0
REG[080Ch] LCD Vertical Total Register	524	525
REG[080Eh] LCD Vertical Display Period Resister	479	480
REG[0810h] LCD Vertical Display Period Start Position Register	34	34
REG[0812h] LCD Vertical Pulse Width	2	3
REG[0814h] LCD Vertical Pulse Start Position	0	0
PLL2 output frequency in MHz	—	100
REG[0446h] LCD Clock Control Register	3	4
FPSHIFT in MHz	—	25
LCD Refresh in Hz	—	59.5

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13513 register values, see the S1D13513 Hardware Functional Specification, document number X78B-A-001-xx.

Table 11-5 Example Register Settings for the S1D13748

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0040h] LCD1 Horizontal Total Register	99	800
REG[0042h] LCD1 Horizontal Display Period Register	319	640
REG[0044h] LCD1 Horizontal Display Period Start Position Register	53	53
REG[0046h] LCD1 Horizontal Pulse Register	15	16
REG[0048h] LCD1 Horizontal Pulse Start Position Register	0	1
REG[004Ah] LCD1 Vertical Total Register	524	525
REG[004Ch] LCD1 Vertical Display Period Resister	479	480
REG[0050h] LCD1 Vertical Pulse Register	34	34
REG[0052h] LCD1 Vertical Pulse Start Position Register	0080h+1	2
REG[0246h] Main1 Window Image Horizontal Size Register	0	1
REG[0248h] Main1 Window Image Vertical Size Register	799	800
REG[004Eh] LCD1 Vertical Display Period Start Position Register	479	480
PLL output frequency in MHz	—	50
REG[0030h] LCD Interface Clock Setting Register	0500h	2
FPSHIFT in MHz	—	25
LCD Refresh in Hz	—	59.5

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13748 register values, see the *S1D13748 Hardware Functional Specification*, document number X80A-A-001-xx.

12 Connecting to the Kyocera TCG085WV1AB-G00

The Kyocera TCG085WV1AB-G00 LCD panel is compatible with the S1D13513, S1D13742, and S1D13748 display controllers. The following sections will provide connector details, pin mappings, and example register settings.

12.1 TCG085WV1AB-G00 Pin Mapping

The TCG085WV1AB-G00 LCD panel uses a 40-pin connector with the following pin mapping.

Table 12-1 TCG085WV1AB-G00 Pin Mapping

Connector Pin#	Pin Name	Pin Description
1	VDD	3.3V power supply
2	VDD	3.3V power supply
3	VDD	3.3V power supply
4	VDD	3.3V power supply
5	NC	not connected
6	DE	Signal to settle the horizontal display position (positive)
7	GND	GND
8	Vsync	Vertical synchronous signal (negative)
9	GND	GND
10	Hsync	Horizontal synchronous signal (negative)
11	GND	GND
12	B5	BLUE data signal (MSB)
13	B4	BLUE data signal
14	B3	BLUE data signal
15	GND	GND
16	B2	BLUE data signal
17	B1	BLUE data signal
18	B0	BLUE data signal (LSB)
19	GND	GND
20	G5	GREEN data signal (MSB)
21	G4	GREEN data signal
22	G3	GREEN data signal
23	GND	GND
24	G2	GREEN data signal
25	G1	GREEN data signal
26	G0	GREEN data signal (LSB)
27	GND	GND
28	R5	RED data signal (MSB)
29	R4	RED data signal
30	R3	RED data signal
31	GND	GND

Connector Pin#	Pin Name	Pin Description
32	R2	RED data signal
33	R1	RED data signal
34	R0	RED data signal (LSB)
35	NC	not connected
36	GND	GND
37	GND	GND
38	CLK	Clock signal for sampling each data signal
39	GND	GND
40	GND	GND

Note
The recommended mounting connector is a IMSA-9637S-40C-TB from Iroso Electronics Co., Ltd. The connector is a 0.5mm pitch 40-pin FPC connector (20.5mm x 0.3mm gold plate).

12.2 Connection Examples

The information in this section provides connection examples for the S1D13513, S1D13742, and S1D13748 display controllers. Some display controllers are available in two packages. The connection information differs for each package and is listed separately.

In addition to the pin connections for the selected display controller, the TCG085WV1AB-G00 requires the following power supply.

VDD +3.3V (±0.3V)

For further details on the TCG085WV1AB-G00, such as power consumption and absolute maximum ratings, please contact your Kyocera representative.

12.2.1 Connecting the TCG085WV1AB-G00 to the S1D13513

The following diagram shows an example implementation of the TCG085WV1AB-G00 panel connected to the S1D13513.

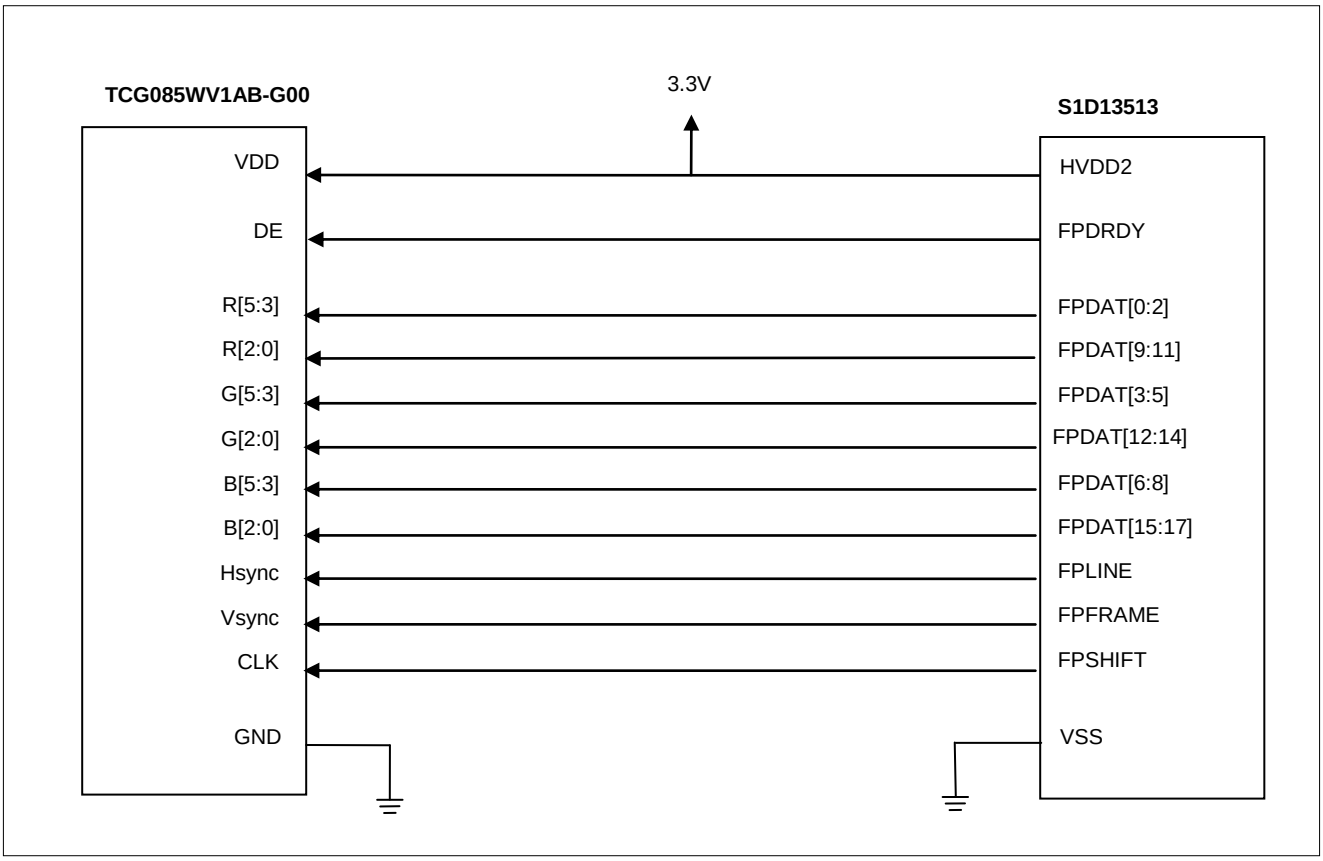

Figure 12-1 Connecting the TCG085WV1AB-G00 to the S1D13513

The following table provides a detailed pin listing for the required connections between the TCG085WV1AB-G00 and the S1D13513. Pin mappings are shown for both S1D13513 package types.

Table 12-2 Connecting the TCG085WV1AB-G00 to the S1D13513

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
1	VDD	3.3V power supply	—	—	HVDD2
2	VDD	3.3V power supply	—	—	HVDD2
3	VDD	3.3V power supply	—	—	HVDD2
4	VDD	3.3V power supply	—	—	HVDD2
5	NC	not connected	—	—	—
6	DE	Signal to settle the horizontal display position (positive)	80	M8	FPDRDY
7	GND	GND	—	—	VSS
8	Vsync	Vertical synchronous signal (negative)	78	T8	FPFRAME
9	GND	GND	—	—	VSS

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
10	Hsync	Horizontal synchronous signal (negative)	79	R8	FPLINE
11	GND	GND	—	—	VSS
12	B5	BLUE data signal (MSB)	68	M6	FPDAT6
13	B4	BLUE data signal	67	K6	FPDAT7
14	B3	BLUE data signal	64	R6	FPDAT8
15	GND	GND	—	—	VSS
16	B2	BLUE data signal	55	T2	FPDAT15
17	B1	BLUE data signal	54	P4	FPDAT16
18	B0	BLUE data signal (LSB)	53	N4	FPDAT17
19	GND	GND	—	—	VSS
20	G5	GREEN data signal (MSB)	71	R7	FPDAT3
21	G4	GREEN data signal	70	P7	FPDAT4
22	G3	GREEN data signal	69	L7	FPDAT5
23	GND	GND	—	—	VSS
24	G2	GREEN data signal	60	T5	FPDAT12
25	G1	GREEN data signal	59	T4	FPDAT13
26	G0	GREEN data signal (LSB)	56	R4	FPDAT14
27	GND	GND	—	—	VSS
28	R5	RED data signal (MSB)	74	M7	FPDAT0
29	R4	RED data signal	73	N7	FPDAT1
30	R3	RED data signal	72	T7	FPDAT2
31	GND	GND	—	—	VSS
32	R2	RED data signal	63	P6	FPDAT9
33	R1	RED data signal	62	M5	FPDAT10
34	R0	RED data signal (LSB)	61	N5	FPDAT11
35	NC	not connected	—	—	—
36	GND	GND	—	—	VSS
37	GND	GND	—	—	VSS
38	CLK	Clock signal for sampling each data signal	77	P8	FPSHIFT
39	GND	GND	—	—	VSS
40	GND	GND	—	—	VSS

12.2.2 Connecting the TCG085WV1AB-G00 to the S1D13742

The following diagram shows an example implementation of the TCG085WV1AB-G00 panel connected to the S1D13742.

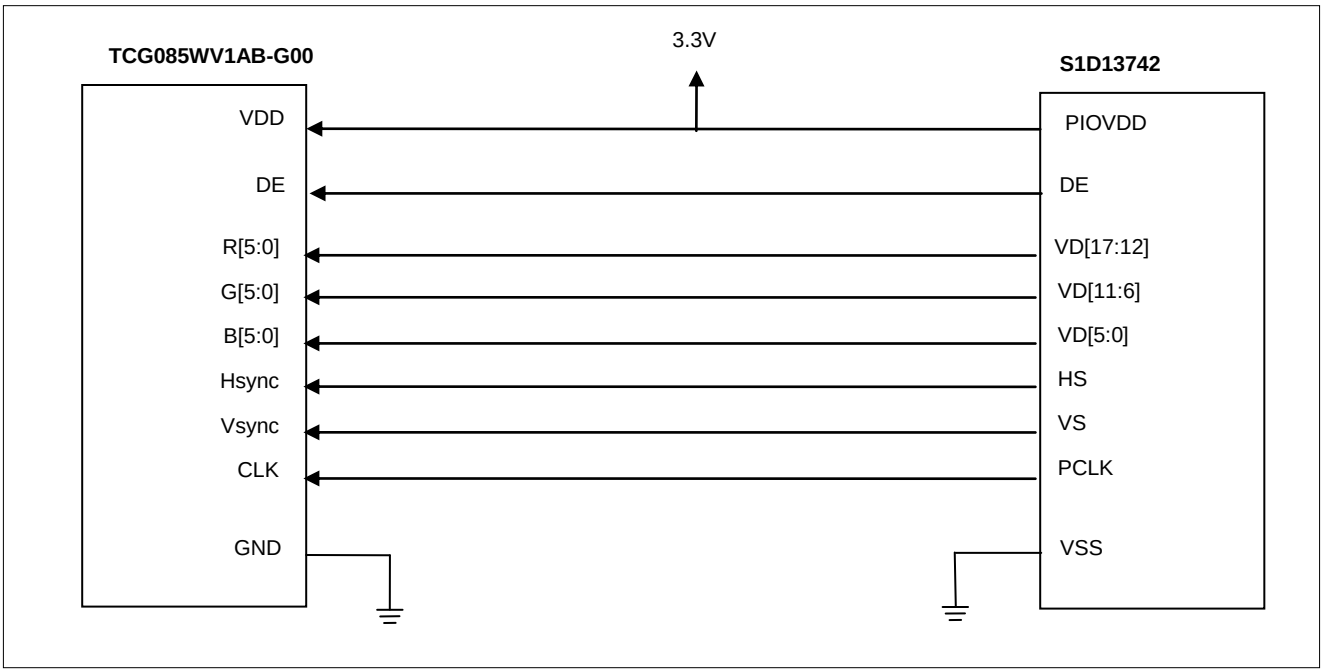

Figure 12-2 Connecting the TCG085WV1AB-G00 to the S1D13742

The following table provides a detailed pin listing for the required connections between the TCG085WV1AB-G00 and the S1D13742. Pin mappings are shown for both S1D13742 package types.

Table 12-3 Connecting the TCG085WV1AB-G00 to the S1D13742

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13742 QFP Pin#	S1D13742 FCBGA Ball#	S1D13742 Pin Name
1	VDD	3.3V power supply	—	—	PIOVDD
2	VDD	3.3V power supply	—	—	PIOVDD
3	VDD	3.3V power supply	—	—	PIOVDD
4	VDD	3.3V power supply	—	—	PIOVDD
5	NC	not connected	—	—	—
6	DE	Signal to settle the horizontal display position (positive)	8	C11	DE
7	GND	GND	—	—	VSS
8	Vsync	Vertical synchronous signal (negative)	10	D10	VS
9	GND	GND	—	—	VSS
10	Hsync	Horizontal synchronous signal (negative)	9	D9	HS
11	GND	GND	—	—	VSS
12	B5	BLUE data signal (MSB)	65	L4	VD5
13	B4	BLUE data signal	62	L5	VD4
14	B3	BLUE data signal	59	L6	VD3

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13742 QFP Pin#	S1D13742 FCBGA Ball#	S1D13742 Pin Name
15	GND	GND	—	—	VSS
16	B2	BLUE data signal	54	L7	VD2
17	B1	BLUE data signal	49	L8	VD1
18	B0	BLUE data signal (LSB)	45	L9	VD0
19	GND	GND	—	—	VSS
20	G5	GREEN data signal (MSB)	58	K6	VD11
21	G4	GREEN data signal	51	K7	VD10
22	G3	GREEN data signal	48	K8	VD9
23	GND	GND	—	—	VSS
24	G2	GREEN data signal	44	K9	VD8
25	G1	GREEN data signal	42	K10	VD7
26	G0	GREEN data signal (LSB)	66	L3	VD6
27	GND	GND	—	—	VSS
28	R5	RED data signal (MSB)	47	J8	VD17
29	R4	RED data signal	43	J9	VD16
30	R3	RED data signal	29	J10	VD15
31	GND	GND	—	—	VSS
32	R2	RED data signal	30	J11	VD14
33	R1	RED data signal	64	K4	VD13
34	R0	RED data signal (LSB)	61	K5	VD12
35	NC	not connected	—	—	—
36	GND	GND	—	—	VSS
37	GND	GND	—	—	VSS
38	CLK	Clock signal for sampling each data signal	11	D11	PCLK
39	GND	GND	—	—	VSS
40	GND	GND	—	—	VSS

12.2.3 Connecting the TCG085WV1AB-G00 to the S1D13748

The following diagram shows an example implementation of the TCG085WV1AB-G00 panel connected to the S1D13748.

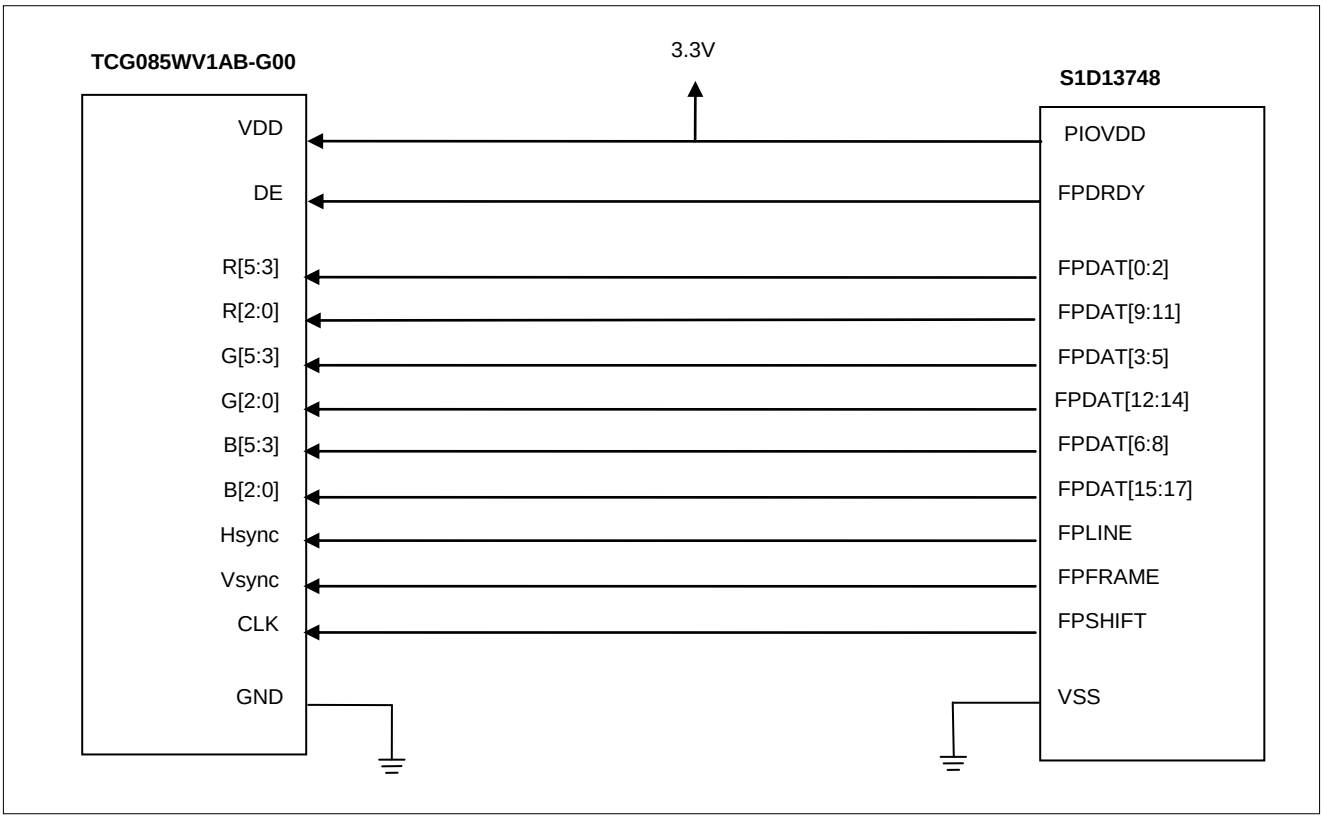

Figure 12-3 Connecting the TCG085WV1AB-G00 to the S1D13748

The following table provides a detailed pin listing for the required connections between the TCG085WV1AB-G00 and the S1D13748. Pin mappings are shown for both S1D13748 package types.

Table 12-4 Connecting the TCG085WV1AB-G00 to the S1D13748

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
1	VDD	3.3V power supply	—	—	PIOVDD
2	VDD	3.3V power supply	—	—	PIOVDD
3	VDD	3.3V power supply	—	—	PIOVDD
4	VDD	3.3V power supply	—	—	PIOVDD
5	NC	not connected	—	—	—
6	DE	Signal to settle the horizontal display position (positive)	78	G7	FPDRDY
7	GND	GND	—	—	VSS
8	Vsync	Vertical synchronous signal (negative)	76	J10	FPFRAME
9	GND	GND	—	—	VSS
10	Hsync	Horizontal synchronous signal (negative)	77	H10	FPLINE

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13748 QFP Pin#	S1D13748 PFBGA Ball#	S1D13748 Pin Name
11	GND	GND	—	—	VSS
12	B5	BLUE data signal (MSB)	58	L7	FPDAT6
13	B4	BLUE data signal	59	J7	FPDAT7
14	B3	BLUE data signal	60	K7	FPDAT8
15	GND	GND	—	—	VSS
16	B2	BLUE data signal	70	L10	FPDAT15
17	B1	BLUE data signal	71	K10	FPDAT16
18	B0	BLUE data signal (LSB)	72	J9	FPDAT17
19	GND	GND	—	—	VSS
20	G5	GREEN data signal (MSB)	52	H6	FPDAT3
21	G4	GREEN data signal	53	J6	FPDAT4
22	G3	GREEN data signal	70	L10	FPDAT5
23	GND	GND	—	—	VSS
24	G2	GREEN data signal	64	L9	FPDAT12
25	G1	GREEN data signal	68	K9	FPDAT13
26	G0	GREEN data signal (LSB)	69	H8	FPDAT14
27	GND	GND	—	—	VSS
28	R5	RED data signal (MSB)	49	J5	FPDAT0
29	R4	RED data signal	50	L5	FPDAT1
30	R3	RED data signal	51	K5	FPDAT2
31	GND	GND	—	—	VSS
32	R2	RED data signal	61	K8	FPDAT9
33	R1	RED data signal	62	J8	FPDAT10
34	R0	RED data signal (LSB)	63	L8	FPDAT11
35	NC	not connected	—	—	—
36	GND	GND	—	—	VSS
37	GND	GND	—	—	VSS
38	CLK	Clock signal for sampling each data signal	75	J11	FPSHIFT
39	GND	GND	—	—	VSS
40	GND	GND	—	—	VSS

12.3 Example Register Settings

In addition to the pin connections, the S1D13513/S1D13742/S1D13748 internal registers must be configured appropriately for the TCG085WV1AB-G00 LCD panel. The following tables provide example settings for each display controller. However, these values are for reference only and may differ according to each specific implementation.

Also included in the table is an example clock configuration designed to achieve a typical LCD refresh.

Table 12-5 Example Register Settings for the S1D13513

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0800h] LCD Panel Type Select Register	0280h	—
REG[0802h] LCD Horizontal Total Register	1055	1056
REG[0804h] LCD Horizontal Display Period Register	399	800
REG[0806h] LCD Horizontal Display Period Start Position Register	29	29
REG[0808h] LCD Horizontal Pulse Width	16	17
REG[080Ah] LCD Horizontal Pulse Start Position	0	0
REG[080Ch] LCD Vertical Total Register	524	525
REG[080Eh] LCD Vertical Display Period Resister	479	480
REG[0810h] LCD Vertical Display Period Start Position Register	34	34
REG[0812h] LCD Vertical Pulse Width	2	3
REG[0814h] LCD Vertical Pulse Start Position	0	0
PLL2 output frequency in MHz	—	130
REG[0446h] LCD Clock Control Register	3	4
FPSHIFT in MHz	—	32.5
LCD Refresh in Hz	—	58.6

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13513 register values, see the *S1D13513 Hardware Functional Specification*, document number X78B-A-001-xx.

Table 12-6 Example Register Settings for the S1D13742

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[14h] Panel Type Register	00h	—
REG[16h] Horizontal Display Width Register	100	800
REG[18h] Horizontal Non-Display Period Register	30	30
REG[1Ah]~[1Ch] Vertical Display Height Registers	480	480
REG[1Eh] Vertical Non-Display Period Register	45	45
REG[20h] HS Pulse Width Register	16	16
REG[22h] HS Pulse Start Position Register 0	16	16
REG[24h] VS Pulse Width Register	2	2
REG[26h] VS Pulse Start Position Register 0	34	34
PLL output frequency in MHz	—	66
REG[12h] Pixel Clock Configuration Register	09h	2
FPSHIFT in MHz	—	33
LCD Refresh in Hz	—	75.7

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13742 register values, see the *S1D13742 Hardware Functional Specification*, document number X63A-A-001-xx.

Table 12-7 Example Register Settings for the S1D13748

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0040h] LCD1 Horizontal Total Register	127	1024
REG[0042h] LCD1 Horizontal Display Period Register	399	800
REG[0044h] LCD1 Horizontal Display Period Start Position Register	20	20
REG[0046h] LCD1 Horizontal Pulse Register	15	16
REG[0048h] LCD1 Horizontal Pulse Start Position Register	0	1
REG[004Ah] LCD1 Vertical Total Register	524	525
REG[004Ch] LCD1 Vertical Display Period Resister	479	480
REG[0050h] LCD1 Vertical Pulse Register	34	34
REG[0052h] LCD1 Vertical Pulse Start Position Register	0	1
REG[0246h] Main1 Window Image Horizontal Size Register	0	1
REG[0248h] Main1 Window Image Vertical Size Register	799	800
REG[004Eh] LCD1 Vertical Display Period Start Position Register	479	480
PLL output frequency in MHz	—	50
REG[0030h] LCD Interface Clock Setting Register	0500h	2
FPSHIFT in MHz	—	25
LCD Refresh in Hz	—	46.5

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13748 register values, see the *S1D13748 Hardware Functional Specification*, document number X80A-A-001-xx.

13 Connecting to the Kyocera TCG104VG2AA-G00

The Kyocera TCG104VG2AA-G00 LCD panel is compatible with the S1D13513 display controller. The following sections will provide connector details, pin mappings, and example register settings.

13.1 TCG104VG2AA-G00 Pin Mapping

The TCG104VG2AA-G00 LCD panel uses a 31-pin connector with the following pin mapping.

TCG104VG2AA-G00 Pin Mapping

Connector Pin#	Pin Name	Pin Description
1	GND	GND
2	CK	Clock signal for sampling each data signal
3	Hsync	Horizontal synchronous signal (negative)
4	Vsync	Vertical synchronous signal (negative)
5	GND	GND
6	R0	RED data signal (LSB)
7	R1	RED data signal
8	R2	RED data signal
9	R3	RED data signal
10	R4	RED data signal
11	R5	RED data signal (MSB)
12	GND	GND
13	G0	GREEN data signal (LSB)
14	G1	GREEN data signal
15	G2	GREEN data signal
16	G3	GREEN data signal
17	G4	GREEN data signal
18	G5	GREEN data signal (MSB)
19	GND	GND
20	B0	BLUE data signal (LSB)
21	B1	BLUE data signal
22	B2	BLUE data signal
23	B3	BLUE data signal
24	B4	BLUE data signal
25	B5	BLUE data signal (MSB)
26	GND	GND
27	DE	Signal to settle the horizontal display position (positive)
28	VDD	+3.3V/+5.0V power supply
29	VDD	+3.3V/+5.0V power supply
30	NC	not connected
31	SC	Scan direction mode select signal GND or OPEN: Normal, High: Reverse

Note
The recommended connectors are:
LCD panel connector is DF9-31S-1V from Hirose Electric Co., Ltd.
Cable side connector is DF9-31S-1V and DF9A-31S-1V(32) from Hirose Electric Co., Ltd.

13.2 Connection Examples

The information in this section provides a connection example for the S1D13513 display controller. The S1D13513 display controller is available in two packages. The connection information differs for each package and is listed separately.

In addition to the pin connections for the selected display controller, the TCG104VG2AA-G00 requires the following power supply.

VDD +3.3V or +5.0V (+3.0V ≤ VDD ≤ +5.25V)

For further details on the TCG104VG2AA-G00, such as power consumption and absolute maximum ratings, please contact your Kyocera representative.

13.2.1 Connecting the TCG104VG2AA-G00 to the S1D13513

The following diagram shows an example implementation of the TCG104VG2AA-G00 panel connected to the S1D13513.

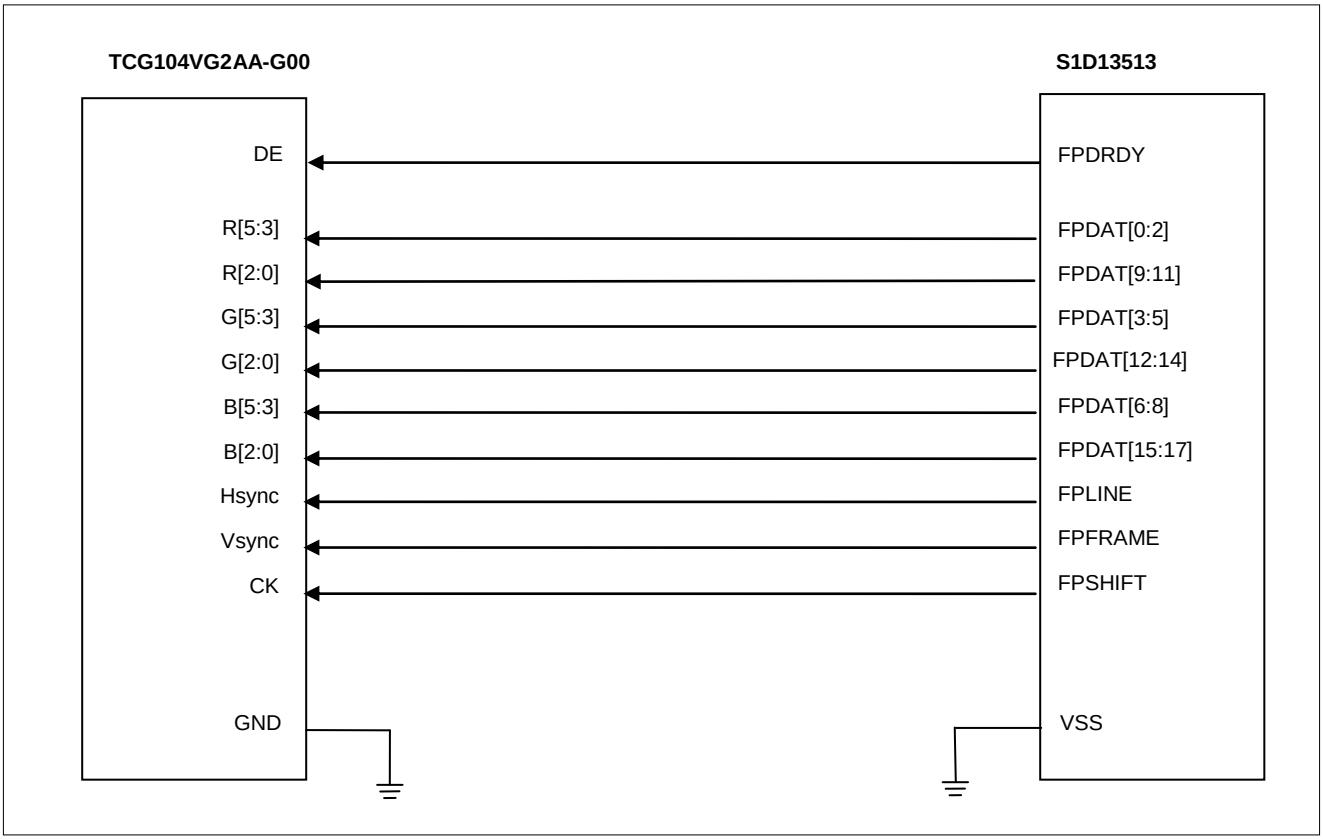

Figure 13-1 Connecting the TCG104VG2AA-G00 to the S1D13513

The following table provides a detailed pin listing for the required connections between the TCG104VG2AA-G00 and the S1D13513. Pin mappings are shown for both S1D13513 package types.

Table 13-1 Connecting the TCG104VG2AA-G00 to the S1D13513

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
1	GND	GND	—	—	VSS
2	CK	Clock signal for sampling each data signal	77	P8	FPSHIFT
3	Hsync	Horizontal synchronous signal (negative)	79	R8	FPLINE
4	Vsync	Vertical synchronous signal (negative)	78	T8	FPFRAME
5	GND	GND	—	—	VSS
6	R0	RED data signal (LSB)	61	N5	FPDAT11
7	R1	RED data signal	62	M5	FPDAT10
8	R2	RED data signal	63	P6	FPDAT9
9	R3	RED data signal	72	T7	FPDAT2
10	R4	RED data signal	73	N7	FPDAT1
11	R5	RED data signal (MSB)	74	M7	FPDAT0
12	GND	GND	—	—	VSS
13	G0	GREEN data signal (LSB)	56	R4	FPDAT14
14	G1	GREEN data signal	59	T4	FPDAT13
15	G2	GREEN data signal	60	T5	FPDAT12
16	G3	GREEN data signal	69	L7	FPDAT5
17	G4	GREEN data signal	70	P7	FPDAT4
18	G5	GREEN data signal (MSB)	71	R7	FPDAT3
19	GND	GND	—	—	VSS
20	B0	BLUE data signal (LSB)	53	N4	FPDAT17
21	B1	BLUE data signal	54	P4	FPDAT16
22	B2	BLUE data signal	55	T2	FPDAT15
23	B3	BLUE data signal	64	R6	FPDAT8
24	B4	BLUE data signal	67	K6	FPDAT7
25	B5	BLUE data signal (MSB)	68	M6	FPDAT6
26	GND	GND	—	—	VSS
27	DE	Signal to settle the horizontal display position (positive)	80	M8	FPDRDY
28	VDD	+3.3V/+5.0V power supply	—	—	—
29	VDD	+3.3V/+5.0V power supply	—	—	—
30	NC	not connected	—	—	—
31	SC	Scan direction mode select signal GND or OPEN: normal, High: Reverse	—	—	—

13.3 Example Register Settings

In addition to the pin connections, the S1D13513 internal registers must be configured appropriately for the TCG104VG2AA-G00 LCD panel. The following table provides example settings. However, these values are for reference only and may differ according to each specific implementation.

Also included in the table is an example clock configuration designed to achieve a typical LCD refresh.

Table 13-2 Example Register Settings for the S1D13513

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0800h] LCD Panel Type Select Register	0280h	—
REG[0802h] LCD Horizontal Total Register	799	800
REG[0804h] LCD Horizontal Display Period Register	319	640
REG[0806h] LCD Horizontal Display Period Start Position Register	61	61
REG[0808h] LCD Horizontal Pulse Width	16	17
REG[080Ah] LCD Horizontal Pulse Start Position	0	0
REG[080Ch] LCD Vertical Total Register	524	525
REG[080Eh] LCD Vertical Display Period Resister	479	480
REG[0810h] LCD Vertical Display Period Start Position Register	34	34
REG[0812h] LCD Vertical Pulse Width	2	3
REG[0814h] LCD Vertical Pulse Start Position	0	0
PLL2 output frequency in MHz	—	100
REG[0446h] LCD Clock Control Register	3	4
FPSHIFT in MHz	—	25
LCD Refresh in Hz	—	59.5

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13513 register values, see the *S1D13513 Hardware Functional Specification*, document number X78B-A-001-xx.

14 Change Record

X00A-G-007-01 Revision 1.0 - Issued: April 18, 2012

- Re-format and edit document for release

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Document Code: X94A-G-007-01
First Issue April 2012
Revised April 2012 in JAPAN