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Connecting EPSON Display Controllers to Chimei LCD Panels

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SEIKO EPSON CORPORATION

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NOTICE

Table of Contents

1 Introduction

This document provides connection information enabling EPSON Display Controllers to control a variety of Chimei Innolux Co., Ltd LCD panels. This document includes connector details, pin mappings, and example register settings.

For detailed technical information on EPSON Display Controllers or CHIMEI LCD panels, please refer to the specification or technical manual for each product.

This document is updated as appropriate. Please check for the latest revision of this document before beginning any development. The latest revision can be downloaded at
http://www.epson.jp/device/semicon_e/product/index.htm#lcd_controllers

2 Display Controller Compatibility

This document discusses the following CHIMEI TFT panels.

- AT070TN94（TFT 7.0inch, WVGA）

Each CHIMEI TFT panel is compatible with one or more of the following EPSON display controllers.

- S1D13513 (QFP 208-pin or PBGA 256-pin)
- S1D13517 (QFP 128-pin)

3 Connecting to the Chimei AT070TN94

The CHIMEI AT070TN94 TFT panel is compatible with the S1D13513 and S1D13517 display controllers. The following sections will provide connector details, pin mappings, and example register settings for these combinations.

3.1 AT070TN94 Pin Mapping

The AT070TN94 TFT panel uses a connector with the following pin mapping.

Table 3-1 AT070TN94 Pin Mapping

Connector Pin#	Pin Name	Pin Description
1	VLED+	Power for LED backlight (Anode)
2	VLED+	Power for LED backlight (Anode)
3	VLED-	Power for LED backlight (Cathode)
4	VLED-	Power for LED backlight (Cathode)
5	GND	Power ground
6	Vcom	Common voltage
7	DVDD	Power for Digital Circuit
8	MODE	DE/SYNC mode select
9	DE	Data Input Enable
10	VS	Vertical Sync Input
11	HS	Horizontal Sync Input
12	B7	Blue data (MSB)
13	B6	Blue data
14	B5	Blue data
15	B4	Blue data
16	B3	Blue data
17	B2	Blue data
18	B1	Blue data
19	B0	Blue data (LSB)
20	G7	Green data (MSB)
21	G6	Green data
22	G5	Green data
23	G4	Green data
24	G3	Green data
25	G2	Green data
26	G1	Green data
27	G0	Green data (LSB)
28	R7	Red data (MSB)
29	R6	Red data
30	R5	Red data
31	R4	Red data

32	R3	Red data
33	R2	Red data
34	R1	Red data
35	R0	Red data (LSB)
36	GND	Power Ground
37	DCLK	Sample clock
38	GND	Power Ground
39	L/R	Left/right selection
40	U/D	Up/down selection
41	VGH	Gate ON Voltage
42	VGL	Gate OFF Voltage
43	AVDD	Power for Analog Circuit
44	RESET	Global reset pin
45	NC	No connection
46	Vcom	Common Voltage
47	DITHB	Dithering function
48	GND	Power Ground
49	NC	No connection
50	NC	No connection

3.2 Connection Examples

The information in this section provides connection example for the S1D13513 and S1D13517 display controllers.

3.2.1 Connecting the AT070TN94 to the S1D13513

The following diagram shows an example implementation of the AT070TN94 panel connected to the S1D13513.

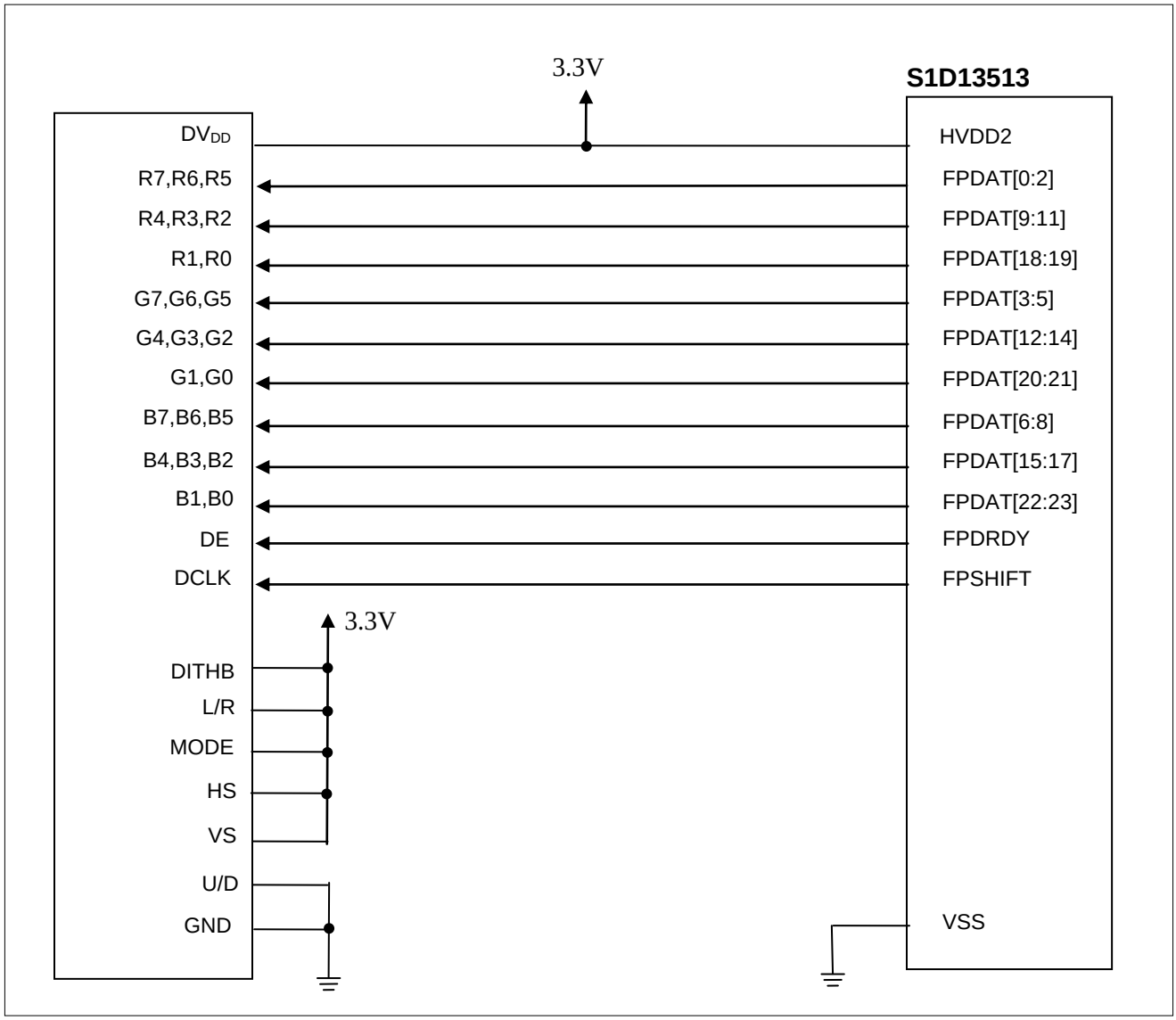

Figure 3-1 Connecting the AT070TN94 to the S1D13513

The following table provides a detailed pin listing for the required connections between the AT070TN94 and the S1D13513. Pin mappings are shown for both S1D13513 package types.

Table 3-2 Connecting the AT070TN94 to the S1D13513

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
1	VLED+	Power for LED backlight (Anode)	—	—	—
2	VLED+	Power for LED backlight (Anode)	—	—	—
3	VLED-	Power for LED backlight (Cathode)	—	—	—
4	VLED-	Power for LED backlight (Cathode)	—	—	—
5	GND	Power ground	Note 1	Note 1	VSS
6	Vcom	Common voltage	-	-	-
7	DVDD	Power for Digital Circuit	57,65,75	L5,L8,T6	HVDD2
8	MODE	DE/SYNC mode select	57,65,75	L5,L8,T6	HVDD2
9	DE	Data Input Enable	80	M8	FPDRDY
10	VS	Vertical Sync Input	57,65,75	L5,L8,T6	HVDD2
11	HS	Horizontal Sync Input	57,65,75	L5,L8,T6	HVDD2
12	B7	Blue data (MSB)	68	M6	FPDAT6
13	B6	Blue data	67	K6	FPDAT7
14	B5	Blue data	64	R6	FPDAT8
15	B4	Blue data	55	T2	FPDAT15
16	B3	Blue data	54	P4	FPDAT16
17	B2	Blue data	53	N4	FPDAT17
18	B1	Blue data	Note 2	R3	FPDAT22
19	B0	Blue data (LSB)	Note 2	K4	FPDAT23
20	G7	Green data (MSB)	71	R7	FPDAT3
21	G6	Green data	70	P7	FPDAT4
22	G5	Green data	69	L7	FPDAT5
23	G4	Green data	60	T5	FPDAT12
24	G3	Green data	59	T4	FPDAT13
25	G2	Green data	56	R4	FPDAT14
26	G1	Green data	Note 2	P5	FPDAT20
27	G0	Green data (LSB)	Note 2	T3	FPDAT21
28	R7	Red data (MSB)	74	M7	FPDAT0
29	R6	Red data	73	N7	FPDAT1
30	R5	Red data	72	T7	FPDAT2
31	R4	Red data	63	P6	FPDAT9
32	R3	Red data	62	M5	FPDAT10
33	R2	Red data	61	N5	FPDAT11
34	R1	Red data	Note 2	R5	FPDAT18

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13513 QFP Pin#	S1D13513 PBGA Ball#	S1D13513 Pin Name
35	R0	Red data (LSB)	Note 2	K5	FPDAT19
36	GND	Power Ground	Note 1	Note 1	VSS
37	DCLK	Sample clock	77	P8	FPSHIFT
38	GND	Power Ground	Note 1	Note 1	VSS
39	L/R	Left/right selection	57,65,75	L5,L8,T6	HVDD2
40	U/D	Up/down selection	Note 1	Note 1	VSS
41	VGH	Gate ON Voltage	—	—	—
42	VGL	Gate OFF Voltage	—	—	—
43	AVDD	Power for Analog Circuit	—	—	—
44	RESET	Global reset pin	57,65,75	L5,L8,T6	HVDD2
45	NC	No connection	—	—	—
46	Vcom	Common Voltage	—	—	—
47	DITHB	Dithering function	57,65,75	L5,L8,T6	HVDD2
48	GND	Power Ground	Note 1	Note 1	VSS
49	NC	No connection	—	—	—
50	NC	No connection	—	—	—

Note 1
Allocation of VSS pin for each package is as follows.
QFP: 10, 20, 38, 58, 66, 76, 92, 99, 106, 120, 133, 139, 151, 163, 169, 175, 184, 197
BGA: A1, A16, D4, D8, D13, G7-G10, G13, H7-H10, J1, J7-J10, K2, K7-K10, K13, N3, N6, N9, N13, T1, T16

Note 2
For QFP package, connect to S1D13513 VSS pin.

3.2.2 Connecting the AT070TN94 to the S1D13517

The following diagram shows an example implementation of the AT070TN94 panel connected to the S1D13517.

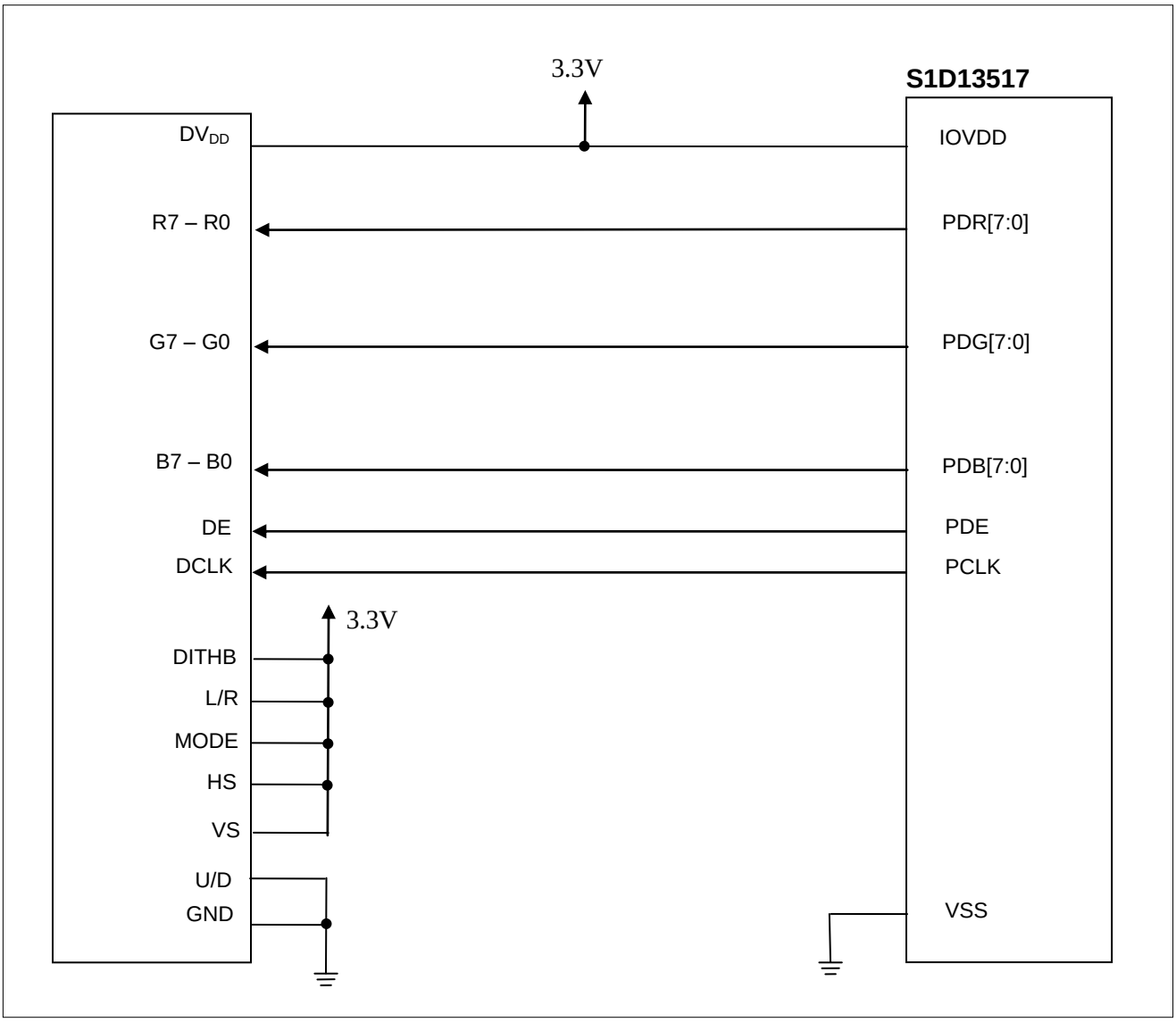

Figure 3-2 Connecting the AT070TN94 to the S1D13517

The following table provides a detailed pin listing for the required connections between the AT070TN94 and the S1D13517.

Table 3-3 Connecting the COM37H3M04 to the S1D13517

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13517 QFP Pin#	S1D13517 Pin Name
1	VLED+	Power for LED backlight (Anode)	—	—
2	VLED+	Power for LED backlight (Anode)	—	—
3	VLED-	Power for LED backlight (Cathode)	—	—
4	VLED-	Power for LED backlight (Cathode)	—	—
5	GND	Power ground	Note 1	VSS
6	Vcom	Common voltage	—	—
7	DVDD	Power for Digital Circuit	Note 2	IOVDD
8	MODE	DE/SYNC mode select	Note 2	IOVDD
9	DE	Data Input Enable	81	PDE
10	VS	Vertical Sync Input	Note 2	IOVDD
11	HS	Horizontal Sync Input	Note 2	IOVDD
12	B7	Blue data (MSB)	84	PDB7
13	B6	Blue data	85	PDB6
14	B5	Blue data	86	PDB5
15	B4	Blue data	87	PDB4
16	B3	Blue data	88	PDB3
17	B2	Blue data	89	PDB2
18	B1	Blue data	90	PDB1
19	B0	Blue data (LSB)	91	PDB0
20	G7	Green data (MSB)	92	PDG7
21	G6	Green data	93	PDG6
22	G5	Green data	94	PDG5
23	G4	Green data	95	PDG4
24	G3	Green data	98	PDG3
25	G2	Green data	99	PDG2
26	G1	Green data	100	PDG1
27	G0	Green data (LSB)	101	PDG0
28	R7	Red data (MSB)	102	PDR7
29	R6	Red data	103	PDR6
30	R5	Red data	104	PDR5
31	R4	Red data	105	PDR4
32	R3	Red data	106	PDR3
33	R2	Red data	107	PDR2
34	R1	Red data	108	PDR1
35	R0	Red data (LSB)	109	PDR0
36	GND	Power Ground	Note 1	VSS
37	DCLK	Sample clock	110	PCLK

38	GND	Power Ground	Note 1	VSS
39	L/R	Left/right selection	Note 2	IOVDD
40	U/D	Up/down selection	Note 1	VSS
41	VGH	Gate ON Voltage	—	—
42	VGL	Gate OFF Voltage	—	—
43	AVDD	Power for Analog Circuit	—	—
44	RESET	Global reset pin	Note 2	IOVDD
45	NC	No connection	—	—
46	Vcom	Common Voltage	—	—
47	DITHB	Dithering function	Note 2	IOVDD
48	GND	Power Ground	Note 1	VSS
49	NC	No connection	—	—
50	NC	No connection	—	—

Note 1
Allocation of VSS pin for each packages are as follows.
QFP: 1, 17, 24, 32, 48, 54, 65, 80, 97, 114

Note 2
Allocation of IOVDD pin for each packages are as follows.
QFP: 16, 31, 47, 64, 79, 96, 113, 128

3.3 Example Register Settings

In addition to the pin connections, the S1D13513 and S1D13517 internal registers must be configured appropriately for the AT070TN94 LCD panel. The following tables provide example settings for each display controller. However, these values are for reference only and may differ according to each specific implementation. For details on configuring the S1D13513 register values, see the S1D13513 Hardware Functional Specification, document number X78B-A-001-xx. For details on configuring the S1D13517 register values, see the S1D13517 Hardware Functional Specification, document number X92A-A-001-xx.

Table 3-4 Example Register Settings for the S1D13513

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[0800h] LCD Panel Type Select Register	0380h	24bpp mode, FPSHIFT polarity is rising edge
REG[0802h] LCD Horizontal Total Register	041Fh	1056
REG[0804h] LCD Horizontal Display Period Register	018Fh	800
REG[0806h] LCD Horizontal Display Period Start Position Register	002Dh	46
REG[0808h] LCD Horizontal Pulse Width	0013h	20
REG[080Ah] LCD Horizontal Pulse Start Position	0000h	0
REG[080Ch] LCD Vertical Total Register	020Ch	525
REG[080Eh] LCD Vertical Display Period Resister	01DFh	480
REG[0810h] LCD Vertical Display Period Start Position Register	0017h	23
REG[0812h] LCD Vertical Pulse Width	0009h	10
REG[0814h] LCD Vertical Pulse Start Position	0000h	0
REG[0C1Eh] GPIOH Pin Function Register	0555h	Set GPIO pins for 24bpp mode configuration
PLL2 output frequency in MHz	—	130
REG[0446h] LCD Clock Control Register	0003h	4
FPSHIFT in MHz	—	32.5
LCD Refresh in Hz	—	58.62

Note
Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13513 register values, see the S1D13513 Hardware Functional Specification, document number X78B-A-001-xx.

Table 3-5 Example Register Settings for the S1D13517

Register Index and Name	Register Setting	Parameter Value (see Note)
REG[14h] LCD Panel Type Register	00h	24bpp mode1 (packed), 24bit
REG[16h] Horizontal Display Width Register (HDISP)	63h	800
REG[18h] Horizontal Non-Display Period Register (HNDP)	57h	176
REG[1Ah] Vertical Display Height Register 0 (VDISP)	DFh	480
REG[1Ch] Vertical Display Height Register 1 (VDISP)	01h	—
REG[1Eh] Vertical Non-Display Period Register (VNDP)	0Fh	32
REG[20h] PHS Pulse Width Register (HSW)	13h	20
REG[22h] PHS Pulse Start Position Register (HPS)	82h	130
REG[24h] PVS Pulse Width Register (VSW)	09h	10
REG[26h] PVS Pulse Start Position Register (VPS)	09h	9
REG[28h] PCLK Polarity Register	00h	PCLK polarity is rising edge
REG[04h] PLL D-Divider Register	97h	PLL D-div is 1:24. Input 24MHz -> Output 1MHz
REG[06h] PLL Setting Register 0	51h	PLL output =180MHz
REG[08h] PLL Setting Register 1	01h	PLL clock Divide ratio = 1/2. (180MHz/2)
REG[0Ch] PLL N-Divider Register	59	PLL N-counter 90MHz
REG[0Eh] SS Control Register 0	3Fh	SS disabled
REG[12h] Clock Source Select Register	80h	SYSCLK = 1/3 (90MHz/3 = 30MHz)
REG[8Ch] SDRAM Refresh Counter Register 0	D1h	Refresh counter 1/30MHz x 465 =15.5us
REG[8Eh] SDRAM Refresh Counter Register 1	01h	—
FPSHIFT in MHz	—	30
LCD Refresh in Hz	—	60.03

Note

Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13517 register values, see the S1D13517 Hardware Functional Specification, document number X92A-G-001-xx.

4 Change Record

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- Re-format and edit document for release

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