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S2R72A21
Application Note

SEIKO EPSON CORPORATION

Rev.1.00

NOTICE

Table of Contents

1. Description

This document is the application note of the USB2.0 Re-Synchronization IC: S2R72A21.

This document explains the USB connection description, system implementation, compliance test for products which equip S2R72A21 as well as the remark point during PCB designing using this Re-Synchronization IC. Please refer to the S2R72A21 data sheet for Hardware related information.

2. Terms & Abbreviations

The followings are the terms and abbreviations used within this application note.

Table 2.1 terms & abbreviation

Terms & abbreviation	Definition
Attach	Operation when the cable is inserted or the moment when it is inserted
ADJ pin	The pin of S2R72A21 which setup the HS transmit current
BC	Battery Charge
BC Regulator	Regulator which correspond to BC specification
Bus Reset	Bus reset which invoke HS detection handshake
Bus Switch	Bus switch which connect between the port (analog switch)
Chip Reset	Provide the reset signal to XRESET pin (S2R72A21)
Compliance Test	USB product test to license the USB logo. USB-IF adds the product which passed the test to the Integrators List, and grants license.
Connect	Condition which Device Rpu is ON
Detach	Operation when the cable is pulled out or the moment when it is pulled out
Device	Device which is defined within the USB specification
Disconnect	Condition where the USB connection via the S2R72A21 is shut down electrically.
EOP	End-of-Packet
EXT port	External port of S2R72A21
FS	Full-Speed
FS_J	Bus state “J” during FS (Differential"1")
FS_K	Bus state “K” during FS (Differential"0")
Host	Host which is defined within the USB specification The host issues the SOF.
Host SoC	The SoC which is a Host during initial conditions
HS	High-Speed
HS Synchronizer	Circuit which perform the Re-Synchronization
I2C	Inter-Integrated Circuit. A kind of serial interface.
INT port	Internal port of S2R72A21
LS	Low-Speed
Portable Device (PD)	Mobile device such as Smart phone or Tablet
Re-Synchronization	To Re-synchronize the received HS packet from one port and send it out to the other port
Role Switch	Switch positions between Host and Device *Note: Role Switch here doesn’t mean the function of OTG device which take role of host partially)
SOF	Start-of-Frame
USB-IF	USB Implementers Forum, Inc.
USB specification	Universal Serial Bus Specification Revision 2.0

3. Operation

3.1 Description

S2R72A21 prepares 2 USB paths, Bus Switch and the HS Synchronizer.

The Bus switch electrically connects INT_DP/DM and EXT_DP/DM. The LS/FS signal or BC signals are passed by.

The HS Synchronizer is a feature which re-synchronizes the HS signal received from either INT_DP/DM or EXT_DP/DM and send out to the other port.

The objective paths are switched automatically by the internal Bus Monitor.

3.2 Basic system structure

As the basic system structure, here shows an example where S2R72A21 is mounted on the Car Navigation or Display Audio's board (Host SoC board). S2R72A21 intervenes between the Host SoC's USB port and the USB type-A receptacle, and connects the Host SoC (as Host) and Portable device such as smart phones (as Device).

The following is the pin connection example of S2R72A21 with this structure.

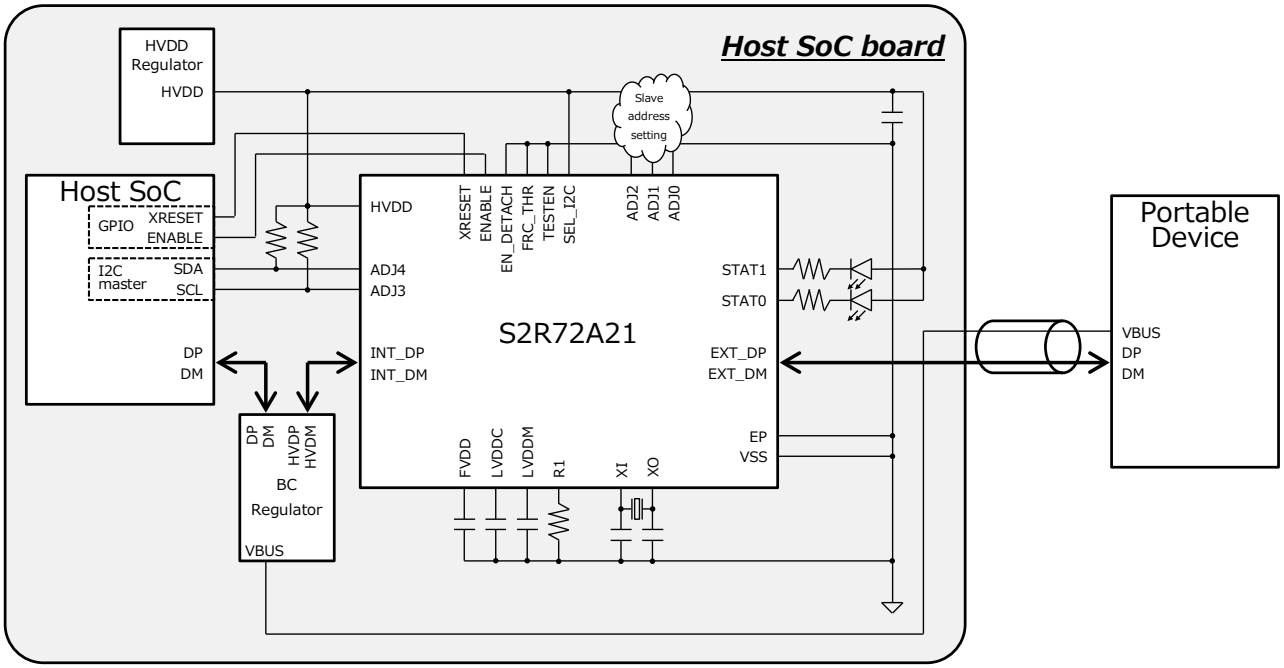


Figure 3.2.1 Basic system structure of S2R72A21

- INT_DP/DM : Please connect the Host SoC's USB port.
  Please connect the Host SoC's USB OTG port in case Role Switch is executed. It is possible to connect the BC Regulator for VBUS supply between the Host SoC's USB OTG port and the S2R72A21's INT port.
  BC Regulator can select the VBUS supply capability by negotiation with BC capable Portable Device. If connected with non-BC capable portable Device, the VBUS supply capability should be set to a fixed value or set by the Host SoC.
- EXT_DP/DM : Please connect to the USB Type-A receptacle.
  Please connect or disconnect the portable device using a USB cable.
- ENABLE : Please control it via the Host SoC's GPIO.
  Please set "1" when it is able to connect to the Device, and set "0" when the Device is disconnected
- EN_DETACH: Please set and stable it either to "0" or "1" on the boards. In this chapter, the case EN_DETACH=0 is explained as the basic setting.
- FRC_THR : Please set and stable it to "0" on the boards.
- SEL_I2C : Please set and stable it either to "0" or "1" on the boards. In this chapter, the case SEL_I2C=1 (I2C is in use) is explained as the basic setting.
- ADJ[4:0] : Please set and stable it either to "0" or "1" on the boards.
  ADJ[4:0] pins are assigned as I2C slave function pins in case SEL_I2C=1.
  ADJ[2:0] : Please set up either "0" or "1" on the boards and select the slave address.
  ADJ[3] : Please pull up to the HVDD and connect SCL of the I2C master
  ADJ[4] :Please pull up to the HVDD and connect SDA of the I2C master
- STAT[1:0] : This is outputting the internal condition. During default, it would be open drain (0/HiZ) outputs. Please monitor according to the needs.

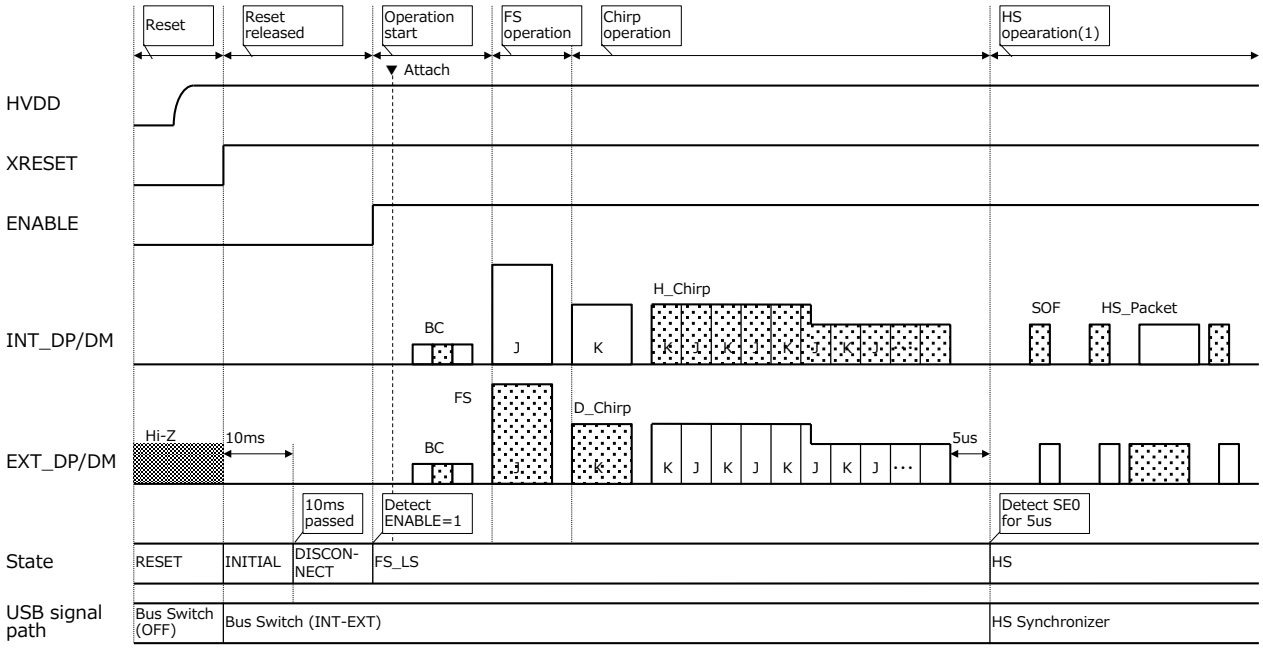
Please refer to chapter 4 and 5 for detail connection as well as the operation (example).

3.3 Basic operation

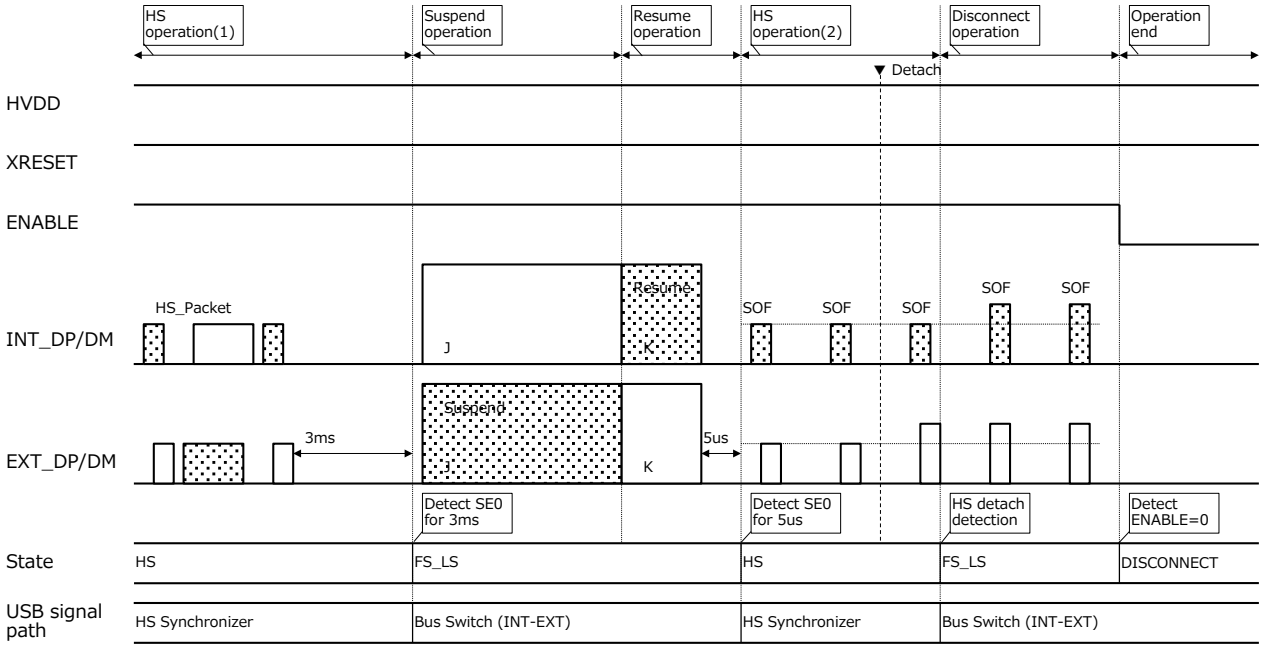
The basic operation of the S2R72A21 under the above basic system structure is explained based on an example of the USB2.0+BC operation waveform.

3.3.1 Operation waveform

Figure 3.3.1.1 shows an example of the S2R72A21 operation waveform on the basic system structure of Figure 3.2.1.



a) From Reset to HS operation (1)



b) From HS operation (1) to operation end

Figure 3.3.1.1 Basic operation waveform

3.3.2 Each operation

Each operation for the figure above is explained in time order.

3.3.2.1 RESET condition

S2R72A21 maintains the RESET state during XRESET=0 condition after power on.

During this period, the Bus Switch along with HS synchronizer would be stopped so the internal USB signal path's condition would be disconnected. Within this condition the EXT port would be Hi-Z.

3.3.2.2 RESET release

Once the reset is released (XRSET=1), the S2R72A21 would transit to INITIAL state and furthermore, it would transit to DISCONNECT state when it passes 10ms.

During this time, the USB signal path would connect the INT port and EXT port via the Bus Switch. Both INT port and EXT port would be VSS level due to the pull down resistor of the BC Regulator.

3.3.2.3 Operation start

When the Host SoC set up to ENABLE=1, the S2R72A21 would transit to FS_LS state.

During this period, similar to DISCONNECT state, the USB signal path would connect INT port and EXT via the Bus Switch. So both INT port and EXT port would maintain VSS level by the pull down resistor of the BC Regulator.

Under this condition, if you attach the Portable Device (BC capable) to the EXT port as "Device", a negotiation would start between Portable Device and BC Regulator based on the BC protocol (below 0.6V signal level).

3.3.2.4 FS operation

When the BC negotiation finishes, the Portable Device would indicate the FS_J to the EXT port and notify the IDLE condition.

During this time, the Bus Switch path of the USB signal would connect the INT port and EXT port, so the Host SoC can detect the connection of the Portable Device (IDLE condition).

After detecting the Portable Device, the Host SoC enables its HS termination and issues the Bus Reset by driving the SE0 to the INT port.

3.3.2.5 Chirp operation

After receiving the Bus Reset from the Host SoC, the Portable Device delivers Chirp K to the EXT port to indicate that the Portable Device is capable of HS. After receiving this, the Host SoC delivers Chirp K-J to the INT port to indicate the Host SoC is also capable of HS. These exchanges would occur during the HS termination of the Host SoC is enabled, so resulting USB signal amplitude would be 800mV.

After detecting "Chirp K-J-K-J-K-J", the Portable Device would also enable its HS termination. Due to this, Chirp K-J's amplitude would change from 800mV to 400mV.

S2R72A21 would detect this line of Chirp operation with Bus Monitor, and wait until this Chirp sequence is finished.

3.3.2.6 HS operation (1)

After the Chirp K-J delivery to the INT port from the Host SoC is finished, the S2R72A21 would judge that the Chirp is finished by SE0 detection and it would transit to HS state.

During this period, the USB signal path would be switched from Bus Switch to HS Synchronizer. Please wait over 5us until the first SOF transmit start from the Chirp delivery from the Host SoC is finished.

Within this condition, the HS signal from the Host SoC received from the INT port as well as the HS signal from the Portable Device received from the EXT port would be sent out to the other ports after it has been re-synchronized by HS Synchronizer. During this period, there would be packet delay since the HS Synchronizer compensates the SYNC field to 32bit. So please make the Host SoC communicate with the scheduling considering this point. And please be careful that the timeout (explained in section 7.1.19.2 of USB specification) is not provoked, especially in case multi-tier hubs are connected.

Furthermore, during HS operation, either the INT port or the EXT port is detected as the SOF receiving port. The HS disconnection detector circuit is validated for the port which does not receive the SOF. In this basic operation, SOF is received at INT port from Host SoC, so HS disconnection detector circuit of the EXT port (Portable Device side) is validated.

3.3.2.7 Suspend operation

During HS operation, if HS signal has not been received over 3ms with both INT and EXT port side, the S2R72A21 would judge HS operation cease and the transition to FS_LS state would occur to prepare for any Suspend detection.

During this time, the USB signal path would switch from HS Synchronizer to Bus Switch and the INT and EXT port would be connected. Please do not make the Host SoC and Portable Device transmit any HS signal after 2.95ms from the last HS signal delivery.

After the USB signal path switches to Bus Switch, it would detect the EXT port condition. In case it detects SE0, it would judge that the Host SoC is indicating Bus Reset. In case it detects FS_J, it would judge that the Host SoC is indicating Suspend. The first case is to prepare for Chirp Operation. In the latter case, it maintains the USB signal path along with the state of Suspend active while the FS_J is continuously detected.

3.3.2.8 Resume operation

During Suspend operation active, the detection of the EXT condition would be continued. In case the S2R72A21 detects SE0, it would judge the Host SoC is indicating Bus Reset. In case it detects FS_K, it would judge the Host SoC is indicating Resume and the Suspend operation would be finished. The first case prepares for the Chirp operation. In the latter case, the USB signal path would be maintained along with the Resume operation active while the FS_K is continuously detected.

3.3.2.9 HS operation (2)

When SE0 is detected after the FS_K at EXT port, the S2R72A21 would judge that the Host released the Resume and it would transit to HS state.

During this period, the USB signal path would switch from Bus Switch to HS Synchronizer. Please keep the Host SoC waiting over 5us from Resume end to the first SOF transmission start.

After the Resume is released, the HS operation is maintaining condition before the Suspend. So the HS disconnection detector circuit of the EXT port (Portable Device side) is validated again.

3.3.2.10 Disconnect Operation

When the Portable Device is detached during HS operation, the HS termination of the Portable Devices would be vanished and the amplitude of the EXT port's HS signal would change from 400mV to 800mV. The validated HS detector circuit (EXT port) would detect the amplitude variation by the SOF's EOP (with 40bit time length). When the Portable Device is judged "Detach" then the S2R72A21 would transit to FS_LS state.

During this period, the USB signal path would switch from HS Synchronizer to Bus Switch and the INT port and EXT port would be connected. Afterward the HS packet which is transmitted from the Host SoC would by pass from INT port to EXT port via the Bus Switch. Since the HS termination of the detached Portable Device has been vanished, the Host SoC output would have amplitude of 800mV. Due to this, the Host SoC would be able to detect the Portable Device has been detached using the Host SoC's own HS disconnection detector circuit.

In case EN_DETACH=1, S2R72A21 would transit to DETACH state after detection of Portable Device. During DETACH state, EXT port would be HiZ, since both the Bus Switch and the HS Synchronizer are stopped and the internal USB path is disconnected. Due to this, the USB cable attached to the EXT port is omitted from the USB signal path, so the Host SoC can detect the Portable Device detach with less influence of the returning wave. When 3ms has passed, the S2R72A21 would transit to FS_LS state.

Figure 3.3.2.10.1 shows the disconnection operation waveform in case EN_DETACH=1.

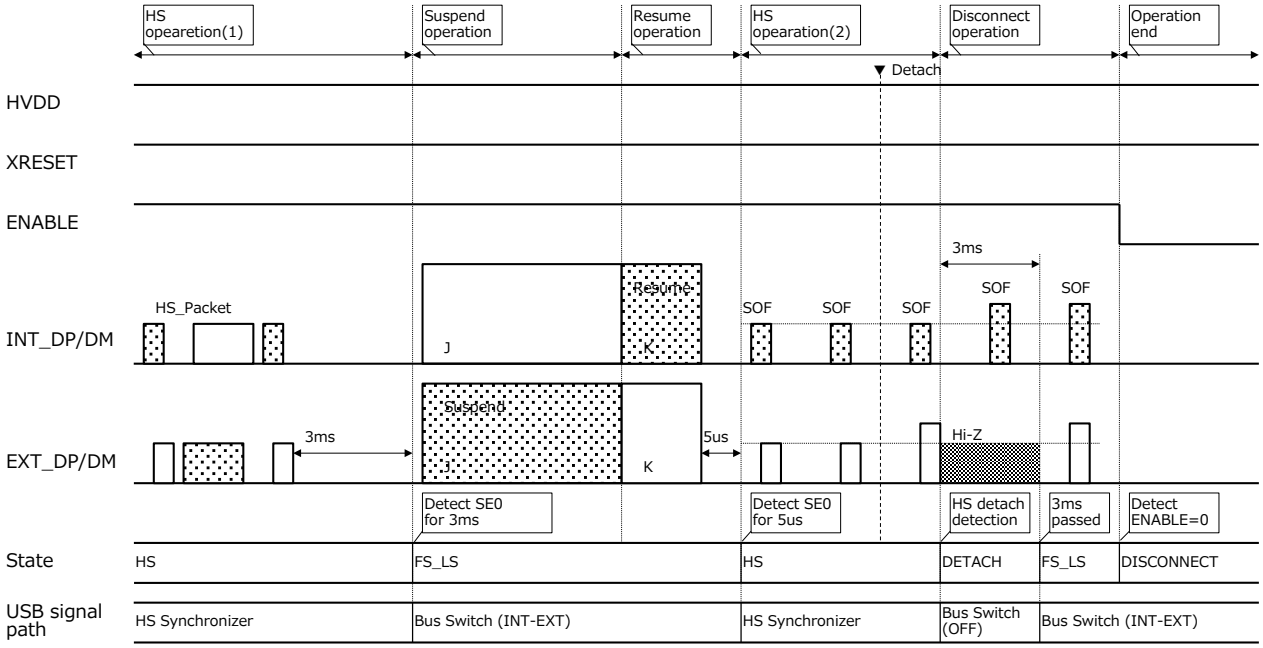


Figure 3.3.2.10.1 Disconnection operation waveform in case EN_DETACH=1

3.3.2.11 Operation end

The Host SoC can notify the Detach detection to the S2R72A21 by ENABLE=0 once the Host SoC has detected the Detach of the Portable Device. The S2R72A21 would transit to DISCONNECT state when ENABLE=0.

Here the connection of the INT port and the EXT port is maintained. Both the INT port and the EXT port would be VSS level due to the pull down resistor of the Host SoC.

Afterward, the S2R72A21 would start operation by ENABLE=1 again, and then the S2R72A21 is ready to accept re-attach of the Device.

Please note that the S2R72A21 would also transit to DISCONNECT state by setting XRESET 0→1 and 10ms passes by. After detecting ENABLE=1, the S2R72A21 is ready to accept re-attach.

3.4 HS transmission current control

HS transmission current control function (ADJ function) is a feature which controls the current used for transmitting from either INT or EXT port during HS connection. By this feature, it enables to control the amplitude of the USB signal. Please refer to the S2R72A21 data sheet section 6.4.1 for details.

This section explains cautions when setting ADJ function.

Figure 3.4.1 shows a USB system example including USB cable and schematic diagrams of HS signal amplitude in the form of Eye pattern.

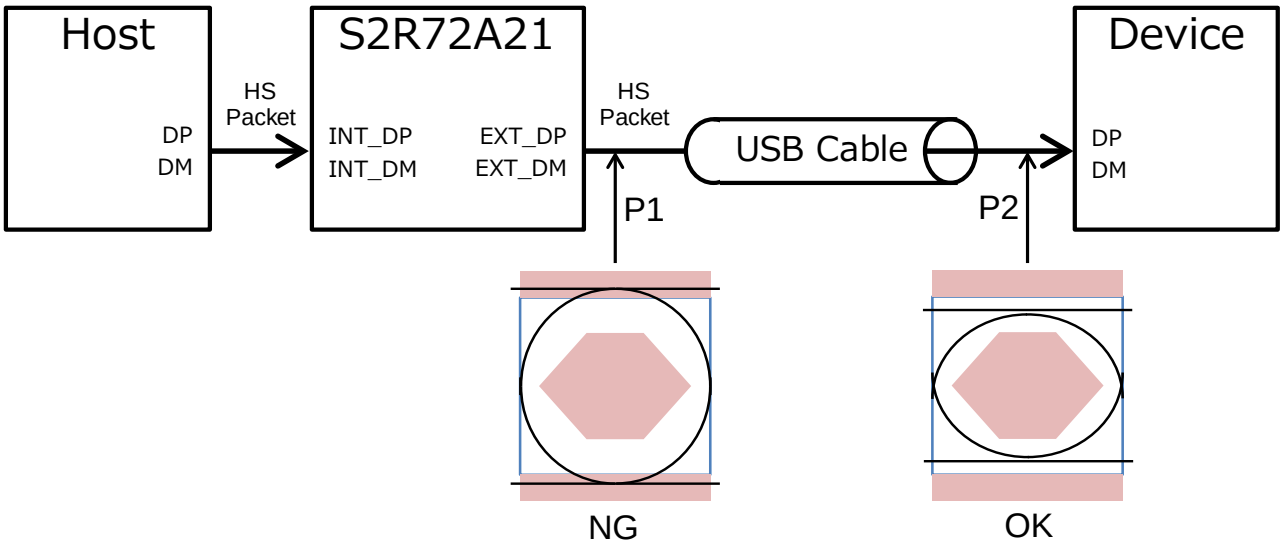


Figure 3.4.1 A USB system example and schematic diagrams of HS signal amplitude

HS packets transmitted from the Host are re-synchronized by S2R72A21, and reach the Device through the USB Cable. P1 is the signal measuring point at the S2R72A21 pin, and P2 is the signal measuring point at the Device.

The HS signal transmitted from the S2R72A21 is attenuated by the USB cable, etc., thus the signal amplitude at P1 is greater than that at P2 as shown in the figure.

The S2R72A21 detects the disconnection when the SOF amplitude level exceeds the threshold at its pin. Therefore, please configure the ADJ settings with care not to exceed the disconnect detection threshold at P1.

4. Connection example

Please refer to the following in regard to the 3 system connection examples using S2R72A21. Please refer to Chapter 5 for detail operation of each connection examples.

In addition, “EP” in the drawing stands for Exposed die pad.

In case where the Portable Device executes the Role Switch and the Bus is floating after the Role Switch, we recommend pulling down the DP and DM of the Portable Device side (ex. 1MΩ).

4.1 Connection ex. Host SoC (on the same board)/INT port, Portable Device/EXT port

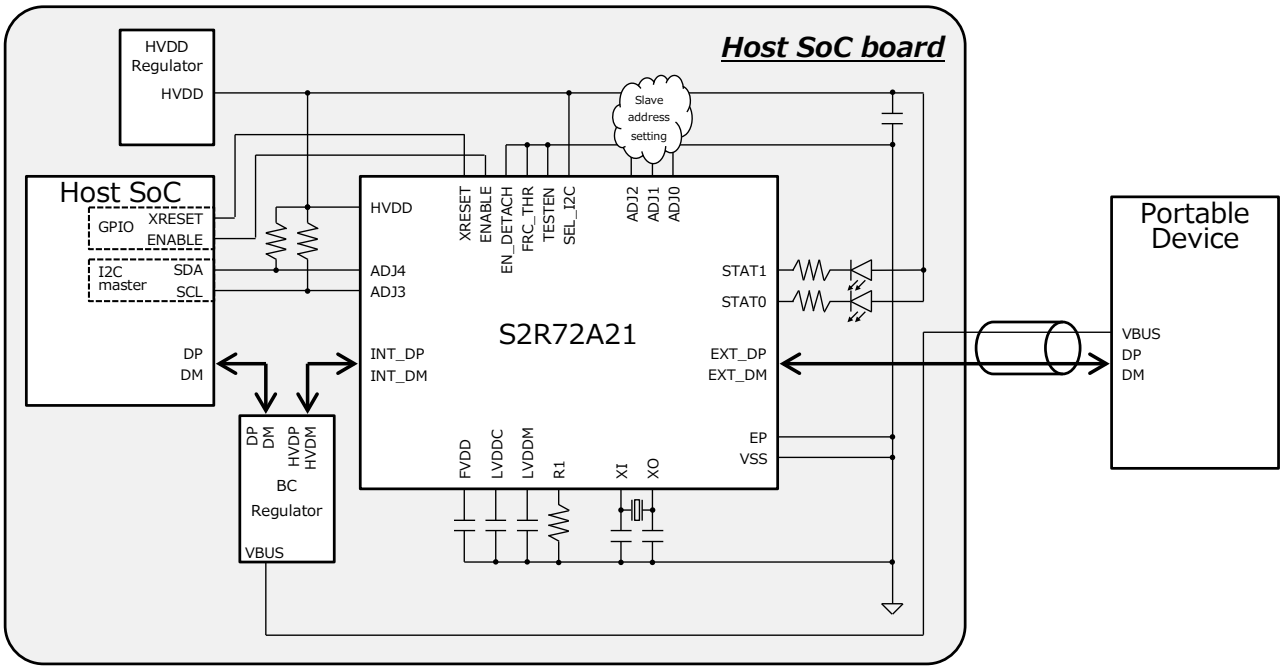


Figure 4.1.1 Connection ex. Host SoC (on the same board)/INT port, Portable Device/EXT port

The same as the basic system structure shown on Figure 3.2.1.

4.2 Connection ex. Host SoC (on the separate board)/INT port, Portable Device/EXT port

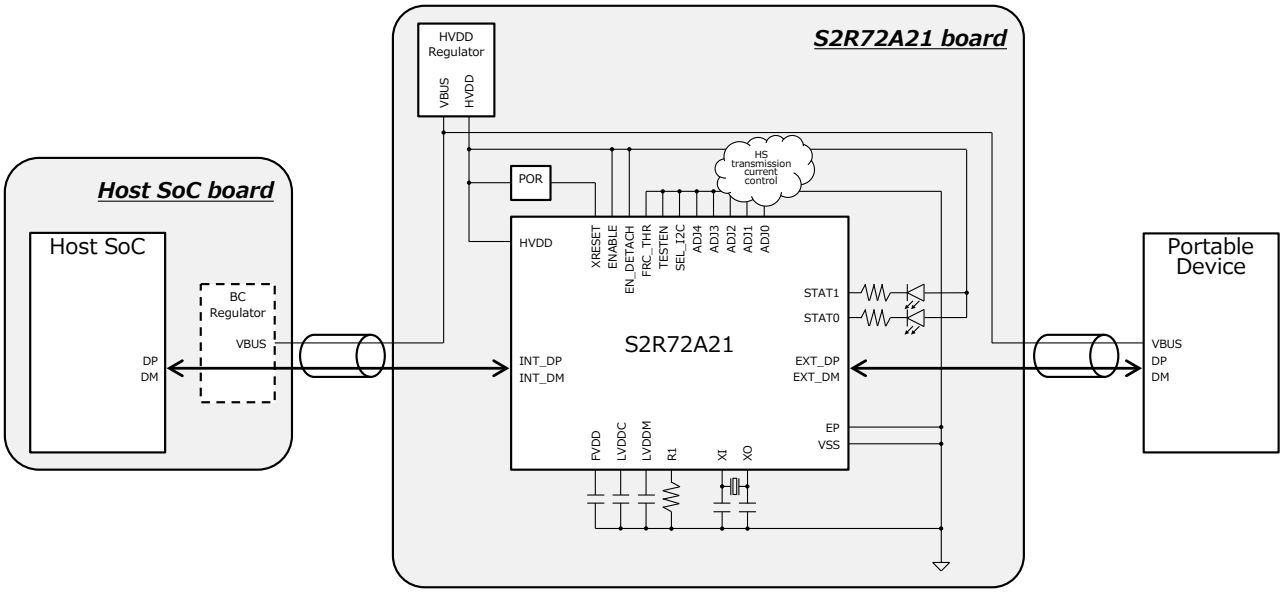


Figure 4.2.1 Connection ex. Host SoC (on the separate board)/INT port, Portable Device/EXT port

4.3 Connection ex. Host SoC (on the separate board)/EXT port, Portable Device/INT port

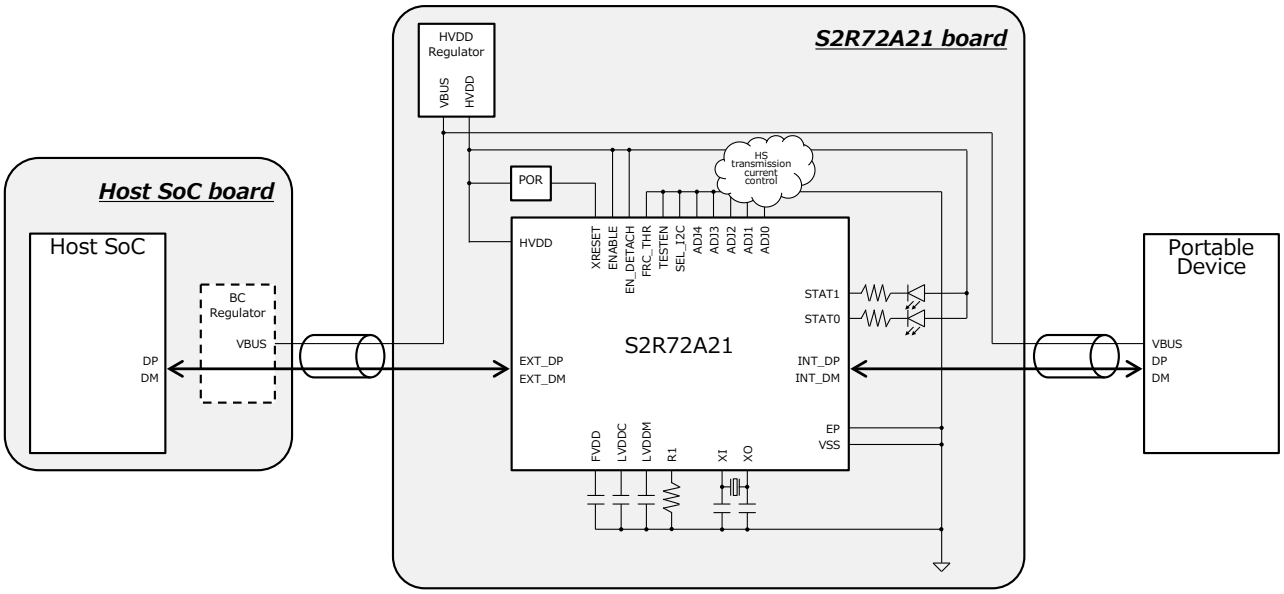


Figure 4.3.1 Connection ex. Host SoC (on the separate board)/EXT port, Portable Device/INT port

5. Operation within each connection example

Within the 3 system connection examples indicated on Chapter 4, we would explain each of the operation such as the ADJ setting, BC control, Role Switch control and the disconnection detection control separately within section 5.1-5.3. Table 5.1 is the summary of the connection, function, pin setting, disconnection detection control for each system structure.

Role Switch is a function to switch the Host & Device role as indicated on Chapter 2, and some Portable Devices have this function. S2R72A21 is a Re-Synchronization IC which also follows the Role Switch function.

In case where the Portable Device has the Role Switch function, there would be a negotiation to switch the role of the Host and the Device after FS to HS connection (corresponding to the USB specification). After that the Portable Device would play as a Host and issue the Bus reset and resume the HS communication again via FS to HS connection.

As mentioned on the S2R72A21 Data sheet (section 6.1.1), S2R72A21 would transit from HS state to FS_LS state automatically when over 3ms of SE0 is detected and the Bus Switch connection between INT-EXT would be valid. In other words, within the above Role switch operation sequence, S2R72A21 would detect over 3ms of SE0, automatically validate the Bus Switch in between INT-EXT for FS communication, and transit to HS communication connection condition after Role Switch.

Table 5.1 Summary of each system structure

Section	USB port connection		Function		Pin	Disconnection detection control after Role Switch
	INT	EXT	I2C IF	HS transmission current control	ADJ	
4.1 5.1	Host SoC (BC)	PD	Usable	INT/EXT Fine adjustment	I2C address	ENABLE pin control; 0 to 1
4.2 5.2	Host SoC (BC)	PD	Unusable	EXT only Rough tuning	HS transmission current control	VBUS supply: Stop to resume
4.3 5.3	PD	Host SoC (BC)	Unusable	EXT only Rough tuning	HS transmission current control	VBUS supply: Stop to resume

BC = BC Regulator

PD = Portable Device

5.1 Connection ex. Host SoC (on the same board)/INT port, Portable Device/EXT port

5.1.1 ADJ settings

S2R72A21 is mounted on the same board as the Host SoC. Each of the ADJ4 pin (SDA pin) and ADJ3 (SCL pin) are connected with the SoC's I2C master. In this case, the HS transmit current control can all be possible to set entire 4bit for both the INT and the EXT port by setting SEL_I2C=1 setting via I2C register. Please follow the S2R72A21 data sheet's section 4.2 Control Pin, and set up the ADJ4-0 pins.

5.1.2 BC control

The Bus Switch of S2R72A21 makes a connection between INT and EXT port when reset is released (XRESET=1). After Portable Device is connected to the EXT port, the Portable Device would communicate with the BC regulator (mounted on the same board) and determine the SDP/CDP/DCP by BC protocol. After the BC protocol, the Portable Device would issue FS_J and the connection with Host SoC would start.

5.1.3 Role Switch control

If the Portable Device is a Device which does not execute the Role Switch, the Host SoC connected to the INT side would consistently function as a Host, and the Portable Device connected to the EXT would act as a Device.

If the Portable Device is a Device which executes the Role Switch, the Portable Device which is connected to the EXT port would become the Host via some designated process after HS connection. At the same time, the Host SoC which is connected to the INT side would switch as a Device (In this case, the Portable Device and the Host SoC would change its role nevertheless it's naming. However for the convenience, within this documents would keep calling the name as Portable Device and Host SoC). If the Bus becomes Floating during the Role Switch period, we recommend to pull down the Bus by 1MΩ and etc.

5.1.4 Method to detect disconnection of Portable Device

When the Portable Device does not execute the Role Switch, it requires the following 3 steps to make the USB connection disconnected via S2R72A21.

1: Detection of HS disconnection by S2R72A21

> S2R72A21 would detect the HS disconnection by detecting the SOF amplitude level changes which is sent out by its EXT port. After that, in case EN_DETACH=0, the HS Synchronizer gets "Off", Bus Switch would be connected in between INT-EXT port and the transition to FS_LS state is done. In case EN_DETACH=1, the S2R72A21 transiently gets into DETACH state for 3ms where both the HS Synchronizer and the Bus Switch would get "Off", and then the transition to FS_LS state is done where the Bus Switch connects INT-EXT port. In case the total cable length of INT port and EXT port is long, the EN_DETACH pin can be set to 1.

2: Detection of HS disconnection by Host SoC

> Host SoC would also monitor the SOF amplitude level and detect the Portable Device disconnection via its built in HS disconnection detector.

3: Notification of HS disconnection from the Host SoC to S2R72A21 (Optional)

> Notification from the Host SoC to S2R72A21 of the disconnection detection can be done by ENABLE=0 as appropriate.

When the Portable Device executed the Role Switch, it requires the following 3steps to make the Host SoC detect HS disconnection of the Portable Device.

1: S2R72A21 would detect the SE0 condition and transit to FS_LS state

Since the periodic SOF sent from the Portable Device (as Host) is lost, the SE0 would be detected by EXT port's Bus state. When the S2R72A21 detects the SE0 condition for 3ms by the Bus state, the HS Synchronizer's operation would stop and the FS_LS state transition is done where the Bus Switch path between INT-EXT gets "ON".

Here, the Host (Portable Device) is lost and the Device (Host SoC) is left on the Bus. In this situation the bus would deviate from the USB specification and the S2R72A21 may not follow the Bus state. Furthermore, the bus state on the EXT port may be unstable depending on the contact situation of the connector during detach, since the Portable Device is detached while packets are exchanged. This may provoke malfunction of the S2R72A21.

2: Host SoC would judge HS disconnection by Bus invalid condition.

From the Bus Switch path connection, the Host SoC will judge the disconnection of the Portable Device by detecting the EXT port's Bus invalid condition for a certain period of time.

3: Notification of HS disconnection from the Host SoC to S2R72A21

Notification from the Host SoC to S2R72A21 of the disconnection detection is done by ENABLE=0.

This initializes the state which deviated from the USB specification, and fixes the malfunction caused by the unstable contact situation of the connector during detach.

In all cases above, re-attach of the Portable Devices are accepted after recovering to ENABLE=1 (ENABLE=1: the Bus Switch Path would return to the initial condition where the INT port and the EXT port are connected).

5.2 Connection ex. Host SoC (on the separate board)/INT port, Portable Device/EXT port

5.2.1 ADJ settings

The S2R72A21 would be connected to the Host SoC via USB cables only, so the HS transmit current control function via the I2C register cannot be used. In this case please set SEL_I2C=0 and follow, section 4.2 control pin of the S2R72A21 data sheet and set up the HS transmit current control function by ADJ2-0.

In addition, EXT port would only be able to control the transmit current (Portable Device side).

5.2.2 BC control

The Bus Switch of S2R72A21 makes a connection between INT and EXT port when reset is released (XRESET=1). After Portable Device is connected to the EXT port, the Portable Device would communicate with the BC regulator (mounted on the separate board) and determine the SDP/CDP/DCP by BC protocol. After the BC protocol, the Portable Device would issue FS_J and the connection with Host SoC would start.

5.2.3 Role Switch control

If the Portable Device is a Device which does not execute the Role Switch, the Host SoC connected to the INT side would consistently function as a Host, and the Portable Device connected to the EXT would act as a Device.

If the Portable Device is a Device which executes the Role Switch, the Portable Device which is connected to the EXT port would become the Host via some designated process after HS connection. At the same time, the Host SoC which is connected to the INT side would switch as a Device (In this case, the Portable Device and the Host SoC would change its role nevertheless it's naming. However for the convenience, within this documents would keep calling the name as Portable Device and Host SoC). If the Bus becomes Floating during the Role Switch period, we recommend to pull down the Bus by 1MΩ and etc.

5.2.4 Method to detect disconnection of Portable Device

When the Portable Device does not execute the Role Switch, it requires the following 3 steps to make the USB connection disconnected via S2R72A21.

1: Detection of HS disconnection by S2R72A21

> S2R72A21 would detect the HS disconnection by detecting the SOF amplitude level changes which is sent out by its EXT port. After that, in case EN_DETACH=0, the HS Synchronizer gets "Off", Bus Switch would be connected in between INT-EXT port and the transition to FS_LS state is done. In case EN_DETACH=1, the S2R72A21 transiently gets into DETACH state for 3ms where both the HS Synchronizer and the Bus Switch would get "Off", and then the transition to FS_LS state is done where the Bus Switch connects INT-EXT port. In case the total cable length of INT port and EXT port is long, the EN_DETACH pin can be set to 1.

2: Detection of HS disconnection by Host SoC

> Host SoC would also monitor the SOF amplitude level and detect the Portable Device disconnection via its built in HS disconnection detector.

3: S2R72A21 is stopped by Host SoC (Optional)

> Notification from the Host SoC to S2R72A21 of the disconnection detection can be done by shut-off VBUS supply as appropriate.

When the Portable Device executed the Role Switch, it requires the following 3steps to make the Host SoC detect HS disconnection of the Portable Device.

1: S2R72A21 would detect the SE0 condition and transit to FS_LS state

Since the periodic SOF sent from the Portable Device (as Host) is lost, the SE0 would be detected by EXT port's Bus state. When the S2R72A21 detects the SE0 condition for 3ms by the Bus state, the HS Synchronizer's operation would stop and the FS_LS state transition is done where the Bus Switch path between INT-EXT gets "ON".

Here, the Host (Portable Device) is lost and the Device (Host SoC) is left on the Bus. In this situation the bus would deviate from the USB specification and the S2R72A21 may not follow the Bus state. Furthermore, the bus state on the EXT port may be unstable depending on the contact situation of the connector during detach, since the Portable Device is detached while packets are exchanged. This may provoke malfunction of the S2R72A21.

2: Host SoC would judge HS disconnection by Bus invalid condition.

From the Bus Switch path connection, the Host SoC will judge the disconnection of the Portable Device by detecting the INT port's Bus invalid condition for a certain period of time.

3: S2R72A21 is stopped by Host SoC

Notification from the Host SoC to S2R72A21 of the disconnection detection is done by shut-off VBUS supply.

This initializes the state which deviated from the USB specification, and fixes the malfunction caused by the unstable contact situation of the connector during detach.

In all cases above, re-attach of the Portable Devices are accepted after recovering VBUS supply (VBUS supply: the Bus Switch Path would return to the initial condition where the INT port and the EXT port are connected).

The disconnection detection notification cannot be done via the ENABLE pin since this connection example would be done via USB cable only (between Host SoC and S2R72A21). In this case please reset the S2R72A21 as indicated above at 3Steps (Stop the VBUS supply and then resuming it). Please refer to the AC characteristics on the Data sheet for the timings (VBUS supply stop to resume).

5.3 Connection ex. Host SoC (on the separate board)/EXT port, Portable Device/INT port

5.3.1 ADJ settings

The S2R72A21 would be connected to the Host SoC via USB cables only, so the HS transmit current control function via the I2C register cannot be used. In this case please set SEL_I2C=0 and follow, section 4.2 control pin of the S2R72A21 data sheet and set up the HS transmit current control function by ADJ2-0.

In addition, EXT port would only be able to control the transmit current (Host SoC side).

5.3.2 BC control

The Bus Switch of S2R72A21 makes a connection between INT and EXT port when reset is released (XRESET=1). After Portable Device is connected to the INT port, the Portable Device would communicate with the BC regulator (mounted on the separate board) and determine the SDP/CDP/DCP by BC protocol. After the BC protocol, the Portable Device would issue FS_J and the connection with Host SoC would start.

5.3.3 Role Switch control

If the Portable Device is a Device which does not execute the Role Switch, the Host SoC connected to the EXT side would consistently function as a Host, and the Portable Device connected to the INT would act as a Device.

If the Portable Device is a Device which executes the Role Switch, the Portable Device which is connected to the INT port would become the Host via some designated process after HS connection. At the same time, the Host SoC which is connected to the EXT side would switch as a Device (In this case, the Portable Device and the Host SoC would change its role nevertheless it's naming. However for the convenience, within this documents would keep calling the name as Portable Device and Host SoC). If the Bus becomes Floating during the Role Switch period, we recommend to pull down the Bus by 1MΩ and etc.

5.3.4 Method to detect disconnection of Portable Device

When the Portable Device does not execute the Role Switch, it requires the following 3 steps to make the USB connection disconnected via S2R72A21.

1: Detection of HS disconnection by S2R72A21

> S2R72A21 would detect the HS disconnection by detecting the SOF amplitude level changes which is sent out by its INT port. After that, in case EN_DETACH=0, the HS Synchronizer gets "Off", Bus Switch would be connected in between INT-EXT port and the transition to FS_LS state is done. In case EN_DETACH=1, the S2R72A21 transiently gets into DETACH state for 3ms where both the HS Synchronizer and the Bus Switch would get "Off", and then the transition to FS_LS state is done where the Bus Switch connects INT-EXT port. In case the total cable length of INT port and EXT port is long, the EN_DETACH pin can be set to 1.

2: Detection of HS disconnection by Host SoC

> Host SoC would also monitor the SOF amplitude level and detect the Portable Device disconnection via its built in HS disconnection detector.

3: S2R72A21 is stopped by Host SoC (Optional)

> Notification from the Host SoC to S2R72A21 of the disconnection detection can be done by shut-off VBUS supply as appropriate.

When the Portable Device executed the Role Switch, it requires the following 3steps to make the Host SoC detect HS disconnection of the Portable Device.

1: S2R72A21 would detect the SE0 condition and transit to FS_LS state

Since the periodic SOF sent from the Portable Device (as Host) is lost, the SE0 would be detected by INT port's Bus state. When the S2R72A21 detects the SE0 condition for 3ms by the Bus state, the HS Synchronizer's operation would stop and the FS_LS state transition is done where the Bus Switch path between INT-EXT gets "ON".

Here, the Host (Portable Device) is lost and the Device (Host SoC) is left on the Bus. In this situation the bus would deviate from the USB specification and the S2R72A21 may not follow the Bus state. Furthermore, the bus state on the INT port may be unstable depending on the contact situation of the connector during detach, since the Portable Device is detached while packets are exchanged. This may provoke malfunction of the S2R72A21.

2: Host SoC would judge HS disconnection by Bus invalid condition.

From the Bus Switch path connection, the Host SoC will judge the disconnection of the Portable Device by detecting the EXT port's Bus invalid condition for a certain period of time.

3: S2R72A21 is stopped by Host SoC

Notification from the Host SoC to S2R72A21 of the disconnection detection is done by shut-off VBUS supply.

This initializes the state which deviated from the USB specification, and fixes the malfunction caused by the unstable contact situation of the connector during detach.

In all cases above, re-attach of the Portable Devices are accepted after recovering VBUS supply (VBUS supply: the Bus Switch Path would return to the initial condition where the INT port and the EXT port are connected).

The disconnection detection notification cannot be done via the ENABLE pin since this connection example would be done via USB cable only (between Host SoC and S2R72A21). In this case please reset the S2R72A21 as indicated above at 3Steps (Stop the VBUS supply and then resuming it). Please refer to the AC characteristics on the Data sheet for the timings (VBUS supply stop to resume).

6. USB Compliance test

S2R72A21 does not belong to Host, Device or Hub within the USB portfolio. This means S2R72A21 does not have any function for USB compliance testing (Host function, Device function and Hub function). Furthermore, S2R72A21 does not have any register to maintain VID/PID. Therefore, S2R72A21 itself cannot be USB certified. Based on the explanation of this chapter, please obtain USB certification for the Host including S2R72A21 through the compliance test as Host.

6.1 S2R72A21 function aimed at USB compliance test

HS Test Packet which is used for the Compliance test is re-synchronized during the S2R72A21 HS operation and transfer INT→EXT or EXT→INT.

Also it has a feature to transmit the High-speed J/K to the other port, when HS Test J/ Test K are detected from one port. Please set “0” to either ENABLE pin or XRESET pin of S2R72A21 to recover from this condition.

With these specific features, USB compliance test can be done with combing the general Host.

6.2 General Test method

6.2.1 High-speed Signal Quality

This is the explanation of HS eye pattern acquisition method. In order to acquire the HS eye pattern, it is required to set the S2R72A21 to HS state (HS synchronizer = ON).

1. Please connect the HS Host to the INT port and HS Device to the EXT port and confirm whether the Host and Device is HS connected. After the connection, Please avoid the Bus to be Suspend or FS/LS condition after connection. Herewith the S2R72A21 would be HS state.

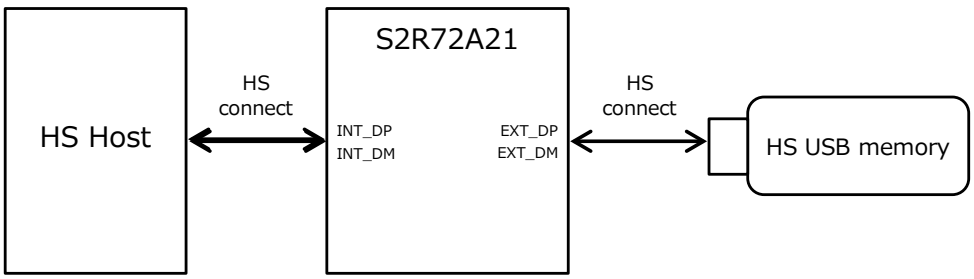


Figure 6.2.1.1 Procedure-1 connection

2. Please make the Host output the Test Packet and input towards the INT port. The Host must output the Test Packet continuously with an appropriate interval in accordance with the USB specification, so that the Bus would not be Suspend condition. By doing this the S2R72A21 would re-synchronize the Test Packet from the INT port and output to the EXT port.
3. Please replace the HS Device of the EXT port to Host Test Fixture.

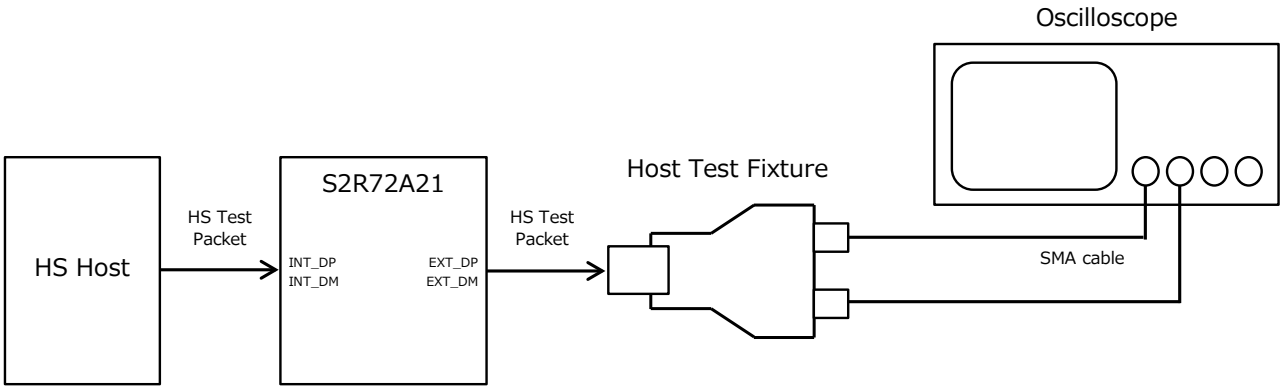


Figure 6.2.1.2 Procedure-3 connection

4. Please acquire the HS eye Pattern from the connected Host Test Fixture on procedure-3 using the oscilloscope.

6.2.2 Test J / K

Here is the explanation of the S2R72A21's output methods of High-speed J/K. It is similar to the method explained on section 6.2.1. Please make the Host output the High-Speed J/K via Test J/K mode instead of Test Packet.

1. Please connect the HS Host to the INT port and HS Device to the EXT port and confirm whether the Host and Device is HS connected. Please avoid the Bus to be Suspend or FS/LS condition after connection. Herewith the S2R72A21 would be HS state.
2. Please make the HS Host into Test J/K mode and input the Test J/K signal from the Host to the INT port. Herewith the S2R72A21 would output the High speed J/K from the EXT port.
3. Please measure the voltage level using the High-speed J/K signal which is output from the EXT port.

When doing another testing after Test_J / K output, please either set the ENABLE pin or XRESET pin of S2R72A21 0>1 or turn off the HVDD power and supply again.

6.3 Test method with Evaluation board

Here are the test method procedure examples using the S2R72A21 evaluation board (S5U2R72A11F0100 / Onnetoh) and the PC which installed the "USB High-Speed Electrical Test Tool".

6.3.1 Test environment

The test environment overview is below.

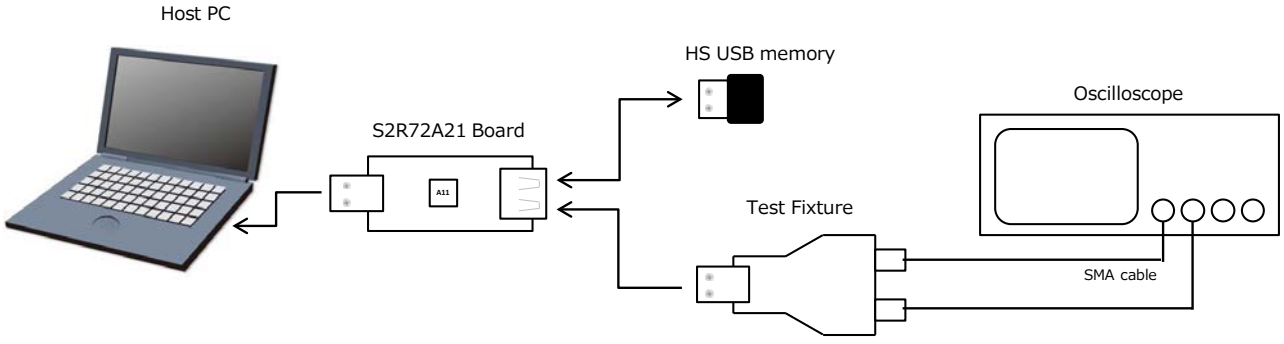


Figure 6.3.1.1 Test Environment

Table 6.3.1.1 System example of Test environment

Tool	Supplier	Model number
S2R72A21 evaluation board	Epson	S5U2R72A11F0100 (Onnetoh)
Host PC	Epson	Endeavor NJ1000 (WindowsXP) Installed the “USB High-Speed Electrical Test Tool” (HS Electrical Test Tool) http://www.usb.org/developers/compliance/electrical_tests//#usbhset
HS USB memory	IO Data	U2-ADP8G
Test Fixture	USB-IF	USB 2.0 Hi-Speed Signal Quality Test Fixture (Host test fixture)
Oscilloscope	Tektronix	MSO70404
SMA cable	Keysight	15443A Matched Cable Pair

6.3.2 Test procedure

1. Connect the Host PC and the S2R72A21 Evaluation board (INT port side).

Figure 6.3.2.1 Procedure-1 connection

2. Connect the HS USB memory to the S2R72A21evaluation board’s EXT port, and check whether there is HS connection between the Host PC and the HS memory. The LED2 (STAT0) would light up when the S2R72A21 is HS state.

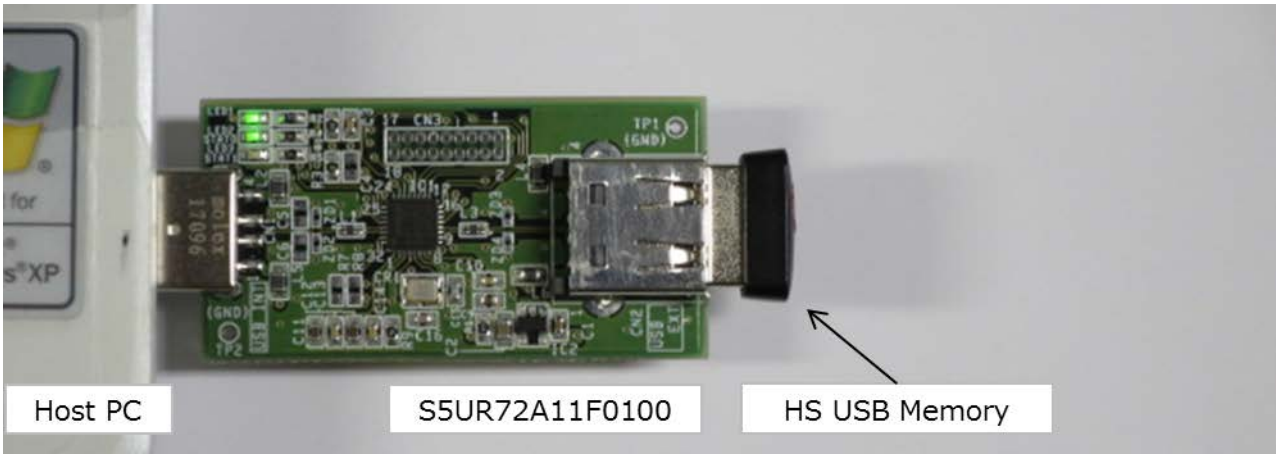


Figure 6.3.2.2 Procedure-2 connection

3. Start the USB Electrical Test Tool which is installed on the Host PC, and select the Host Controller/System from the “Select Type Of Test” and press TEST.

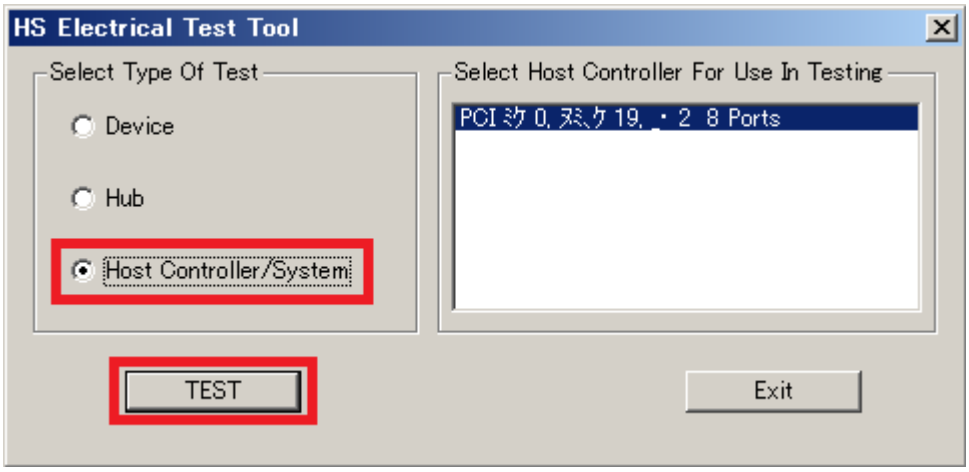


Figure 6.3.2.3 Procedure-3 (HS Electrical Test Tool picture)

4. Select TEST_PACKET, via Port Control.

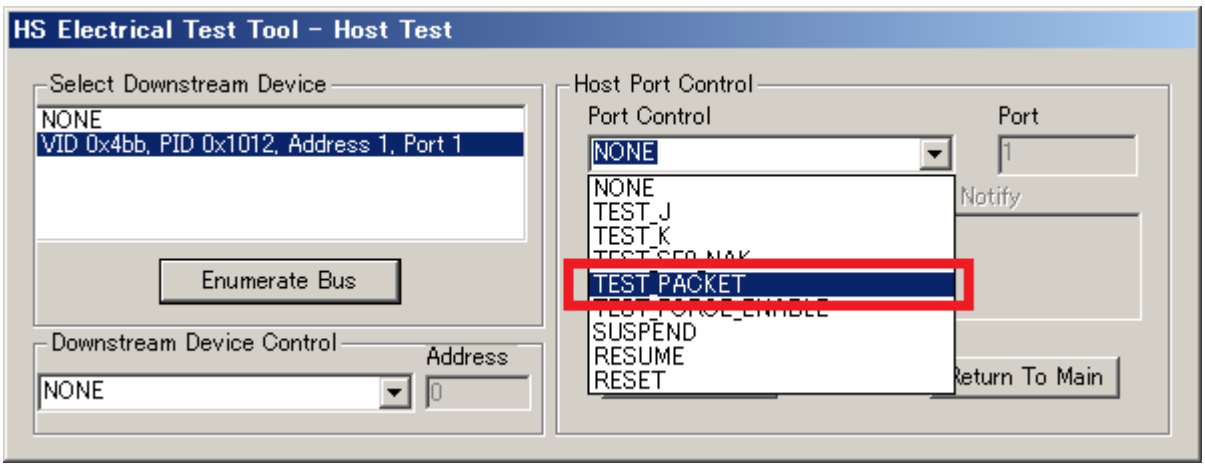


Figure 6.3.2.4 Procedure-4 (HS Electrical Test Tool picture)

5. Push EXECUTE after inputting the Port # connected to the S2R72A21evaluation board.
With this operation, the Test Packet would be output from the Host PC, and then output from the EXT port via S2R72A21’s HS Synchronizer.

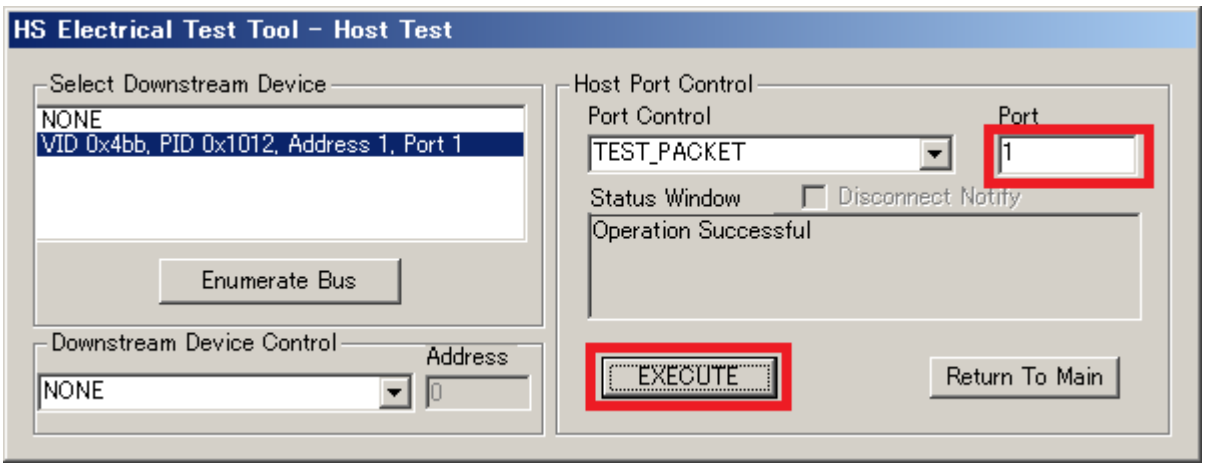


Figure 6.3.2.5 Procedure-5 (HS Electrical Test Tool picture)

6. HS memory connected EXT port would be replaced to Host test fixture.

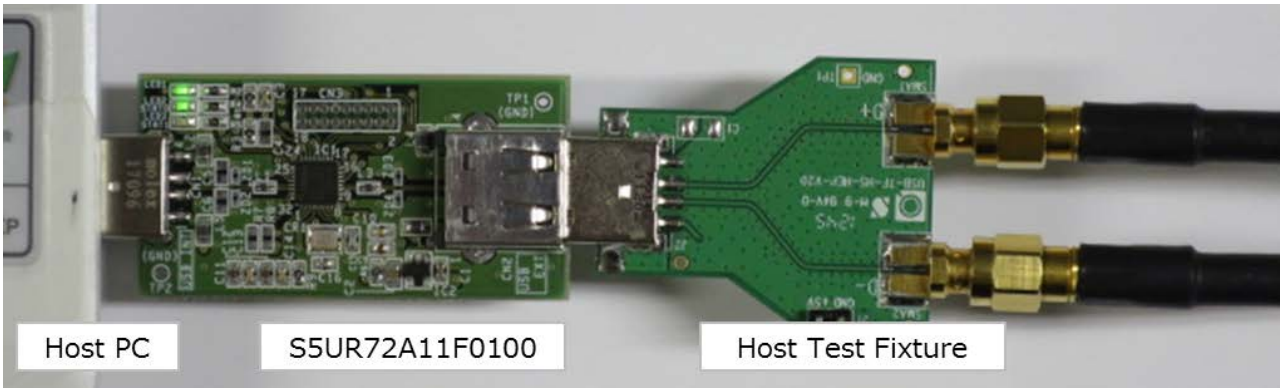


Figure 6.3.2.6 Procedure-6 connection

7. The Eye pattern is acquired via Oscilloscope (using a USB evaluation tool)
   During this period, please check whether the LED2 (STAT0) is lighting. If the LED2 (STAT0) is not lighting, the S2R72A21 is not under HS state so it is not possible to acquire eye pattern correctly.

When outputting the Test J/K, basically the procedures are similar as above. Please select either TEST_J or TEST_K within the Port Control (above procedure-4). When you press EXECUTE on procedure-5, either High-Speed J or K is output via the S2R72A21's EXT port.

6.4 Cautions for each test

6.4.1 EL_22

The EL_22 is a test specified in the USB 2.0 Electrical Compliance Test. When the compliance test is carried out as Host, the EL_22 tests the response period to the HS packet which the Host received from the Device.

As stated on section 6.3 of the data sheet, a packet delay would occur during HS packet re-synchronization. When the system with S2R72A21 is tested as a Host, the total period of the Host Controller's response and the round-trip delay of S2R72A21 would be observed as the total system's period. Due to this, there would be a possibility exceeding the max response period of 192 bit times (stated on the EL_22).

Detail would be explained on the separate document shown below.

6.4.2 Full-speed Signal Quality

The Full-speed Signal Quality is a test specified in the USB 2.0 Electrical Compliance Test. The signal quality of FS packet output from the downstream port is measured in case the system is tested as Host.

The FS signal quality is affected by the impedance elements on the whole bus, such as BC Regulator, cable, and on-resistance of S2R72A21's Bus Switch. Please evaluate on the actual system.

6.5 Compliance test for Host systems with S2R72A21

There is a separate document which explains the compliance test for Host systems which the S2R72A21are used. Please contact our sales window in charge for this document "Compliance test for Host systems with S2R72A21" before the compliance test.

6.6 Contact window regarding Compliance test

Epson built a model product (Host system) with the USB2.0 Re-Synchronization IC and carried out the compliance test. This compliance test was done at Allion Japan Inc. (Allion) and the USB certification has been obtained (TID: 120001008).

Epson has explained the product characteristics of the USB2.0 Re-Synchronization IC to Allion and Granite River Labs Japan Ltd. (GRL).

Please contact the following Allion or GRL window for compliance testing in relates to product using S2R72A21. If the contact person is unknown, please ask Epson's local sales window.

****

Allion Japan Inc.

Standards Compliance Division

Email: SCDivision@allion.co.jp

Tel: +81-3-5488-7368

****

Granite River Labs Japan Ltd.

Email: info_japan@graniteriverlabs.com

Tel: +81-45-470-0030

****

7. PCB design guide

7.1 Power supply and reset

The following is the explanation in regard to power supply related topic towards the S2R72A21.

- Power on / Power down sequence

The power supplied to S2R72A21 is only HVDD (3.3V). There is no Power on / Power down sequence since there is a built in regulator. 1.8V can be supplied internally.

- Noise

Noise on the power supply may affect the USB waveform quality and cause USB communication problems. Care must be taken when designing the power supply to avoid external noise or ripple noise due to irregular series regulator oscillation or if the switching regulator circuit constants are inappropriate.

- Reset

Please release the reset by setting the XRESET pin from Low to High after power supply to S2R72A21 is finished. The OSC circuit would start the oscillation after the reset is released. So there is no necessity of any sequence such as reset release after the oscillation is stabled.

7.2 DP/DM signal line

7.2.1 Circuit board wiring

The following points should be taken into consideration for the DP/DM signal wiring to ensure impedance matching and prevent reflection.

- The differential impedance in the DP/DM signal line must be 90Ω.
- Sufficient attention must be paid to impedance matching if other connectors and cables are inserted between the S2R72A21 and the USB receptacle.
- The inner layer right under the signal line must be a non-separated GND plane.
- Signal lines that could be noise source (e.g. clock, high speed bus line) must be kept away from the DP/DM line.
- A pair of DP/DM signal lines should be parallel and of equal length, and should be kept as short as possible. Branches should be minimized, and curved lines should be subject to curved wire treatment.

7.2.2 Additional component

- Common mode choke coil

The common mode choke coil prevents the occurrence of common mode noise by inhibiting current flowing in the same direction in the differential signal line. Use on the DP/DM signal line can be effective in improving skew and in reducing unnecessary radiated noise. It is not directly involved in improving Eye-pattern opening. Example components used for USB High-speed are listed below. Note that components should preferably be installed linearly with respect to the signal line to ensure signal quality.

- Panasonic EXC24CE900U
- Murata DLW21SN900SQ2

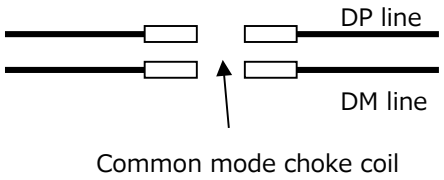


Figure 7.2.2.1 Typical common mode choke coil wiring

- Chip varistor

Use on the DP/DM signal line can be effective in protecting the S2R72A21's DP/DM pins from static electricity and surges. Typical components used for USB High-speed are listed below. Note that components should preferably be installed with shortest possible branches from the signal line to ensure signal quality. The chip varistor mounting position is generally considered more effective in the vicinity of the connectors, but this should be determined after consulting with the respective manufacturers.

- TDK AVR series
- Panasonic EZJZ series

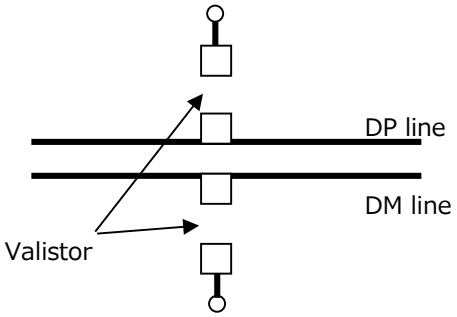


Figure 7.2.2.2 Typical varistor wiring

- Connector

The DP/DM signal quality may deteriorate if a non-USB certified connector is used. It is recommended that USB-certified connectors be used. The same applies to the cables used.

- Connection example of additional components

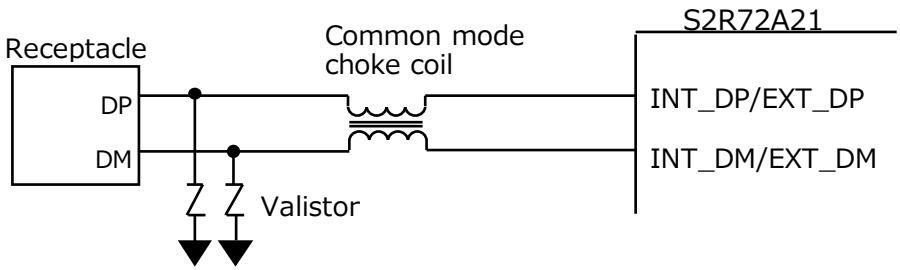


Figure 7.2.2.3 Connection example of additional components

Remarks :

In case when you add some capacity components such as Chip varistor and etc. on the DP/DM signal line, the rising / falling (Tr/Tf) characteristic of the USB HS transmit waveform would be rather gentle. If the capacity component is large, there would be a possibility that the USB compliance test (Tr/Tf characteristics, eye pattern test and etc.) would fail. So please take care of selecting the components.

7.3 Oscillator circuit

Please connect the Crystal oscillator (24MHz) as following. Epson recommends the frequency accuracy within ±100ppm in order to realize a high quality waveform.

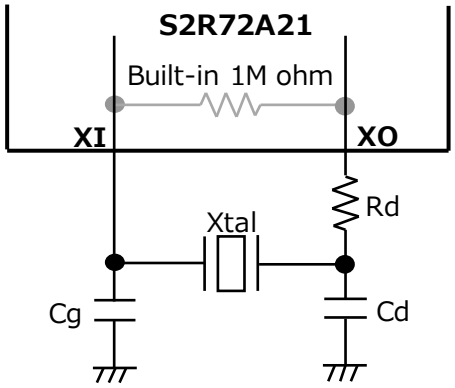


Figure 7.3.1 Typical crystal oscillator connection circuit

Recommended part (Automotive quality): FA-238A (CL=7pF) by Seiko Epson Corp.

Regarding the amount of Cg, Cd and Rd, please decide by evaluating the matching based on the actual boards. For your reference, Epson's evaluation board's constants are Cg=6[pF], Cd=7[pF], Rd=0[Ω]

7.4 Others precautions

- Resistance connected to the R1 pin

A 6.04 kΩ ±1% resistance should be positioned as close as possible to the R1 pin. This is used to generate the standard reference current which determines the USB analog circuit characteristics, so the analog characteristics will be affected if the tolerances are overly large. A resistance with the specified accuracy must always be used.

- FVDD pin, LVDDC pin, LVDDM pin

Each of these 3 pins needs 0.1uF and 10uF capacitors to be placed between the VSS. These capacitors should be mounted as close as possible to these pins in order of 0.1uF and 10uF from pin.

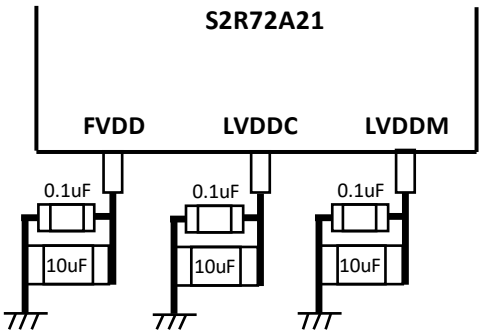


Figure 7.4.1 FVDD pin, LVDDC pin, LVDDM pin (Placement of capacitor)

- HVDD pins

Epson recommends placing the Bypass capacitors as close as possible to each HVDD pin. The capacitance amount on Epson's evaluation board is as following, but it would vary depending on the regulator's characteristics. Epson also recommends this to be assembled towards each power supply pin to ensure a stable IC's operation.

Each HVDD pin: 0.1uF
Power supply source: 10uF

- VSS pins

The VSS pins must be connected to a non-separated GND plane via low impedance.

Revision History

Attachment-1

Rev. No.	Date	Section	Category	Contents
Rev. 1.00	9/12/2020	All	New	New issue

EPSON

International Sales Operations

America

Epson America, Inc.

Headquarter:
3131 Katella Ave., Los Alamitos, CA 90720, USA
Phone: +1-562-290-4677

San Jose Office:
214 Devcon Drive
San Jose, CA 95112 USA
Phone: +1-800-228-3964 or +1-408-922-0200

Europe

Epson Europe Electronics GmbH
Riesstrasse 15, 80992 Munich,
Germany
Phone: +49-89-14005-0 FAX: +49-89-14005-110

Asia

Epson (China) Co., Ltd.
4th Floor, Tower 1 of China Central Place, 81 Jianguo Road, Chaoyang District, Beijing 100025 China
Phone: +86-10-8522-1199 FAX: +86-10-8522-1120

Shanghai Branch
Room 1701 & 1704, 17 Floor, Greenland Center II,
562 Dong An Road, Xu Hui District, Shanghai, China
Phone: +86-21-5330-4888 FAX: +86-21-5423-4677

Shenzhen Branch
Room 804-805, 8 Floor, Tower 2, Ali Center,No.3331
Keyuan South RD(Shenzhen bay), Nanshan District, Shenzhen 518054, China
Phone: +86-10-3299-0588 FAX: +86-10-3299-0560

Epson Taiwan Technology & Trading Ltd.
15F, No.100, Songren Rd, Sinyi Dist, Taipei City 110. Taiwan
Phone: +886-2-8786-6688

Epson Singapore Pte., Ltd.
438B Alexandra Road,
Block B Alexandra TechnoPark, #04-01/04, Singapore 119968
Phone: +65-6586-5500 FAX: +65-6271-7066

Seiko Epson Corp.
Korea Office
10F Posco Tower Yeoksam, Teheranro 134 Gangnam-gu,
Seoul, 06235, Korea
Phone: +82-2-3420-6695

Seiko Epson Corp.
Sales & Marketing Division

Device Sales & Marketing Department
29th Floor, JR Shinjuku Miraina Tower, 4-1-6 Shinjuku,
Shinjuku-ku, Tokyo 160-8801, Japan

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