

S1C31W65_(rev.1.1)

32-bit Single Chip Microcontroller Arm[®] 32-bit RISC CPU core Cortex[®]-M0+ Embedded 56SEG x 4COM / 52SEG x 8COM LCD driver

- Various interfaces such as UART and I2C that support DMA transfer •
- Operating temperature range up to +105°C



DESCRIPTIONS

The S1C31W65 is a 32-bit MCU with an Arm[®] Cortex[®]-M0+ processor included that features low-power operation. It incorporates an LCD driver capable of driving up to a 416 segments LCD panel, a low-power RTC, and a lot of serial interface circuits. The S1C31W65 is suitable for various kinds of control devices that require LCD display and time measurement.

FEATURES

Model		S1C31W65				
CPU						
CPU core		Arm [®] 32-bit RISC CPU core Cortex [®] -M0+				
Other		Serial wire debug ports (SW-DP) and a micro trace buffer (MTB) included				
Embedded Flash memo	ry					
Capacity		128K bytes (for both instructions and data)				
Erase/program count		1,000 times(min.) * When being programmed by the dedicated flash loader				
Other		On-board programming function				
		Flash programming voltage can be generated internally.				
Embedded RAMs						
General-purpose RAM		16K bytes (shared with MTB)				
Display RAM		112 bytes				
Instruction cache		512 bytes				
DMA controller (DMAC)						
Number of channels		4 channels				
Data transfer path		Memory to memory, memory to peripheral, and peripheral to memory				
Transfer mode		Basic, ping-pong, scatter-gather				
DMA trigger source		UART3, SPIA, I2C, T16B, SNDA, ADC12A, and software				
Clock generator (CLG)						
System clock source		4 sources (IOSC/ OSC1/OSC3/EXOSC)				
System clock frequer	ncy (operating	VD1 voltage mode = mode0: 33 MHz(max.)				
frequency)		VD1 voltage mode = mode1: 2.16 MHz(max.)				
IOSC oscillator circuit (bo	ot clock source)	VD1 voltage mode = mode0: 32/24/16/12/8/2/1 MHz(typ.) software selectable				
		embedded oscillator.				
		VD1 voltage mode = mode1: 2/1 MHz(typ.) software selectable				
		2 μs(max.) starting time (time from cancelation of SLEEP state to vector table read by the CPU when the system clock is 32MHz)				
OSC1 oscillator circuit		32.768 kHz(typ.) crystal oscillator				
		32 kHz(typ.) embedded oscillator				
		Oscillation stop detection circuit included				
OSC3 oscillator circuit		33 MHz(max.) crystal/ceramic oscillator				
		32/24/16/12/8 MHz(typ) software selectable				
EXOSC clock input		33 MHz(max.) square or sign wave input				
Other		Configurable system clock division ratio				
		Configurable system clock used at wake up from SLEEP state				
		Operating clock frequency for the CPU and all peripheral circuit is selectable				
I/O port (PPORT)						
Number of general-purp	ose I/O port	63bit (max.)				
I/O ports	Output	1bit				
	port					
Other		Pins are shared with the peripheral I/O.				
Input interrupt Number of		56bit (max.)				
interrupt ports						
		Rising edge interrupts and falling edge interrupts can be enabled individually.				
Number of ports that support universal port		32bit				
multiplexer (UPMUX)		A peripheral circuit I/O function selected via software can be assigned to each port.				

Model	S1C31W65
Timers	
Watchdog timer (WDT2)	Generates NMI or watchdog time reset
	Programmable NMI/reset generation cycle
Real-time-clock (RTCA)	128 – 1Hz counter, second/minute/hour/day/day of the week/monthly/year counters
	Theoretical regulation function for 1-second correction
	Alarm and stopwatch function
16-bit timer (T16)	8 channels
	Generates the SPIA master clock, and the ADC12A operating clock/trigger signal.
16-bit PWM timer (T16B)	3 channels
	Event counter/capture function
	PWM waveform generation function
	Number of PWM output or capture input ports: 4 ports/channel
Supply voltage detector (SVD4)	
Number of channels	1 channel
Detection voltage	V_{DD} or an external voltage (2 external voltage input ports are embedded, so the
	voltage level higher than V_{DD} can be detected.)
	V_{DD} : 32 levels (1.7 to 5.0 V) / external voltage: 32 levels (1.7 to 5.0 V)
Other	Intermittent operation mode
	Generates an interrupt or reset according to the detection level evaluation
UART (UART3)	
	Baud-rate generator included, IdDA1.0 supported
	Open drain output, signal polarity, and baud-rate division ratio are configurable.
Our character and interface (ODIA)	Intrared communication carrier modulation output function
Synchronous serial interface (SPIA)	2 channels
	2 to 16-bit variable data length
	I he 16-bit timer(116) can be used for the baud-rate generator in master mode.
120 (120)	2 channels
Occurred memory (ONIDA)	Baud-rate generator included
Sound generator (SNDA)	512 Hz to 16 kHz output froquonoioo
Buzzer output function	Dre shet sutruit function
Moledy generation function	Ditch: 128 Hz to 16 kHz \sim C3 to C6
	Pitoli. 120 Hz to 10 Ki IZ ~ C3 to C0
	Tempo: 16 tempos (30 to 480)
	Tie/slur may be specified
12-bit A/D converter (ADC12A)	
Conversion method	Successive approximation type
Resolution	12 hits
Number of conversion channels	1 channel
Number of analog signal inputs	8 norts/channel (The temperature sensor output is connected to a port.)
Temperature sensor/reference voltage of	enerator (TSRVR)
Temperature sensor circuit	Sensor output can be measured using ADC12A
Reference voltage generator	Reference voltage for ADC12A is selectable from 2.0V, 2.5V, VDD, and external
LCD driver (LCD8D)	
LCD output	52SEG x 5~8COM (max.), 56SEG x 1~4COM (max.)
LCD contrast	32 levels
LCD drive waveform	2 types (Waveform A. Waveform B) selectable
Other	1/3 or 1/2 bias power supply with voltage booster included, external voltage can be
	applied.
R/F converter (RFC)	
Conversion method	CR oscillation type 24-bit counters
Number of conversion channels	1 channel (Up to two sensors can be connected.)
Supported sensors	DC bias resistive sensors
Reset	
#RESET pin	Reset when the reset pin is set to low. (can be enabled/disabled using a register.)
Power-on reset	Reset at power on
Brown-out reset	Reset when the power supply voltage drops.
Key entry reset	Reset when the P00 to P01/02/03 keys are pressed simultaneously (can be
	enabled/disabled using a register.)

Model	S1C31W65
Watchdog timer reset	Reset when the watchdog timer overflows (can be enabled/disabled using a
	register.)
Supply voltage detector reset	Reset when the supply voltage detector detects the set voltage level (can be
	enabled/disabled using a register.)
Interrupt	
Non-maskable interrupt	6 systems (Reset, NMI, HardFault, SVCall, PendSV, SysTick)
Programmable interrupt	External interrupt: 1 system
	Internal interrupt: 26 systems
Power supply voltage	
V _{DD} operating voltage	1.8~5.5 V
V _{DD} operating voltage for Flash	2.2~5.5 V
programming	
VDD operating voltage when LCD driver	1.8~5.5 V
is used	
Operating temperature	
Operating temperature range	-40~105°C
Operating temperature range for Flash	-40~85°C
programming	
Current consumption (Typ. Value)	
SLEEP mode ^{*2}	0.3 µA
	IOSC = OFF, OSC1 = OFF, OSC3=OFF
	0.8 µA
	IOSC = OFF, OSC1 = 32.768 kHz (crystal oscillator), OSC3 = OFF, RTCA = ON
HALT mode ^{*3}	1.5 µA
	OSC1 = 32.768 kHz (crystal oscillator)
	4.0 μΑ
	OSC1 = 32.768 kHz (crystal oscillator), LCD=ON (No panel load)
RUN mode	195 µA/MHz
	VD1 voltage mode = mode0, CPU = IOSC
	130 µA/MHz
	VD1 voltage mode = mode1, CPU = IOSC
Shipping form	
1 *4	TOEP15-100PIN(P-TOEP100-1414-0.50, 14 x 14 mm, $t = 1.2$ mm, 0.5 mm pitch)

*1 The input filter in I2C (SDA and SCL inputs) does not comply with the standard for removing noise spikes less than 50 ns. *2 SLEEP mode refers to deep sleep mode in the Cortex®-M0+ processor. The RAM retains data even in SLEEP mode. *3 HALT mode refers to sleep mode in the Cortex®-M0+ processor.

*4 Shown in parentheses is a JEITA package name.

Block Diagram



Pin Configuration Diagram

TQFP15-100PIN



Pin Descriptions

Symbol meanings

Assigned signal: The signal listed at the top of each pin is assigned in the initial state. The pin function must be switched via software to assign another signal.

	= Input
0	= Output
I/O	= Input/output
Р	= Power supply
А	= Analog signal
Hi-Z	= High impedance state
l (Pull-up)	= Input with pulled up
I (Pull-down)	= Input with pulled down
Hi-Z	= High impedance state
O (H)	= High level output
0 (L)	= Low level output
fe structure:	
\checkmark	= Over voltage tolerant fail-s
	I O I/O P A Hi-Z I (Pull-up) I (Pull-down) Hi-Z O (H) O (L) Te structure: √

= Over voltage tolerant fail-safe type I/O cell included.

Pin name	Assigned signal	ı/o	Initial state	Tolerant fail-safe structure	Function
VDD	VDD	Р	-		Power supply (+)
VSS	VSS	Р	-		GND
VD1	VD1	Α	-		VD1 regulator output
VC1-3	VC1-3	Р	-		LCD panel drive power supply
OSC1	OSC1	Α	-		OSC1 oscillator circuit input
OSC2	OSC2	Α	-		OSC1oscillator circuit output
#RESET	#RESET	I	l(Pull-up)		Reset input
P00	P00	I/O	Hi-Z	\checkmark	I/O port
	SDI1	I			Synchronous serial interface Ch.1 data input
	UPMUX	I/O			User-selected I/O(universal port multiplexer)
P01	P01	I/O	Hi-Z	\checkmark	I/O port
	SDO1	0			Synchronous serial interface Ch.1 data output
	UPMUX	I/O			User-selected I/O(universal port multiplexer)
P02	P02	I/O	Hi-Z	\checkmark	I/O port
	SPICLK1	I/O			Synchronous serial interface Ch.1 clock input/output
	UPMUX	I/O			User-selected I/O(universal port multiplexer)
P03	P03	I/O	Hi-Z	\checkmark	I/O port
	#SPISS1	I			Synchronous serial interface Ch.1 slave select input
	UPMUX	I/O			User-selected I/O(universal port multiplexer)
P04	P04	I/O	Hi-Z	\checkmark	I/O port
	SENB0	Α	1		R/F converter Ch.0 sensor B oscillator pin
	UPMUX	I/O			User-selected I/O(universal port multiplexer)

P05	P05	I/O	Hi-Z	\checkmark	I/O port
	SENA0	А			R/F converter Ch.0 sensor A oscillator pin
	UPMUX	I/O			User-selected I/O(universal port multiplexer)
P06	P06	I/O	Hi-Z	\checkmark	I/O port
	REFO	Α			R/F converter Ch.0 reference oscillator pin
	UPMUX	I/0			User-selected I/O(universal port multiplexer)
P07	P07	I/O	Hi-Z	-	I/O port
	RFINO	Α	-		R/F converter Ch.0 oscillation input
	UPMUX	I/O			User-selected I/O(universal port multiplexer)
P10	P10	I/O	Hi-Z	-	I/O port
	UPMUX	I/O			User-selected I/O(universal port multiplexer)
	ADIN06	Α			12-bit A/D converter Ch.0 analog signal input 6
P11	P11	I/O	Hi-Z	-	I/O port
	UPMUX	I/0			User-selected I/O(universal port multiplexer)
	ADIN05	Α			12-bit A/D converter Ch.0 analog signal input 5
P12	P12	I/O	Hi-Z	-	I/O port
	UPMUX	I	-		User-selected I/O(universal port multiplexer)
	ADIN04	A	-		12-bit A/D converter Ch.0 analog signal input 4
P13	P13	I/O	Hi-Z	-	I/O port
	UPMUX	I/O	-		User-selected I/O(universal port multiplexer)
	ADIN03	Α	-		12-bit A/D converter Ch.0 analog signal input 3
P14	P14	I/O	Hi-Z	-	I/O port
	UPMUX	I/O	-		User-selected I/O(universal port multiplexer)
	ADIN02	Α	-		12-bit A/D converter Ch.0 analog signal input 2
P15	P15	I/O	Hi-Z	-	I/O port
	EXCL00	I	-		16-bit PWM timer Ch.0 event counter input 0
	UPMUX	0	-		User-selected I/O(universal port multiplexer)
	ADIN01	Α	-		12-bit A/D converter Ch.0 analog signal input 1
P16	P16	I/O	Hi-Z	-	I/O port
	EXCL10	I	-		16-bit PWM timer Ch.1 event counter input 0
	UPMUX	0	-		User-selected I/O(universal port multiplexer)
	ADIN00	Α	-		12-bit A/D converter Ch.0 analog signal input 0
P17	P17	I/O	Hi-Z	-	I/O port
	UPMUX	I/O	-		User-selected I/O(universal port multiplexer)
	VREFA0	Α	-		12-bit A/D converter Ch.0 reference voltage input
P20	P20	I/O	Hi-Z	\checkmark	I/O port
	BZOUT	0	-		Sound generator output
	UPMUX	I/O	-		User-selected I/O(universal port multiplexer)
P21	P21	I/O	Hi-Z	\checkmark	I/O port
	#BZOUT	0			Sound generator inverted output
	UPMUX	I/O	-		User-selected I/O(universal port multiplexer)
P22	P22	I/O	Hi-Z	\checkmark	I/O port
	REMO	0	-		IR remote controller transmit data output
	UPMUX	I/O	-		User-selected I/O(universal port multiplexer)

P23	P23	I/0	Hi-Z	\checkmark	I/O port
	CLPS	0	-		IR remote controller clear pulse output
	UPMUX	I/O	-		User-selected I/O(universal port multiplexer)
P24	P24	I/O	Hi-Z	\checkmark	I/O port
	EXCL20	I/O	-		16-bit PWM timer Ch.2 event counter input 0
	UPMUX	I/O	-		User-selected I/O(universal port multiplexer)
P25	P25	I/O	Hi-Z	\checkmark	I/O port
	EXCL01	I	-		16-bit PWM timer Ch.0 event counter input 1
	UPMUX	I/O	-		User-selected I/O(universal port multiplexer)
	SEG55	Α	-		LCD segment output
P26	P26	I/O	Hi-Z	\checkmark	I/O port
	EXCL11	I			16-bit PWM timer Ch.1 event counter input 1
	UPMUX	I/O			User-selected I/O(universal port multiplexer)
	SEG54	Α			LCD segment output
P27	P27	I/O	Hi-Z	\checkmark	I/O port
	EXCL21	I			16-bit PWM timer Ch.2 event counter input 1
	UPMUX	I/O			User-selected I/O(universal port multiplexer)
	SEG53	Α			LCDs segment output
P30	P30	I/O	Hi-Z	\checkmark	I/O port
	EXOSC	1			Clock generator external clock input
	UPMUX	I/O			User-selected I/O(universal port multiplexer)
	SEG47	А			LCD segment output
P31	P31	I/O	Hi-Z	\checkmark	I/O port
	#ADTRG0	I			12-bit A/D converter Ch.0 trigger input
	UPMUX	I/O			User-selected I/O(universal port multiplexer)
	SEG46	А	-		LCD segment output
P32	P32	I/O	Hi-Z	\checkmark	I/O port
	RTC1S	0			Real-time clock 1-second cycle pulse output
	UPMUX	I/O			User-selected I/O(universal port multiplexer)
	SEG45	А			LCD segment output
P33	P33	I/O	Hi-Z	\checkmark	I/O port
	FOUT	0			Clock external output
	UPMUX	I/O			User-selected I/O(universal port multiplexer)
	SEG44	А			LCD segment output
P34	P34	I/O	Hi-Z	\checkmark	I/O port
	LFRO	0			LCD frame signal monitor output
	UPMUX	I/O			User-selected I/O(universal port multiplexer)
	SEG43	А			LCD segment output
P35	P35	I/O	Hi-Z	\checkmark	I/O port
	UPMUX	I/O			User-selected I/O(universal port multiplexer)
	EXSVD00	A			Supply voltage detector CH.0 external voltage detection input 0
	SEG42	Α	1		LCD segment output

P36	P36	I/0	Hi-Z	\checkmark	I/O port
	UPMUX	I/O			User-selected I/O(universal port multiplexer)
	EXSVD01	A	-		Supply voltage detector CH.0 external voltage detection input 1
	SEG41	А			LCD segment output
P37	P37	I/0	Hi-Z	\checkmark	I/O port
	RFCLKO0	0			R/F converter Ch.0 clock monitor output
	UPMUX	I/0			User-selected I/O(universal port multiplexer)
	SEG40	А			LCD segment output
P40	P40	I/O	Hi-Z	\checkmark	I/O port
	SEG39	А			LCD segment output
P41	P41	I/O	Hi-Z	\checkmark	I/O port
	SEG38	Α			LCD segment output
P42	P42	I/O	Hi-Z	\checkmark	I/O port
	SEG37	Α			LCD segment output
P43	P43	I/O	Hi-Z	\checkmark	I/O port
	SEG36	А			LCD segment output
P44	P44	I/0	Hi-Z	\checkmark	I/O port
	SEG35	А			LCD segment output
P45	P45	I/O	Hi-Z	\checkmark	I/O port
	SEG34	А			LCD segment output
P46	P46	I/O	Hi-Z	\checkmark	I/O port
	SEG33	Α			LCD segment output
P47	P47	I/0	Hi-Z	\checkmark	I/O port
	SEG32	А			LCD segment output
P50	P50	I/O	Hi-Z	\checkmark	I/O port
	SEG24	А			LCD segment output
P51	P51	I/0	Hi-Z	\checkmark	I/O port
	SEG23	А			LCD segment output
P52	P52	I/0	Hi-Z	\checkmark	I/O port
	SEG22	А			LCD segment output
P53	P53	I/0	Hi-Z	\checkmark	I/O port
	SEG21	А			LCD segment output
P54	P54	I/0	Hi-Z	\checkmark	I/O port
	SEG20	А			LCD segment output
P55	P55	I/O	Hi-Z	\checkmark	I/O port
	SEG19	А			LCD segment output
P56	P56	I/0	Hi-Z	\checkmark	I/O port
	SEG18	Α			LCD segment output
P57	P57	I/O	Hi-Z	\checkmark	I/O port
	SEG17	Α			LCD segment output
P60	P60	I/O	Hi-Z	\checkmark	I/O port
	SEG16	А	1		LCD segment output
P61	P61	I/O	Hi-Z	\checkmark	I/O port
	SEG15	А			LCD segment output

P62	P62	I/O	Hi-Z	\checkmark	I/O port
	SEG14	Α			LCD segment output
P63	P63	I/O	Hi-Z	\checkmark	I/O port
	SEG13	Α			LCD segment output
P64	P64	I/O	Hi-Z	\checkmark	I/O port
	COM7	А			LCD common output
	SEG3	А			LCD segment output
P65	P65	I/O	Hi-Z	\checkmark	I/O port
	COM6	Α			LCD common output
	SEG2	Α			LCD segment output
P66	P66	I/O	Hi-Z	\checkmark	I/O port
	COM5	Α			LCD common output
	SEG1	Α			LCD segment output
P67	P67	I/O	Hi-Z	\checkmark	I/O port
	COM4	Α			LCD common output
	SEG0	Α			LCD segment output
PD0	SWCLK	I	l (pull-up)	\checkmark	Serial wire debug clock input
	PD0	I/O			I/O port
PD1	SWD	I/O	l (pull-up)	\checkmark	Serial wire debug data input/output
	PD1	I/O			I/O port
PD2	PD2	I/O	Hi-Z	-	I/O port
	OSC3	Α			OSC3 oscillator circuit input
PD3	PD3	I/O	Hi-Z	-	I/O port
	OSC4	Α			OSC3 oscillator circuit output
PD4	PD4	I/O	O(L)	-	Output port
PD5	VPP	Р	Hi-Z	\checkmark	Power supply for Flash programming
	PD5	I/O			I/O port
PD6	PD6	I/O	Hi-Z	-	I/O port
	CP1	Α			LCD power supply booster capacitor connect pins
PD7	PD7	I/O	Hi-Z	-	I/O port
	CP2	Α			LCD power supply booster capacitor connect pins
COM0-3	COM0-3	A	Hi-Z	-	LCD common outputs
SEG4-12, 25-31,48-52	SEG4-12, 25-31,48-52	A	Hi-Z	-	LCD segment outputs

Universal port multiplexer (UPMUX) The universal port multiplexer (UPMUX) allows software to select the peripheral circuit input/output function to be assigned to each pin from those listed below. However, it is not allowed to assign a function to two or more pins simultaneously.

Peripheral circuit	Signal to be assigned	I/O	Channel number n	Function
Synchronous serial	SDIn	I	n=0	SPIA ch.n data input
Interface	SDOn	0		SPIA ch.n data output
(SPIA)	SPICLKn	I/O		SPIA Ch.n clock input/output
	#SPISSn	Ι		SPIA Ch.n clave-select input
12C	SCLn	I/O	n=0,1	I2C Ch.n clock input/output
(I2C)	SDAn	I/O		I2C Ch.n data input/output
UART	USINn	Ι	n=0,1	UART Ch,n data input
(UART3)	USOUTn	0		UART Ch,n data output
16-bitPWM	TOUTn0/CAPn0	I/O	n=0,1,2	16-bit PWM timer Ch.n PWM output/capture input 0
timer(T16B)	TOUTn1/CAPn1	I/O		16-bit PWM timer Ch.n PWM output/capture input 1
	TOUTn2/CAPn2	I/O		16-bit PWM timer Ch.n PWM output/capture input 2
	TOUTn3/CAPn3	I/O		16-bit PWM timer Ch.n PWM output/capture input 3

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[Examples of Particular Purpose]

Space equipment (artificial satellites, rockets, etc.) /

Transportation vehicles and their control equipment (automobiles, aircraft, trains, ships, etc.) /

Medical equipment / Relay equipment to be placed on ocean floor /

Power station control equipment / Disaster or crime prevention equipment / Traffic control equipment / Financial equipment Other applications requiring similar levels of reliability as those listed above. Please be sure to contact our sales representative for details of the other applications.

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