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CMOS 16-BIT SINGLE CHIP MICROCONTROLLER

S1C17F63
Technical Manual

SEIKO EPSON CORPORATION

Rev. 1.1

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Preface

This is a technical manual for designers and programmers who develop a product using the S1C17F63. This document describes the functions of the IC, embedded peripheral circuit operations, and their control methods.

For the CPU functions and instructions, refer to the "S1C17 Family S1C17 Core Manual." For the functions and operations of the debugging tools, refer to the respective tool manuals. (Our "Products: Document Downloads" website provides the downloadable manuals.)

Notational conventions and symbols in this manual

Register address

Peripheral circuit chapters do not provide control register addresses. Refer to "Peripheral Circuit Area" in the "Memory and Bus" chapter or "List of Peripheral Circuit Control Registers" in the Appendix.

Register and control bit names

In this manual, the register and control bit names are described as shown below to distinguish from signal and pin names.

XXX register: Represents a register including its all bits.
XXX.YYY bit: Represents the one control bit YYY in the XXX register.
XXX.ZZZ[1:0] bits: Represents the two control bits ZZZ1 and ZZZ0 in the XXX register.

Register table contents and symbols

Initial: Value set at initialization

Reset: Initialization condition. The initialization condition depends on the reset group (H0, H1, or S0). For more information on the reset groups, refer to "Initialization Conditions (Reset Groups)" in the "Power Supply, Reset, and Clocks" chapter.

R/W: R = Read only bit
W = Write only bit
WP = Write only bit with a write protection using the MSCPROT.PROT[15:0] bits
R/W = Read/write bit
R/WP = Read/write bit with a write protection using the MSCPROT.PROT[15:0] bits

Control bit read/write values

This manual describes control bit values in a hexadecimal notation except for one-bit values (and except when decimal or binary notation is required in terms of explanation). The values are described as shown below according to the control bit width.

1 bit: 0 or 1
2 to 4 bits: 0x0 to 0xf
5 to 8 bits: 0x00 to 0xff
9 to 12 bits: 0x000 to 0xfff
13 to 16 bits: 0x0000 to 0xffff

Decimal: 0 to 9999...
Binary: 0b0000... to 0b1111...

Channel number

Multiple channels may be implemented in some peripheral circuits (e.g., 16-bit timer, etc.). The peripheral circuit chapters use '*n*' as the value that represents the channel number in the register and pin names regardless of the number of channel actually implemented. Normally, the descriptions are applied to all channels. If there is a channel that has different functions from others, the channel number is specified clearly.

Example) T16_*n*CTL register of the 16-bit timer
If one channel is implemented (Ch.0 only): T16_*n*CTL = T16_0CTL only
If two channels are implemented (Ch.0 and Ch.1): T16_*n*CTL = T16_0CTL and T16_1CTL

For the number of channels implemented in the peripheral circuits of this IC, refer to "Features" in the "Overview" chapter.

– Contents –

1 Overview

The S1C17F63 is a 16-bit MCU that features low power consumption. It includes various serial interfaces, an EPD controller/driver, a temperature sensor, an A/D converter, and various timers as well as a high-performance 16-bit CPU. It is suitable for battery-driven applications that require an EPD display and a temperature measurement function. The S1C17F63 has not only a Flash memory but also an EEPROM that can be reprogrammed from an application software.

1.1 Features

Table 1.1.1 Features

Model		S1C17F63
CPU		
CPU core		Seiko Epson original 16-bit RISC CPU core S1C17
Other		On-chip debugger
Embedded Flash memory		
Capacity		32K bytes (for both instructions and data)
Erase/program count		1,000 times (min.) * Programming by the debugging tool ICDmini
Other		Security function to protect from reading/programming by ICDmini
		On-board programming function using ICDmini
		Flash programming voltage can be generated internally.
Embedded EEPROM		
Capacity		256 bytes
Erase/program count		100,000 times (min.)
Embedded RAM		
Capacity		2K bytes
Clock generator (CLG)		
System clock source		4 sources (IOSC/RTCLP(OSC1)/OSC3/EXOSC)
System clock frequency (operating frequency)		16.8 MHz (max.)
IOSC oscillator circuit (boot clock source)		700 kHz (typ.) embedded oscillator
		23 µs (max.) starting time (time from cancelation of SLEEP state to vector table read by the CPU)
		Auto-trimming function for the embedded oscillator
RTCLP clock (OSC1 oscillator circuit)		Clock output from the RTCLP 32.768 kHz (typ.) crystal oscillator
		Can be used as the OSC1 clock in the MCU core block.
OSC3 oscillator circuit		16, 12, 8, 4, 2, 1, and 0.5 MHz-switchable embedded oscillator
EXOSC clock input		16.8 MHz (max.) square or sine wave input
Other		Configurable system clock division ratio
		Clock external outputs: 2 channels
		Configurable system clock used at wake up from SLEEP state
		Operating clock frequency for the CPU and all peripheral circuits is selectable.
I/O port (PPORT)		
Number of general-purpose ports	I/O port	17 bits (MCU core block) (max.)
	Other	Pins are shared with the peripheral I/O.
Number of input interrupt ports		14 bits (MCU core block) (max.)
Number of ports that support universal port multiplexer (UPMUX)		14 bits
		A peripheral circuit I/O function selected via software can be assigned to each port.
Timers		
Watchdog timer (WDT2)		Generates NMI or watchdog timer reset.
		Programmable NMI/reset generation cycle
16-bit timer (T16)		4 channels
		Generates the SPIA master clocks and the ADC12A trigger signal.
16-bit PWM timer (T16B)		2 channels
		Event counter/capture function
		PWM waveform generation function
		Number of PWM output or capture input ports: 2 ports/channel
Supply voltage detector (SVD3)		
Detection voltage		V_{DD} or external voltage (one external voltage input port is provided and an external voltage level can be detected even if it exceeds V_{DD}.)
Detection level		V_{DD}: 28 levels (1.8 to 5.0 V)/external voltage: 32 levels (1.2 to 5.0 V)
Other		Intermittent operation mode
		Generates an interrupt or reset according to the detection level evaluation.

Model		S1C17F63
Serial interfaces		
UART (UART3)		1 channel
		Baud-rate generator included, IrDA1.0 supported
		Open drain output, signal polarity, and baud rate division ratio are configurable.
		Infrared communication carrier modulation output function
Synchronous serial interface (SPIA)		2 channels * Ch.0 is also used as the interface with the RTCLP block.
		2 to 16-bit variable data length
		The 16-bit timer (T16) can be used for the baud-rate generator in master mode.
I²C (I2C) *1		1 channel
		Baud-rate generator included
Smart card interface (SMCIF)		1 channel
		Baud-rate generator included
Sound generator (SNDA)		
Buzzer output function		512 Hz to 16 kHz output frequencies
		One-shot output function
Melody generation function		Pitch: 128 Hz to 16 kHz ≈ C3 to C6
		Duration: 7 notes/rests (Half note/rest to thirty-second note/rest)
		Tempo: 16 tempos (30 to 480)
		Tie/slur may be specified.
12-bit A/D converter (ADC12A)		
Conversion method		Successive approximation type
Resolution		12 bits
Number of conversion channels		1 channel
Number of external analog signal inputs		7 ports
Number of internal analog signal inputs		1 port (The temperature sensor output is connected.)
Temperature sensor/reference voltage generator (TSRVR)		
Temperature sensor circuit		Sensor output can be measured using ADC12A.
Reference voltage generator		Reference voltage for ADC12A is selectable from 2.0 V, 2.5 V, V_{DD}, and external input.
EPD controller/driver (EPDC)		
Number of driver outputs	Segment output	42 outputs
	Top plane output	1 output
	Back plane output	1 output
Output voltage		48 levels
Other		Includes a drive power generator.
		Includes a display data memory.
		Output drive waveforms can be programmed.
		Supports pin output direct control.
		The segment, top plane, and back plane output pin assignments are selectable.
Independent low-power real-time clock (RTCLP)		
Interface		Register access via SPIA Ch.0.
OSC1 oscillator circuit		32.768 kHz (typ.) crystal oscillator
Oscillation stop detector		Issues a system reset when oscillation stop is detected.
Real-time clock		Second/minute/hour/day/day of the week/month/year counters
		Automatic leap year correction function
		Day/hour/minute/second, alarm, and programmable periodic timer interrupts
I/O ports (P20, P21)		GPIO: 2 bits (max.)
		Input interrupt generation function: 2 bits (max.)
		Pins are shared with the peripheral I/O.
Power management function		MCU power shut down and restart by interruption
Backup RAM function		RAM capacity: 128 bytes
Multiplier/divider (COPRO2)		
Arithmetic functions		16-bit × 16-bit multiplier
		16-bit × 16-bit + 32-bit multiply and accumulation unit
		32-bit ÷ 32-bit divider
Reset		
#RESET pin		Reset when the reset pin is set to low.
Power-on reset		Reset at power on.
Brownout reset		Reset when the power supply voltage drops.
Oscillation stop detection reset		Reset when stop of the OSC1 crystal oscillator is detected.
Key entry reset		Reset when the P00 to P01/P02/P03 keys are pressed simultaneously (can be enabled/disabled using a register).
Watchdog timer reset		Reset when the watchdog timer overflows (can be enabled/disabled using a register).

Model		S1C17F63
Supply voltage detector reset		Reset when the supply voltage detector detects the set voltage level (can be enabled/ disabled using a register).
Interrupt		
Non-maskable interrupt		4 systems (Reset, address misaligned interrupt, debug, NMI)
Programmable interrupt	External int.	1 system (8 levels)
	Internal int.	15 systems (8 levels)
Power supply voltage		
V_{DD} operating voltage		1.8 to 5.5 V
V_{DD} operating voltage for Flash programming		2.2 to 5.5 V (Programming voltage V_{PP}: 7.5 V external voltage or internal boosted voltage)
V_{DD} operating voltage for EEPROM programming		2.2 to 5.5 V (Programming voltage V_{PP}: internal boosted voltage)
Operating temperature		
Operating temperature range		-40 to 85°C
Current consumption (typ. value)		
RTC mode		0.11 µA OSC1 = 32,768 Hz, real-time clock = ON, MCU core = OFF
SLEEP mode *2		0.45 µA IOSC = OFF, OSC1 = 32,768 Hz, real-time clock = ON, OSC3 = OFF
HALT mode		0.70 µA IOSC = OFF, OSC1 = 32,768 Hz, real-time clock = ON, OSC3 = OFF
RUN mode		5 µA OSC1 = 32,768 Hz, real-time clock = ON, CPU = OSC1
		1,950 µA OSC3 = 16 MHz, OSC1 = 32,768 Hz, real-time clock = ON, CPU = OSC3 (Flash read: 3 cycles)
Shipping form		
1		Gold bump chip (Bump pitch: 85 µm (min.))
2		Aluminum pad chip (Pad pitch: 85 µm (min.))
3 *3		QFP15-100PIN (P-LQFP100-1414-0.50, 14 × 14 mm, t = 1.7 mm, 0.5 mm pitch)

*1 The input filter in I2C (SDA and SCL inputs) does not comply with the standard for removing noise spikes less than 50 ns.
*2 The RAM retains data even in SLEEP mode.
*3 Shown in parentheses is a JEITA package name.

1.2 Block Diagram

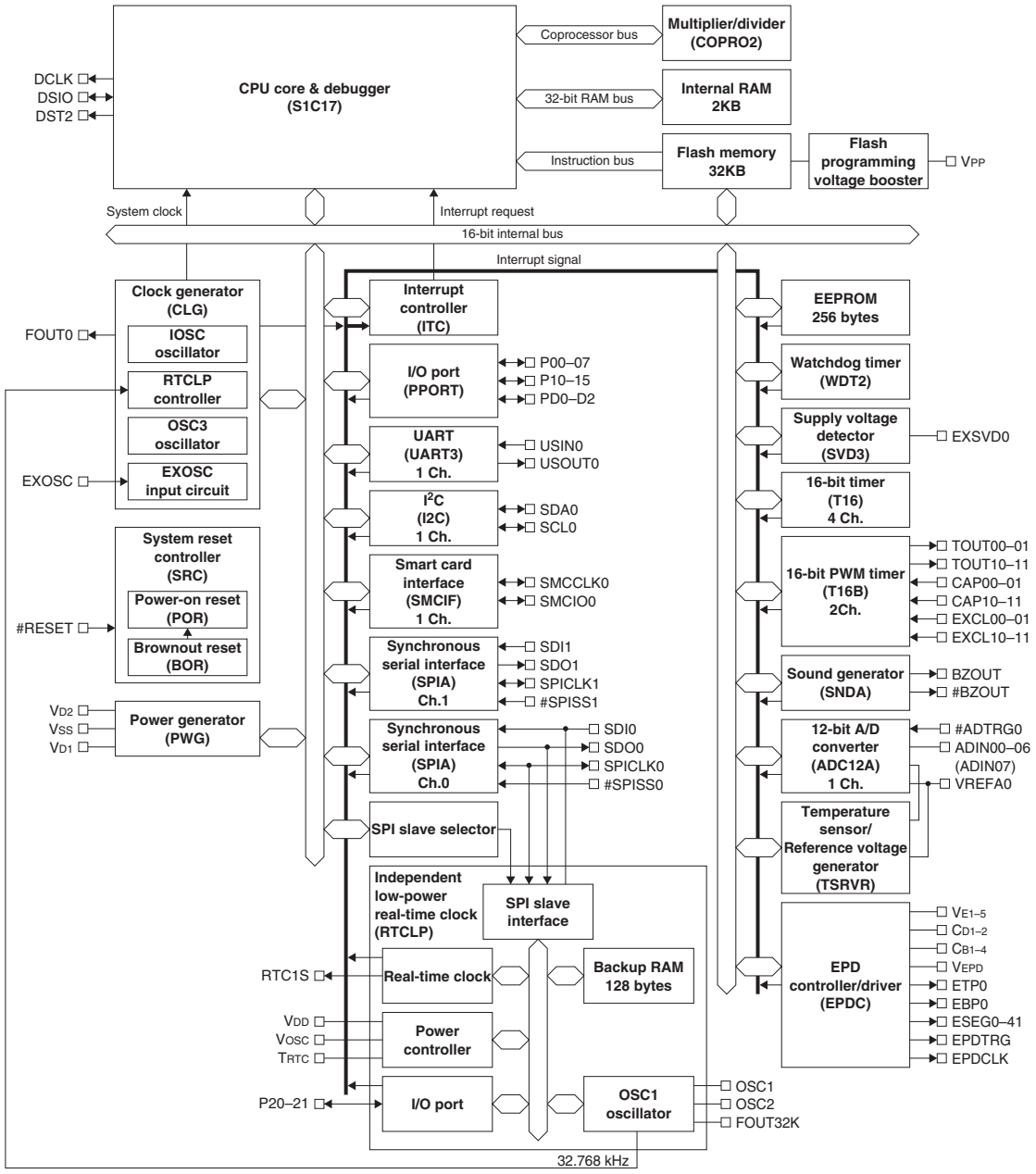


Figure 1.2.1 S1C17F63 Block Diagram

1.3 Pins

1.3.1 QFP15-100PIN

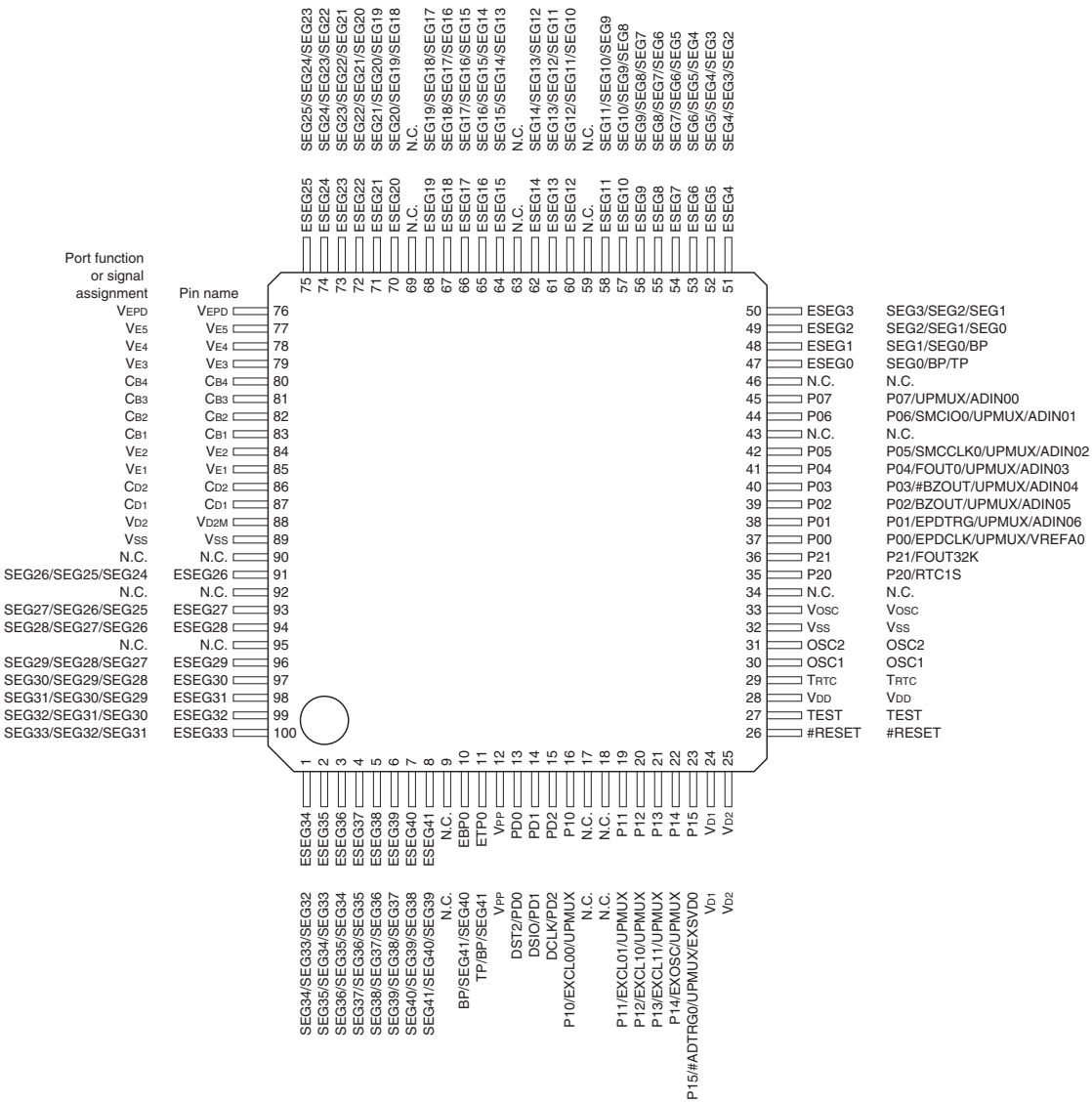
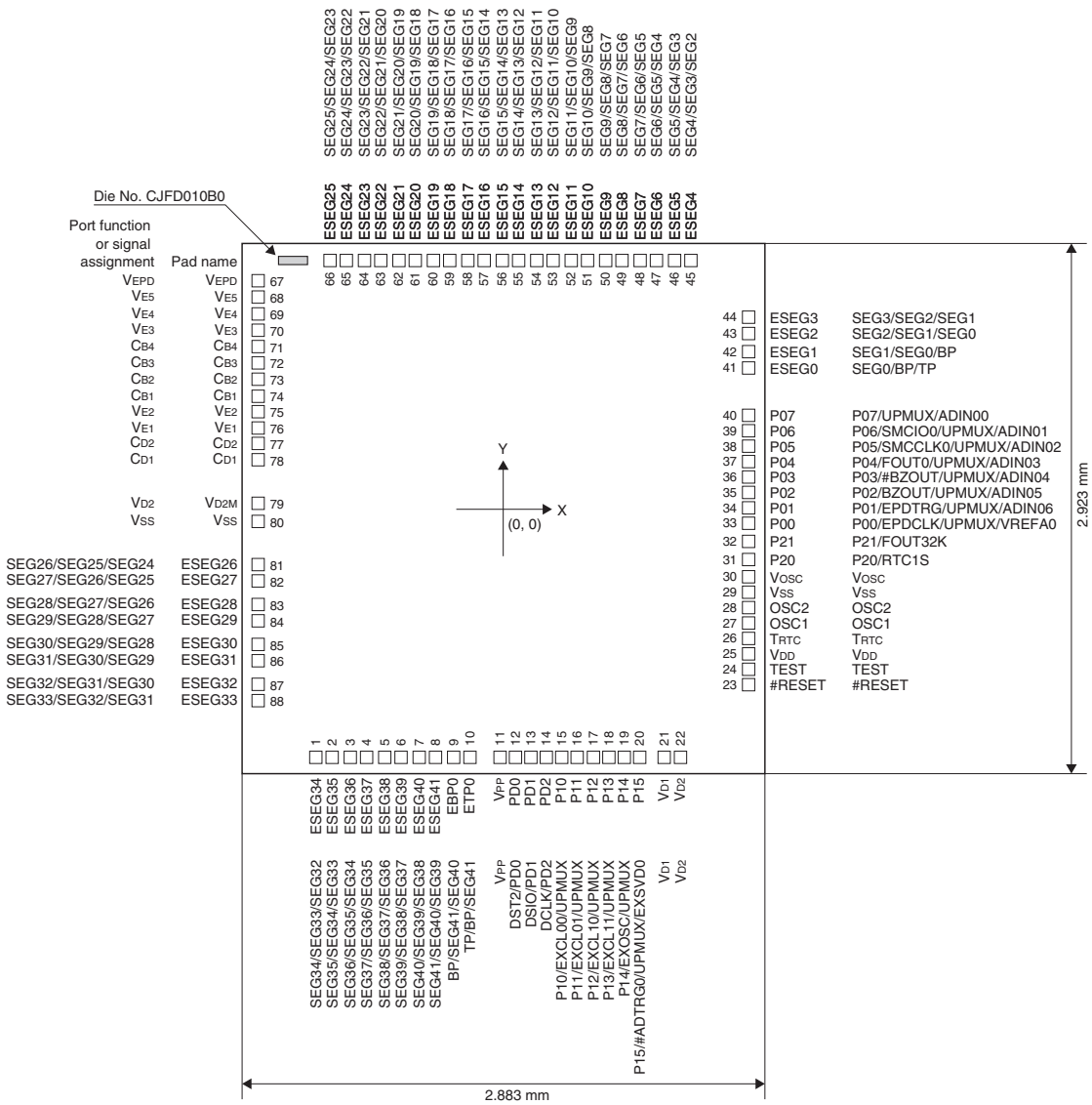


Figure 1.3.1.1 QFP15-100PIN Configuration Diagram

1.3.2 Aluminum Pad Chip



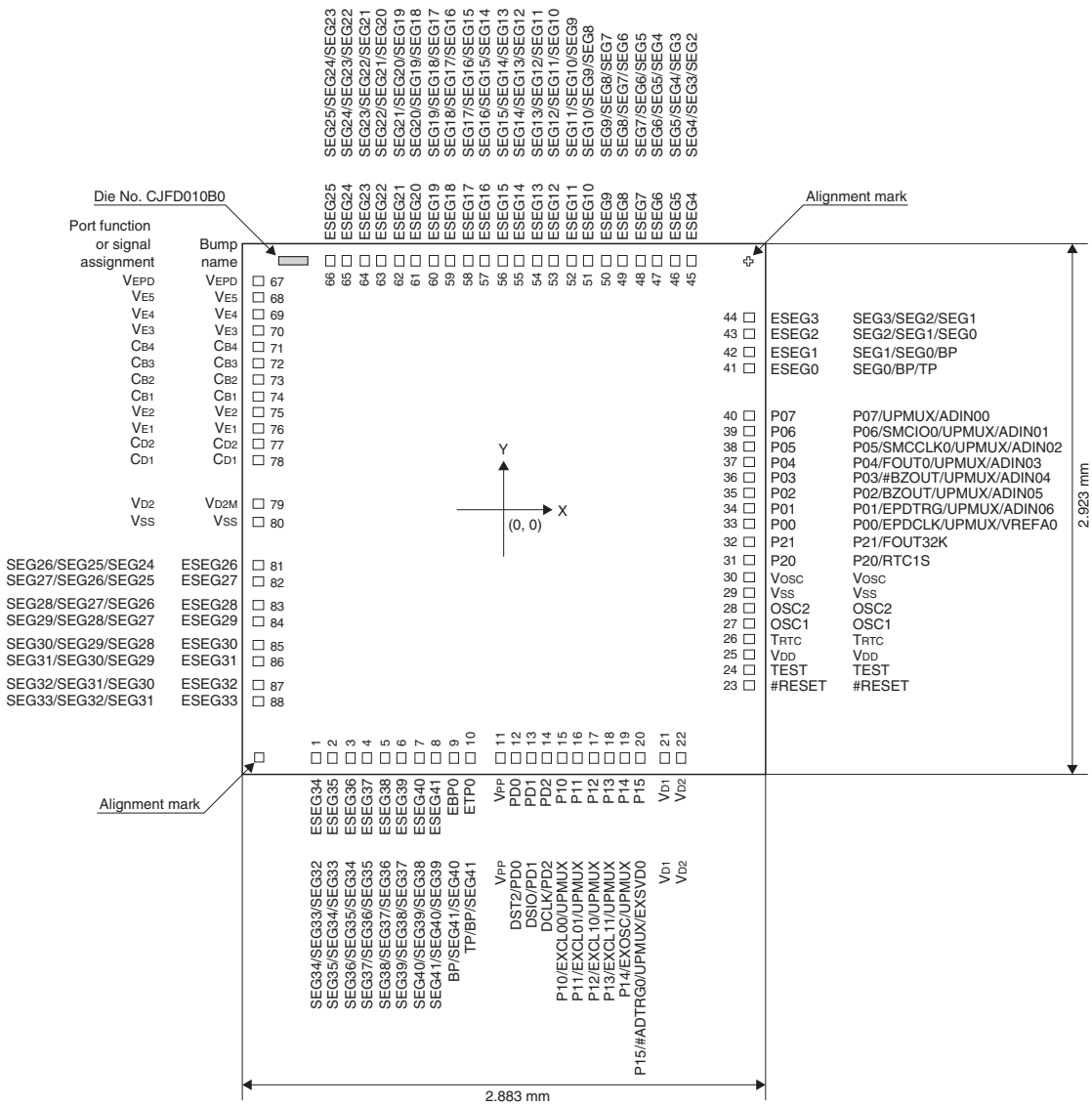
Pad opening X = 68 µm, Y = 68 µm
Chip thickness 200 µm

Figure 1.3.2.1 Aluminum Pad Chip Pad Configuration Diagram

Table 1.3.2.1 Pad Coordinates

No.	X µm	Y µm	No.	X µm	Y µm	No.	X µm	Y µm	No.	X µm	Y µm
1	-1,035	-1,372	23	1,352	-971	45	1,035	1,372	67	-1,352	1,260
2	-945	-1,372	24	1,352	-886	46	945	1,372	68	-1,352	1,170
3	-845	-1,372	25	1,352	-801	47	845	1,372	69	-1,352	1,077
4	-755	-1,372	26	1,352	-716	48	755	1,372	70	-1,352	987
5	-655	-1,372	27	1,352	-631	49	655	1,372	71	-1,352	897
6	-565	-1,372	28	1,352	-546	50	565	1,372	72	-1,352	807
7	-465	-1,372	29	1,352	-461	51	465	1,372	73	-1,352	717
8	-375	-1,372	30	1,352	-376	52	375	1,372	74	-1,352	623
9	-275	-1,372	31	1,352	-281	53	275	1,372	75	-1,352	538
10	-185	-1,372	32	1,352	-181	54	185	1,372	76	-1,352	448
11	-19	-1,372	33	1,352	-81	55	85	1,372	77	-1,352	363
12	66	-1,372	34	1,352	4	56	-5	1,372	78	-1,352	273
13	151	-1,372	35	1,352	89	57	-105	1,372	79	-1,352	33
14	236	-1,372	36	1,352	174	58	-195	1,372	80	-1,352	-67
15	321	-1,372	37	1,352	259	59	-295	1,372	81	-1,352	-305
16	406	-1,372	38	1,352	344	60	-385	1,372	82	-1,352	-395
17	496	-1,372	39	1,352	429	61	-485	1,372	83	-1,352	-525
18	581	-1,372	40	1,352	514	62	-575	1,372	84	-1,352	-615
19	666	-1,372	41	1,352	775	63	-675	1,372	85	-1,352	-745
20	751	-1,372	42	1,352	865	64	-765	1,372	86	-1,352	-835
21	886	-1,372	43	1,352	965	65	-865	1,372	87	-1,352	-965
22	976	-1,372	44	1,352	1,055	66	-955	1,372	88	-1,352	-1,055

1.3.3 Gold Bump Chip



Bump size No. 1–22, 45–66: X = 50 µm, Y = 58 µm No. 23–44, 67–88: X = 58 µm, Y = 50 µm
Chip thickness 200 µm

Figure 1.3.3.1 Gold Bump Chip Bump Configuration Diagram

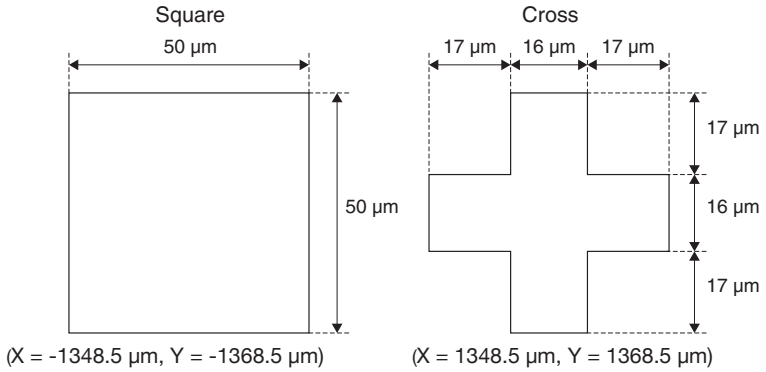


Figure 1.3.3.2 Alignment Marks

Table 1.3.3.1 Bump Coordinates

No.	X µm	Y µm	No.	X µm	Y µm	No.	X µm	Y µm	No.	X µm	Y µm
1	-1,035	-1,372	23	1,352	-971	45	1,035	1,372	67	-1,352	1,260
2	-945	-1,372	24	1,352	-886	46	945	1,372	68	-1,352	1,170
3	-845	-1,372	25	1,352	-801	47	845	1,372	69	-1,352	1,077
4	-755	-1,372	26	1,352	-716	48	755	1,372	70	-1,352	987
5	-655	-1,372	27	1,352	-631	49	655	1,372	71	-1,352	897
6	-565	-1,372	28	1,352	-546	50	565	1,372	72	-1,352	807
7	-465	-1,372	29	1,352	-461	51	465	1,372	73	-1,352	717
8	-375	-1,372	30	1,352	-376	52	375	1,372	74	-1,352	623
9	-275	-1,372	31	1,352	-281	53	275	1,372	75	-1,352	538
10	-185	-1,372	32	1,352	-181	54	185	1,372	76	-1,352	448
11	-19	-1,372	33	1,352	-81	55	85	1,372	77	-1,352	363
12	66	-1,372	34	1,352	4	56	-5	1,372	78	-1,352	273
13	151	-1,372	35	1,352	89	57	-105	1,372	79	-1,352	33
14	236	-1,372	36	1,352	174	58	-195	1,372	80	-1,352	-67
15	321	-1,372	37	1,352	259	59	-295	1,372	81	-1,352	-305
16	406	-1,372	38	1,352	344	60	-385	1,372	82	-1,352	-395
17	496	-1,372	39	1,352	429	61	-485	1,372	83	-1,352	-525
18	581	-1,372	40	1,352	514	62	-575	1,372	84	-1,352	-615
19	666	-1,372	41	1,352	775	63	-675	1,372	85	-1,352	-745
20	751	-1,372	42	1,352	865	64	-765	1,372	86	-1,352	-835
21	886	-1,372	43	1,352	965	65	-865	1,372	87	-1,352	-965
22	976	-1,372	44	1,352	1,055	66	-955	1,372	88	-1,352	-1,055

Table 1.3.3.2 Gold Bump Specifications

Characteristic		Specification
Bump shape		Strait bump
Bump height (Distance between Al trace and top of bump)	Central height	15 µm Typ.
	Bump-to-bump variation tolerances in all lots	Central height ± 4 µm
	Bump-to-bump variation tolerances in a chip	R(Max. - Min.) ≤ 3 µm
Bump hardness	All bumps in all lots	30 to 70 HV
Bump strength	All bumps in all lots	0.0067g/µm^2, shearing within a gold bump
Bump surface asperities	Height Max. - Min. in a bump	3.0 µm or less
Bump dimensions	X and Y plane dimension tolerances (at top of bump)	X ± 4 µm, Y ± 4 µm
Clearance between bumps	Minimum value	S = 20 µm

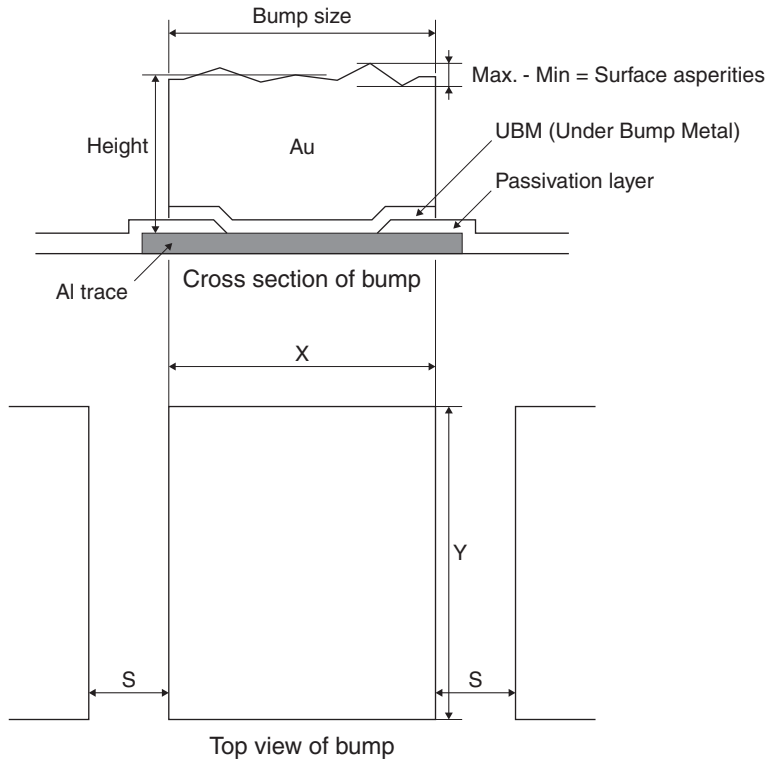


Figure 1.3.3.3 Gold Bump Specifications

1.3.4 Pin Descriptions

Symbol meanings

Assigned signal: The signal listed at the top of each pin is assigned in the initial state. The pin function must be switched via software to assign another signal (see the "I/O Ports" chapter).

I/O:
- I = Input
- O = Output
- I/O = Input/output
- P = Power supply
- A = Analog signal
- Hi-Z = High impedance state

Initial state:
- I (Pull-up) = Input with pulled up
- I (Pull-down) = Input with pulled down
- Hi-Z = High impedance state
- O (H) = High level output
- O (L) = Low level output

Tolerant fail-safe structure:
- ✓ = Over voltage tolerant fail-safe type I/O cell included (see the "I/O Ports" chapter)

Table 1.3.4.1 Pin Description

Pin name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function
V_{DD}	V_{DD}	P	–	–	Power supply (+)
V_{SS}	V_{SS}	P	–	–	GND
V_{PP}	V_{PP}	P	–	–	Power supply for Flash programming
V_{D1}	V_{D1}	A	–	–	V_{D1} regulator output
V_{D2}	V_{D2}	A	–	–	MCU core block operating power supply
V_{D2M}	V_{D2}	A	–	–	V_{D2} voltage monitor
V_{OSC}	V_{OSC}	P	–	–	V_{OSC} regulator output (OSC1 oscillator power supply)
T_{RTC}	T_{RTC}	A	–	–	Test output pin (Leave the pin open during normal operation.)
V_{EPD}	V_{EPD}	P	–	–	EPD drive voltage output
$V_{E1–5}$	$V_{E1–5}$	P	–	–	EPD power voltage booster outputs
$C_{D1–2}$	$C_{D1–2}$	A	–	–	EPD power voltage booster capacitor connecting pins
$C_{B1–4}$	$C_{B1–4}$	A	–	–	EPD power voltage booster capacitor connecting pins
OSC1	OSC1	A	–	–	OSC1 oscillator circuit input
OSC2	OSC2	A	–	–	OSC1 oscillator circuit output
#RESET	#RESET	I	I (Pull-up)	–	Reset input
TEST	TEST	I	I	–	Test input
P00	P00	I/O	Hi-Z	–	I/O port
	EPDCLK	O			EPD clock output for external EPD driver
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	VREFA0	A			12-bit A/D converter Ch.0 reference voltage input/Reference voltage generator constant voltage output
P01	P01	I/O	Hi-Z	–	I/O port
	EPDTRG	O			EPD trigger output for external EPD driver
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN06	A			12-bit A/D converter Ch.0 analog signal input 6
P02	P02	I/O	Hi-Z	–	I/O port
	BZOUT	O			Sound generator output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN05	A			12-bit A/D converter Ch.0 analog signal input 5
P03	P03	I/O	Hi-Z	–	I/O port
	#BZOUT	O			Sound generator inverted output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN04	A			12-bit A/D converter Ch.0 analog signal input 4
P04	P04	I/O	Hi-Z	–	I/O port
	FOUT0	O			Clock external output 0
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN03	A			12-bit A/D converter Ch.0 analog signal input 3
P05	P05	I/O	Hi-Z	–	I/O port
	SMCCLK0	I/O			Smart card interface clock input/output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN02	A			12-bit A/D converter Ch.0 analog signal input 2

Pin name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function
P06	P06	I/O	Hi-Z	–	I/O port
	SMCIO0	I/O			Smart card interface data input/output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN01	A			12-bit A/D converter Ch.0 analog signal input 1
P07	P07	I/O	Hi-Z	–	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN00	A			12-bit A/D converter Ch.0 analog signal input 0
P10	P10	I/O	Hi-Z	✓	I/O port
	EXCL00	I			16-bit PWM timer Ch.0 event counter input 0
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P11	P11	I/O	Hi-Z	✓	I/O port
	EXCL01	I			16-bit PWM timer Ch.0 event counter input 1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P12	P12	I/O	Hi-Z	✓	I/O port
	EXCL10	I			16-bit PWM timer Ch.1 event counter input 0
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P13	P13	I/O	Hi-Z	✓	I/O port
	EXCL11	I			16-bit PWM timer Ch.1 event counter input 1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P14	P14	I/O	Hi-Z	–	I/O port
	EXOSC	I			Clock generator external clock input
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P15	P15	I/O	Hi-Z	✓	I/O port
	#ADTRG0	I			12-bit A/D converter Ch.0 trigger input
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	EXSVD0	A			External power supply voltage detection input
P20	P20	I/O	Hi-Z	✓	I/O port
	RTC1S	O			Real-time clock 1-second cycle pulse output
P21	P21	I/O	Hi-Z	✓	I/O port
	FOUT32K	O			Clock external output (32 kHz clock output)
PD0	DST2	O	O (L)	–	On-chip debugger status output
	PD0	I/O			I/O port
PD1	DSIO	I/O	I (Pull-up)	✓	On-chip debugger data input/output
	PD1	I/O			I/O port
PD2	DCLK	O	O (H)	✓	On-chip debugger clock output
	PD2	I/O			I/O port
ETP0	TP	O	Hi-Z	–	EPD top plane output
	BP	O			EPD back plane output
	SEG41	O			EPD segment output
EBP0	BP	O	Hi-Z	–	EPD back plane output
	SEG41	O			EPD segment output
	SEG40	O			EPD segment output
ESEG0	SEG0	O	Hi-Z	–	EPD segment output
	BP	O			EPD back plane output
	TP	O			EPD top plane output
ESEG1	SEG1	O	Hi-Z	–	EPD segment output
	SEG0	O			EPD segment output
	BP	O			EPD back plane output
ESEG2–41	SEG0–41	O	Hi-Z	–	EPD segment outputs

Note: In the peripheral circuit descriptions, the assigned signal name is used as the pin name.

Universal port multiplexer (UPMUX)

The universal port multiplexer (UPMUX) allows software to select the peripheral circuit input/output function to be assigned to each pin from those listed below.

Table 1.3.4.2 Peripheral Circuit Input/output Function Selectable by UPMUX

Peripheral circuit	Signal to be assigned	I/O	Channel number *n*	Function
Synchronous serial interface (SPIA)	SDI*n*	I	*n* = 0, 1	SPIA Ch.*n* data input
	SDO*n*	O		SPIA Ch.*n* data output
	SPICLK*n*	I/O		SPIA Ch.*n* clock input/output
	#SPISS*n*	I		SPIA Ch.*n* slave-select input
I²C (I2C)	SCL*n*	I/O	*n* = 0	I2C Ch.*n* clock input/output
	SDA*n*	I/O		I2C Ch.*n* data input/output
UART (UART3)	USIN*n*	I	*n* = 0	UART3 Ch.*n* data input
	USOUT*n*	O		UART3 Ch.*n* data output
16-bit PWM timer (T16B)	TOUT*n*0/CAP*n*0	I/O	*n* = 0, 1	T16B Ch.*n* PWM output/capture input 0
	TOUT*n*1/CAP*n*1	I/O		T16B Ch.*n* PWM output/capture input 1

Note: Do not assign a function to two or more pins simultaneously.

2 Power Supply, Reset, and Clocks

The power supply, reset, and clocks in this IC are managed by the embedded power generator, system reset controller, and clock generator, respectively.

2.1 Power Generator (PWG)

2.1.1 Overview

PWG is the power generator that controls the MCU core block power supply system to drive this IC with stability and low power. The main features of PWG are outlined below.

- Driven with V_{D2} supplied from the independent low-power real-time clock
- Embedded V_{D1} regulator
  - The V_{D1} regulator generates the V_{D1} voltage to drive internal circuits, this makes it possible to keep current consumption constant independent of the V_{D2} voltage level.
  - The V_{D1} regulator supports two operation modes, normal mode and economy mode, and setting the V_{D1} regulator into economy mode at light loads helps achieve low-power operations.

Figure 2.1.1.1 shows the PWG configuration.

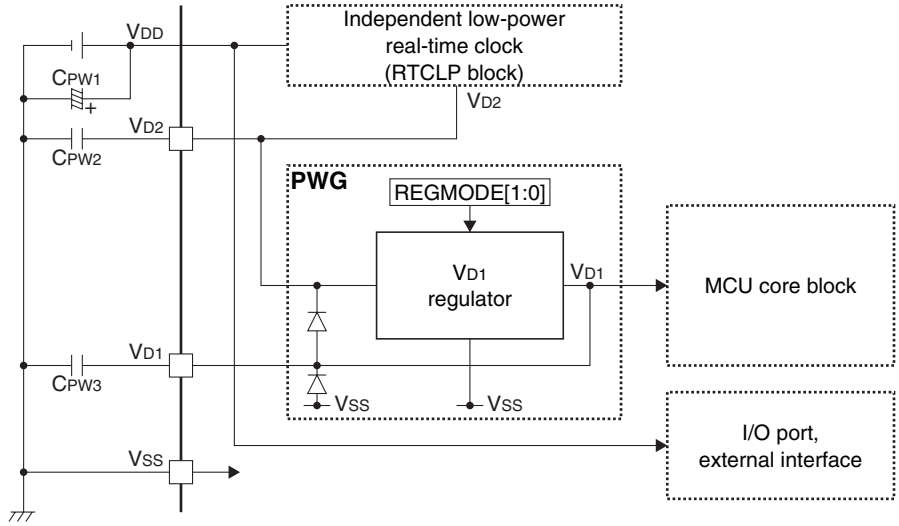


Figure 2.1.1.1 PWG Configuration

For how to control V_{D2}, refer to the "Independent Low-Power Real-Time Clock" chapter.

2.1.2 Pins

Table 2.1.2.1 lists the PWG pins.

Table 2.1.2.1 List of PWG Pins

Pin name	I/O	Initial status	Function
V_{DD}	P	–	Power supply (+)
V_{SS}	P	–	GND
V_{D2}	A	–	MCU core block operating power supply
V_{D1}	A	–	V_{D1} regulator output

For the V_{DD} operating voltage range and recommended external parts, refer to "Recommended Operating Conditions, Power supply voltage V_{DD}" in the "Electrical Characteristics" chapter and the "Basic External Connection Diagram" chapter, respectively.

2.1.3 V_{D1} Regulator Operation Mode

The V_{D1} regulator supports two operation modes, normal mode and economy mode. Setting the V_{D1} regulator into economy mode at light loads helps achieve low-power operations. Table 2.1.3.1 lists examples of light load conditions in which economy mode can be set.

Table 2.1.3.1 Examples of Light Load Conditions in which Economy Mode Can be Set

Light load condition	Exceptions
SLEEP mode (when all oscillators are stopped, or OSC1 only is active)	When a clock source except for OSC1 is active
HALT mode (when OSC1 only is active)	
RUN mode (when OSC1 only is active)	

The V_{D1} regulator also supports automatic mode in which the hardware detects a light load condition and automatically switches between normal mode and economy mode. Use the V_{D1} regulator in automatic mode when no special control is required.

2.2 System Reset Controller (SRC)

2.2.1 Overview

SRC is the system reset controller that resets the internal circuits according to the requests from the reset sources to archive steady IC operations. The main features of SRC are outlined below.

- Embedded reset hold circuit maintains reset state to boot the system safely while the internal power supply is unstable after power on or the oscillation frequency is unstable after the clock source is initiated.
- Supports reset requests from multiple reset sources.
  - #RESET pin
  - POR and BOR
  - Oscillation stop detection reset
  - Key-entry reset
  - Watchdog timer reset
  - Supply voltage detector reset
  - Peripheral circuit software reset (supports some peripheral circuits only)
- The CPU registers and peripheral circuit control bits will be reset with an appropriate initialization condition according to changes in status.

Figure 2.2.1.1 shows the SRC configuration.

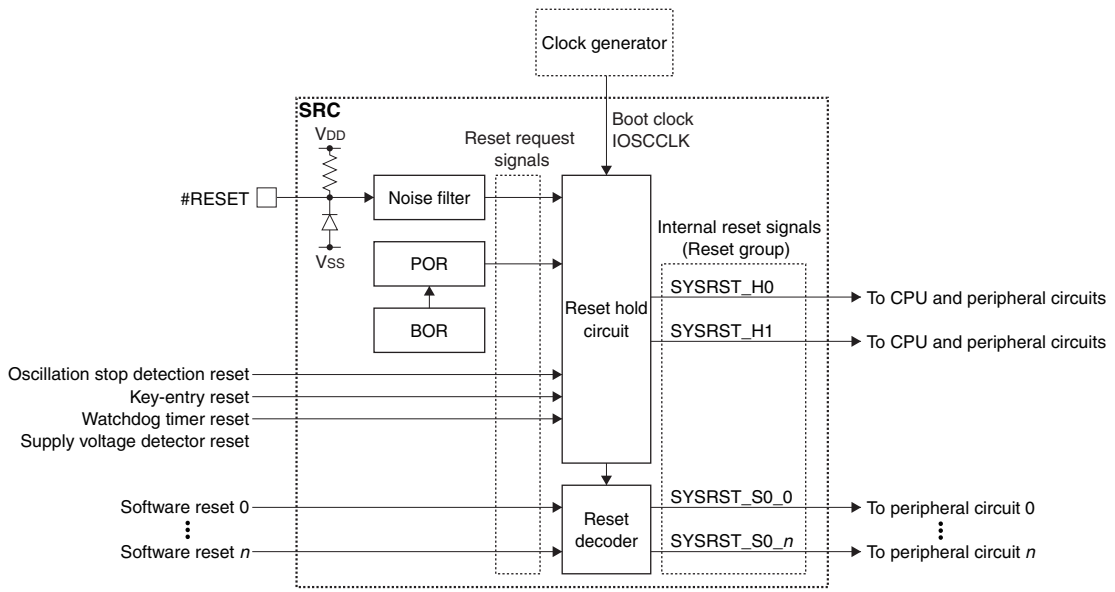


Figure 2.2.1.1 SRC Configuration

2.2.2 Input Pin

Table 2.2.2.1 shows the SRC pin.

Table 2.2.2.1 SRC Pin

Pin name	I/O	Initial status	Function
#RESET	I	I (Pull-up)	Reset input

The #RESET pin is connected to the noise filter that removes pulses not conforming to the requirements. An internal pull-up resistor is connected to the #RESET pin, so the pin can be left open. For the #RESET pin characteristics, refer to "#RESET pin characteristics" in the "Electrical Characteristics" chapter.

2.2.3 Reset Sources

The reset source refers to causes that request system initialization. The following shows the reset sources.

#RESET pin

Inputting a reset signal with a certain low level period to the #RESET pin issues a reset request.

POR and BOR

POR (Power On Reset) issues a reset request when the rise of VDD is detected. BOR (Brownout Reset) issues a reset request when a certain VDD voltage level is detected. Reset requests from these circuits ensure that the system will be reset properly when the power is turned on and the supply voltage is out of the operating voltage range. Figure 2.2.3.1 shows an example of POR and BOR internal reset operation according to variations in VDD.

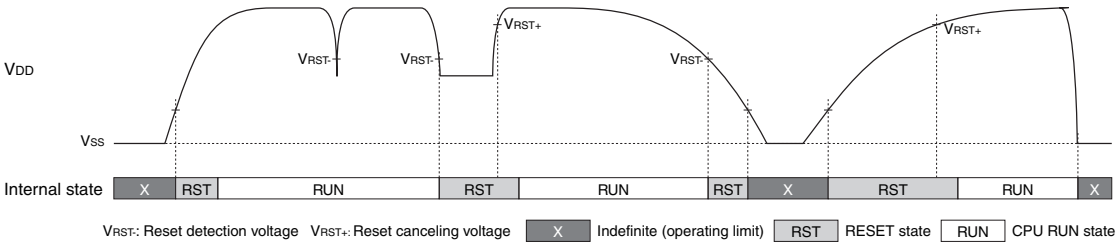


Figure 2.2.3.1 Example of Internal Reset by POR and BOR

For the POR and BOR electrical specifications, refer to "POR/BOR characteristics" in the "Electrical Characteristics" chapter.

Oscillation stop detection reset

The independent low-power real-time clock issues a reset request after turning power on until the OSC1 oscillation has stabilized, or when the OSC1 oscillation stops while the system is running. For more information, refer to the "Independent Low-Power Real-Time Clock" chapter.

Key-entry reset

Inputting a low level signal of a certain period to the I/O port pins configured to a reset input issues a reset request. This function must be enabled using an I/O port register. For more information, refer to the "I/O Ports" chapter.

Watchdog timer reset

Setting the watchdog timer into reset mode will issue a reset request when the counter overflows. This helps return the runaway CPU to a normal operating state. For more information, refer to the "Watchdog timer" chapter.

Supply voltage detector reset

By enabling the low power supply voltage detection reset function, the supply voltage detector will issue a reset request when a drop in the power supply voltage is detected. This makes it possible to put the system into reset state if the IC must be stopped under a low voltage condition. For more information, refer to the "Supply Voltage Detector" chapter.

Peripheral circuit software reset

Some peripheral circuits provide a control bit for software reset (MODEN or SFTRST). Setting this bit initializes the peripheral circuit control bits. Note, however, that the software reset operations depend on the peripheral circuit. For more information, refer to "Control Registers" in each peripheral circuit chapter.

Note: The MODEN bit of some peripheral circuits does not issue software reset.

2.2.4 Initialization Conditions (Reset Groups)

A different initialization condition is set for the CPU registers and peripheral circuit control bits, individually. The reset group refers to an initialization condition. Initialization is performed when a reset source included in a reset group issues a reset request. Table 2.2.4.1 lists the reset groups. For the reset group to initialize the registers and control bits, refer to the "CPU and Debugger" chapter or "Control Registers" in each peripheral circuit chapter.

Table 2.2.4.1 List of Reset Groups

Reset group	Reset source	Reset cancelation timing
H0	#RESET pin POR and BOR Oscillation stop detection reset Key-entry reset Supply voltage detector reset Watchdog timer reset	Reset state is maintained for the reset hold time t_{RSTR} after the reset request is canceled.
H1	#RESET pin POR and BOR	
S0	Peripheral circuit software reset (MODEN and SFTRST bits. The software reset operations depend on the peripheral circuit.	Reset state is canceled immediately after the reset request is canceled.

2.3 Clock Generator (CLG)

2.3.1 Overview

CLG is the clock generator that controls the clock sources and manages clock supply to the CPU and the peripheral circuits. The main features of CLG are outlined below.

- Supports multiple clock sources.
  - IOSC oscillator circuit that oscillates with a fast startup and no external parts required
  - RTCLP controller for controlling the clock generated by the independent low-power real-time clock that operates independently of the MCU
  - OSC3 oscillator circuit that generates a clock for high-speed operations without an external part
  - EXOSC clock input circuit that allows input of square wave and sine wave clock signals
- The system clock (SYSCLK), which is used as the operating clock for the CPU and bus, and the peripheral circuit operating clocks can be configured individually by selecting the suitable clock source and division ratio.
- IOSCCLK output from the IOSC oscillator circuit is used as the boot clock for fast booting.
- Controls the oscillator and clock input circuits to enable/disable according to the operating mode, RUN or SLEEP mode.
- Provides a flexible system clock switching function at SLEEP mode cancelation.
  - The clock sources to be stopped in SLEEP mode can be selected.
  - SYSCLK to be used at SLEEP mode cancelation can be selected from all clock sources.
  - The oscillator and clock input circuit on/off state can be maintained or changed at SLEEP mode cancelation.
- Provides the FOUT function to output an internal clock for driving external ICs or for monitoring the internal state.

Figure 2.3.1.1 shows the CLG configuration.

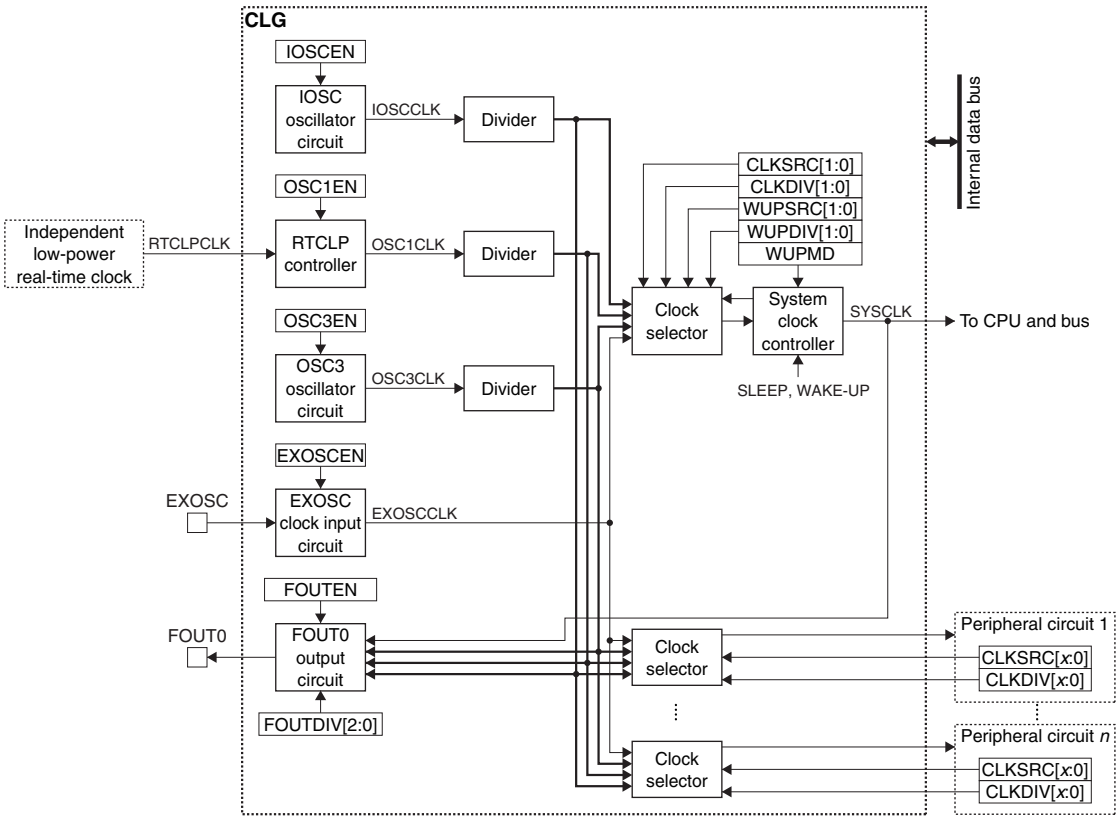


Figure 2.3.1.1 CLG Configuration

2.3.2 Input/Output Pins

Table 2.3.2.1 lists the CLG pins.

Table 2.3.2.1 List of CLG Pins

Pin name	I/O*	Initial status*	Function
EXOSC	I	I	EXOSC clock input
FOUT0	O	O (L)	FOUT0 clock outputs

* Indicates the status when the pin is configured for CLG.

If the port is shared with the CLG input/output function and other functions, the CLG function must be assigned to the port. For more information, refer to the "I/O Ports" chapter.

2.3.3 Clock Sources

IOSC oscillator circuit

The IOSC oscillator circuit features a fast startup and no external parts are required for oscillating. Figure 2.3.3.1 shows the configuration of the IOSC oscillator circuit.

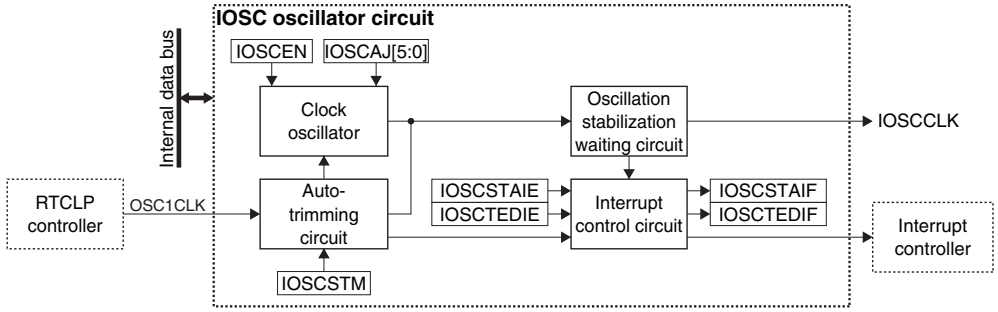


Figure 2.3.3.1 IOSC Oscillator Circuit Configuration

The IOSC oscillator circuit output clock IOSCCLK is used as SYSCLK at booting. The IOSC oscillator circuit is equipped with an auto-trimming function that automatically adjusts the frequency. This helps reduce frequency deviation due to unevenness in manufacturing quality, temperature, and changes in voltage. For more information on the auto-trimming function and the oscillation characteristics, refer to "IOSC oscillation auto-trimming function" in this chapter and "IOSC oscillator circuit characteristics" in the "Electrical Characteristics" chapter, respectively.

OSC3 oscillator circuit

The OSC3 oscillator circuit is a high-speed oscillator circuit and no external parts are required for oscillating. Figure 2.3.3.2 shows the configuration of the OSC3 oscillator circuit.

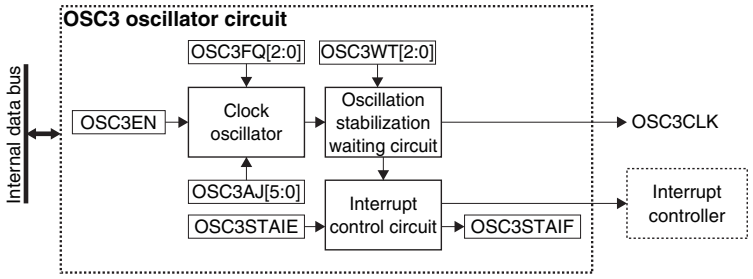


Figure 2.3.3.2 OSC3 Oscillator Circuit Configuration

The OSC3CLK frequency can be selected using the CLGOSC3.OSC3FQ[2:0] bits. For the oscillation characteristics, refer to "OSC3 oscillator circuit characteristics" in the "Electrical Characteristics" chapter.

EXOSC clock input

EXOSC is an external clock input circuit that supports square wave and sine wave clocks. Figure 2.3.3.3 shows the configuration of the EXOSC clock input circuit.

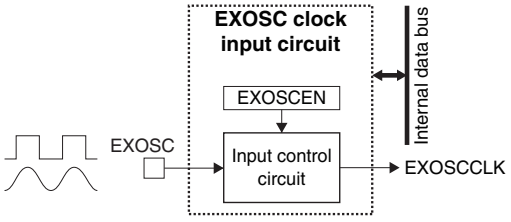


Figure 2.3.3.3 EXOSC Clock Input Circuit

EXOSC has no oscillation stabilization waiting circuit included, therefore, it must be enabled when a stabilized clock is being supplied. For the input clock characteristics, refer to "EXOSC external clock input characteristics" in the "Electrical Characteristics" chapter.

RTCLP controller

The RTCLP controller controls the clock generated by the independent low-power real-time clock. Figure 2.3.3.4 shows the configuration of the RTCLP controller.

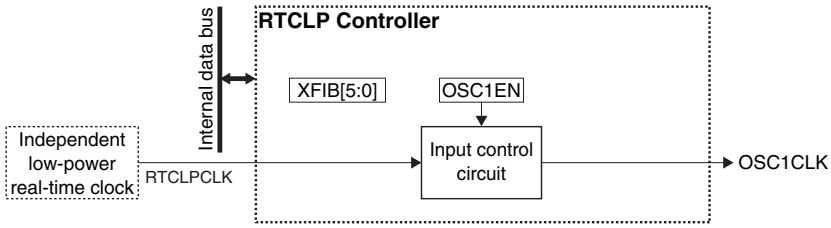


Figure 2.3.3.4 RTCLP Controller

When using OSC1CLK in the MCU core block, set the CLGOSC1.OSC1EN bit to 1 after controlling the independent low-power real-time clock to output RTCLPCLK.

The RTCLP controller does not control the independent low-power real-time clock directly. For the independent low-power real-time clock control method, refer to the "Independent Low-Power Real-Time Clock" chapter. RTCLPCLK is a 32.768 kHz clock.

2.3.4 Operations

Oscillation start time and oscillation stabilization waiting time

The oscillation start time refers to the time after the oscillator circuit is enabled until the oscillation signal is actually sent to the internal circuits. The oscillation stabilization waiting time refers to the time it takes the clock to stabilize after the oscillation starts. To avoid malfunctions of the internal circuits due to an unstable clock during this period, the oscillator circuit includes an oscillation stabilization waiting circuit that can disable supplying the clock to the system until the designated time has elapsed. Figure 2.3.4.1 shows the relationship between the oscillation start time and the oscillation stabilization waiting time.

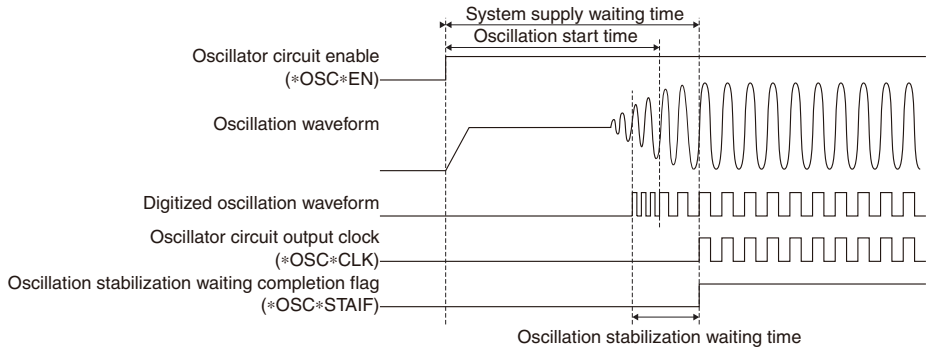


Figure 2.3.4.1 Oscillation Start Time and Oscillation Stabilization Waiting Time

The oscillation stabilization waiting time for the OSC3 oscillator circuit can be set using the CLGOSC3.OSC3WT[2:0] bits. It should be set to four OSC3CLK clocks or more. To check whether the oscillation stabilization waiting time is set properly and the clock is stabilized immediately after the oscillation starts or not, monitor the oscillation clock using the FOUT output function. The oscillation stabilization waiting time for the IOSC oscillator circuit is fixed at 16 IOSCCLK clocks. When the oscillation stabilization waiting operation has completed, the oscillator circuit sets the oscillation stabilization waiting completion flag and starts clock supply to the internal circuits.

Note: The oscillation stabilization waiting time is always expended at start of oscillation even if the oscillation stabilization waiting completion flag has not be cleared to 0.

Oscillation start procedure for the IOSC oscillator circuit

Follow the procedure shown below to start oscillation of the IOSC oscillator circuit.

1. Write 1 to the CLGINTF.IOSCSTAIF bit. (Clear interrupt flag)
2. Write 1 to the CLGINTE.IOSCSTAIE bit. (Enable interrupt)
3. Write 0x0096 to the MSCPROT.PROT[15:0] bits. (Remove system protection)
4. Set the CLGTRIM.IOSCAJ[5:0] bits as necessary. (Finely adjust oscillation frequency)
5. Write a value other than 0x0096 to the MSCPROT.PROT[15:0] bits. (Set system protection)
6. Write 1 to the CLGOSC.IOSCEN bit. (Start oscillation)
7. IOSCCLK can be used if the CLGINTF.IOSCSTAIF bit = 1 after an interrupt occurs.

The setting value of the CLGTRIM.IOSCAJ[5:0] bits should be determined after performing evaluation using the populated circuit board.

Note: Make sure the CLGOSC.IOSCEN bit is set to 0 (while the IOSC oscillation is halted) when setting the CLGTRIM.IOSCAJ[5:0] bits.

Oscillation start procedure for the OSC3 oscillator circuit

Follow the procedure shown below to start oscillation of the OSC3 oscillator circuit.

1. Write 1 to the CLGINTF.OSC3STAIF bit. (Clear interrupt flag)
2. Write 1 to the CLGINTE.OSC3STAIE bit. (Enable interrupt)
3. Write 0x0096 to the MSCPROT.PROT[15:0] bits. (Remove system protection)
4. Set the CLGTRIM.OSC3AJ[5:0] bits as necessary. (Finely adjust oscillation frequency)
5. Configure the following CLGOSC3 register bits:
   - CLGOSC3.OSC3FQ[2:0] bits (Select oscillation frequency)
   - CLGOSC3.OSC3WT[2:0] bits (Set oscillation stabilization waiting time)
6. Write a value other than 0x0096 to the MSCPROT.PROT[15:0] bits. (Set system protection)
7. Write 1 to the CLGOSC.OSC3EN bit. (Start oscillation)
8. OSC3CLK can be used if the CLGINTF.OSC3STAIF bit = 1 after an interrupt occurs.

The setting value of the CLGOSC3.OSC3WT[2:0] bits should be determined after performing evaluation using the populated circuit board.

Note: Make sure the CLGOSC.OSC3EN bit is set to 0 (while the OSC3 oscillation is halted) when setting the CLGTRIM.OSC3AJ[5:0] bits.

System clock switching

The CPU boots using IOSCCLK as SYSCLK. After booting, the clock source of SYSCLK can be switched according to the processing speed required. The SYSCLK frequency can also be set by selecting the clock source division ratio, this makes it possible to run the CPU at the most suitable performance for the process to be executed. The CLGSCLK.CLKSRC[1:0] and CLGSCLK.CLKDIV[1:0] bits are used for this control.
The CLGSCLK register bits are protected against writings by the system protect function, therefore, the system protection must be removed by writing 0x0096 to the MSCPROT.PROT[15:0] bits before the register setting can be altered. For the transition between the operating modes including the system clock switching, refer to "Operating Mode."

Clock control in SLEEP mode

The CPU enters SLEEP mode when it executes the slp instruction. Whether the clock sources being operated are stopped or not at this point can be selected in each source individually. This allows the CPU to fast switch between SLEEP mode and RUN mode, and the peripheral circuits to continue operating without disabling the clock in SLEEP mode. The CLGOSC.IOSCSLPC, CLGOSC.OSC1SLPC, CLGOSC.OSC3SLPC, and CLGOSC.EXOSCSLPC bits are used for this control. Figure 2.3.4.2 shows a control example.

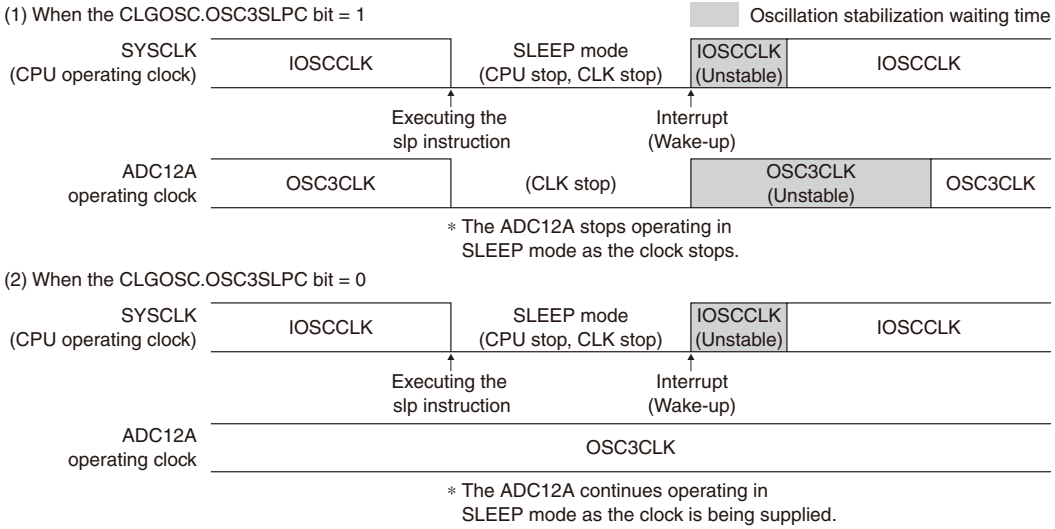


Figure 2.3.4.2 Clock Control Example in SLEEP Mode

The SYSCLK condition (clock source and division ratio) at wake-up from SLEEP mode to RUN mode can also be configured. This allows flexible clock control according to the wake-up process. Configure the clock using the CLGSCLK.WUPSRC[1:0] and CLGSCLK.WUPDIV[1:0] bits, and write 1 to the CLGSCLK.WUPMD bit to enable this function.

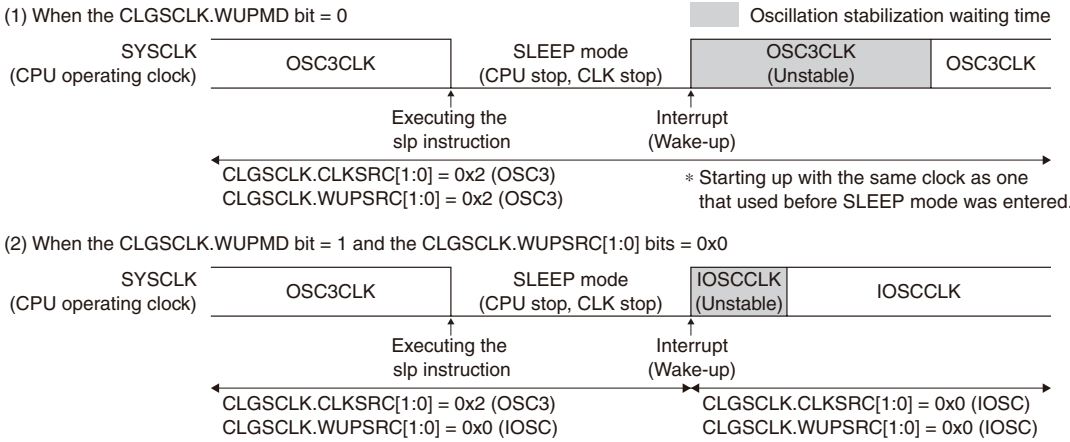


Figure 2.3.4.3 Clock Control Example at SLEEP Cancelation

Clock external outputs (FOUT0)

The FOUT0 pin can output the clock generated by a clock source or its divided clock to outside the IC. This allows monitoring the oscillation frequency of the oscillator circuit or supplying an operating clock to external ICs. Follow the procedure shown below to start clock external output.

1. Assign the FOUT0 function to the port. (Refer to the "I/O Ports" chapter.)
2. Configure the following CLGFOUT0 register bits:
   - CLGFOUT0.FOUTSRC[1:0] bits (Select clock source)
   - CLGFOUT0.FOUTDIV[2:0] bits (Set clock division ratio)
   - Set the CLGFOUT0.FOUTEN bit to 1. (Enable clock external output)

IOSC oscillation auto-trimming function

The auto-trimming function adjusts the IOSCCLK clock frequency by trimming the clock with reference to the high precision OSC1CLK clock. Follow the procedure shown below to enable the auto-trimming function.

1. Make sure that OSC1CLK is supplied (CLGOSC.OSC1EN bit = 1).
2. After enabling the IOSC oscillation, check if the stabilized clock is supplied (CLGINTF.IOSCSTAIF bit = 1).
3. Write 0x0096 to the MSCPROT.PROT[15:0] bits. (Remove system protection)
4. If the SYSCLK clock source is IOSC, set the CLGSCLK.CLKSRC[1:0] bits to a value other than 0x0 (IOSC).
5. Write 1 to the CLGINTF.IOSCTEDIF bit. (Clear interrupt flag)
6. Write 1 to the CLGINTE.IOSCTEDIE bit. (Enable interrupt)
7. Write 1 to the CLGIOSC.IOSCSTM bit. (Enable IOSC oscillation auto-trimming)
8. Write a value other than 0x0096 to the MSCPROT.PROT[15:0] bits. (Set system protection)
9. The trimmed IOSCCLK can be used if the CLGINTF.IOSCTEDIF bit = 1 after an interrupt occurs.

After the trimming operation has completed, the CLGIOSC.IOSCSTM bit automatically reverts to 0. Although the trimming time depends on the temperature, an average of several 10 ms is required. When IOSCCLK is being used as the system clock or a peripheral circuit clock, do not use the auto-trimming function.

2.4 Operating Mode

2.4.1 Initial Boot Sequence

Figure 2.4.1.1 shows the initial boot sequence after power is turned on.

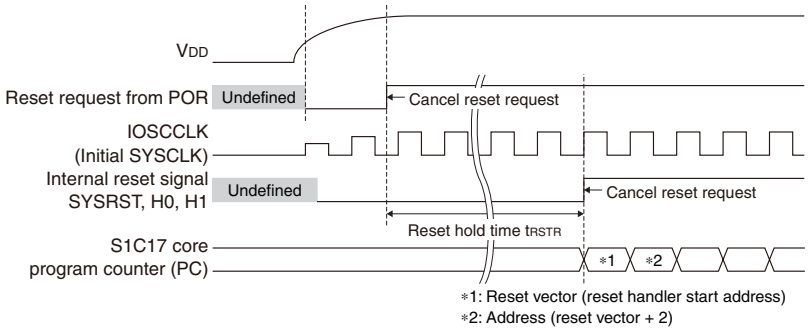


Figure 2.4.1.1 Initial Boot Sequence

Note: The reset cancelation time at power-on varies according to the power rise time and reset request cancelation time.

For the reset hold time tRSTR, refer to "Reset hold circuit characteristics" in the "Electrical Characteristics" chapter.

2.4.2 Transition between Operating Modes

State transitions between operating modes shown in Figure 2.4.2.1 take place in this IC.

RUN mode

RUN mode refers to the state in which the CPU is executing the program. A transition to this mode takes place when the system reset request from the system reset controller is canceled. RUN mode is classified into "IOSC RUN," "OSC1 RUN," "OSC3 RUN," and "EXOSC RUN" by the SYSCLK clock source.

HALT mode

When the CPU executes the halt instruction, it suspends program execution and stops operating. This state is HALT mode. In this mode, the clock sources and peripheral circuits keep operating. This mode can be set while no software processing is required and it reduces power consumption as compared with RUN mode. HALT mode is classified into "IOSC HALT," "OSC1 HALT," "OSC3 HALT," and "EXOSC HALT" by the SYSCLK clock source.

SLEEP mode

When the CPU executes the slp instruction, it suspends program execution and stops operating. This state is SLEEP mode. In this mode, the clock sources stop operating as well. However, the clock source in which the CLGOSC.IOSCSLPC/OSC1SLPC/OSC3SLPC/EXOSCSLPC bit is set to 0 keeps operating, so the peripheral circuits with the clock being supplied can also operate. By setting this mode when no software processing and peripheral circuit operations are required, power consumption can be less than HALT mode.
The RAM retains data even in SLEEP mode.

Notes: • The current consumption when a clock source is active in SLEEP mode by setting the CLGOSC.IOSCSLPC/OSC1SLPC/OSC3SLPC/EXOSCSLPC bit to 0 is equivalent to the value in HALT mode with the same clock source condition (refer to "Current Consumption, Current consumption in HALT mode I_{HALT1}, I_{HALT2}, and I_{HALT3}" in the "Electrical Characteristics" chapter).

• When the CLGOSC.OSC1SLPC bit = 1, the CLG stops inputting RTCLPCLK during SLEEP mode. However, the OSC1 oscillator circuit in the independent low-power real-time clock continues oscillating.

DEBUG mode

When a debug interrupt occurs, the CPU enters DEBUG mode. DEBUG mode is canceled when the retd instruction is executed. For more information on DEBUG mode, refer to "Debugger" in the "CPU and Debugger" chapter.

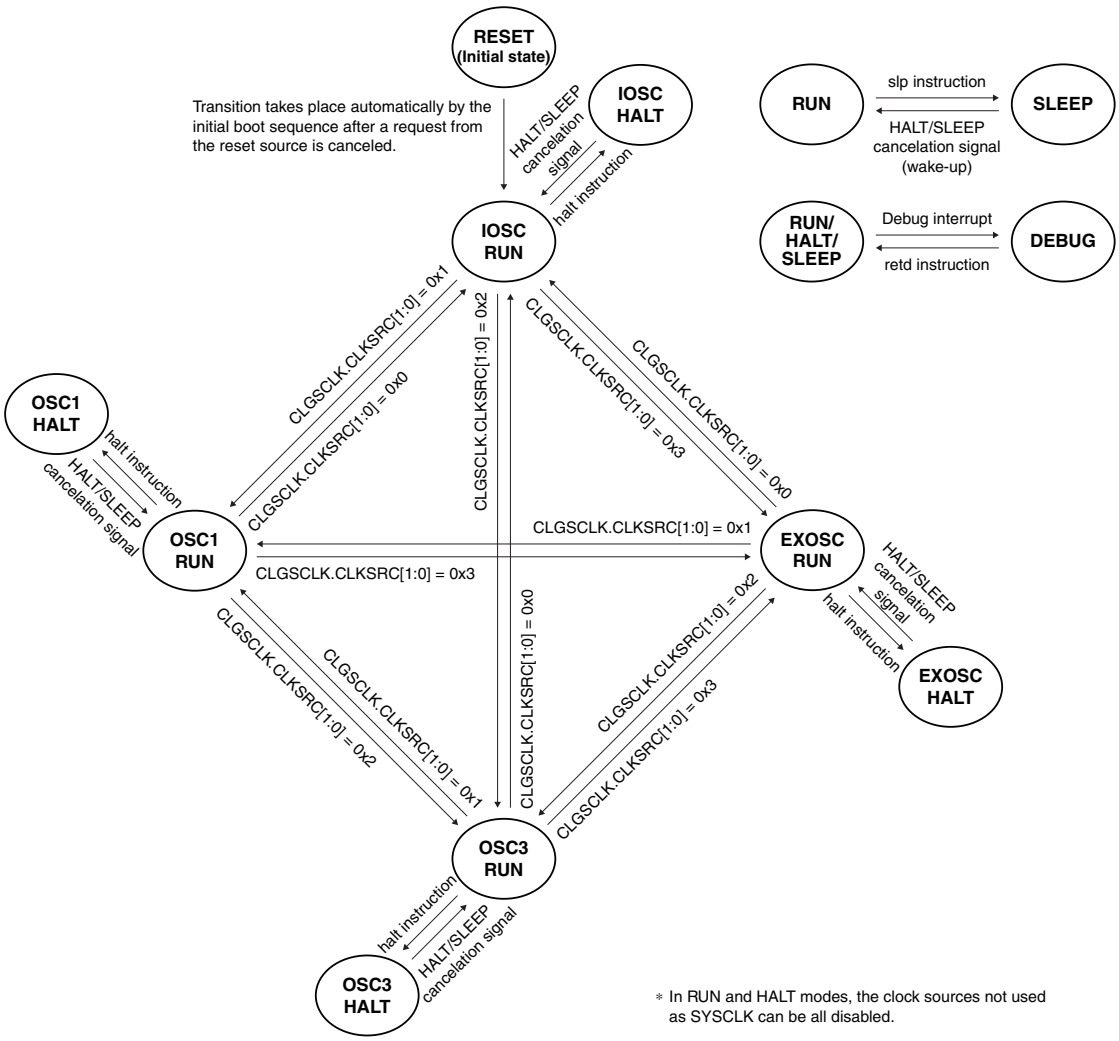


Figure 2.4.2.1 Operating Mode-to-Mode State Transition Diagram

Canceling HALT or SLEEP mode

The conditions listed below generate the HALT/SLEEP cancelation signal to cancel HALT or SLEEP mode and put the CPU into RUN mode. This transition is executed even if the CPU does not accept the interrupt request.

- Interrupt request from a peripheral circuit
- NMI from the watchdog timer
- Debug interrupt
- Reset request

2.5 Interrupts

CLG has a function to generate the interrupts shown in Table 2.5.1.

Table 2.5.1 CLG Interrupt Functions

Interrupt	Interrupt flag	Set condition	Clear condition
IOSC oscillation stabilization waiting completion	CLGINTF.IOSCSTAIF	When the IOSC oscillation stabilization waiting operation has completed after the oscillation starts	Writing 1
OSC3 oscillation stabilization waiting completion	CLGINTF.OSC3STAIF	When the OSC3 oscillation stabilization waiting operation has completed after the oscillation starts	Writing 1
IOSC oscillation auto-trimming completion	CLGINTF.IOSCTEDIF	When the IOSC oscillation auto-trimming operation has completed	Writing 1

CLG provides interrupt enable bits corresponding to each interrupt flag. An interrupt request is sent to the interrupt controller only when the interrupt flag, of which interrupt has been enabled by the interrupt enable bit, is set. For more information on interrupt control, refer to the "Interrupt Controller" chapter.

2.6 Control Registers

Note: Do not alter the initial values of the control bits for the functions that are not supported in the model to be used.

PWG V_{D1} Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
PWGVD1CTL	15–8	–	0x00	–	R	–
	7–2	–	0x00	–	R	
	1–0	REGMODE[1:0]	0x0	H0	R/WP	

Bits 15–2 Reserved

Bits 1–0 REGMODE[1:0]

These bits control the internal regulator operating mode.

Table 2.6.1 Internal Regulator Operating Mode

PWGVD1CTL.REGMODE[1:0] bits	Operating mode
0x3	Economy mode
0x2	Normal mode
0x1	Reserved
0x0	Automatic mode

CLG System Clock Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
CLGSCLK	15	WUPMD	0	H0	R/WP	–
	14	–	0	–	R	
	13–12	WUPDIV[1:0]	0x0	H0	R/WP	
	11–10	–	0x0	–	R	
	9–8	WUPSRC[1:0]	0x0	H0	R/WP	
	7–6	–	0x0	–	R	
	5–4	CLKDIV[1:0]	0x0	H0	R/WP	
	3–2	–	0x0	–	R	
	1–0	CLKSRC[1:0]	0x0	H0	R/WP	

Bit 15 WUPMD

This bit enables the SYSCLK switching function at wake-up.
1 (R/WP): Enable
0 (R/WP): Disable

When the CLGSCLK.WUPMD bit = 1, setting values of the CLGSCLK.WUPSRC[1:0] bits and the CLGSCLK.WUPDIV[1:0] bits are loaded to the CLGSCLK.CLKSRC[1:0] bits and the CLGSCLK.CLKDIV[1:0] bits, respectively, at wake-up from SLEEP mode to switch SYSCLK. When the CLGSCLK.WUPMD bit = 0, the CLGSCLK.CLKSRC[1:0] and CLGSCLK.CLKDIV[1:0] bits are not altered at wake-up.

Note: When the CLGSCLK.WUPMD bit = 1, the clock source enable bits (CLGOSC.EXOSCEN, CLGOSC.OSC1EN, CLGOSC.OSC3EN, CLGOSC.IOSCEN) except for the SYSCLK source selected by the CLGSCLK.CLKSRC[1:0] bits will be cleared to 0 to stop the clocks after a system wake-up. However, the enable bit of the clock source being operated during SLEEP mode by setting the CLGOSC.****SLPC bit retains 1 after a wake-up.

Bit 14 Reserved

Bits 13–12 WUPDIV[1:0]

These bits select the SYSCLK division ratio for resetting the CLGSCLK.CLKDIV[1:0] bits at wake-up. This setting is ineffective when the CLGSCLK.WUPMD bit = 0.

Bits 11–10 Reserved

Bits 9–8 WUPSRC[1:0]

These bits select the SYSCLK clock source for resetting the CLGSCLK.CLKSRC[1:0] bits at wake-up. When a currently stopped clock source is selected, it will automatically start oscillating or clock input at wake-up. However, this setting is ineffective when the CLGSCLK.WUPMD bit = 0.

Table 2.6.2 SYSCLK Clock Source and Division Ratio Settings at Wake-up

CLGSCLK. WUPDIV[1:0] bits	CLGSCLK.WUPSRC[1:0] bits			
	0x0	0x1	0x2	0x3
	IOSCCLK	OSC1CLK	OSC3CLK	EXOSCCLK
0x3	1/8	Reserved	1/8	Reserved
0x2	1/4	Reserved	1/4	Reserved
0x1	1/2	1/2	1/2	Reserved
0x0	1/1	1/1	1/1	1/1

Bits 7–6 Reserved

Bits 5–4 CLKDIV[1:0]

These bits set the division ratio of the clock source to determine the SYSCLK frequency.

Bits 3–2 Reserved

Bits 1–0 CLKSRC[1:0]

These bits select the SYSCLK clock source.
When a currently stopped clock source is selected, it will automatically start oscillating or clock input.

Table 2.6.3 SYSCLK Clock Source and Division Ratio Settings

CLGSCLK.CLKDIV[1:0] bits	CLGSCLK.CLKSRC[1:0] bits			
	0x0	0x1	0x2	0x3
	IOSCCLK	OSC1CLK	OSC3CLK	EXOSCCLK
0x3	1/8	Reserved	1/8	Reserved
0x2	1/4	Reserved	1/4	Reserved
0x1	1/2	1/2	1/2	Reserved
0x0	1/1	1/1	1/1	1/1

CLG Oscillation Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
CLGOSC	15–12	–	0x0	–	R	–
	11	EXOSCSLPC	1	H0	R/W	
	10	OSC3SLPC	1	H0	R/W	
	9	OSC1SLPC	1	H0	R/W	
	8	IOSCSLPC	1	H0	R/W	
	7–4	–	0x0	–	R	
	3	EXOSCEN	0	H0	R/W	
	2	OSC3EN	0	H0	R/W	
	1	OSC1EN	0	H0	R/W	
	0	IOSCEN	1	H0	R/W	

Bits 15–12 Reserved

Bit 11 EXOSCSLPC
Bit 10 OSC3SLPC
Bit 9 OSC1SLPC
Bit 8 IOSCSLPC

These bits control the clock source operations in SLEEP mode.
1 (R/W): Stop clock source in SLEEP mode
0 (R/W): Continue operation state before SLEEP

Each bit corresponds to the clock source as follows:
CLGOSC.EXOSCSLPC bit: EXOSC clock input
CLGOSC.OSC3SLPC bit: OSC3 oscillator circuit
CLGOSC.OSC1SLPC bit: RTCLP controller
CLGOSC.IOSCSLPC bit: IOSC oscillator circuit

Bits 7–4 Reserved

Bit 3 EXOSCEN
Bit 2 OSC3EN
Bit 1 OSC1EN
Bit 0 IOSCEN

These bits control the clock source operation.
1(R/W): Start oscillating or clock input
0(R/W): Stop oscillating or clock input

Each bit corresponds to the clock source as follows:
CLGOSC.EXOSCEN bit: EXOSC clock input
CLGOSC.OSC3EN bit: OSC3 oscillator circuit
CLGOSC.OSC1EN bit: RTCLP controller
CLGOSC.IOSCEN bit: IOSC oscillator circuit

CLG IOSC Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
CLGIOSC	15–8	–	0x00	–	R	–
	7–5	–	0x0	–	R	
	4	IOSCSTM	0	H0	R/WP	
	3–0	–	0x0	–	R	

Bits 15–5 Reserved

Bit 4 IOSCSTM

This bit controls the IOSCCLK auto-trimming function.

1 (WP): Start trimming
0 (WP): Stop trimming
1 (R): Trimming is executing.
0 (R): Trimming has finished. (Trimming operation inactivated.)

This bit is automatically cleared to 0 when trimming has finished.

Notes: • Do not use IOSCCLK as the system clock or peripheral circuit clocks while the CLGIOSC. IOSCSTM bit = 1.

• The auto-trimming function does not work if OSC1CLK is not supplied.

Bits 3–0 Reserved

CLG OSC1 Trimming Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
CLGOSC1TRIM	15–8	–	0x00	–	R	–
	7–6	–	0x0	–	R	
	5–0	XFIB[5:0]	*	H0	R	

Bits 15–6 Reserved

Bits 5–0 XFIB[5:0]

These bits indicate the adjustment value of the Vosc regulator included in the independent low-power real-time clock that was set at factory shipment. Read this value and set it to the VOSCTRIM. XFIB[5:0] bits in the independent low-power real-time clock.

CLG OSC3 Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
CLGOSC3	15–13	–	0x0	–	R	–
	12–10	OSC3FQ[2:0]	0x3	H0	R/WP	
	9–8	–	0x0	–	R	
	7–3	–	0x00	–	R	
	2–0	OSC3WT[2:0]	0x6	H0	R/WP	

Bits 15–13 Reserved

Bits 12–10 OSC3FQ[2:0]

These bits set the oscillation frequency of the OSC3 internal oscillator circuit.

Table 2.6.4 Setting Oscillation Frequency of OSC3 Internal Oscillator Circuit

CLGOSC3.OSC3FQ[2:0] bits	Oscillation frequency
0x7	Reserved
0x6	16 MHz
0x5	12 MHz
0x4	8 MHz
0x3	4 MHz
0x2	2 MHz
0x1	1 MHz
0x0	500 kHz

Bits 9–3 Reserved

Bits 2–0 OSC3WT[2:0]

These bits set the oscillation stabilization waiting time for the OSC3 oscillator circuit.

Table 2.6.5 OSC3 Oscillation Stabilization Waiting Time Setting

CLGOSC3.OSC3WT[2:0] bits	Oscillation stabilization waiting time
0x7	65,536 clocks
0x6	16,384 clocks
0x5	4,096 clocks
0x4	1,024 clocks
0x3	256 clocks
0x2	64 clocks
0x1	16 clocks
0x0	4 clocks

CLG Interrupt Flag Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
CLGINTF	15–8	–	0x00	–	R	–
	7	–	0x0	–	R	
	6–5	(reserved)	0x0	H0	R	
	4	IOSCTEDIF	0	H0	R/W	Cleared by writing 1.
	3	–	0	–	R	–
	2	OSC3STAIF	0	H0	R/W	Cleared by writing 1.
	1	–	0	–	R	–
	0	IOSCSTAIF	0	H0	R/W	Cleared by writing 1.

Bits 15–5, 3, 1 Reserved

Bit 4 IOSCTEDIF
Bit 2 OSC3STAIF
Bit 0 IOSCSTAIF

These bits indicate the CLG interrupt cause occurrence statuses.

1 (R): Cause of interrupt occurred
0 (R): No cause of interrupt occurred
1 (W): Clear flag
0 (W): Ineffective

Each bit corresponds to the interrupt as follows:
CLGINTF.IOSCTEDIF bit: IOSC oscillation auto-trimming completion interrupt
CLGINTF.OSC3STAIF bit: OSC3 oscillation stabilization waiting completion interrupt
CLGINTF.IOSCSTAIF bit: IOSC oscillation stabilization waiting completion interrupt

Note: The CLGINTF.IOSCSTAIF bit is 0 after system reset is canceled, but IOSCCLK has already been stabilized.

CLG Interrupt Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
CLGINTE	15–8	–	0x00	–	R	–
	7	–	0	–	R	
	6–5	(reserved)	0x0	H0	R	
	4	IOSCTEDIE	0	H0	R/W	
	3	–	0	–	R	
	2	OSC3STAIE	0	H0	R/W	
	1	–	0	–	R	
	0	IOSCSTAIE	0	H0	R/W	

Bits 15–5, 3, 1 Reserved

Bit 4 IOSCTEDIE
Bit 2 OSC3STAIE
Bit 0 IOSCSTAIE

These bits enable the CLG interrupts.
1 (R/W): Enable interrupts
0 (R/W): Disable interrupts

Each bit corresponds to the interrupt as follows:
CLGINTE.IOSCTEDIE bit: IOSC oscillation auto-trimming completion interrupt
CLGINTE.OSC3STAIE bit: OSC3 oscillation stabilization waiting completion interrupt
CLGINTE.IOSCSTAIE bit: IOSC oscillation stabilization waiting completion interrupt

CLG FOUT Control Register 0

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
CLGFOUT0	15–8	–	0x00	–	R	–
	7	–	0	–	R	
	6–4	FOUTDIV[2:0]	0x0	H0	R/W	
	3–2	FOUTSRC[1:0]	0x0	H0	R/W	
	1	–	0	–	R	
	0	FOUTEN	0	H0	R/W	

Bits 15–7 Reserved

Bits 6–4 FOUTDIV[2:0]

These bits set the FOUT0 clock division ratio.

Bits 3–2 FOUTSRC[1:0]

These bits select the FOUT0 clock source.

Table 2.6.6 FOUT0 Clock Source and Division Ratio Settings

CLGFOUT0. FOUTDIV[2:0] bits	CLGFOUT0.FOUTSRC[1:0] bits			
	0x0	0x1	0x2	0x3
	IOSCCLK	OSC1CLK	OSC3CLK	SYSCLK
0x7	1/128	1/32,768	1/128	Reserved
0x6	1/64	1/4,096	1/64	Reserved
0x5	1/32	1/1,024	1/32	Reserved
0x4	1/16	1/256	1/16	Reserved
0x3	1/8	1/8	1/8	Reserved
0x2	1/4	1/4	1/4	Reserved
0x1	1/2	1/2	1/2	Reserved
0x0	1/1	1/1	1/1	1/1

Note: When the CLGFOUT0.FOUTSRC[1:0] bits are set to 0x3, the FOUT0 output will be stopped in SLEEP/HALT mode as SYSCLK is stopped.

Bit 1 Reserved

Bit 0 FOUTEN

This bit controls the FOUT0 clock external output.
1 (R/W): Enable external output
0 (R/W): Disable external output

Note: Since the FOUT0 signal generated is out of sync with writings to the CLGFOUT0.FOUTEN bit, a glitch may occur when the FOUT0 output is enabled or disabled.

CLG Oscillation Frequency Trimming Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
CLGTRIM	15–14	–	0x0	–	R	–
	13–8	OSC3AJ[5:0]	*	H0	R/WP	* Determined by factory adjustment.
	7–6	–	0x0	–	R	–
	5–0	IOSCAJ[5:0]	*	H0	R/WP	* Determined by factory adjustment.

Bits 15–14 Reserved

Bits 13–8 OSC3AJ[5:0]

These bits sets the frequency trimming value for the OSC3 internal oscillator circuit.
This setting affects all the frequencies from 500 kHz to 16 MHz.

Table 2.6.7 Frequency Trimming Setting of OSC3 Internal Oscillator Circuit

CLGTRIM.OSC3AJ[5:0] bits	OSC3 internal oscillator frequency
0x3f	High
:	:
0x00	Low

Bits 7–6 Reserved

Bits 5–0 IOSCAJ[5:0]

These bits sets the frequency trimming value for the IOSC internal oscillator circuit.

Table 2.6.8 Frequency Trimming Setting of IOSC Internal Oscillator Circuit

CLGTRIM.IOSCAJ[5:0] bits	IOSC internal oscillator frequency
0x3f	High
:	:
0x00	Low

Note: The initial values of the CLGTRIM.OSC3AJ[5:0] and CLGTRIM.IOSCAJ[5:0] bits were adjusted so that the OSC3 and IOSC oscillator circuit characteristics described in the “Electrical Characteristics” chapter can be guaranteed. Be aware that the frequency characteristics may not be satisfied when these settings are altered. When altering these settings, always make sure that the relevant oscillator circuit is inactive.

3 CPU and Debugger

3.1 Overview

This IC incorporates the Seiko Epson original 16-bit CPU core (S1C17) with a debugger. The main features of the CPU core are listed below.

- Seiko Epson original 16-bit RISC processor
  - 24-bit general-purpose registers: 8
  - 24-bit special registers: 2
  - 8-bit special register: 1
  - Up to 16M bytes of memory space (24-bit address)
  - Harvard architecture using separated instruction bus and data bus
- Compact and fast instruction set optimized for development in C language
  - Code length: 16-bit fixed length
  - Number of instructions: 111 basic instructions (184 including variations)
  - Execution cycle: Main instructions are executed in one cycle.
  - Extended immediate instructions: Immediate data can be extended up to 24 bits.
- Supports reset, NMI, address misaligned, debug, and external interrupts.
  - Reads a vector from the vector table and branches to the interrupt handler routine directly.
  - Can generate software interrupts with a vector number specified (all vector numbers specifiable).
- HALT mode (halt instruction) and SLEEP mode (slp instruction) are provided as the standby function.
- Incorporates a debugger with three-wire communication interface to assist in software development.

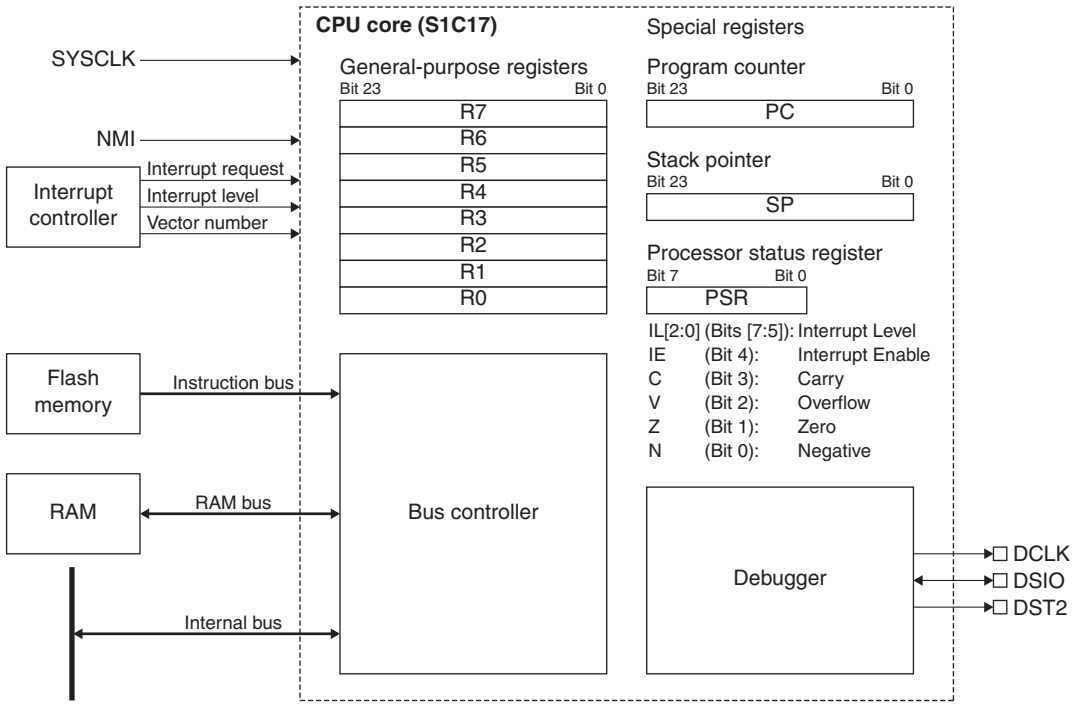


Figure 3.1.1 S1C17 Configuration

3.2 CPU Core

3.2.1 CPU Registers

The CPU includes eight general-purpose registers and three special registers (Table 3.2.1.1).

Table 3.2.1.1 Initialization of CPU Registers

CPU register name			Initial	Reset
General-purpose registers		R0 to R7	0x000000	H0
Special registers	Program counter	PC	The reset vector is automatically loaded.	H0
	Stack pointer	SP	0x000000	H0
	Processor status register	PSR	0x00	H0

For details on the CPU registers, refer to the "S1C17 Family S1C17 Core Manual." For more information on the reset vector, refer to the "Interrupt Controller" chapter.

3.2.2 Instruction Set

The CPU instruction codes are all fixed to 16 bits in length which, combined with pipelined processing, allows the most important instructions to be executed in one cycle. For details on the instructions, refer to the "S1C17 Family S1C17 Core Manual."

3.2.3 Reading PSR

The PSR contents can be read through the MSCPSR register. Note, however, that data cannot be written to PSR through the MSCPSR register.

3.2.4 I/O Area Reserved for the S1C17 Core

The address range from 0xfffc00 to 0xffffff is the I/O area reserved for the S1C17 core. Do not access this area except when it is required.

3.3 Debugger

3.3.1 Debugging Functions

The debugger provides the following functions:

- Instruction break: A debug interrupt is generated immediately before the set instruction address is executed. An instruction break can be set at up to four addresses.
- Single step: A debug interrupt is generated after each instruction has been executed.
- Forcible break: A debug interrupt is generated using an external input signal.
- Software break: A debug interrupt is generated when the brk instruction is executed.

When a debug interrupt occurs, the CPU enters DEBUG mode. The peripheral circuit operations in DEBUG mode depend on the setting of the DBRUN bit provided in the clock control register of each peripheral circuit. For more information on the DBRUN bit, refer to "Clock Supply in DEBUG Mode" in each peripheral circuit chapter. DEBUG mode continues until a cancel command is sent from the personal computer or the CPU executes the retd instruction. Neither hardware interrupts nor NMI are accepted during DEBUG mode.

3.3.2 Resource Requirements and Debugging Tools

Debugging work area

Debugging requires a 64-byte debugging work area. For more information on the work area location, refer to the "Memory and Bus" chapter. The start address of this debugging work area can be read from the DBRAM register.

Debugging tools

To perform debugging, connect ICDmini (S5U1C17001H) to the input/output pin for the debugger embedded in this IC and control it from the personal computer. This requires the tools shown below.

- S1C17 Family In-Circuit Debugger ICDmini (S5U1C17001H)
- S1C17 Family C Compiler Package (e.g., S5U1C17001C)

3.3.3 List of Debugger Input/Output Pins

Table 3.3.3.1 lists the debug pins.

Table 3.3.3.1 List of Debug Pins

Pin name	I/O	Initial state	Function
DCLK	O	O	On-chip debugger clock output pin Outputs a clock to the ICDmini (S5U1C17001H).
DSIO	I/O	I	On-chip debugger data input/output pin Used to input/output debugging data and input the break signal.
DST2	O	O	On-chip debugger status output pin Outputs the processor status during debugging.

The debugger input/output pins are shared with general-purpose I/O ports and are initially set as the debug pins. If the debugging function is not used, these pins can be switched to general-purpose I/O port pins. For details, refer to the "I/O Ports" chapter.

Notes: • Do not drive the DCLK pin with a high level from outside (e.g. pulling up with a resistor). Also, do not connect (short-circuit) between the DCLK pin and another GPIO port. In the both cases, the IC may not start up normally due to unstable pin input/output status at power on.

• Do not drive the DSIO pin with a low level from outside, as it generates a debug interrupt that puts the CPU into DEBUG mode.

3.3.4 External Connection

Figure 3.3.4.1 shows a connection example between this IC and ICDmini when performing debugging.

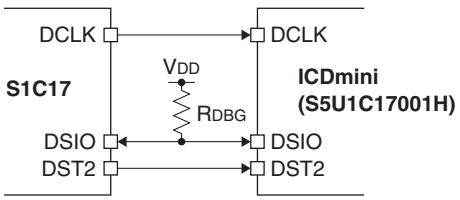


Figure 3.3.4.1 External Connection

For the recommended pull-up resistor value, refer to "Recommended Operating Conditions, DSIO pull-up resistor R_{DBG}" in the "Electrical Characteristics" chapter. R_{DBG} is not required when using the DSIO pin as a general-purpose I/O port pin.

3.3.5 Flash Security Function

This IC provides a security function to protect the internal Flash memory from unauthorized reading and tampering by using the debugger through ICDmini. Figure 3.3.5.1 shows a Flash security function setting flow.

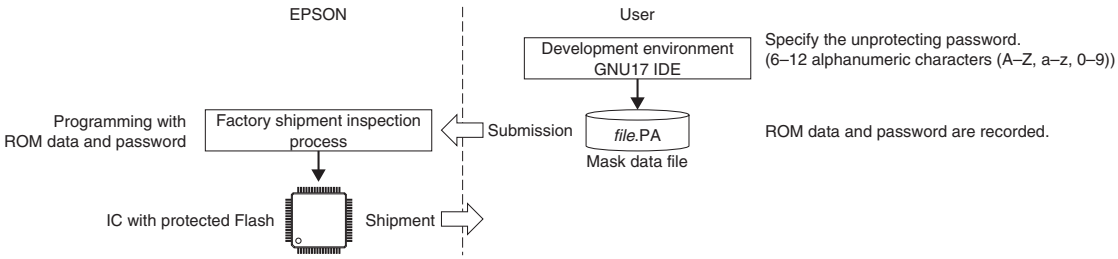


Figure 3.3.5.1 Shipment of IC with ROM Data Programmed and Flash Security Function Setting Flow

The following shows the status of the IC with protected Flash:

- The Flash memory data is undefined if it is read from the debugger.
- An error occurs if an attempt is made to program the Flash memory through ICDmini.

However, the Flash security function can be disabled by entering the unprotecting password predefined to GNU17 IDE (the security function will take effect again after a reset). For setting the password, refer to the "(S1C17 Family C Compiler Package) S5U1C17001C Manual."

Note: Disable the Flash security function before debugging an IC with protected Flash via ICDmini. The debugging functions may not run normally if the Flash security function is enabled.

3.4 Control Register

MISC PSR Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
MSCPSR	15–8	–	0x00	–	R	–
	7–5	PSRIL[2:0]	0x0	H0	R	
	4	PSRIE	0	H0	R	
	3	PSRC	0	H0	R	
	2	PSRV	0	H0	R	
	1	PSRZ	0	H0	R	
	0	PSRN	0	H0	R	

Bits 15–8 Reserved

Bits 7–5 PSRIL[2:0]

The value (0 to 7) of the PSR IL[2:0] (interrupt level) bits can be read out with these bits.

Bit 4 PSRIE

The value (0 or 1) of the PSR IE (interrupt enable) bit can be read out with this bit.

Bit 3 PSRC

The value (0 or 1) of the PSR C (carry) flag can be read out with this bit.

Bit 2 PSRV

The value (0 or 1) of the PSR V (overflow) flag can be read out with this bit.

Bit 1 PSRZ

The value (0 or 1) of the PSR Z (zero) flag can be read out with this bit.

Bit 0 PSRN

The value (0 or 1) of the PSR N (negative) flag can be read out with this bit.

Debug RAM Base Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
DBRAM	31–24	–	0x00	–	R	–
	23–0	DBRAM[23:0]	*1	H0	R	

*1 Debugging work area start address

Bits 31–24 Reserved

Bits 23–0 DBRAM[23:0]

The start address of the debugging work area (64 bytes) can be read out with these bits.

4 Memory and Bus

4.1 Overview

This IC supports up to 16M bytes of accessible memory space for both instructions and data.
The features are listed below.

- Embedded Flash memory that supports on-board programming
- All memory and control registers are accessible in 16-bit width and one cycle.
- Write-protect function to protect system control registers

Figure 4.1.1 shows the memory map.

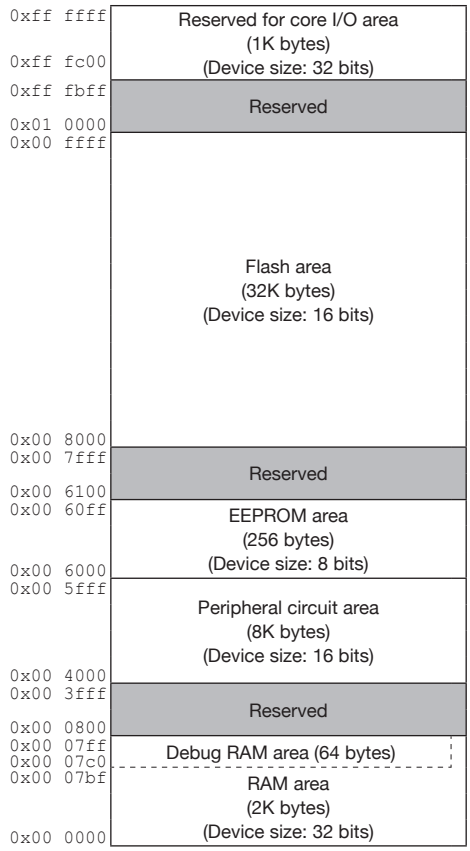


Figure 4.1.1 Memory Map

4.2 Bus Access Cycle

The CPU uses the system clock for bus access operations. First, "Bus access cycle," "Device size," and "Access size" are defined as follows:

- Bus access cycle: One system clock period = 1 cycle
- Device size: Bit width of the memory and peripheral circuits that can be accessed in one cycle
- Access size: Access size designated by the CPU instructions (e.g., ld %rd, [%rb] → 16-bit data transfer)

Table 4.2.1 lists numbers of bus access cycles by different device size and access size. The peripheral circuits can be accessed with an 8-bit, 16-bit, or 32-bit instruction.

Table 4.2.1 Number of Bus Access Cycles

Device size	Access size	Number of bus access cycles
8 bits	8 bits	1
	16 bits	2
	32 bits	4
16 bits	8 bits	1
	16 bits	1
	32 bits	2
32 bits	8 bits	1
	16 bits	1
	32 bits	1

Note: When data is transferred to a memory in 32-bit access, the eight high-order bits are written to the memory as 0x00 since the bit width of the S1C17 core general-purpose registers is 24 bits. Conversely when sending from a memory to a register, the eight high-order bits are ignored.
The CPU performs 32-bit access for stack operations in an interrupt handling. In this case, the CPU read/write 32-bit data that consists of the PSR value as the eight high-order bits and the return address as the 24 low-order bits. For more information, refer to the "S1C17 Family S1C17 Core Manual."

The CPU adopts Harvard architecture that allows simultaneous processing of an instruction fetch and a data access. However, they are not performed simultaneously under one of the conditions listed below. This prolongs the instruction fetch cycle for the number of data area bus cycles.

- When the CPU executes an instruction stored in the Flash area and accesses data in the Flash area
- When the CPU executes an instruction stored in the Flash area and accesses data in the EEPROM area
- When the CPU executes an instruction stored in the internal RAM area and accesses data in the internal RAM area/EEPROM area

4.3 Flash Memory

The Flash memory is used to store application programs and data. Address 0x8000 in the Flash area is defined as the vector table base address by default, therefore a vector table must be located beginning from this address. For more information on the vector table, refer to "Vector Table" in the "Interrupt Controller" chapter.

4.3.1 Flash Memory Pin

Table 4.3.1.1 shows the Flash memory pin.

Table 4.3.1.1 Flash Memory Pin

Pin name	I/O	Initial status	Function
VPP	P	–	Flash programming power supply

For the VPP voltage, refer to "Recommended Operating Conditions, Flash programming voltage VPP" in the "Electrical Characteristics" chapter.

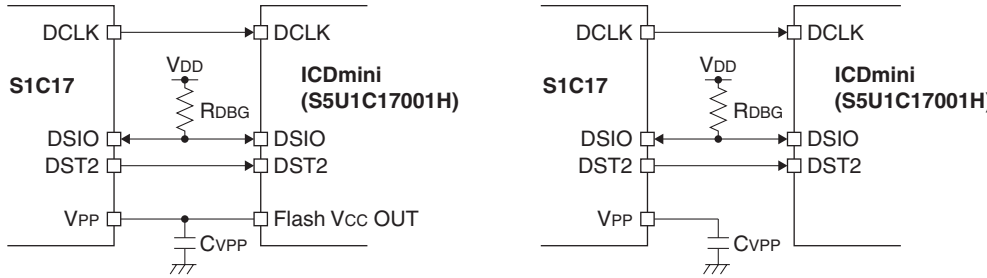
Note: Always leave the VPP pin open except when programming the Flash memory.

4.3.2 Flash Bus Access Cycle Setting

There is a limit of frequency to access the Flash memory with no wait cycle, therefore, the number of bus access cycles for reading must be changed according to the system clock frequency. The number of bus access cycles for reading can be configured using the FLASHCWAIT.RDWAIT[1:0] bits. Select a setting for higher frequency than the system clock.

4.3.3 Flash Programming

The Flash memory supports on-board programming, so it can be programmed with the ROM data by using the debugger through an ICDmini. Figure 4.3.3.1 shows connection diagrams for on-board programming.



(1) When VPP is supplied externally (2) When VPP is generated internally

Figure 4.3.3.1 External Connection

The VPP pin must be left open except when programming the Flash memory. However, it is not necessary to disconnect the wire when using ICDmini to supply the VPP voltage, as ICDmini controls the power supply so that it will be supplied during Flash programming only. The VPP voltage can also be generated by the internal power supply for generating the Flash programming voltage. Be sure to connect CVPP for stabilizing the voltage when the VPP voltage is supplied externally or for generating the voltage when the internal power supply is used.
For detailed information on ROM data programming method, refer to the "(S1C17 Family C Compiler Package) S5U1C17001C Manual." The IC can also be shipped after being programmed in the factory with the ROM data developed. Should you desire to ship the IC with ROM data programmed from the factory, please contact our customer support.

Notes: • When programming the Flash memory, 2.2 V or more VDD voltage is required.

• Be sure to avoid using the VPP pin output for driving external circuits when the VPP voltage is generated internally.

4.4 EEPROM

This MCU includes an EEPROM that can be reprogrammed in one-byte units. This EEPROM supports 8-bit reading only, therefore, no instruction code can be stored.

4.4.1 EEPROM Pin

Table 4.4.1.1 shows the EEPROM pin.

Table 4.4.1.1 EEPROM Pin

Pin name	I/O	Initial status	Function
VPP	P	–	EEPROM programming power supply

When reprogramming the EEPROM, the EEPROM controller (EEPROMC) uses the VPP voltage generated internally. Connect CVPP to the VPP pin as shown in "(2) When VPP is generated internally" of Figure 4.3.3.1. The notes described in Section 4.3.3 are also applied to EEPROM reprogramming.

4.4.2 Operations of EEPROM

Reprogramming EEPROM data

Follow the procedure below to reprogram the EEPROM.

1. Write 0x0096 to the MSCPROT.PROT[15:0] bits. (Remove system protection)
2. Set the following EPRCCTL0 register bits:
   - Set the EPRCCTL0.EP_WMODE bit to 1. (Start reprogramming mode)
   - Set the EPRCCTL0.EP_PWRSET bit to 1. (Turn programming power supply on)
3. Wait for the programming power supply to stabilize (for the wait time, refer to "EEPROM Characteristics" in the "Electrical Characteristics" chapter).
4. Write 1 to the EPRCINTF.RXBIF bit. (Clear interrupt flag)
5. Set the EPRCINTE.RXBIF bit to 1. (Enable interrupt)
6. Set the EPRCADR.EP_ADDR[7:0] bits. (Set reprogramming address)
7. Set the EPRCWDAT.EP_WDAT[7:0] bits. (Set programming data)
   The programming data should be stored in the RAM for the verification to be performed later.
8. Write 1 to the EPRCCTL1.EP_CK bit. (Output clock pulse)
9. Wait for an interrupt.
   When the reprogramming has completed, the EPRCINTF.RXBIF bit is set to 1.
10. Repeat Steps 4 to 9 for the addresses to be programmed.
11. Set the following EPRCCTL0 register bits:
    - Set the EPRCCTL0.EP_WMODE bit to 0. (Stop reprogramming mode)
    - Set the EPRCCTL0.EP_PWRSET bit to 0. (Turn programming power supply off)
12. Write a value other than 0x0096 to the MSCPROT.PROT[15:0] bits. (Set system protection)
13. Read EEPROM data and verify it with the programming data.

Reading EEPROM data

EEPROM data can be read from the memory area (logical address) where the EEPROM has been assigned using a standard 8-bit memory read instruction. If a 16-bit or 32-bit memory read instruction is used, only 8 bits are read from the EEPROM and the high-order bits are all set to 0. Note that EEPROM data is indefinite if it is read while the EPRCCTL0.EP_WMODE bit = 1 (reprogramming mode). When a ECC interrupt has occurred during reading data, the EPRCINTF.ECCERIF bit is set to 1.

Note: If an ECC interrupt has occurred, the reprogramming count may reach the limit. In this case, copy the data to another address and the address that generates an ECC interrupt should not be used in the subsequent reprogramming.

4.4.3 Interrupts

EEPROMC has a function to generate the interrupts shown in Table 4.4.3.1.

Table 4.4.3.1 EEPROMC Interrupt Function

Interrupt	Interrupt flag	Set condition	Clear condition
Reprogram/read completion	EPRCINTF.RXBIF	When reprogramming/reading of the EEPROM has completed	Writing 1
ECC	EPRCINTF.ECCERIF	When data has been corrected via ECC during data reading	Writing 1

The EEPROMC provides interrupt enable bits corresponding to each interrupt flag. An interrupt request is sent to the interrupt controller only when the interrupt flag, of which interrupt has been enabled by the interrupt enable bit, is set. For more information on interrupt control, refer to the "Interrupt Controller" chapter.

4.5 RAM

The RAM can be used to execute the instruction codes copied from another memory as well as storing variables or other data. This allows higher speed processing and lower power consumption than Flash memory.

Note: The 64 bytes at the end of the RAM is reserved as the debug RAM area. When using the debug functions under application development, do not access this area from the application program. This area can be used for applications of mass-produced devices that do not need debugging.

The RAM size used by the application can be configured to equal or less than the implemented size using the MSCIRAMSZ.IRAMSZ[2:0] bits. For example, this function can be used to prevent creating programs that seek to access areas outside the RAM area of the target model when developing an application for a model in which the RAM size is smaller than this IC. After the limitation is applied, accessing an address outside the RAM area results in the same operation (undefined value is read out) as when a reserved area is accessed.

4.6 Peripheral Circuit Control Registers

The control registers for the peripheral circuits are located in the 8K-byte area beginning with address 0x4000. Table 4.6.1 shows the control register map. For details of each control register, refer to "List of Peripheral Circuit Registers" in the appendix or "Control Registers" in each peripheral circuit chapter.

Table 4.6.1 Peripheral Circuit Control Register Map

Peripheral circuit	Address	Register name	
MISC registers (MISC)	0x4000	MSCPROT	MISC System Protect Register
	0x4002	MSCIRAMSZ	MISC IRAM Size Register
	0x4004	MSCTTBRL	MISC Vector Table Address Low Register
	0x4006	MSCTTBRH	MISC Vector Table Address High Register
	0x4008	MSCPSR	MISC PSR Register
Power generator (PWG)	0x4020	PWGVD1CTL	PWG V_{D1} Control Register
Clock generator (CLG)	0x4040	CLGSCLK	CLG System Clock Control Register
	0x4042	CLGOSC	CLG Oscillation Control Register
	0x4044	CLGIOSC	CLG IOSC Control Register
	0x4046	CLGOSC1TRIM	CLG OSC1 Trimming Register
	0x4048	CLGOSC3	CLG OSC3 Control Register
	0x404c	CLGINTF	CLG Interrupt Flag Register
	0x404e	CLGINTE	CLG Interrupt Enable Register
	0x4050	CLGFOUT0	CLG FOUT Control Register 0
	0x4054	CLGTRIM	CLG Oscillation Frequency Trimming Register
Interrupt controller (ITC)	0x4080	ITCLV0	ITC Interrupt Level Setup Register 0
	0x4082	ITCLV1	ITC Interrupt Level Setup Register 1
	0x4084	ITCLV2	ITC Interrupt Level Setup Register 2
	0x4086	ITCLV3	ITC Interrupt Level Setup Register 3
	0x4088	ITCLV4	ITC Interrupt Level Setup Register 4
	0x408a	ITCLV5	ITC Interrupt Level Setup Register 5
	0x408c	ITCLV6	ITC Interrupt Level Setup Register 6
	0x408e	ITCLV7	ITC Interrupt Level Setup Register 7
	0x4090	ITCLV8	ITC Interrupt Level Setup Register 8
Watchdog timer (WDT2)	0x40a0	WDTCLK	WDT2 Clock Control Register
	0x40a2	WDTCTL	WDT2 Control Register
	0x40a4	WDTCMP	WDT2 Counter Compare Match Register
Supply voltage detector (SVD3)	0x4100	SVDCLK	SVD3 Clock Control Register
	0x4102	SVDCTL	SVD3 Control Register
	0x4104	SVDINTF	SVD3 Status and Interrupt Flag Register
	0x4106	SVDINTE	SVD3 Interrupt Enable Register
16-bit timer (T16) Ch.0	0x4160	T16_0CLK	T16 Ch.0 Clock Control Register
	0x4162	T16_0MOD	T16 Ch.0 Mode Register
	0x4164	T16_0CTL	T16 Ch.0 Control Register
	0x4166	T16_0TR	T16 Ch.0 Reload Data Register
	0x4168	T16_0TC	T16 Ch.0 Counter Data Register
	0x416a	T16_0INTF	T16 Ch.0 Interrupt Flag Register
	0x416c	T16_0INTE	T16 Ch.0 Interrupt Enable Register

Peripheral circuit	Address	Register name	
Flash controller (FLASHC)	0x41b0	FLASHCWAIT	FLASHC Flash Read Cycle Register
EEPROM controller (EEPROMC)	0x41c0	EPRCCTL0	EEPROMC Control Register 0
	0x41c2	EPRCCTL1	EEPROMC Control Register 1
	0x41c4	EPRCADR	EEPROMC Address Register
	0x41c6	EPRCWDAT	EEPROMC Write Data Register
	0x41c8	EPRCINTF	EEPROMC Interrupt Flag Register
	0x41ca	EPRCINTE	EEPROMC Interrupt Enable Register
I/O ports (PPORT)	0x4200	P0DAT	P0 Port Data Register
	0x4202	P0IOEN	P0 Port Enable Register
	0x4204	P0RCTL	P0 Port Pull-up/down Control Register
	0x4206	P0INTF	P0 Port Interrupt Flag Register
	0x4208	P0INTCTL	P0 Port Interrupt Control Register
	0x420a	P0CHATEN	P0 Port Chattering Filter Enable Register
	0x420c	P0MODSEL	P0 Port Mode Select Register
	0x420e	P0FNCSEL	P0 Port Function Select Register
	0x4210	P1DAT	P1 Port Data Register
	0x4212	P1IOEN	P1 Port Enable Register
	0x4214	P1RCTL	P1 Port Pull-up/down Control Register
	0x4216	P1INTF	P1 Port Interrupt Flag Register
	0x4218	P1INTCTL	P1 Port Interrupt Control Register
	0x421a	P1CHATEN	P1 Port Chattering Filter Enable Register
	0x421c	P1MODSEL	P1 Port Mode Select Register
	0x421e	P1FNCSEL	P1 Port Function Select Register
	0x42d0	PDDAT	Pd Port Data Register
	0x42d2	PDIOEN	Pd Port Enable Register
	0x42d4	PDRCTL	Pd Port Pull-up/down Control Register
	0x42dc	PDMODSEL	Pd Port Mode Select Register
	0x42de	PDFNCSEL	Pd Port Function Select Register
	0x42e0	PCLK	P Port Clock Control Register
	0x42e2	PINTFGRP	P Port Interrupt Flag Group Register
Universal port multiplexer (UPMUX)	0x4300	P0UPMUX0	P00–01 Universal Port Multiplexer Setting Register
	0x4302	P0UPMUX1	P02–03 Universal Port Multiplexer Setting Register
	0x4304	P0UPMUX2	P04–05 Universal Port Multiplexer Setting Register
	0x4306	P0UPMUX3	P06–07 Universal Port Multiplexer Setting Register
	0x4308	P1UPMUX0	P10–11 Universal Port Multiplexer Setting Register
	0x430a	P1UPMUX1	P12–13 Universal Port Multiplexer Setting Register
	0x430c	P1UPMUX2	P14–15 Universal Port Multiplexer Setting Register
UART (UART3) Ch.0	0x4380	UA0CLK	UART3 Ch.0 Clock Control Register
	0x4382	UA0MOD	UART3 Ch.0 Mode Register
	0x4384	UA0BR	UART3 Ch.0 Baud-Rate Register
	0x4386	UA0CTL	UART3 Ch.0 Control Register
	0x4388	UA0TXD	UART3 Ch.0 Transmit Data Register
	0x438a	UA0RXD	UART3 Ch.0 Receive Data Register
	0x438c	UA0INTF	UART3 Ch.0 Status and Interrupt Flag Register
	0x438e	UA0INTE	UART3 Ch.0 Interrupt Enable Register
	0x4390	UA0CAWF	UART3 Ch.0 Carrier Waveform Register
16-bit timer (T16) Ch.1	0x43a0	T16_1CLK	T16 Ch.1 Clock Control Register
	0x43a2	T16_1MOD	T16 Ch.1 Mode Register
	0x43a4	T16_1CTL	T16 Ch.1 Control Register
	0x43a6	T16_1TR	T16 Ch.1 Reload Data Register
	0x43a8	T16_1TC	T16 Ch.1 Counter Data Register
	0x43aa	T16_1INTF	T16 Ch.1 Interrupt Flag Register
	0x43ac	T16_1INTE	T16 Ch.1 Interrupt Enable Register
Synchronous serial interface (SPIA) Ch.0	0x43b0	SPI0MOD	SPIA Ch.0 Mode Register
	0x43b2	SPI0CTL	SPIA Ch.0 Control Register
	0x43b4	SPI0TXD	SPIA Ch.0 Transmit Data Register
	0x43b6	SPI0RXD	SPIA Ch.0 Receive Data Register
	0x43b8	SPI0INTF	SPIA Ch.0 Interrupt Flag Register
	0x43ba	SPI0INTE	SPIA Ch.0 Interrupt Enable Register
I²C (I2C)	0x43c0	I2C0CLK	I2C Ch.0 Clock Control Register
	0x43c2	I2C0MOD	I2C Ch.0 Mode Register
	0x43c4	I2C0BR	I2C Ch.0 Baud-Rate Register

Peripheral circuit	Address	Register name	
I²C (I2C)	0x43c8	I2C0OADR	I2C Ch.0 Own Address Register
	0x43ca	I2C0CTL	I2C Ch.0 Control Register
	0x43cc	I2C0TXD	I2C Ch.0 Transmit Data Register
	0x43ce	I2C0RXD	I2C Ch.0 Receive Data Register
	0x43d0	I2C0INTF	I2C Ch.0 Status and Interrupt Flag Register
	0x43d2	I2C0INTE	I2C Ch.0 Interrupt Enable Register
SPI slave selector (SPISLV_SEL)	0x43e0	SPISLVSEL	SPI Slave Select Register
16-bit PWM timer (T16B) Ch.0	0x5000	T16B0CLK	T16B Ch.0 Clock Control Register
	0x5002	T16B0CTL	T16B Ch.0 Counter Control Register
	0x5004	T16B0MC	T16B Ch.0 Max Counter Data Register
	0x5006	T16B0TC	T16B Ch.0 Timer Counter Data Register
	0x5008	T16B0CS	T16B Ch.0 Counter Status Register
	0x500a	T16B0INTF	T16B Ch.0 Interrupt Flag Register
	0x500c	T16B0INTE	T16B Ch.0 Interrupt Enable Register
	0x5010	T16B0CCCTL0	T16B Ch.0 Compare/Capture 0 Control Register
	0x5012	T16B0CCR0	T16B Ch.0 Compare/Capture 0 Data Register
	0x5018	T16B0CCCTL1	T16B Ch.0 Compare/Capture 1 Control Register
	0x501a	T16B0CCR1	T16B Ch.0 Compare/Capture 1 Data Register
16-bit PWM timer (T16B) Ch.1	0x5040	T16B1CLK	T16B Ch.1 Clock Control Register
	0x5042	T16B1CTL	T16B Ch.1 Counter Control Register
	0x5044	T16B1MC	T16B Ch.1 Max Counter Data Register
	0x5046	T16B1TC	T16B Ch.1 Timer Counter Data Register
	0x5048	T16B1CS	T16B Ch.1 Counter Status Register
	0x504a	T16B1INTF	T16B Ch.1 Interrupt Flag Register
	0x504c	T16B1INTE	T16B Ch.1 Interrupt Enable Register
	0x5050	T16B1CCCTL0	T16B Ch.1 Compare/Capture 0 Control Register
	0x5052	T16B1CCR0	T16B Ch.1 Compare/Capture 0 Data Register
	0x5058	T16B1CCCTL1	T16B Ch.1 Compare/Capture 1 Control Register
	0x505a	T16B1CCR1	T16B Ch.1 Compare/Capture 1 Data Register
Smart card interface (SMCIF) Ch.0	0x5220	SMC0CLK	SMCIF Ch.0 Clock Control Register
	0x5222	SMC0MOD	SMCIF Ch.0 Mode Register
	0x5224	SMC0BR	SMCIF Ch.0 Baud Rate Register
	0x5226	SMC0CTL	SMCIF Ch.0 Control Register
	0x5228	SMC0TXD	SMCIF Ch.0 Transmit Data Register
	0x522a	SMC0RXD	SMCIF Ch.0 Receive Data Register
	0x522c	SMC0WTC0	SMCIF Ch.0 Wait Time Compare Data Register 0
	0x522e	SMC0WTC1	SMCIF Ch.0 Wait Time Compare Data Register 1
	0x5230	SMC0GTC	SMCIF Ch.0 Guard Time Compare Data Register
	0x5232	SMC0INTF	SMCIF Ch.0 Status and Interrupt Flag Register
	0x5234	SMC0INTE	SMCIF Ch.0 Interrupt Enable Register
	0x5236	SMC0ETU0	SMCIF Ch.0 Etu Counter Data Register 0
	0x5238	SMC0ETU1	SMCIF Ch.0 Etu Counter Data Register 1
16-bit timer (T16) Ch.3	0x5260	T16_3CLK	T16 Ch.3 Clock Control Register
	0x5262	T16_3MOD	T16 Ch.3 Mode Register
	0x5264	T16_3CTL	T16 Ch.3 Control Register
	0x5266	T16_3TR	T16 Ch.3 Reload Data Register
	0x5268	T16_3TC	T16 Ch.3 Counter Data Register
	0x526a	T16_3INTF	T16 Ch.3 Interrupt Flag Register
	0x526c	T16_3INTE	T16 Ch.3 Interrupt Enable Register
Synchronous serial interface (SPIA) Ch.1	0x5270	SPI1MOD	SPIA Ch.1 Mode Register
	0x5272	SPI1CTL	SPIA Ch.1 Control Register
	0x5274	SPI1TXD	SPIA Ch.1 Transmit Data Register
	0x5276	SPI1RXD	SPIA Ch.1 Receive Data Register
	0x5278	SPI1INTF	SPIA Ch.1 Interrupt Flag Register
	0x527a	SPI1INTE	SPIA Ch.1 Interrupt Enable Register
Sound generator (SNDA)	0x5300	SNDCLK	SNDA Clock Control Register
	0x5302	SNDSEL	SNDA Select Register
	0x5304	SNDCTL	SNDA Control Register
	0x5306	SNDDAT	SNDA Data Register
	0x5308	SNDINTF	SNDA Interrupt Flag Register
	0x530a	SNDINTE	SNDA Interrupt Enable Register

Peripheral circuit	Address	Register name	
EPD controller/driver (EPDC)	0x5500	EPDTIMCLK	EPDC Timing Clock Control Register
	0x5502	EPDDBLCLK	EPDC Doubler Clock Control Register
	0x5504	EPDBSTCLK	EPDC Booster Clock Control Register
	0x5506	EPDCTL	EPDC Control Register
	0x5508	EPDPWR0	EPDC Power Supply Control Register 0
	0x550a	EPDPWR1	EPDC Power Supply Control Register 1
	0x550c	EPDDSP	EPDC Display Control Register
	0x550e	EPDPOS	EPDC Pin Assignment Select Register
	0x5510	EPDINTF	EPDC Interrupt Flag/Status Register
	0x5512	EPDINTE	EPDC Interrupt Enable Register
	0x5520	EPDTPBP	EPDC Top/Back Plane Data Register
	0x5522	EPDSEG0	EPDC Segment Data Register 0
	0x5524	EPDSEG1	EPDC Segment Data Register 1
	0x5526	EPDSEG2	EPDC Segment Data Register 2
	0x5530	EPDTPBPEN	EPDC Top/Back Plane Enable Register
	0x5532	EPDSEGEN0	EPDC Segment Enable Register 0
	0x5534	EPDSEGEN1	EPDC Segment Enable Register 1
	0x5536	EPDSEGEN2	EPDC Segment Enable Register 2
	0x5540	EPDWAVE0	EPDC Waveform Timing Set Register 0
	0x5542	EPDWAVE1	EPDC Waveform Timing Set Register 1
	0x5544	EPDWAVE2	EPDC Waveform Timing Set Register 2
	0x5546	EPDWAVE3	EPDC Waveform Timing Set Register 3
	0x5548	EPDWAVE4	EPDC Waveform Timing Set Register 4
	0x554a	EPDWAVE5	EPDC Waveform Timing Set Register 5
	0x554c	EPDWAVE6	EPDC Waveform Timing Set Register 6
	0x554e	EPDWAVE7	EPDC Waveform Timing Set Register 7
	0x5550	EPDWAVE8	EPDC Waveform Timing Set Register 8
	0x5552	EPDWAVE9	EPDC Waveform Timing Set Register 9
	0x5554	EPDWAVE10	EPDC Waveform Timing Set Register 10
	0x5556	EPDWAVE11	EPDC Waveform Timing Set Register 11
	0x5558	EPDWAVE12	EPDC Waveform Timing Set Register 12
	0x555a	EPDWAVE13	EPDC Waveform Timing Set Register 13
	0x555c	EPDWAVE14	EPDC Waveform Timing Set Register 14
	0x555e	EPDWAVE15	EPDC Waveform Timing Set Register 15
	0x5560	EPDWAVE16	EPDC Waveform Timing Set Register 16
	0x5562	EPDWAVE17	EPDC Waveform Timing Set Register 17
	0x5564	EPDWAVE18	EPDC Waveform Timing Set Register 18
	0x5566	EPDWAVE19	EPDC Waveform Timing Set Register 19
	0x5568	EPDWAVE20	EPDC Waveform Timing Set Register 20
	0x556a	EPDWAVE21	EPDC Waveform Timing Set Register 21
	0x556c	EPDWAVE22	EPDC Waveform Timing Set Register 22
	0x556e	EPDWAVE23	EPDC Waveform Timing Set Register 23
	0x5570	EPDWAVE24	EPDC Waveform Timing Set Register 24
	0x5572	EPDWAVE25	EPDC Waveform Timing Set Register 25
	0x5574	EPDWAVE26	EPDC Waveform Timing Set Register 26
	0x5576	EPDWAVE27	EPDC Waveform Timing Set Register 27
	0x5578	EPDWAVE28	EPDC Waveform Timing Set Register 28
	0x557a	EPDWAVE29	EPDC Waveform Timing Set Register 29
	0x557c	EPDWAVE30	EPDC Waveform Timing Set Register 30
	0x557e	EPDWAVE31	EPDC Waveform Timing Set Register 31
16-bit timer (T16) Ch.2	0x5480	T16_2CLK	T16 Ch.2 Clock Control Register
	0x5482	T16_2MOD	T16 Ch.2 Mode Register
	0x5484	T16_2CTL	T16 Ch.2 Control Register
	0x5486	T16_2TR	T16 Ch.2 Reload Data Register
	0x5488	T16_2TC	T16 Ch.2 Counter Data Register
	0x548a	T16_2INTF	T16 Ch.2 Interrupt Flag Register
	0x548c	T16_2INTE	T16 Ch.2 Interrupt Enable Register

Peripheral circuit	Address	Register name	
12-bit A/D converter (ADC12A)	0x54a2	ADC12_0CTL	ADC12A Ch.0 Control Register
	0x54a4	ADC12_0TRG	ADC12A Ch.0 Trigger/Analog Input Select Register
	0x54a6	ADC12_0CFG	ADC12A Ch.0 Configuration Register
	0x54a8	ADC12_0INTF	ADC12A Ch.0 Interrupt Flag Register
	0x54aa	ADC12_0INTE	ADC12A Ch.0 Interrupt Enable Register
	0x54ac	ADC12_0AD0D	ADC12A Ch.0 Result Register 0
	0x54ae	ADC12_0AD1D	ADC12A Ch.0 Result Register 1
	0x54b0	ADC12_0AD2D	ADC12A Ch.0 Result Register 2
	0x54b2	ADC12_0AD3D	ADC12A Ch.0 Result Register 3
	0x54b4	ADC12_0AD4D	ADC12A Ch.0 Result Register 4
	0x54b6	ADC12_0AD5D	ADC12A Ch.0 Result Register 5
	0x54b8	ADC12_0AD6D	ADC12A Ch.0 Result Register 6
	0x54ba	ADC12_0AD7D	ADC12A Ch.0 Result Register 7
Temperature sensor/reference voltage generator (TSRVR)	0x54c0	TSRVR0TCTL	TSRVR Ch.0 Temperature Sensor Control Register
	0x54c2	TSRVR0VCTL	TSRVR Ch.0 Reference Voltage Generator Control Register

4.6.1 System-Protect Function

The system-protect function protects control registers and bits from writings. They cannot be rewritten unless write protection is removed by writing 0x0096 to the MSCPROT.PROT[15:0] bits. This function is provided to prevent deadlock that may occur when a system-related register is altered by a runaway CPU. See "Control Registers" in each peripheral circuit to identify the registers and bits with write protection.

Note: Once write protection is removed using the MSCPROT.PROT[15:0] bits, write enabled status is maintained until write protection is applied again. After the registers/bits required have been altered, apply write protection.

4.7 Control Registers

MISC System Protect Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
MSCPROT	15–0	PROT[15:0]	0x0000	H0	R/W	–

Bits 15–0 PROT[15:0]

These bits protect the control registers related to the system against writings.
0x0096 (R/W): Disable system protection
Other than 0x0096 (R/W): Enable system protection

While the system protection is enabled, any data will not be written to the affected control bits (bits with "WP" or "R/WP" appearing in the R/W column).

MISC IRAM Size Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
MSCIRAMSZ	15–9	–	0x00	–	R	–
	8	(reserved)	0	H0	R/WP	Always set to 0.
	7–3	–	0x04	–	R	–
	2–0	IRAMSZ[2:0]	0x2	H0	R/WP	

Bits 15–3 Reserved

Bits 2–0 IRAMSZ[2:0]

These bits set the internal RAM size that can be used.

Table 4.7.1 Internal RAM Size Selections

MSCIRAMSZ.IRAMSZ[2:0] bits	Internal RAM size
0x7–0x3	Reserved
0x2	2KB
0x1	1KB
0x0	512B

FLASHC Flash Read Cycle Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
FLASHCWAIT	15–8	–	0x00	–	R	–
	7–2	–	0x00	–	R	–
	1–0	RDWAIT[1:0]	0x1	H0	R/WP	

Bits 15–2 Reserved

Bits 1–0 RDWAIT[1:0]

These bits set the number of bus access cycles for reading from the Flash memory.

Table 4.7.2 Setting Number of Bus Access Cycles for Flash Read

FLASHCWAIT.RDWAIT[1:0] bits	Number of bus Access cycles	System clock frequency
0x3	4	16.0 MHz (max.)
0x2	3	16.0 MHz (max.)
0x1	2	12.6 MHz (max.)
0x0	1	6.3 MHz (max.)

Note: Be sure to set the FLASHCWAIT.RDWAIT[1:0] bits before the system clock is configured.

EEPROMC Control Register 0

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
EPRCCTL0	15–9	–	0x00	–	R	–
	8	EP_XPOR	1	H0	R/WP	
	7–2	–	0x00	–	R	
	1	EP_PWRSET	0	H0	R/WP	
	0	EP_WMODE	0	H0	R/WP	

Bits 15–9 Reserved

Bit 8 EP_XPOR

This bit controls the reset signal of the EEPROM.
1 (R/W): Negate the reset signal.
0 (R/W): Assert the reset signal.

When a reprogram/read completion interrupt has not occurred (EPRCINTF.RXBIF bit has not been set to 1) after starting an EEPROM reprogramming operation, write 0 to this bit to reset the EEPROM. While this bit is 0, the EEPROM control functions including reading of the EEPROM are all disabled. To resume the EEPROM operations again, write 1 to this bit to cancel reset state after waiting for a time more than the effective EEPROM reset pulse width t_{XPOR} (refer to "EEPROM Characteristics" in the "Electrical Characteristics" chapter).

Bits 7–2 Reserved

Bit 1 EP_PWRSET

This bit controls the programming power supply.
1 (R/W): Programming power supply ON
0 (R/W): Programming power supply OFF

When this bit is set to 1, the EEPROM programming power supply circuit goes on and it generates the EEPROM programming voltage by boosting the V_{PP} voltage. This bit is effective when the EPRCCTL0.EP_WMODE bit = 1.

Bit 0 EP_WMODE

This bit starts/stops reprogramming mode.
1 (R/W): Start reprogramming mode
0 (R/W): Stop reprogramming mode

Setting this bit to 1 puts the EEPROM into reprogramming mode to enable data reprogramming. Note that read data are indefinite when the EEPROM is read while this bit is 1.

EEPROMC Control Register 1

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
EPRCCTL1	15–8	–	0x00	–	R	–
	7–1	–	0x00	–	R	
	0	EP_CK	0	H0	WP	

Bits 15–1 Reserved

Bit 0 EP_CK

This bit controls the clock pulse output to reprogram the EEPROM.

1 (W): Output one clock pulse

0 (W): Ineffective

Writing 1 to this bit outputs a clock to the EEPROM to reprogram the EEPROM address specified by the EPRCADR.EP_ADDR[7:0] bits with the data specified by the EPRCWDAT.EP_WDAT[7:0] bits. This bit automatically reverts to 0 after writing 1.

This bit is effective when the EPRCCTL0.EP_WMODE bit = 1.

EEPROMC Address Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
EPRCADR	15–8	–	0x00	–	R	–
	7–0	EP_ADDR[7:0]	0x00	H0	R/WP	

Bits 15–8 Reserved

Bits 7–0 EP_ADDR[7:0]

These bits specify the EEPROM physical address (0 to 255) to be reprogrammed.

EEPROM (logical) address = 0x6000 + EPRCADR.EP_ADDR[7:0] bits

EEPROMC Write Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
EPRCWDAT	15–8	–	0x00	–	R	–
	7–0	EP_WDAT[7:0]	0x00	H0	R/WP	

Bits 15–8 Reserved

Bits 7–0 EP_WDAT[7:0]

These bits specify the 8-bit data to program the EEPROM.

EEPROMC Interrupt Flag Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
EPRCINTF	15–8	–	0x00	–	R	–
	7–2	–	0x00	–	R	
	1	ECCERIF	0	H0	R/W	Cleared by writing 1.
	0	RXBIF	0	H0	R/W	

Bits 15–2 Reserved

Bit 1 ECCERIF

Bit 0 RXBIF

These bits indicate the EEPROMC interrupt cause occurrence status.

1 (R): Cause of interrupt occurred

0 (R): No cause of interrupt occurred

1 (W): Clear flag

0 (W): Ineffective

The following shows the correspondence between the bit and interrupt:

EPRCINTF.ECCERIF bit: ECC interrupt

EPRCINTF.RXBIF bit: Reprogram/read completion interrupt

EEPROMC Interrupt Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
EPRCINTE	15–8	–	0x00	–	R	–
	7–2	–	0x00	–	R	
	1	ECCERIE	0	H0	R/W	
	0	RXBIE	0	H0	R/W	

Bits 15–2 Reserved

Bit 1 ECCERIE

Bit 0 RXBIE

These bits enable EEPROMC interrupts.
1 (R/W): Enable interrupts
0 (R/W): Disable interrupts

The following shows the correspondence between the bit and interrupt:
EPRCINTE.ECCERIE bit: ECC interrupt
EPRCINTE.RXBIE bit: Reprogram/read completion interrupt

Note: To prevent generating unnecessary interrupts, the corresponding interrupt flag should be cleared before enabling interrupts.

5 Interrupt Controller (ITC)

5.1 Overview

The features of the ITC are listed below.

- Honors interrupt requests from the peripheral circuits and outputs the interrupt request, interrupt level and vector number signals to the CPU.
- The interrupt level of each interrupt source is selectable from among eight levels.
- Priorities of the simultaneously generated interrupts are established from the interrupt level.
- Handles the simultaneously generated interrupts with the same interrupt level as smaller vector number has higher priority.

Figure 5.1.1 shows the configuration of the ITC.

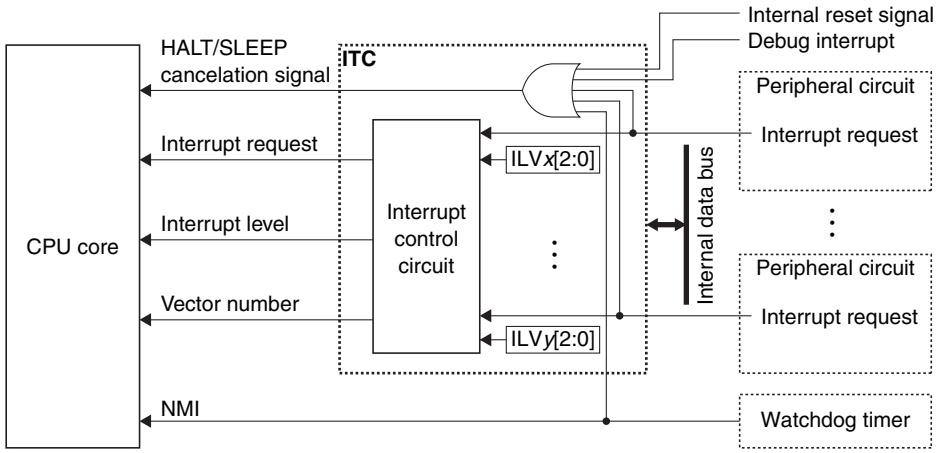


Figure 5.1.1 ITC Configuration

5.2 Vector Table

The vector table contains the vectors to the interrupt handler routines (handler routine start address) that will be read by the CPU to execute the handler when an interrupt occurs.
Table 5.2.1 shows the vector table.

Table 5.2.1 Vector Table

TTBR initial value = 0x8000

Vector number/ Software interrupt number	Vector address	Hardware interrupt name	Cause of hardware interrupt	Priority
0 (0x00)	TTBR + 0x00	Reset	• Low input to the #RESET pin • Power-on reset • Oscillation stop detection reset • Key reset • Watchdog timer overflow *2 • Supply voltage detector reset	1
1 (0x01)	TTBR + 0x04	Address misaligned interrupt	Memory access instruction	2
–	(0xfffc00)	Debugging interrupt	brk instruction, etc.	3
2 (0x02)	TTBR + 0x08	NMI	Watchdog timer overflow *2	4
3 (0x03)	TTBR + 0x0c	Reserved for C compiler	–	–

Vector number/ Software interrupt number	Vector address	Hardware interrupt name	Hardware interrupt flag	Priority
4 (0x04)	TTBR + 0x10	Supply voltage detector interrupt	Low power supply voltage detection	High *1 ↑
5 (0x05)	TTBR + 0x14	Port interrupt	Port input	
6 (0x06)	TTBR + 0x18	reserved	–	
7 (0x07)	TTBR + 0x1c	Clock generator interrupt	• IOSC oscillation stabilization waiting completion • OSC3 oscillation stabilization waiting completion • IOSC oscillation auto-trimming completion	
8 (0x08)	TTBR + 0x20	Real-time clock interrupt	• 1-day, 1-hour, 1-minute, and 1-second • 1/32-second, 1/8-second, 1/4-second, and 1/2-second • Stopwatch 1 Hz, 10 Hz, and 100 Hz • Alarm • Theoretical regulation completion • Down counter underflow	
9 (0x09)	TTBR + 0x24	16-bit timer Ch.0 interrupt	Underflow	
10 (0x0a)	TTBR + 0x28	UART Ch.0 interrupt	• End of transmission • Framing error • Parity error • Overrun error • Receive buffer two bytes full • Receive buffer one byte full • Transmit buffer empty	
11 (0x0b)	TTBR + 0x2c	16-bit timer Ch.1 interrupt	Underflow	
12 (0x0c)	TTBR + 0x30	Synchronous serial interface Ch.0 interrupt	• End of transmission • Receive buffer full • Transmit buffer empty • Overrun error	
13 (0x0d)	TTBR + 0x34	I^2C interrupt	• End of data transfer • General call address reception • NACK reception • STOP condition • START condition • Error detection • Receive buffer full • Transmit buffer empty	
14 (0x0e)	TTBR + 0x38	16-bit PWM timer Ch.0 interrupt	• Capture overwrite • Compare/capture • Counter MAX • Counter zero	
15 (0x0f)	TTBR + 0x3c	16-bit PWM timer Ch.1 interrupt	• Capture overwrite • Compare/capture • Counter MAX • Counter zero	
16 (0x10)	TTBR + 0x40	Smart card interface Ch.0 interrupt	• Wait time error • End of transmission • Error signal detection • Parity error • Overrun error • Receive buffer two bytes full • Receive buffer one byte full • Transmit buffer empty	
17 (0x11)	TTBR + 0x44	Sound generator interrupt	• Sound buffer empty • Sound output completion	
18 (0x12)	TTBR + 0x48	16-bit timer Ch.2 interrupt	Underflow	
19 (0x13)	TTBR + 0x4c	12-bit A/D converter interrupt	• Analog input signal *m* A/D conversion completion • Analog input signal *m* A/D conversion result overwrite error	
20 (0x14)	TTBR + 0x50	EPD controller/driver interrupt	Display update	
21 (0x15)	TTBR + 0x54	EEPROM controller interrupt	• Reprogram/read completion • ECC	
22 (0x16)	TTBR + 0x58	16-bit timer Ch.3 interrupt	Underflow	
23 (0x17)	TTBR + 0x5c	Synchronous serial interface Ch.1 interrupt	• End of transmission • Receive buffer full • Transmit buffer empty • Overrun error	
24 (0x18) : 31 (0x1f)	TTBR + 0x60 : TTBR + 0x7c	reserved : reserved	– : –	↓ Low *1

*1 When the same interrupt level is set

*2 Either reset or NMI can be selected as the watchdog timer interrupt with software.

5.2.1 Vector Table Base Address (TTBR)

The MSCTTBRL and MSCTTBRH registers are provided to set the base (start) address of the vector table in which interrupt vectors are programmed. "TTBR" described in Table 5.2.1 means the value set to these registers. After an initial reset, the MSCTTBRL and MSCTTBRH registers are set to address 0x8000. Therefore, even when the vector table location is changed, it is necessary that at least the reset vector be written to the above address. Bits 7 to 0 in the MSCTTBRL register are fixed at 0, so the vector table always begins from a 256-byte boundary address.

5.3 Initialization

The following shows an example of the initial setting procedure related to interrupts:

1. Execute the di instruction to set the CPU into interrupt disabled state.
2. If the vector table start address is different from the default address, set it to the MSCTTBRL and MSCTTBRH registers after removing system protection by writing 0x0096 to the MSCPROT.PROT[15:0] bits. Then, write a value other than 0x0096 to the MSCPROT.PROT[15:0] bits to set system protection.
3. Set the interrupt enable bit of the peripheral circuit to 0 (interrupt disabled).
4. Set the interrupt level for the peripheral circuit using the ITCLV*x*.ILV*x*[2:0] bits in the ITC.
5. Configure the peripheral circuit and start its operation.
6. Clear the interrupt factor flag of the peripheral circuit.
7. Set the interrupt enable bit of the peripheral circuit to 1 (interrupt enabled).
8. Execute the ei instruction to set the CPU into interrupt enabled state.

5.4 Maskable Interrupt Control and Operations

5.4.1 Peripheral Circuit Interrupt Control

The peripheral circuit that generates interrupts includes an interrupt enable bit and an interrupt flag for each interrupt cause.

Interrupt flag: The flag is set to 1 when the interrupt cause occurs. The clear condition depends on the peripheral circuit.

Interrupt enable bit: By setting this bit to 1 (interrupt enabled), an interrupt request will be sent to the ITC when the interrupt flag is set to 1. When this bit is set to 0 (interrupt disabled), no interrupt request will be sent to the ITC even if the interrupt flag is set to 1. An interrupt request is also sent to the ITC if the status is changed to interrupt enabled when the interrupt flag is 1.

For specific information on causes of interrupts, interrupt flags, and interrupt enable bits, refer to the respective peripheral circuit descriptions.

Note: To prevent occurrence of unnecessary interrupts, the corresponding interrupt flag should be cleared before setting the interrupt enable bit to 1 (interrupt enabled) and before terminating the interrupt handler routine.

5.4.2 ITC Interrupt Request Processing

On receiving an interrupt signal from a peripheral circuit, the ITC sends an interrupt request, the interrupt level, and the vector number to the CPU. Vector numbers are determined by the ITC internal hardware for each interrupt cause, as shown in Table 5.2.1. The interrupt level is a value to configure the priority, and it can be set to between 0 (low) and 7 (high) using the ITCLV*x*.ILV*x*[2:0] bits provided for each interrupt source. The default ITC settings are level 0 for all maskable interrupts. Interrupt requests are not accepted by the CPU if the level is 0.

The ITC outputs the interrupt request with the highest priority to the CPU in accordance with the following conditions if interrupt requests are input to the ITC simultaneously from two or more peripheral circuits.

- The interrupt with the highest interrupt level takes precedence.
- If multiple interrupt requests are input with the same interrupt level, the interrupt with the lowest vector number takes precedence.

The other interrupts occurring at the same time are held until all interrupts with higher priority levels have been accepted by the CPU.
If an interrupt cause with higher priority occurs while the ITC is outputting an interrupt request signal to the CPU (before being accepted by the CPU), the ITC alters the vector number and interrupt level signals to the setting information on the more recent interrupt. The previously occurring interrupt is held. The held interrupt is canceled and no interrupt is generated if the interrupt flag in the peripheral circuit is cleared via software.

Note: Before changing the interrupt level, make sure that no interrupt of which the level is changed can be generated (the interrupt enable bit of the peripheral circuit is set to 0 or the peripheral circuit is deactivated).

5.4.3 Conditions to Accept Interrupt Requests by the CPU

The CPU accepts an interrupt request sent from the ITC when all of the following conditions are met:

- The IE (Interrupt Enable) bit of the PSR has been set to 1.
- The interrupt request that has occurred has a higher interrupt level than the value set in the IL[2:0] (Interrupt Level) bits of the PSR.
- No other interrupt request having higher priority, such as NMI, has occurred.

5.5 NMI

The watchdog timer embedded in this IC can generate a non-maskable interrupt (NMI). This interrupt takes precedence over other interrupts and is unconditionally accepted by the CPU.
For detailed information on generating NMI, refer to the "Watchdog Timer" chapter.

5.6 Software Interrupts

The CPU provides the "int *imm5*" and "intl *imm5*, *imm3*" instructions allowing the software to generate any interrupts. The operand *imm5* specifies a vector number (0–31) in the vector table. In addition to this, the intl instruction has the operand *imm3* to specify the interrupt level (0–7) to be set to the IL[2:0] bits in the PSR. The software interrupt cannot be disabled (non-maskable interrupt). The processor performs the same interrupt processing operation as that of the hardware interrupt.

5.7 Interrupt Processing by the CPU

The CPU samples interrupt requests for each cycle. On accepting an interrupt request, the CPU switches to interrupt processing immediately after execution of the current instruction has been completed.
Interrupt processing involves the following steps:

1. The PSR and current program counter (PC) values are saved to the stack.
2. The PSR IE bit is cleared to 0 (disabling subsequent maskable interrupts).
3. The PSR IL[2:0] bits are set to the received interrupt level. (The NMI does not affect the IL bits.)
4. The vector for the interrupt occurred is loaded to the PC to execute the interrupt handler routine.

When an interrupt is accepted, Step 2 prevents subsequent maskable interrupts. Setting the IE bit to 1 in the interrupt handler routine allows handling of multiple interrupts. In this case, since the IL[2:0] bits are changed by Step 3, only an interrupt with a higher level than that of the currently processed interrupt will be accepted.
Ending interrupt handler routines using the reti instruction returns the PSR to the state before the interrupt occurred. The program resumes processing following the instruction being executed at the time the interrupt occurred.

Note: When HALT or SLEEP mode is canceled, the CPU jumps to the interrupt handler routine after executing one instruction. To execute the interrupt handler routine immediately after HALT or SLEEP mode is canceled, place the nop instruction at just behind the halt/slp instruction.

5.8 Control Registers

MISC Vector Table Address Low Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
MSCTTBRL	15–8	TTBR[15:8]	0x80	H0	R/WP	–
	7–0	TTBR[7:0]	0x00	H0	R	

Bits 15–0 TTBR[15:0]

These bits set the vector table base address (16 low-order bits).

MISC Vector Table Address High Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
MSCTTBRH	15–8	–	0x00	–	R	–
	7–0	TTBR[23:16]	0x00	H0	R/WP	

Bits 15–8 Reserved

Bits 7–0 TTBR[23:16]

These bits set the vector table base address (eight high-order bits).

ITC Interrupt Level Setup Register *x*

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
ITCLV*x*	15–11	–	0x00	–	R	–
	10–8	ILVy_1[2:0]	0x0	H0	R/W	
	7–3	–	0x00	–	R	
	2–0	ILVy_0[2:0]	0x0	H0	R/W	

Bits 15–11 Reserved

Bits 7–3 Reserved

Bits 10–8 ILVy_1[2:0] ($y_1 = 2x + 1$)

Bits 2–0 ILVy_0[2:0] ($y_0 = 2x$)

These bits set the interrupt level of each interrupt.

Table 5.8.1 Interrupt Level and Priority Settings

ITCLV*x*.ILV*y*[2:0] bits	Interrupt level	Priority
0x7	7	High
0x6	6	↑
. . .	. . .	
0x1	1	↓
0x0	0	Low

The following shows the ITCLV*x* register configuration in this IC.

Table 5.8.2 List of ITCLV*x* Registers

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
ITCLV0 (ITC Interrupt Level Setup Register 0)	15–11	–	0x00	–	R	–
	10–8	ILV1[2:0]	0x0	H0	R/W	Port interrupt (ILVPPORT)
	7–3	–	0x00	–	R	–
	2–0	ILV0[2:0]	0x0	H0	R/W	Supply voltage detector interrupt (ILVSVD3)
ITCLV1 (ITC Interrupt Level Setup Register 1)	15–11	–	0x00	–	R	–
	10–8	ILV3[2:0]	0x0	H0	R/W	Clock generator interrupt (ILVCLG)
	7–0	–	0x00	–	R	–
ITCLV2 (ITC Interrupt Level Setup Register 2)	15–11	–	0x00	–	R	–
	10–8	ILV5[2:0]	0x0	H0	R/W	16-bit timer Ch.0 interrupt (ILVT16_0)
	7–3	–	0x00	–	R	–
	2–0	ILV4[2:0]	0x0	H0	R/W	Real-time clock interrupt (ILVRTCB_0)
ITCLV3 (ITC Interrupt Level Setup Register 3)	15–11	–	0x00	–	R	–
	10–8	ILV7[2:0]	0x0	H0	R/W	16-bit timer Ch.1 interrupt (ILVT16_1)
	7–3	–	0x00	–	R	–
	2–0	ILV6[2:0]	0x0	H0	R/W	UART Ch.0 interrupt (ILVUART3_0)
ITCLV4 (ITC Interrupt Level Setup Register 4)	15–11	–	0x00	–	R	–
	10–8	ILV9[2:0]	0x0	H0	R/W	I^2C interrupt (ILVI2C_0)
	7–3	–	0x00	–	R	–
	2–0	ILV8[2:0]	0x0	H0	R/W	Synchronous serial interface Ch.0 interrupt (ILVSPIA_0)
ITCLV5 (ITC Interrupt Level Setup Register 5)	15–11	–	0x00	–	R	–
	10–8	ILV11[2:0]	0x0	H0	R/W	16-bit PWM timer Ch.1 interrupt (ILVT16B_1)
	7–3	–	0x00	–	R	–
	2–0	ILV10[2:0]	0x0	H0	R/W	16-bit PWM timer Ch.0 interrupt (ILVT16B_0)
ITCLV6 (ITC Interrupt Level Setup Register 6)	15–11	–	0x00	–	R	–
	10–8	ILV13[2:0]	0x0	H0	R/W	Sound generator interrupt (ILVSNDA_0)
	7–3	–	0x00	–	R	–
	2–0	ILV12[2:0]	0x0	H0	R/W	Smart card interface interrupt (ILSMCIF_0)
ITCLV7 (ITC Interrupt Level Setup Register 7)	15–8	–	0x00	–	R	–
	10–8	ILV15[2:0]	0x0	–	R/W	12-bit A/D converter interrupt (ILVADC12A_0)
	7–3	–	0x00	–	R	
	2–0	ILV14[2:0]	0x0	H0	R/W	16-bit timer Ch.2 interrupt (ILVT16_2)
ITCLV8 (ITC Interrupt Level Setup Register 8)	15–11	–	0x00	–	R	–
	10–8	ILV17[2:0]	0x0	H0	R/W	EEPROM controller interrupt (ILVEPRC)
	7–3	–	0x00	–	R	–
	2–0	ILV16[2:0]	0x0	H0	R/W	EPD controller/driver interrupt (ILVEPDC)
ITCLV9 (ITC Interrupt Level Setup Register 9)	15–11	–	0x00	–	R	–
	10–8	ILV19[2:0]	0x0	H0	R/W	Synchronous serial interface Ch.1 interrupt (ILVSPIA_1)
	7–3	–	0x00	–	R	–
	2–0	ILV18[2:0]	0x0	H0	R/W	16-bit timer Ch.3 interrupt (ILVT16_3)

6 I/O Ports (PPORT)

6.1 Overview

PPORT controls the I/O ports. The main features are outlined below.

- Allows port-by-port function configurations.
  - Each port can be configured with or without a pull-up or pull-down resistor.
  - Each port can be configured with or without a chattering filter.
  - Allows selection of the function (general-purpose I/O port (GPIO) function, up to four peripheral I/O functions) to be assigned to each port.
- Ports, except for those shared with debug pins, are initially placed into Hi-Z state. (No current passes through the pin during this Hi-Z state.)

Note: '*x*', which is used in the port names P*xy*, register names, and bit names, refers to a port group (*x* = 0, 1, 2, d) and '*y*' refers to a port number (*y* = 0, 1, 2, ··· , 7).

Figure 6.1.1 shows the configuration of PPORT.

Table 6.1.1 Port Configuration of S1C17F63

Item	S1C17F63
Port groups included	P0[7:0], P1[5:0], (P2[1:0]*), Pd[2:0]
Ports with general-purpose I/O function (GPIO)	P0[7:0], P1[5:0], (P2[1:0]*), Pd[2:0]
Ports with interrupt function	P0[7:0], P1[5:0], (P2[1:0]*)
Ports for debug function	Pd[2:0]
Key-entry reset function	Supported (P0[3:0])

* The P2[1:0] ports have a different control register assignment and an access method from other ports, as they are included in the independent low-power real-time clock. For more information, refer to the "Independent Low-Power Real-Time Clock" chapter. The P2[1:0] port functions are the same as the other ports and the description in this chapter is applied as is.

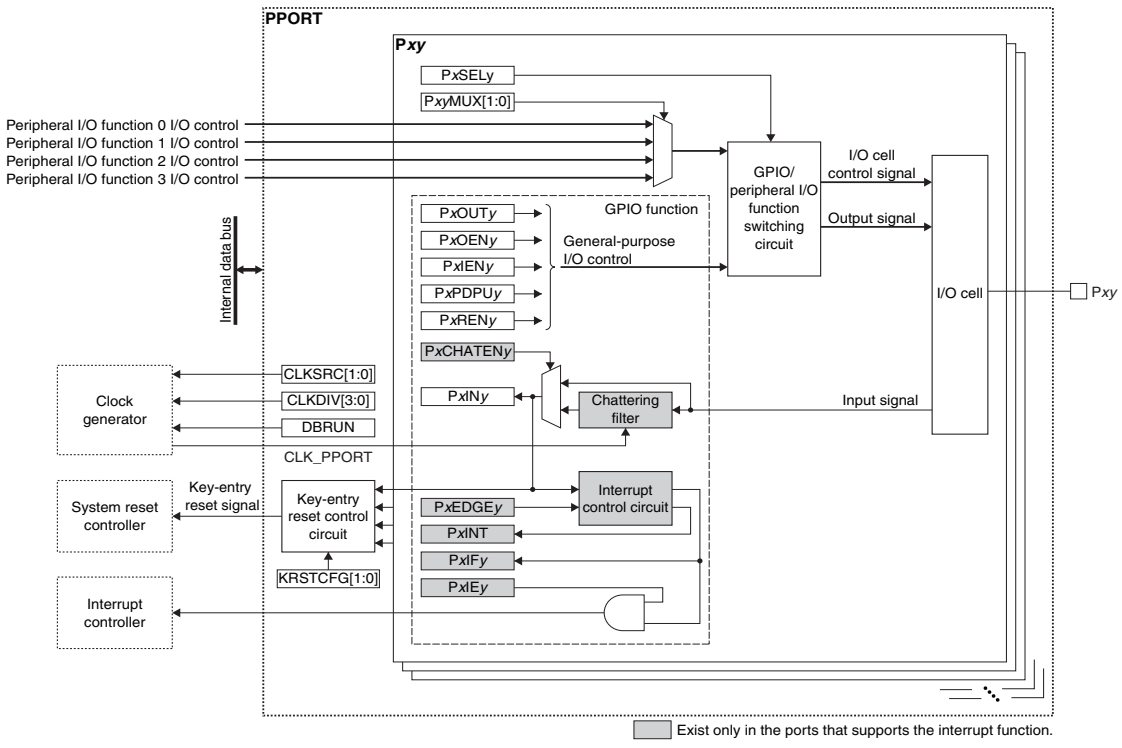


Figure 6.1.1 PPORT Configuration

6.2 I/O Cell Structure and Functions

Figure 6.2.1 shows the I/O cell Configuration.

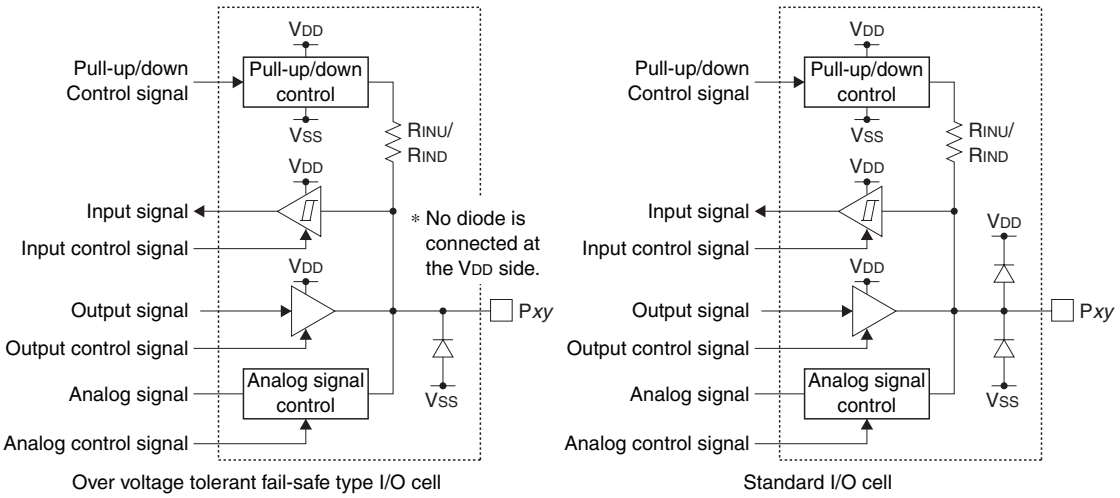


Figure 6.2.1 I/O Cell Configuration

Refer to "Pin Descriptions" in the "Overview" chapter for the cell type, either the over voltage tolerant fail-safe type I/O cell or the standard I/O cell, included in each port.

6.2.1 Schmitt Input

The input functions are all configured with the Schmitt interface level. When a port is set to input disable status (P*x*IOEN.P*x*IEN*y* bit = 0), unnecessary current is not consumed if the P*xy* pin is placed into floating status.

6.2.2 Over Voltage Tolerant Fail-Safe Type I/O Cell

The over voltage tolerant fail-safe type I/O cell allows interfacing without passing unnecessary current even if a voltage exceeding V_{DD} is applied to the port. Also unnecessary current is not consumed when the port is externally biased without supplying V_{DD}. However, be sure to avoid applying a voltage exceeding the recommended maximum operating power supply voltage to the port.

6.2.3 Pull-Up/Pull-Down

The GPIO port has a pull-up/pull-down function. Either pull-up or pull-down may be selected for each port individually. This function may also be disabled for the port that does not require pulling up/down.
When the port level is switched from low to high through the pull-up resistor included in the I/O cell or from high to low through the pull-down resistor, a delay will occur in the waveform rising/falling edge depending on the time constant by the pull-up/pull-down resistance and the pin load capacitance. The rising/falling time is commonly determined by the following equation:

$$t_{PR} = -R_{INU} \times (C_{IN} + C_{BOARD}) \times \ln(1 - V_{T+}/V_{DD}) \quad \text{(Eq. 6.1)}$$
$$t_{PF} = -R_{IND} \times (C_{IN} + C_{BOARD}) \times \ln(1 - V_{T-}/V_{DD})$$

Where

- t_{PR}: Rising time (port level = low → high) [second]
- t_{PF}: Falling time (port level = high → low) [second]
- V_{T+}: High level Schmitt input threshold voltage [V]
- V_{T-}: Low level Schmitt input threshold voltage [V]
- R_{INU}/R_{IND}: Pull-up/pull-down resistance [Ω]
- C_{IN}: Pin capacitance [F]
- C_{BOARD}: Parasitic capacitance on the board [F]

6.2.4 CMOS Output and High Impedance State

The I/O cells except for analog output can output signals in the VDD and VSS levels. Also the GPIO ports may be put into high-impedance (Hi-Z) state.

6.3 Clock Settings

6.3.1 PPORT Operating Clock

When using the chattering filter for entering external signals to PPORT, the PPORT operating clock CLK_PPORT must be supplied to PPORT from the clock generator.
The CLK_PPORT supply should be controlled as in the procedure shown below.

1. Enable the clock source in the clock generator if it is stopped (refer to "Clock Generator" in the "Power Supply, Reset, and Clocks" chapter).
2. Write 0x0096 to the MSCPROT.PROT[15:0] bits. (Remove system protection)
3. Set the following PCLK register bits:
   - PCLK.CLKSRC[1:0] bits (Clock source selection)
   - PCLK.CLKDIV[3:0] bits (Clock division ratio selection = Clock frequency setting)
4. Write a value other than 0x0096 to the MSCPROT.PROT[15:0] bits. (Set system protection)

Settings in Step 3 determine the input sampling time of the chattering filter.

6.3.2 Clock Supply in SLEEP Mode

When using the chattering filter function during SLEEP mode, the PPORT operating clock CLK_PPORT must be configured so that it will keep suppling by writing 0 to the CLGOSC.*xxxx*SLPC bit for the CLK_PPORT clock source.
If the CLGOSC.*xxxx*SLPC bit for the CLK_PPORT clock source is 1, the CLK_PPORT clock source is deactivated during SLEEP mode and it disables the chattering filter function regardless of the P*x*CHATEN.P*x*CHATEN*y* bit setting (chattering filter enabled/disabled).

6.3.3 Clock Supply in DEBUG Mode

The CLK_PPORT supply during DEBUG mode should be controlled using the PCLK.DBRUN bit.
The CLK_PPORT supply to PPORT is suspended when the CPU enters DEBUG mode if the PCLK.DBRUN bit = 0. After the CPU returns to normal mode, the CLK_PPORT supply resumes. The PPORT chattering filter stops operating when the CLK_PPORT supply is suspended. If the chattering filter is enabled in PPORT, the input port function is also deactivated. However, the control registers can be altered. If the PCLK.DBRUN bit = 1, the CLK_PPORT supply is not suspended and the chattering filter will keep operating in DEBUG mode.

6.4 Operations

6.4.1 Initialization

After a reset, the ports except for the debugging function are configured as shown below.

- Port input: Disabled
- Port output: Disabled
- Pull-up: Off
- Pull-down: Off
- Port pins: High impedance state
- Port function: Configured to GPIO

This status continues until the ports are configured via software. The debugging function ports are configured for debug signal input/output.

Initial settings when using a port for a peripheral I/O function

When using the P*xy* port for a peripheral I/O function, perform the following software initial settings:

1. Set the following P*x*IOEN register bits:
   - Set the P*x*IOEN.P*x*IEN*y* bit to 0. (Disable input)
   - Set the P*x*IOEN.P*x*OEN*y* bit to 0. (Disable output)
2. Set the P*x*MODSEL.P*x*SEL*y* bit to 0. (Disable peripheral I/O function)
3. Initialize the peripheral circuit that uses the pin.
4. Set the P*x*FNCSEL.P*xy*MUX[1:0] bits. (Select peripheral I/O function)
5. Set the P*x*MODSEL.P*x*SEL*y* bit to 1. (Enable peripheral I/O function)

For the list of the peripheral I/O functions that can be assigned to each port of this IC, refer to "Control Register and Port Function Configuration of this IC." For the specific information on the peripheral I/O functions, refer to the respective peripheral circuit chapter.

Initial settings when using a port as a general-purpose output port (only for the ports with GPIO function)

When using the P*xy* port pin as a general-purpose output pin, perform the following software initial settings:

1. Set the P*x*IOEN.P*x*OEN*y* bit to 1. (Enable output)
2. Set the P*x*MODSEL.P*x*SEL*y* bit to 0. (Enable GPIO function)

Initial settings when using a port as a general-purpose input port (only for the ports with GPIO function)

When using the P*xy* port pin as a general-purpose input pin, perform the following software initial settings:

1. Write 0 to the P*x*INTCTL.P*x*IE*y* bit. * (Disable interrupt)
2. When using the chattering filter, configure the PPORT operating clock (see "PPORT Operating Clock") and set the P*x*CHATEN.P*x*CHATEN*y* bit to 1. *

   When the chattering filter is not used, set the P*x*CHATEN.P*x*CHATEN*y* bit to 0 (supply of the PPORT operating clock is not required).
3. Configure the following P*x*RCTL register bits when pulling up/down the port using the internal pull-up or down resistor:
   - P*x*RCTL.P*x*PDPU*y* bit (Select pull-up or pull-down resistor)
   - Set the P*x*RCTL.P*x*REN*y* bit to 1. (Enable pull-up/down)

   Set the P*x*RCTL.P*x*REN*y* bit to 0 if the internal pull-up/down resistors are not used.
4. Set the P*x*MODSEL.P*x*SEL*y* bit to 0. (Enable GPIO function)
5. Configure the following bits when using the port input interrupt: *
   - Write 1 to the P*x*INTF.P*x*IF*y* bit. (Clear interrupt flag)
   - P*x*INTCTL.P*x*EDGE*y* bit (Select interrupt edge (input rising edge/falling edge))
   - Set the P*x*INTCTL.P*x*IE*y* bit to 1. (Enable interrupt)
6. Set the following P*x*IOEN register bits:
   - Set the P*x*IOEN.P*x*OEN*y* bit to 0. (Disable output)
   - Set the P*x*IOEN.P*x*IEN*y* bit to 1. (Enable input)

∗ Steps 1 and 5 are required for the ports with an interrupt function. Step 2 is required for the ports with a chattering filter function.

Table 6.4.1.1 lists the port status according to the combination of data input/output control and pull-up/down control.

Table 6.4.1.1 GPIO Port Control List

PxIOEN. PxIENy bit	PxIOEN. PxOENy bit	PxRCTL. PxRENy bit	PxRCTL. PxPDPUy bit	Input	Output	Pull-up/pull-down condition
0	0	0	×	Disabled		Off (Hi-Z) *1
0	0	1	0	Disabled		Pulled down
0	0	1	1	Disabled		Pulled up
1	0	0	×	Enabled	Disabled	Off (Hi-Z) *2
1	0	1	0	Enabled	Disabled	Pulled down
1	0	1	1	Enabled	Disabled	Pulled up
0	1	0	×	Disabled	Enabled	Off
0	1	1	0	Disabled	Enabled	Off
0	1	1	1	Disabled	Enabled	Off
1	1	1	0	Enabled	Enabled	Off
1	1	1	1	Enabled	Enabled	Off

*1: Initial status. Current does not flow if the pin is placed into floating status.
*2: Use of the pull-up or pull-down function is recommended, as undesired current will flow if the port input is set to floating status.

Note: If the PxMODSEL.PxSELy bit for the port without a GPIO function is set to 0, the port goes into initial status (refer to "Initial Settings"). The GPIO control bits are configured to a read-only bit always read out as 0.

6.4.2 Port Input/Output Control

Peripheral I/O function control

The port for which a peripheral I/O function is selected is controlled by the peripheral circuit. For more information, refer to the respective peripheral circuit chapter.

Setting output data to a GPIO port

Write data (1 = high output, 0 = low output) to be output from the P*xy* pin to the PxDAT.PxOUTy bit.

Reading input data from a GPIO port

The data (1 = high input, 0 = low input) input from the P*xy* pin can be read out from the PxDAT.PxINy bit.

Chattering filter function

Some ports have a chattering filter function and it can be controlled in each port. This function is enabled by setting the PxCHATEN.PxCHATENy bit to 1. The input sampling time to remove chattering is determined by the CLK_PPORT frequency configured using the PCLK register in common to all ports. The chattering filter removes pulses with a shorter width than the input sampling time.

$$\text{Input sampling time} = \frac{2 \text{ to } 3}{\text{CLK\_PPORT frequency [Hz]}} \text{ [second]} \qquad \text{(Eq.6.2)}$$

Make sure the P*xy* port interrupt is disabled before altering the PCLK register and PxCHATEN.PxCHATENy bit settings. A P*xy* port interrupt may erroneously occur if these settings are altered in an interrupt enabled status. Furthermore, enable the interrupt after a lapse of four or more CLK_PPORT cycles from enabling the chattering filter function.
If the clock generator is configured so that it will supply CLK_PPORT to PPORT in SLEEP mode, the chattering filter of the port will function even in SLEEP mode. If CLK_PPORT is configured to stop in SLEEP mode, PPORT inactivates the chattering filter during SLEEP mode to input pin status transitions directly to itself.

Key-entry reset function

This function issues a reset request when low-level pulses are input to all the specified ports simultaneously. Make the following settings when using this function:

1. Configure the ports to be used for key-entry reset as general-purpose input ports (refer to "Initial settings when using a port as a general-purpose input port (only for the ports with GPIO function)").
2. Configure the input pin combination for key-entry reset using the PCLK.KRSTCFG[1:0] bits.

Note: When enabling the key-entry reset function, be sure to configure the port pins to be used for it as general-purpose input pins before setting the PCLK.KRSTCFG[1:0] bits.

PPORT issues a reset request immediately after all the input pins specified by the PCLK.KRSTCFG[1:0] are set to a low level if the chattering filter function is disabled (initial status). To issue a reset request only when low-level signals longer than the time configured are input, enable the chattering filter function for all the ports used for key-entry reset.
The pins configured for key-entry reset can also be used as general-purpose input pins.

6.5 Interrupts

When the GPIO function is selected for the port with an interrupt function, the port input interrupt function can be used.

Table 6.5.1 Port Input Interrupt Function

Interrupt	Interrupt flag	Set condition	Clear condition
Port input interrupt	P*x*INTF.P*x*IF*y*	Rising or falling edge of the input signal	Writing 1
	PINTFGRP.P*x*INT	Setting an interrupt flag in the port group	Clearing P*x*INTF.P*x*IF*y*

Interrupt edge selection

Port input interrupts will occur at the falling edge of the input signal when setting the P*x*INTCTL.P*x*EDGE*y* bit to 1, or the rising edge when setting to 0.

Interrupt enable

PPORT provides interrupt enable bits (P*x*INTCTL.P*x*IE*y* bit) corresponding to each interrupt flag. An interrupt request is sent to the interrupt controller only when the interrupt flag, of which interrupt has been enabled by the interrupt enable bit, is set. For more information on interrupt control, refer to the "Interrupt Controller" chapter.

Interrupt check in port group unit

When interrupts are enabled in two or more port groups, check the PINTFGRP.P*x*INT bit in the interrupt handler first. It helps minimize the handler codes for finding the port that has generated an interrupt. If this bit is set to 1, an interrupt has occurred in the port group. Next, check the P*x*INTF.P*x*IF*y* bit set to 1 in the port group to determine the port that has generated an interrupt. Clearing the P*x*INTF.P*x*IF*y* bit also clears the PINTFGRP.P*x*INT bit. If the port is set to interrupt disabled status by the P*x*INTCTL.P*x*IE*y* bit, the PINTFGRP.P*x*INT bit will not be set even if the P*x*INTF.P*x*IF*y* bit is set to 1.

6.6 Control Registers

This section describes the same control registers of all port groups as a single register. For the register and bit configurations in each port group and their initial values, refer to "Control Register and Port Function Configuration of this IC."

P*x* Port Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P*x*DAT	15–8	P*x*OUT[7:0]	0x00	H0	R/W	–
	7–0	P*x*IN[7:0]	0x00	H0	R	

∗1: This register is effective when the GPIO function is selected.
∗2: The bit configuration differs depending on the port group.
∗3: The initial value may be changed by the port.

Bits 15–8 P*x*OUT[7:0]

These bits are used to set data to be output from the GPIO port pins.
1 (R/W): Output high level from the port pin
0 (R/W): Output low level from the port pin

When output is enabled (P*x*IOEN.P*x*OEN*y* bit = 1), the port pin outputs the data set here. Although data can be written when output is disabled (P*x*IOEN.P*x*OEN*y* bit = 0), it does not affect the pin status.
These bits do not affect the outputs when the port is used as a peripheral I/O function.

Bits 7–0 P*x*IN[7:0]

The GPIO port pin status can be read out from these bits.
1 (R): Port pin = High level
0 (R): Port pin = Low level

The port pin status can be read out when input is enabled (P*x*IOEN.P*x*IEN*y* bit = 1). When input is disabled (P*x*IOEN.P*x*IEN*y* bit = 0), these bits are always read as 0.
When the port is used for a peripheral I/O function, the input value cannot be read out from these bits.

P*x* Port Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P*x*IOEN	15–8	P*x*IEN[7:0]	0x00	H0	R/W	–
	7–0	P*x*OEN[7:0]	0x00	H0	R/W	

∗1: This register is effective when the GPIO function is selected.
∗2: The bit configuration differs depending on the port group.

Bits 15–8 P*x*IEN[7:0]

These bits enable/disable the GPIO port input.
1 (R/W): Enable (The port pin status is input.)
0 (R/W): Disable (Input data is fixed at 0.)

When both data output and data input are enabled, the pin output status controlled by this IC can be read.
These bits do not affect the input control when the port is used as a peripheral I/O function.

Bits 7–0 P*x*OEN[7:0]

These bits enable/disable the GPIO port output.
1 (R/W): Enable (Data is output from the port pin.)
0 (R/W): Disable (The port is placed into Hi-Z.)

These bits do not affect the output control when the port is used as a peripheral I/O function.

P*x* Port Pull-up/down Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P*x*RCTL	15–8	P*x*PDPU[7:0]	0x00	H0	R/W	–
	7–0	P*x*REN[7:0]	0x00	H0	R/W	

∗1: This register is effective when the GPIO function is selected.
∗2: The bit configuration differs depending on the port group.

Bits 15–8 P*x*PDPU[7:0]

These bits select either the pull-up resistor or the pull-down resistor when using a resistor built into the port.
1 (R/W): Pull-up resistor
0 (R/W): Pull-down resistor

The selected pull-up/down resistor is enabled when the P*x*RCTL.P*x*REN*y* bit = 1.

Bits 7–0 P*x*REN[7:0]

These bits enable/disable the port pull-up/down control.
1 (R/W): Enable (The built-in pull-up/down resistor is used.)
0 (R/W): Disable (No pull-up/down control is performed.)

Enabling this function pulls up or down the port when output is disabled (P*x*IOEN.P*x*OEN*y* bit = 0). When output is enabled (P*x*IOEN.P*x*OEN*y* bit = 1), the P*x*RCTL.P*x*REN*y* bit setting is ineffective regardless of how the P*x*IOEN.P*x*IEN*y* bit is set and the port is not pulled up/down.
These bits do not affect the pull-up/down control when the port is used as a peripheral I/O function.

P*x* Port Interrupt Flag Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P*x*INTF	15–8	–	0x00	–	R	–
	7–0	P*x*IF[7:0]	0x00	H0	R/W	Cleared by writing 1.

∗1: This register is effective when the GPIO function is selected.
∗2: The bit configuration differs depending on the port group.

Bits 15–8 Reserved

Bits 7–0 P*x*IF[7:0]

These bits indicate the port input interrupt cause occurrence status.
1 (R): Cause of interrupt occurred
0 (R): No cause of interrupt occurred
1 (W): Clear flag
0 (W): Ineffective

P*x* Port Interrupt Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P*x*INTCTL	15–8	P*x*EDGE[7:0]	0x00	H0	R/W	–
	7–0	P*x*IE[7:0]	0x00	H0	R/W	

∗1: This register is effective when the GPIO function is selected.
∗2: The bit configuration differs depending on the port group.

Bits 15–8 P*x*EDGE[7:0]

These bits select the input signal edge to generate a port input interrupt.
1 (R/W): An interrupt will occur at a falling edge.
0 (R/W): An interrupt will occur at a rising edge.

Bits 7–0 P*x*IE[7:0]

These bits enable port input interrupts.
1 (R/W): Enable interrupts
0 (R/W): Disable interrupts

Note: To prevent generating unnecessary interrupts, the corresponding interrupt flag should be cleared before enabling interrupts.

P*x* Port Chattering Filter Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P*x*CHATEN	15–8	–	0x00	–	R	–
	7–0	P*x*CHATEN[7:0]	0x00	H0	R/W	

∗1: The bit configuration differs depending on the port group.

Bits 15–8 Reserved

Bits 7–0 P*x*CHATEN[7:0]

These bits enable/disable the chattering filter function.

1 (R/W): Enable (The chattering filter is used.)

0 (R/W): Disable (The chattering filter is bypassed.)

P*x* Port Mode Select Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P*x*MODSEL	15–8	–	0x00	–	R	–
	7–0	P*x*SEL[7:0]	0x00	H0	R/W	

∗1: The bit configuration differs depending on the port group.

∗2: The initial value may be changed by the port.

Bits 15–8 Reserved

Bits 7–0 P*x*SEL[7:0]

These bits select whether each port is used for the GPIO function or a peripheral I/O function.

1 (R/W): Use peripheral I/O function

0 (R/W): Use GPIO function

P*x* Port Function Select Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P*x*FNCSEL	15–14	P*x*7MUX[1:0]	0x0	H0	R/W	–
	13–12	P*x*6MUX[1:0]	0x0	H0	R/W	
	11–10	P*x*5MUX[1:0]	0x0	H0	R/W	
	9–8	P*x*4MUX[1:0]	0x0	H0	R/W	
	7–6	P*x*3MUX[1:0]	0x0	H0	R/W	
	5–4	P*x*2MUX[1:0]	0x0	H0	R/W	
	3–2	P*x*1MUX[1:0]	0x0	H0	R/W	
	1–0	P*x*0MUX[1:0]	0x0	H0	R/W	

∗1: The bit configuration differs depending on the port group.

∗2: The initial value may be changed by the port.

Bits 15–14 P*x*7MUX[1:0]

: :

Bits 1–0 P*x*0MUX[1:0]

These bits select the peripheral I/O function to be assigned to each port pin.

Table 6.6.1 Selecting Peripheral I/O Function

P*x*FNCSEL.P*xy*MUX[1:0] bits	Peripheral I/O function
0x3	Function 3
0x2	Function 2
0x1	Function 1
0x0	Function 0

This selection takes effect when the P*x*MODSEL.P*x*SEL*y* bit = 1.

P Port Clock Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
PCLK	15–9	–	0x00	–	R	–
	8	DBRUN	0	H0	R/WP	
	7–4	CLKDIV[3:0]	0x0	H0	R/WP	
	3–2	KRSTCFG[1:0]	0x0	H0	R/WP	
	1–0	CLKSRC[1:0]	0x0	H0	R/WP	

Bits 15–9 Reserved

Bit 8 DBRUN

This bit sets whether the PPORT operating clock is supplied in DEBUG mode or not.
1 (R/WP): Clock supplied in DEBUG mode
0 (R/WP): No clock supplied in DEBUG mode

Bits 7–4 CLKDIV[3:0]

These bits select the division ratio of the PPORT operating clock (chattering filter clock).

Bits 3–2 KRSTCFG[1:0]

These bits configure the key-entry reset function.

Table 6.6.2 Key-Entry Reset Function Settings

PCLK.KRSTCFG[1:0] bits	key-entry reset
0x3	Reset when P0[3:0] inputs = all low
0x2	Reset when P0[2:0] inputs = all low
0x1	Reset when P0[1:0] inputs = all low
0x0	Disable

Bits 1–0 CLKSRC[1:0]

These bits select the clock source of PPORT (chattering filter).
The PPORT operating clock should be configured by selecting the clock source using the PCLK.CLKSRC[1:0] bits and the clock division ratio using the PCLK.CLKDIV[3:0] bits as shown in Table 6.6.3. These settings determine the input sampling time of the chattering filter.

Table 6.6.3 Clock Source and Division Ratio Settings

PCLK.CLKDIV[3:0] bits	PCLK.CLKSRC[1:0] bits			
	0x0	0x1	0x2	0x3
	IOSC	OSC1	OSC3	EXOSC
0xf	1/32,768			1/1
0xe	1/16,384			
0xd	1/8,192			
0xc	1/4,096			
0xb	1/2,048			
0xa	1/1,024			
0x9	1/512			
0x8	1/256			
0x7	1/128			
0x6	1/64			
0x5	1/32			
0x4	1/16			
0x3	1/8			
0x2	1/4			
0x1	1/2			
0x0	1/1			

(Note) The oscillation circuits/external input that are not supported in this IC cannot be selected as the clock source.

P Port Interrupt Flag Group Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
PINTFGRP	15–13	–	0x0	–	R	–
	12	PcINT	0	H0	R	
	11	PbINT	0	H0	R	
	10	PaINT	0	H0	R	
	9	P9INT	0	H0	R	
	8	P8INT	0	H0	R	
	7	P7INT	0	H0	R	
	6	P6INT	0	H0	R	
	5	P5INT	0	H0	R	
	4	P4INT	0	H0	R	
	3	P3INT	0	H0	R	
	2	P2INT	0	H0	R	
	1	P1INT	0	H0	R	
	0	P0INT	0	H0	R	

∗1: Only the bits corresponding to the port groups that support interrupts are provided.

Bits 15–13 Reserved

Bits 12–0 P*x*INT

These bits indicate that P*x* port group includes a port that has generated an interrupt.

1 (R): A port generated an interrupt

0 (R): No port generated an interrupt

The PINTFGRP.P*x*INT bit is cleared when the interrupt flag for the port that has generated an interrupt is cleared.

6.7 Control Register and Port Function Configuration of this IC

This section shows the PPORT control register/bit configuration in this IC and the list of peripheral I/O functions selectable for each port.

6.7.1 P0 Port Group

The P0 port group supports the GPIO and interrupt functions.

Table 6.7.1.1 Control Registers for P0 Port Group

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P0DAT (P0 Port Data Register)	15–8	P0OUT[7:0]	0x00	H0	R/W	–
	7–0	P0IN[7:0]	0x00	H0	R	
P0IOEN (P0 Port Enable Register)	15–8	P0IEN[7:0]	0x00	H0	R/W	–
	7–0	P0OEN[7:0]	0x00	H0	R/W	
P0RCTL (P0 Port Pull-up/ down Control Register)	15–8	P0PDPU[7:0]	0x00	H0	R/W	–
	7–0	P0REN[7:0]	0x00	H0	R/W	
P0INTF (P0 Port Interrupt Flag Register)	15–8	–	0x00	–	R	–
	7–0	P0IF[7:0]	0x00	H0	R/W	Cleared by writing 1.
P0INTCTL (P0 Port Interrupt Control Register)	15–8	P0EDGE[7:0]	0x00	H0	R/W	–
	7–0	P0IE[7:0]	0x00	H0	R/W	
P0CHATEN (P0 Port Chattering Filter Enable Register)	15–8	–	0x00	–	R	–
	7–0	P0CHATEN[7:0]	0x00	H0	R/W	
P0MODSEL (P0 Port Mode Select Register)	15–8	–	0x00	–	R	–
	7–0	P0SEL[7:0]	0x00	H0	R/W	
P0FNCSEL (P0 Port Function Select Register)	15–14	P07MUX[1:0]	0x0	H0	R/W	–
	13–12	P06MUX[1:0]	0x0	H0	R/W	
	11–10	P05MUX[1:0]	0x0	H0	R/W	
	9–8	P04MUX[1:0]	0x0	H0	R/W	
	7–6	P03MUX[1:0]	0x0	H0	R/W	
	5–4	P02MUX[1:0]	0x0	H0	R/W	
	3–2	P01MUX[1:0]	0x0	H0	R/W	
	1–0	P00MUX[1:0]	0x0	H0	R/W	

Table 6.7.1.2 P0 Port Group Function Assignment

Port name	P0SEL*y* = 0	P0SEL*y* = 1							
	GPIO	P0*y*MUX = 0x0 (Function 0)		P0*y*MUX = 0x1 (Function 1)		P0*y*MUX = 0x2 (Function 2)		P0*y*MUX = 0x3 (Function 3)	
		Peripheral	Pin	Peripheral	Pin	Peripheral	Pin	Peripheral	Pin
P00	P00	EPDC	EPDCLK	UPMUX	*1	ADC12A	VREFA0	–	–
P01	P01	EPDC	EPDTRG	UPMUX	*1	ADC12A	ADIN06	–	–
P02	P02	SNDA	BZOUT	UPMUX	*1	ADC12A	ADIN05	–	–
P03	P03	SNDA	#BZOUT	UPMUX	*1	ADC12A	ADIN04	–	–
P04	P04	CLG	FOUT0	UPMUX	*1	ADC12A	ADIN03	–	–
P05	P05	SMCIF Ch.0	SMCCLK0	UPMUX	*1	ADC12A	ADIN02	–	–
P06	P06	SMCIF Ch.0	SMCIO0	UPMUX	*1	ADC12A	ADIN01	–	–
P07	P07	–	–	UPMUX	*1	ADC12A	ADIN00	–	–

*1: Refer to the “Universal Port Multiplexer” chapter.

6.7.2 P1 Port Group

The P1 port group consists of six ports P10–P15 and they support the GPIO and interrupt functions.

Table 6.7.2.1 Control Registers for P1 Port Group

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P1DAT (P1 Port Data Register)	15–14	–	0x0	–	R	–
	13–8	P1OUT[5:0]	0x00	H0	R/W	
	7–6	–	0x0	–	R	
	5–0	P1IN[5:0]	0x00	H0	R	
P1IOEN (P1 Port Enable Register)	15–14	–	0x0	–	R	–
	13–8	P1IEN[5:0]	0x00	H0	R/W	
	7–6	–	0x0	–	R	
	5–0	P1OEN[5:0]	0x00	H0	R/W	
P1RCTL (P1 Port Pull-up/down Control Register)	15–14	–	0x0	–	R	–
	13–8	P1PDPU[5:0]	0x00	H0	R/W	
	7–6	–	0x0	–	R	
	5–0	P1REN[5:0]	0x00	H0	R/W	
P1INTF (P1 Port Interrupt Flag Register)	15–8	–	0x00	–	R	–
	7–6	–	0x0	–	R	
	5–0	P1IF[5:0]	0x00	H0	R/W	Cleared by writing 1.
P1INTCTL (P1 Port Interrupt Control Register)	15–14	–	0x0	–	R	–
	13–8	P1EDGE[5:0]	0x00	H0	R/W	
	7–6	–	0x0	–	R	
	5–0	P1IE[5:0]	0x00	H0	R/W	
P1CHATEN (P1 Port Chattering Filter Enable Register)	15–8	–	0x00	–	R	–
	7–6	–	0x0	–	R	
	5–0	P1CHATEN[5:0]	0x00	H0	R/W	
P1MODSEL (P1 Port Mode Select Register)	15–8	–	0x00	–	R	–
	7–6	–	0x0	–	R	
	5–0	P1SEL[5:0]	0x00	H0	R/W	
P1FNCSEL (P1 Port Function Select Register)	15–12	–	0x0	–	R	–
	11–10	P15MUX[1:0]	0x0	H0	R/W	
	9–8	P14MUX[1:0]	0x0	H0	R/W	
	7–6	P13MUX[1:0]	0x0	H0	R/W	
	5–4	P12MUX[1:0]	0x0	H0	R/W	
	3–2	P11MUX[1:0]	0x0	H0	R/W	
	1–0	P10MUX[1:0]	0x0	H0	R/W	

Table 6.7.2.2 P1 Port Group Function Assignment

Port name	P1SEL*y* = 0	P1SEL*y* = 1							
	GPIO	P1*y*MUX = 0x0 (Function 0)		P1*y*MUX = 0x1 (Function 1)		P1*y*MUX = 0x2 (Function 2)		P1*y*MUX = 0x3 (Function 3)	
		Peripheral	Pin	Peripheral	Pin	Peripheral	Pin	Peripheral	Pin
P10	P10	T16B Ch.0	EXCL00	UPMUX	*1	–	–	–	–
P11	P11	T16B Ch.0	EXCL01	UPMUX	*1	–	–	–	–
P12	P12	T16B Ch.1	EXCL10	UPMUX	*1	–	–	–	–
P13	P13	T16B Ch.1	EXCL11	UPMUX	*1	–	–	–	–
P14	P14	CLG	EXOSC	UPMUX	*1	–	–	–	–
P15	P15	ADC12A	#ADTRG0	UPMUX	*1	SVD3	EXSVD0	–	–

*1: Refer to the “Universal Port Multiplexer” chapter.

6.7.3 Pd Port Group

The Pd port group consists of three ports Pd0–Pd2 and they are configured as a debugging function port at initialization. These three ports support the GPIO function.

Table 6.7.3.1 Control Registers for Pd Port Group

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
PDDAT (Pd Port Data Register)	15–11	–	0x00	–	R	–
	10–8	PDOUT[2:0]	0x0	H0	R/W	
	7–3	–	0x00	–	R	
	2–0	PDIN[2:0]	x	H0	R	
PDIOEN (Pd Port Enable Register)	15–11	–	0x00	–	R	–
	10–8	PDIEN[2:0]	0x0	H0	R/W	
	7–3	–	0x00	–	R	
	2–0	PDOEN[2:0]	0x0	H0	R/W	
PDRCTL (Pd Port Pull-up/down Control Register)	15–11	–	0x00	–	R	–
	10–8	PDPDPU[2:0]	0x0	H0	R/W	
	7–3	–	0x00	–	R	
	2–0	PDREN[2:0]	0x0	H0	R/W	
PDINTF PDINTCTL PDCHATEN	15–0	–	0x0000	–	R	–
PDMODSEL (Pd Port Mode Select Register)	15–8	–	0x00	–	R	–
	7–3	–	0x00	–	R	
	2–0	PDSEL[2:0]	0x7	H0	R/W	
PDFNCSEL (Pd Port Function Select Register)	15–8	–	0x00	–	R	–
	7–6	–	0x0	–	R	
	5–4	PD2MUX[1:0]	0x0	H0	R/W	
	3–2	PD1MUX[1:0]	0x0	H0	R/W	
	1–0	PD0MUX[1:0]	0x0	H0	R/W	

Table 6.7.3.2 Pd Port Group Function Assignment

Port name	PdSEL*y* = 0	PdSEL*y* = 1							
	GPIO	Pd*y*MUX = 0x0 (Function 0)		Pd*y*MUX = 0x1 (Function 1)		Pd*y*MUX = 0x2 (Function 2)		Pd*y*MUX = 0x3 (Function 3)	
		Peripheral	Pin	Peripheral	Pin	Peripheral	Pin	Peripheral	Pin
Pd0	Pd0	DBG	DST2	–	–	–	–	–	–
Pd1	Pd1	DBG	DSIO	–	–	–	–	–	–
Pd2	Pd2	DBG	DCLK	–	–	–	–	–	–

6.7.4 Common Registers between Port Groups

Table 6.7.4.1 Control Registers for Common Use with Port Groups

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
PCLK (P Port Clock Control Register)	15–9	–	0x00	–	R	–
	8	DBRUN	0	H0	R/WP	
	7–4	CLKDIV[3:0]	0x0	H0	R/WP	
	3–2	KRSTCFG[1:0]	0x0	H0	R/WP	
	1–0	CLKSRC[1:0]	0x0	H0	R/WP	
PINTFGRP (P Port Interrupt Flag Group Register)	15–8	–	0x00	–	R	–
	7–3	–	0x00	–	R	
	2	P2INT	0	H0	R	
	1	P1INT	0	H0	R	
	0	P0INT	0	H0	R	

7 Universal Port Multiplexer (UPMUX)

7.1 Overview

UPMUX is a multiplexer that allows software to assign the desired peripheral I/O function to an I/O port. The main features are outlined below.

- Allows programmable assignment of the synchronous serial interface, I²C, UART, and 16-bit PWM timer peripheral I/O functions to the P0 and P1 port groups.
- The peripheral I/O function assigned via UPMUX is enabled by setting the P*x*FNCSEL.P*xy*MUX[1:0] bits to 0x1.

Note: '*x*', which is used in the port names P*xy*, register names, and bit names, refers to a port group (*x* = 0, 1) and '*y*' refers to a port number (*y* = 0, 1, 2, ··· , 7).

Figure 7.1.1 shows the configuration of UPMUX.

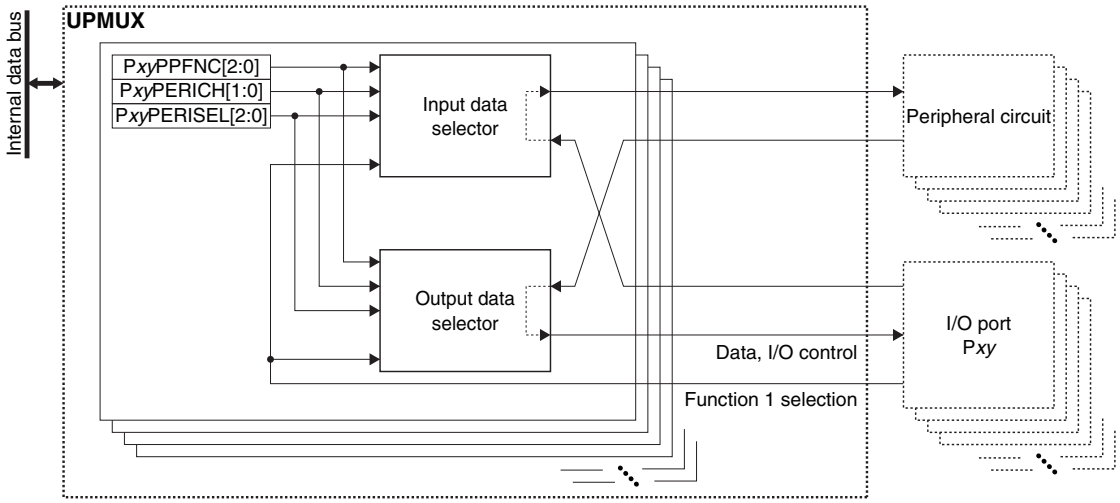


Figure 7.1.1 UPMUX Configuration

7.2 Peripheral Circuit I/O Function Assignment

An I/O function of a peripheral circuit supported may be assigned to peripheral I/O function 1 of an I/O port listed above. The following shows the procedure to assign a peripheral I/O function and enable it in the I/O port:

1. Configure the P*x*IOEN register of the I/O port.
   - Set the P*x*IOEN.P*x*IEN*y* bit to 0. (Disable input)
   - Set the P*x*IOEN.P*x*OEN*y* bit to 0. (Disable output)
2. Set the P*x*MODSEL.P*x*SEL*y* bit of the I/O port to 0. (Disable peripheral I/O function)
3. Set the following P*x*UPMUX*n* register bits (*n* = 0 to 3).
   - P*x*UPMUX*n*.P*xy*PERISEL[2:0] bits (Select peripheral circuit)
   - P*x*UPMUX*n*.P*xy*PERICH[1:0] bits (Select peripheral circuit channel)
   - P*x*UPMUX*n*.P*xy*PPFNC[2:0] bits (Select function to assign)
4. Initialize the peripheral circuit.
5. Set the P*x*FNCSEL.P*xy*MUX[1:0] bits of the I/O port to 0x1. (Select peripheral I/O function 1)
6. Set the P*x*MODSEL.P*x*SEL*y* bit of the I/O port to 1. (Enable peripheral I/O function)

7.3 Control Registers

P*xy–xz* Universal Port Multiplexer Setting Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P*x*UPMUX*n*	15–13	P*xz*PPFNC[2:0]	0x0	H0	R/W	–
	12–11	P*xz*PERICH[1:0]	0x0	H0	R/W	
	10–8	P*xz*PERISEL[2:0]	0x0	H0	R/W	
	7–5	P*xy*PPFNC[2:0]	0x0	H0	R/W	
	4–3	P*xy*PERICH[1:0]	0x0	H0	R/W	
	2–0	P*xy*PERISEL[2:0]	0x0	H0	R/W	

∗1: '*x*' in the register name refers to a port group number and '*n*' refers to a register number (0–3).
∗2: '*x*' in the bit name refers to a port group number, '*y*' refers to an even port number (0, 2, 4, 6), and '*z*' refers to an odd port number (*z* = *y* + 1).

Bits 15–13 P*xz*PPFNC[2:0]
Bits 7–5 P*xy*PPFNC[2:0]

These bits specify the peripheral I/O function to be assigned to the port. (See Table 7.3.1.)

Bits 12–11 P*xz*PERICH[1:0]
Bits 4–3 P*xy*PERICH[1:0]

These bits specify a peripheral circuit channel number. (See Table 7.3.1.)

Bits 10–8 P*xz*PERISEL[2:0]
Bits 2–0 P*xy*PERISEL[2:0]

These bits specify a peripheral circuit. (See Table 7.3.1.)

Table 7.3.1 Peripheral I/O Function Selections

P*x*UPMUX*n*.P*xy*PPFNC[2:0] bits (Peripheral I/O function)	P*x*UPMUX*n*.P*xy*PERISEL[2:0] bits (Peripheral circuit)							
	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7
	None ∗	I2C	SPIA	UART3	T16B	Reserved	Reserved	Reserved
	P*x*UPMUX*n*.P*xy*PERICH[1:0] bits (Peripheral circuit channel)							
	–	0x0	0x0, 0x1	0x0	0x0, 0x1	–	–	–
	–	Ch.0	Ch.0, 1	Ch.0	Ch.0, 1	–	–	–
0x0	None ∗	None ∗	None ∗	None ∗	None ∗	None ∗	None ∗	None ∗
0x1	Reserved	SCL*n*	SDI*n*	USIN*n*	TOUT*n*0/ CAP*n*0	Reserved	Reserved	Reserved
0x2		SDA*n*	SDO*n*	USOUT*n*	TOUT*n*1/ CAP*n*1			
0x3		Reserved	SPICLK*n*	Reserved	Reserved			
0x4			#SPISS*n*					
0x5			Reserved					
0x6								
0x7								

∗ "None" means no assignment. Selecting this will put the P*xy* pin into Hi-Z status when peripheral I/O function 1 is selected and enabled in the I/O port.

Note: Do not assign a peripheral input function to two or more I/O ports. Although the I/O ports output the same waveforms when an output function is assigned to two or more I/O port, a skew occurs due to the internal delay.

8 Watchdog Timer (WDT2)

8.1 Overview

WDT2 restarts the system if a problem occurs, such as when the program cannot be executed normally.
The features of WDT2 are listed below.

- Includes a 10-bit up counter to count NMI/reset generation cycle.
- A counter clock source and clock division ratio are selectable.
- Can generate a reset or NMI in a cycle given via software.
- Can generate a reset at the next NMI generation cycle after an NMI is generated.

Figure 8.1.1 shows the configuration of WDT2.

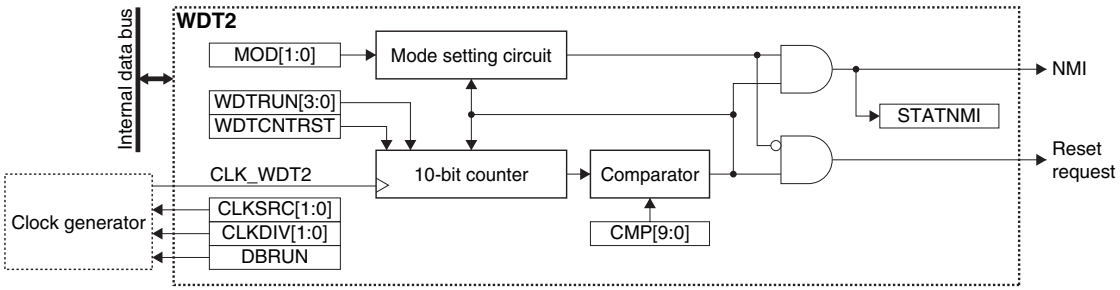


Figure 8.1.1 WDT2 Configuration

8.2 Clock Settings

8.2.1 WDT2 Operating Clock

When using WDT2, the WDT2 operating clock CLK_WDT2 must be supplied to WDT2 from the clock generator. The CLK_WDT2 supply should be controlled as in the procedure shown below.

1. Write 0x0096 to the MSCPROT.PROT[15:0] bits. (Remove system protection)
2. Enable the clock source in the clock generator if it is stopped (refer to "Clock Generator" in the "Power Supply, Reset, and Clocks" chapter).
3. Set the following WDTCLK register bits:
   WDTCLK.CLKSRC[1:0] bits (Clock source selection)
   WDTCLK.CLKDIV[1:0] bits (Clock division ratio selection = Clock frequency setting)
4. Write a value other than 0x0096 to the MSCPROT.PROT[15:0] bits. (Set system protection)

8.2.2 Clock Supply in DEBUG Mode

The CLK_WDT2 supply during DEBUG mode should be controlled using the WDTCLK.DBRUN bit.
The CLK_WDT2 supply to WDT2 is suspended when the CPU enters DEBUG mode if the WDTCLK.DBRUN bit = 0. After the CPU returns to normal mode, the CLK_WDT2 supply resumes. Although WDT2 stops operating when the CLK_WDT2 supply is suspended, the register retains the status before DEBUG mode was entered.
If the WDTCLK.DBRUN bit = 1, the CLK_WDT2 supply is not suspended and WDT2 will keep operating in DEBUG mode.

8.3 Operations

8.3.1 WDT2 Control

Activating WDT2

WDT2 should be initialized and started up with the procedure listed below.

1. Write 0x0096 to the MSCPROT.PROT[15:0] bits. (Remove system protection)
2. Configure the WDT2 operating clock.
3. Set the WDTCTL.MOD[1:0] bits. (Select WDT2 operating mode)
4. Set the WDTCMP.CMP[9:0] bits. (Set NMI/reset generation cycle)
5. Write 1 to the WDTCTL.WDTCNTRST bit. (Reset WDT2 counter)
6. Write a value other than 0xa to the WDTCTL.WDTRUN[3:0] bits. (Start up WDT2)
7. Write a value other than 0x0096 to the MSCPROT.PROT[15:0] bits. (Set system protection)

NMI/reset generation cycle

Use the following equation to calculate the WDT2 NMI/reset generation cycle.

$$t_{WDT} = \frac{CMP + 1}{CLK\_WDT2} \qquad \text{(Eq. 8.1)}$$

Where

t_{WDT}: NMI/reset generation cycle [second]
CLK_WDT2: WDT2 operating clock frequency [Hz]
CMP: Setting value of the WDTCMP.CMP[9:0] bits

Example) t_{WDT} = 2.5 seconds when CLK_WDT2 = 256 Hz and the WDTCMP.CMP[9:0] bits = 639

Resetting WDT2 counter

To prevent an unexpected NMI/reset to be generated by WDT2, its embedded counter must be reset periodically via software while WDT2 is running.

1. Write 0x0096 to the MSCPROT.PROT[15:0] bits. (Remove system protection)
2. Write 1 to the WDTCTL.WDTCNTRST bit. (Reset WDT2 counter)
3. Write a value other than 0x0096 to the MSCPROT.PROT[15:0] bits. (Set system protection)

A location should be provided for periodically processing this routine. Process this routine within the t_{WDT} cycle. After resetting, WDT2 starts counting with a new NMI/reset generation cycle.

Occurrence of counter compare match

If WDT2 is not reset within the t_{WDT} cycle for any reason and the counter reaches the setting value of the WDTCMP.CMP[9:0] bits, a compare match occurs to cause WDT2 to issue an NMI or reset according to the setting of the WDTCTL.MOD[1:0] bits.
If an NMI is issued, the WDTCTL.STATNMI bit is set to 1. This bit can be cleared to 0 by writing 1 to the WDTCTL.WDTCNTRST bit. Be sure to clear the WDTCTL.STATNMI bit in the NMI handler routine,
If a compare match occurs, the counter is automatically reset to 0 and it continues counting.

Deactivating WDT2

WDT2 should be stopped with the procedure listed below.

1. Write 0x0096 to the MSCPROT.PROT[15:0] bits. (Remove system protection)
2. Write 0xa to the WDTCTL.WDTRUN[3:0] bits. (Stop WDT2)
3. Write a value other than 0x0096 to the MSCPROT.PROT[15:0] bits. (Set system protection)

8.3.2 Operations in HALT and SLEEP Modes

During HALT mode

WDT2 operates in HALT mode. HALT mode is therefore cleared by an NMI or reset if it continues for more than the NMI/reset generation cycle and the CPU executes the interrupt handler. To disable WDT2 in HALT mode, stop WDT2 by writing 0xa to the WDTCTL.WDTRUN[3:0] bits before executing the halt instruction. Reset WDT2 before resuming operations after HALT mode is cleared.

During SLEEP mode

WDT2 operates in SLEEP mode if the selected clock source is running. SLEEP mode is cleared by an NMI or reset if it continues for more than the NMI/reset generation cycle and the CPU executes the interrupt handler. Therefore, stop WDT2 by setting the WDTCTL.WDTRUN[3:0] bits before executing the slp instruction.
If the clock source stops in SLEEP mode, WDT2 stops. To prevent generation of an unnecessary NMI or reset after clearing SLEEP mode, reset WDT2 before executing the slp instruction. WDT2 should also be stopped as required using the WDTCTL.WDTRUN[3:0] bits.

8.4 Control Registers

WDT2 Clock Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
WDTCLK	15–9	–	0x00	–	R	–
	8	DBRUN	0	H0	R/WP	
	7–6	–	0x0	–	R	
	5–4	CLKDIV[1:0]	0x0	H0	R/WP	
	3–2	–	0x0	–	R	
	1–0	CLKSRC[1:0]	0x0	H0	R/WP	

Bits 15–9 Reserved

Bit 8 DBRUN

This bit sets whether the WDT2 operating clock is supplied in DEBUG mode or not.
1 (R/WP): Clock supplied in DEBUG mode
0 (R/WP): No clock supplied in DEBUG mode

Bits 7–6 Reserved

Bits 5–4 CLKDIV[1:0]

These bits select the division ratio of the WDT2 operating clock (counter clock). The clock frequency should be set to around 256 Hz.

Bits 3–2 Reserved

Bits 1–0 CLKSRC[1:0]

These bits select the clock source of WDT2.

Table 8.4.1 Clock Source and Division Ratio Settings

WDTCLK. CLKDIV[1:0] bits	WDTCLK.CLKSRC[1:0] bits			
	0x0	0x1	0x2	0x3
	IOSC	OSC1	OSC3	EXOSC
0x3	1/16,384	1/128	1/65,536	1/1
0x2	1/8,192		1/32,768	
0x1	1/4,096		1/16,384	
0x0	1/2,048		1/8,192	

(Note) The oscillation circuits/external input that are not supported in this IC cannot be selected as the clock source.

WDT2 Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
WDTCTL	15–11	–	0x00	–	R	–
	10–9	MOD[1:0]	0x0	H0	R/WP	
	8	STATNMI	0	H0	R	
	7–5	–	0x0	–	R	
	4	WDTCNTRST	0	H0	WP	Always read as 0.
	3–0	WDTRUN[3:0]	0xa	H0	R/WP	–

Bits 15–11 Reserved

Bits 10–9 MOD[1:0]

These bits set the WDT2 operating mode.

Table 8.4.2 Operating Mode Setting

WDTCTL. MOD[1:0] bits	Operating mode	Description
0x3	Reserved	–
0x2	RESET after NMI mode	If the WDTCTL.STATNMI bit is not cleared to 0 after an NMI has occurred due to a counter compare match, WDT2 issues a reset when the next compare match occurs.
0x1	NMI mode	WDT2 issues an NMI when a counter compare match occurs.
0x0	RESET mode	WDT2 issues a reset when a counter compare match occurs.

Bit 8 STATNMI

This bit indicates that a counter compare match and NMI have occurred.

1 (R): NMI (counter compare match) occurred

0 (R): NMI not occurred

When the NMI generation function of WDT2 is used, read this bit in the NMI handler routine to confirm that WDT2 was the source of the NMI.

The WDTCTL.STATNMI bit set to 1 is cleared to 0 by writing 1 to the WDTCTL.WDTCNTRST bit.

Bits 7–5 Reserved

Bit 4 WDTCNTRST

This bit resets the 10-bit counter and the WDTCTL.STATNMI bit.

1 (WP): Reset

0 (WP): Ignored

0 (R): Always 0 when being read

Bits 3–0 WDTRUN[3:0]

These bits control WDT2 to run and stop.

0xa (WP): Stop

Values other than 0xa (WP): Run

0xa (R): Idle

0x0 (R): Running

Always 0x0 is read if a value other than 0xa is written.

Since an NMI or reset may be generated immediately after running depending on the counter value, WDT2 should also be reset concurrently when running WDT2.

WDT2 Counter Compare Match Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
WDTCMP	15–10	–	0x00	–	R	–
	9–0	CMP[9:0]	0x3ff	H0	R/WP	

Bits 15–10 Reserved

Bits 9–0 CMP[9:0]

These bits set the NMI/reset generation cycle.

The value set in this register is compared with the 10-bit counter value while WDT2 is running, and an NMI or reset is generated when they are matched.

9 Supply Voltage Detector (SVD3)

9.1 Overview

SVD3 is a supply voltage detector to monitor the power supply voltage on the VDD pin or the voltage applied to an external pin. The main features are listed below.

- Power supply voltage to be detected: Selectable from VDD and external power sources (EXSVD0 and EXSVD1) (Note: See the table below.)
- Detectable voltage level: Selectable from among 32 levels (max.) (Note: See the table below.)
- Detection results:
  - Can be read whether the power supply voltage is lower than the detection voltage level or not.
  - Can generate an interrupt or a reset when low power supply voltage is detected.
- Interrupt: 1 system (Low power supply voltage detection interrupt)
- Supports intermittent operations:
  - Three detection cycles are selectable.
  - Low power supply voltage detection count function to generate an interrupt/reset when low power supply voltage is successively detected the number of times specified.
  - Continuous operation is also possible.

Figure 9.1.1 shows the configuration of SVD3.

Table 9.1.1 SVD3 Configuration of S1C17F63

Item	S1C17F63
Power supply voltage to be detected	VDD and one externally input voltage (EXSVD0)
Detectable voltage level	VDD: 28 levels (1.8 to 5.0 V)/external voltage: 32 levels (1.2 to 5.0 V)

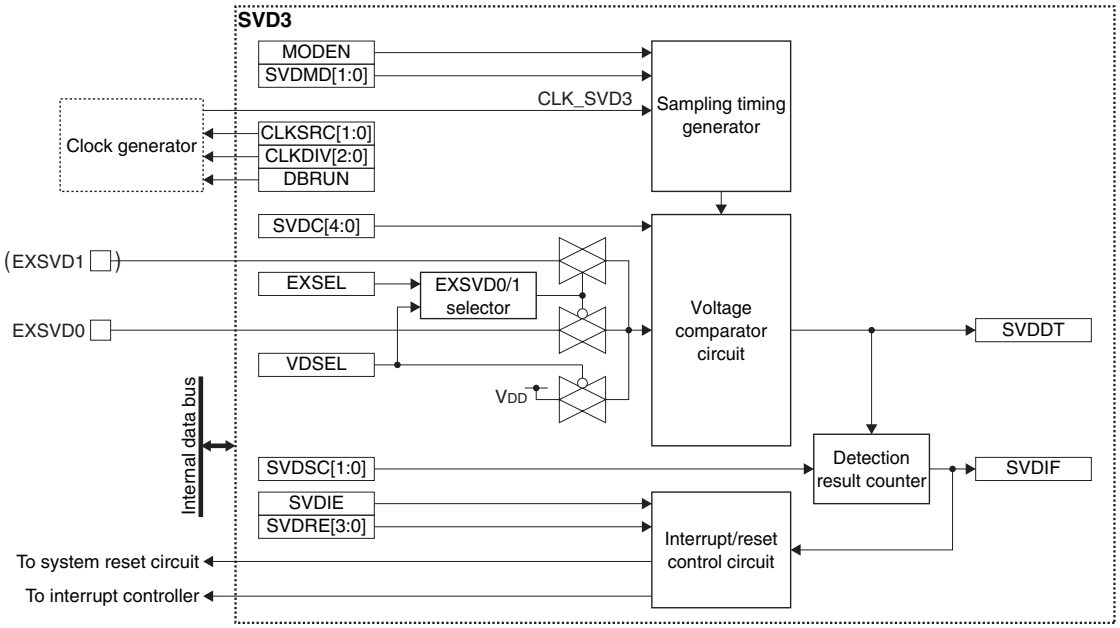


Figure 9.1.1 SVD3 Configuration

9.2 Input Pins and External Connection

9.2.1 Input Pins

Table 9.2.1.1 shows the SVD3 input pins.

Table 9.2.1.1 SVD3 Input Pins

Pin name	I/O*	Initial status*	Function
EXSVD0	A	A (Hi-Z)	External power supply voltage detection pin 0
EXSVD1	A	A (Hi-Z)	External power supply voltage detection pin 1

* Indicates the status when the pin is configured for SVD3.

If the port is shared with the EXSVD0/1 pin and other functions, the EXSVD0/1 function must be assigned to the port before SVD3 can be activated. For more information, refer to the "I/O Ports" chapter.

9.2.2 External Connection

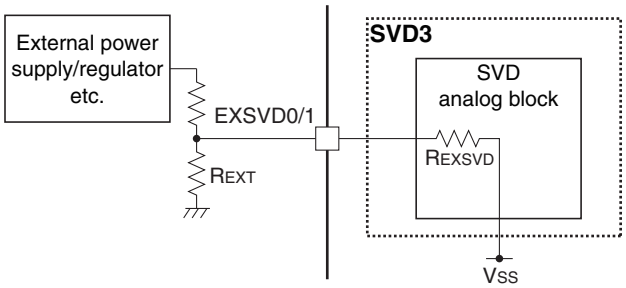


Figure 9.2.2.1 Connection between EXSVD0/1 Pin and External Power Supply

REXT resistance value must be determined so that it will be sufficiently smaller than the EXSVD input impedance REXSVD. For the EXSVD0/1 pin input voltage range and the EXSVD input impedance, refer to "Supply Voltage Detector Characteristics" in the "Electrical Characteristics" chapter.

9.3 Clock Settings

9.3.1 SVD3 Operating Clock

When using SVD3, the SVD3 operating clock CLK_SVD3 must be supplied to SVD3 from the clock generator. The CLK_SVD3 supply should be controlled as in the procedure shown below.

1. Write 0x0096 to the MSCPROT.PROT[15:0] bits. (Remove system protection)
2. Enable the clock source in the clock generator if it is stopped (refer to "Clock Generator" in the "Power Supply, Reset, and Clocks" chapter).
3. Set the following SVDCLK register bits:
   - SVDCLK.CLKSRC[1:0] bits (Clock source selection)
   - SVDCLK.CLKDIV[2:0] bits (Clock division ratio selection = Clock frequency setting)
4. Write a value other than 0x0096 to the MSCPROT.PROT[15:0] bits. (Set system protection)

The CLK_SVD3 frequency should be set to around 32 kHz.

9.3.2 Clock Supply in SLEEP Mode

When using SVD3 during SLEEP mode, the SVD3 operating clock CLK_SVD3 must be configured so that it will keep supplying by writing 0 to the CLGOSC.*xxxx*SLPC bit for the CLK_SVD3 clock source.
If the CLGOSC.*xxxx*SLPC bit for the CLK_SVD3 clock source is 1, the CLK_SVD3 clock source is deactivated during SLEEP mode and SVD3 stops with the register settings maintained at those before entering SLEEP mode. After the CPU returns to normal mode, CLK_SVD3 is supplied and the SVD3 operation resumes.

9.3.3 Clock Supply in DEBUG Mode

The CLK_SVD3 supply during DEBUG mode should be controlled using the SVDCLK.DBRUN bit.
The CLK_SVD3 supply to SVD3 is suspended when the CPU enters DEBUG mode if the SVDCLK.DBRUN bit = 0. After the CPU returns to normal mode, the CLK_SVD3 supply resumes. Although SVD3 stops operating when the CLK_SVD3 supply is suspended, the registers retain the status before DEBUG mode was entered.
If the SVDCLK.DBRUN bit = 1, the CLK_SVD3 supply is not suspended and SVD3 will keep operating in DEBUG mode.

9.4 Operations

9.4.1 SVD3 Control

Starting detection

SVD3 should be initialized and activated with the procedure listed below.

1. Write 0x0096 to the MSCPROT.PROT[15:0] bits. (Remove system protection)
2. Configure the operating clock using the SVDCLK.CLKSRC[1:0] and SVDCLK.CLKDIV[2:0] bits.
3. Set the following SVDCTL register bits:
   - SVDCTL.VDSEL and SVDCTL.EXSEL bits (Select detection voltage (V_{DD}, EXSVD0, or EXSVD1))
   - SVDCTL.SVDSC[1:0] bits (Set low power supply voltage detection counter)
   - SVDCTL.SVDC[4:0] bits (Set SVD detection voltage V_{SVD}/EXSVD detection voltage V_{SVD_EXT})
   - SVDCTL.SVDRE[3:0] bits (Select reset/interrupt mode)
   - SVDCTL.SVDMD[1:0] bits (Set intermittent operation mode)
4. Set the following bits when using the interrupt:
   - Write 1 to the SVDINTF.SVDIF bit. (Clear interrupt flag)
   - Set the SVDINTE.SVDIE bit to 1. (Enable SVD3 interrupt)
5. Set the SVDCTL.MODEN bit to 1. (Enable SVD3 detection)
6. Write a value other than 0x0096 to the MSCPROT.PROT[15:0] bits. (Set system protection)

Terminating detection

Follow the procedure shown below to stop SVD3 operation.

1. Write 0x0096 to the MSCPROT.PROT[15:0] bits. (Remove system protection)
2. Write 0 to the SVDCTL.MODEN bit. (Disable SVD3 detection)
3. Write a value other than 0x0096 to the MSCPROT.PROT[15:0] bits. (Set system protection)

Reading detection results

The following two detection results can be obtained by reading the SVDINTF.SVDDT bit:

- When SVDINTF.SVDDT bit = 0
  Power supply voltage (V_{DD} or EXSVD0/1) ≥ SVD detection voltage V_{SVD} or EXSVD detection voltage V_{SVD_EXT}
- When SVDINTF.SVDDT bit = 1
  Power supply voltage (V_{DD} or EXSVD0/1) < SVD detection voltage V_{SVD} or EXSVD detection voltage V_{SVD_EXT}

Before reading the SVDINTF.SVDDT bit, wait for at least SVD circuit enable response time after 1 is written to the SVDCTL.MODEN bit (refer to "Supply Voltage Detector Characteristics, SVD circuit enable response time t_{SVDEN}" in the "Electrical Characteristics" chapter).
After the SVDCTL.SVDC[4:0] bits setting value is altered to change the SVD detection voltage V_{SVD}/EXSVD detection voltage V_{SVD_EXT} when the SVDCTL.MODEN bit = 1, wait for at least SVD circuit response time before reading the SVDINTF.SVDDT bit (refer to "Supply Voltage Detector Characteristics, SVD circuit response time t_{SVD}" in the "Electrical Characteristics" chapter).

9.4.2 SVD3 Operations

Continuous operation mode

SVD3 operates in continuous operation mode by default (SVDCTL.SVDMD[1:0] bits = 0x0). In this mode, SVD3 operates continuously while the SVDCTL.MODEN bit is set to 1 and it keeps loading the detection results to the SVDINTF.SVDDT bit. During this period, the current detection results can be obtained by reading the SVDINTF.SVDDT bit as necessary. Furthermore, an interrupt (if the SVDCTL.SVDRE[3:0] bits ≠ 0xa) or a reset (if the SVDCTL.SVDRE[3:0] bits = 0xa) can be generated when the SVDINTF.SVDDT bit is set to 1 (low power supply voltage is detected). This mode can keep detecting power supply voltage drop after the voltage detection masking time has elapsed even if the IC is placed into SLEEP status or accidental clock stoppage has occurred.

Intermittent operation mode

SVD3 operates in intermittent operation mode when the SVDCTL.SVDMD[1:0] bits are set to 0x1 to 0x3. In this mode, SVD3 turns on at an interval set using the SVDCTL.SVDMD[1:0] bits to perform detection operation and then it turns off while the SVDCTL.MODEN bit is set to 1. During this period, the latest detection results can be obtained by reading the SVDINTF.SVDDT bit as necessary. Furthermore, an interrupt or a reset can be generated when SVD3 has successively detected low power supply voltage the number of times specified by the SVDCTL.SVDSC[1:0] bits.

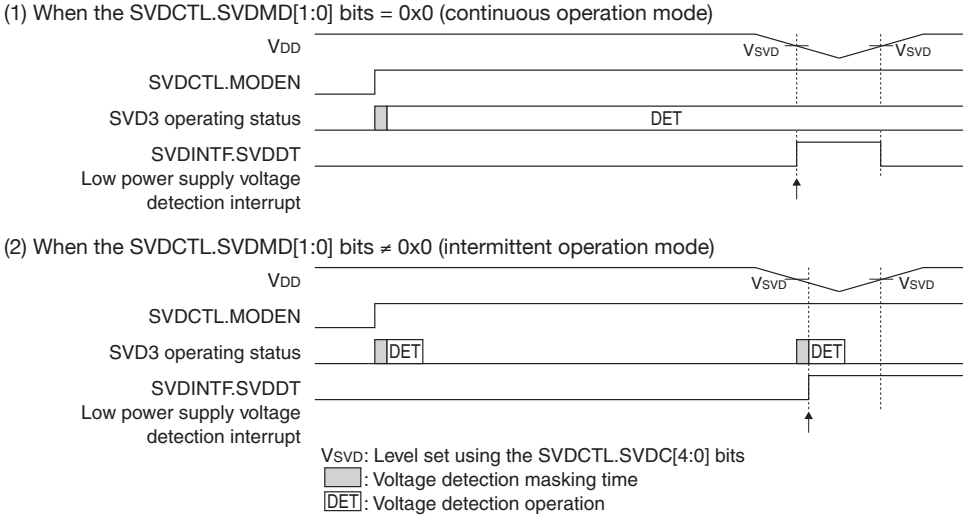


Figure 9.4.2.1 SVD3 Operations

9.5 SVD3 Interrupt and Reset

9.5.1 SVD3 Interrupt

Setting the SVDCTL.SVDRE[3:0] bits to a value other than 0xa allows use of the low power supply voltage detection interrupt function.

Table 9.5.1.1 Low Power Supply Voltage Detection Interrupt Function

Interrupt	Interrupt flag	Set condition	Clear condition
Low power supply voltage detection	SVDINTF.SVDIF	In continuous operation mode When the SVDINTF.SVDDT bit is 1 In intermittent operation mode When low power supply voltage is successively detected the specified number of times	Writing 1

SVD3 provides the interrupt enable bit (SVDINTE.SVDIE bit) corresponding to the interrupt flag (SVDINTF.SVDIF bit). An interrupt request is sent to the interrupt controller only when the SVDINTF.SVDIF bit is set while the interrupt is enabled by the SVDINTE.SVDIE bit. For more information on interrupt control, refer to the "Interrupt Controller" chapter.

Once the SVDINTF.SVDIF bit is set, it will not be cleared even if the power supply voltage subsequently returns to a value exceeding the SVD detection voltage V_{SVD}/EXSVD detection voltage V_{SVD_EXT}. An interrupt may occur due to a temporary power supply voltage drop, check the power supply voltage status by reading the SVDINTF.SVDDT bit in the interrupt handler routine.

9.5.2 SVD3 Reset

Setting the SVDCTL.SVDRE[3:0] bits to 0xa allows use of the SVD3 reset issuance function.
The reset issuing timing is the same as that of the SVDINTF.SVDIF bit being set when a low voltage is detected.
After a reset has been issued, SVD3 enters continuous operation mode even if it was operating in intermittent operation mode, and continues operating. Issuing an SVD3 reset initializes the port assignment. However, when EXSVD0/1 is being detected, the input of the port for the EXSVD0/1 pin is sent to SVD3 so that SVD3 will continue the EXSVD0/1 detection operation.
If the power supply voltage reverts to the normal level, the SVDINTF.SVDDT bit goes 0 and the reset state is canceled. After that, SVD3 resumes operating in the operation mode set previously via the initialization routine.
During reset state, the SVD3 control bits are set as shown in Table 9.5.2.1.

Table 9.5.2.1 SVD3 Control Bits During Reset State

Control register	Control bit	Setting
SVDCLK	DBRUN	Reset to the initial values.
	CLKDIV[2:0]	
	CLKSRC[1:0]	
SVDCTL	VDSEL	The set value is retained.
	SVDSC[1:0]	Cleared to 0. (The set value becomes invalid as SVD3 enters continuous operation mode.)
	SVDC[4:0]	The set value is retained.
	SVDRE[3:0]	The set value (0xa) is retained.
	EXSEL	The set value is retained.
	SVDMD[1:0]	Cleared to 0 to set continuous operation mode.
	MODEN	The set value (1) is retained.
SVDINTF	SVDIF	The status (1) before being reset is retained.
SVDINTE	SVDIE	Cleared to 0.

9.6 Control Registers

SVD3 Clock Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SVDCLK	15–9	–	0x00	–	R	–
	8	DBRUN	1	H0	R/WP	
	7	–	0	–	R	
	6–4	CLKDIV[2:0]	0x0	H0	R/WP	
	3–2	–	0x0	–	R	
	1–0	CLKSRC[1:0]	0x0	H0	R/WP	

Bits 15–9 Reserved

Bit 8 DBRUN

This bit sets whether the SVD3 operating clock is supplied in DEBUG mode or not.
1 (R/WP): Clock supplied in DEBUG mode
0 (R/WP): No clock supplied in DEBUG mode

Bit 7 Reserved

Bits 6–4 CLKDIV[2:0]

These bits select the division ratio of the SVD3 operating clock.

Bits 3–2 Reserved

Bits 1–0 CLKSRC[1:0]

These bits select the clock source of SVD3.

Table 9.6.1 Clock Source and Division Ratio Settings

SVDCLK.CLKDIV[2:0] bits	SVDCLK.CLKSRC[1:0] bits			
	0x0	0x1	0x2	0x3
	IOSC	OSC1	OSC3	EXOSC
0x7, 0x6	Reserved	1/1	Reserved	1/1
0x5	1/512		1/512	
0x4	1/256		1/256	
0x3	1/128		1/128	
0x2	1/64		1/64	
0x1	1/32		1/32	
0x0	1/16		1/16	

(Note) The oscillation circuits/external input that are not supported in this IC cannot be selected as the clock source.

Note: The clock frequency should be set to around 32 kHz.

SVD3 Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SVDCTL	15	VDSEL	0	H1	R/WP	–
	14–13	SVDSC[1:0]	0x0	H0	R/WP	Writing takes effect when the SVDCTL.SVDMD[1:0] bits are not 0x0.
	12–8	SVDC[4:0]	0x1e	H1	R/WP	–
	7–4	SVDRE[3:0]	0x0	H1	R/WP	
	3	EXSEL	0	H1	R/WP	
	2–1	SVDMD[1:0]	0x0	H0	R/WP	
	0	MODEN	0	H1	R/WP	

Bit 15 VDSEL

This bit selects the power supply voltage to be detected by SVD3.
1 (R/WP): Voltage applied to the EXSVD0/1 pin
0 (R/WP): V_{DD}

Bits 14–13 SVDSC[1:0]

These bits set the condition to generate an interrupt/reset (number of successive low voltage detections) in intermittent operation mode (SVDCTL.SVDMD[1:0] bits = 0x1 to 0x3).

Table 9.6.2 Interrupt/Reset Generating Condition in Intermittent Operation Mode

SVDCTL.SVDSC[1:0] bits	Interrupt/reset generating condition
0x3	Low power supply voltage is successively detected eight times.
0x2	Low power supply voltage is successively detected four times.
0x1	Low power supply voltage is successively detected twice.
0x0	Low power supply voltage is successively detected once.

This setting is ineffective in continuous operation mode (SVDCTL.SVDMD[1:0] bits = 0x0).

Bits 12–8 SVDC[4:0]

These bits select an SVD detection voltage V_{SVD}/EXSVD detection voltage V_{SVD_EXT} for detecting low voltage.

Table 9.6.3 Setting of SVD Detection Voltage V_{SVD}/EXSVD Detection Voltage V_{SVD_EXT}

SVDCTL.SVDC[4:0] bits	SVD detection voltage V_{SVD}/ EXSVD detection voltage V_{SVD_EXT} [V]
0x1f	High
0x1e	↑
0x1d	
:	
0x02	
0x01	↓
0x00	Low

For the configurable range and voltage values, refer to "Supply Voltage Detector Characteristics, SVD detection voltage V_{SVD}/EXSVD detection voltage V_{SVD_EXT}" in the "Electrical Characteristics" chapter.

Bits 7–4 SVDRE[3:0]

These bits enable/disable the reset issuance function when a low power supply voltage is detected.
0xa (R/WP): Enable (Issue reset)
Other than 0xa (R/WP): Disable (Generate interrupt)

For more information on the SVD3 reset issuance function, refer to "SVD3 Reset."

Bit 3 EXSEL

This bit selects the external voltage to be detected when the SVDCTL.VDSEL bit = 1.
1 (R/WP): EXSVD1
0 (R/WP): EXSVD0

Note: The EXSVD1 pin does not exist depending on the model (see "Power supply voltage to be detected" in Table 9.1.1). In this case, the external voltage detection function does not work if the SVDCTL.EXSEL bit is set to 1. When using the external voltage detection function (SVDCTL.VDSEL bit = 1), the SVDCTL.EXSEL bit should be set to 0.

Bits 2–1 SVDMD[1:0]

These bits select intermittent operation mode and its detection cycle.

Table 9.6.4 Intermittent Operation Mode Detection Cycle Selection

SVDCTL.SVDMD[1:0] bits	Operation mode (detection cycle)
0x3	Intermittent operation mode (CLK_SVD3/512)
0x2	Intermittent operation mode (CLK_SVD3/256)
0x1	Intermittent operation mode (CLK_SVD3/128)
0x0	Continuous operation mode

For more information on intermittent and continuous operation modes, refer to "SVD3 Operations."

Bit 0 MODEN

This bit enables/disables for the SVD3 circuit to operate.
1 (R/WP): Enable (Start detection operations)
0 (R/WP): Disable (Stop detection operations)

After this bit has been altered, wait until the value written is read out from this bit without subsequent operations being performed.

Notes:
- Writing 0 to the SVDCTL.MODEN bit resets the SVD3 hardware. However, the register values set and the interrupt flag are not cleared. The SVDCTL.MODEN bit is actually set to 0 after this processing has finished. If 1 is written to the SVDCTL.MODEN bit continuously without waiting for the bit being read as 0 at this time, writing 0 may be ignored and a malfunction may occur as the hardware restarts without resetting.
- The SVD3 internal circuit is initialized if the SVDCTL.SVDSC[1:0] bits, SVDCTL.SVDRE[3:0] bits, or SVDCTL.SVDMD[1:0] bits are altered while SVD3 is in operation after 1 is written to the SVDCTL.MODEN bit.

SVD3 Status and Interrupt Flag Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SVDINTF	15–9	–	0x00	–	R	–
	8	SVDDT	x	–	R	
	7–1	–	0x00	–	R	
	0	SVDIF	0	H1	R/W	Cleared by writing 1.

Bits 15–9 Reserved

Bit 8 SVDDT

The power supply voltage detection results can be read out from this bit.
1 (R): Power supply voltage (V_{DD} or EXSVD0/1) < SVD detection voltage V_{SVD} or EXSVD detection voltage V_{SVD_EXT}
0 (R): Power supply voltage (V_{DD} or EXSVD0/1) ≥ SVD detection voltage V_{SVD} or EXSVD detection voltage V_{SVD_EXT}

Bits 7–1 Reserved

Bit 0 SVDIF

This bit indicates the low power supply voltage detection interrupt cause occurrence status.

1 (R): Cause of interrupt occurred
0 (R): No cause of interrupt occurred
1 (W): Clear flag
0 (W): Ineffective

Note: The SVD3 internal circuit is initialized if the interrupt flag is cleared while SVD3 is in operation after 1 is written to the SVDCTL.MODEN bit.

SVD3 Interrupt Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SVDINTE	15–8	–	0x00	–	R	–
	7–1	–	0x00	–	R	
	0	SVDIE	0	H0	R/W	

Bits 15–1 Reserved

Bit 0 SVDIE

This bit enables low power supply voltage detection interrupts.

1 (R/W): Enable interrupts
0 (R/W): Disable interrupts

Notes:
- If the SVDCTL.SVDRE[3:0] bits are set to 0xa, no low power supply voltage detection interrupt will occur, as a reset is issued at the same timing as an interrupt.
- To prevent generating unnecessary interrupts, the corresponding interrupt flag should be cleared before enabling interrupts.

10 16-bit Timers (T16)

10.1 Overview

T16 is a 16-bit timer. The features of T16 are listed below.

- 16-bit presettable down counter
- Provides a reload data register for setting the preset value.
- A clock source and clock division ratio for generating the count clock are selectable.
- Repeat mode or one-shot mode is selectable.
- Can generate counter underflow interrupts.

Figure 10.1.1 shows the configuration of a T16 channel.

Table 10.1.1 T16 Channel Configuration of S1C17F63

Item	S1C17F63
Number of channels	4 channels (Ch.0–Ch.3)
Event counter function	Not supported (No EXCL*m* pins are provided.)
Peripheral clock output (Outputs the counter underflow signal.)	Ch.1 → Synchronous serial interface Ch.0 master clock Ch.2 → 12-bit A/D converter trigger signal Ch.3 → Synchronous serial interface Ch.1 master clock

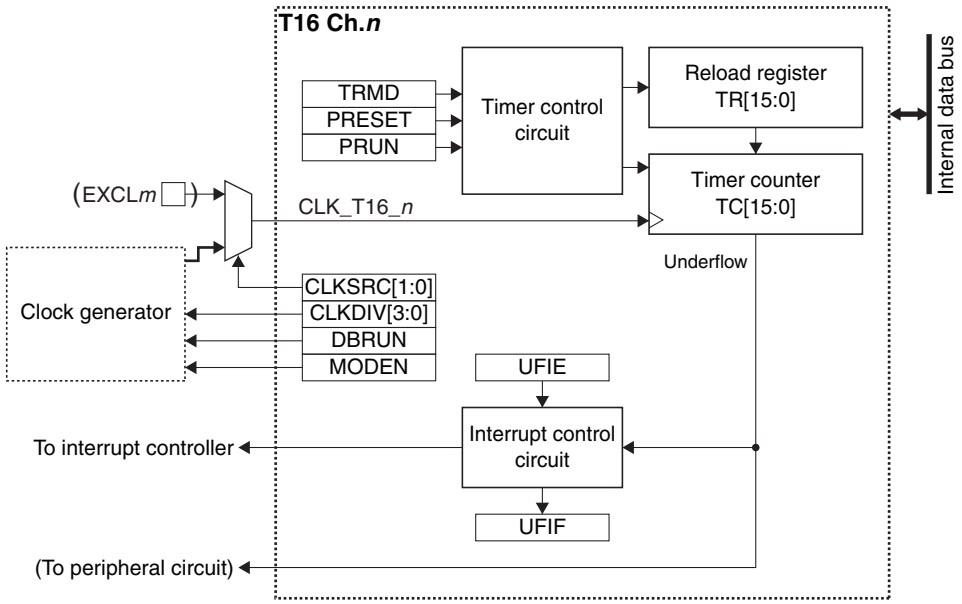


Figure 10.1.1 Configuration of a T16 Channel

10.2 Input Pin

Table 10.2.1 shows the T16 input pin.

Table 10.2.1 T16 Input Pin

Pin name	I/O*	Initial status*	Function
EXCL*m*	I	I (Hi-Z)	External event signal input pin

* Indicates the status when the pin is configured for T16.

If the port is shared with the EXCL*m* pin and other functions, the EXCL*m* input function must be assigned to the port before using the event counter function. For more information, refer to the "I/O Ports" chapter.

10.3 Clock Settings

10.3.1 T16 Operating Clock

When using T16 Ch.*n*, the T16 Ch.*n* operating clock CLK_T16_*n* must be supplied to T16 Ch.*n* from the clock generator. The CLK_T16_*n* supply should be controlled as in the procedure shown below.

1. Enable the clock source in the clock generator if it is stopped (refer to "Clock Generator" in the "Power Supply, Reset, and Clocks" chapter).
2. Set the following T16_*n*CLK register bits:
   - T16_*n*CLK.CLKSRC[1:0] bits (Clock source selection)
   - T16_*n*CLK.CLKDIV[3:0] bits (Clock division ratio selection = Clock frequency setting)

10.3.2 Clock Supply in SLEEP Mode

When using T16 during SLEEP mode, the T16 operating clock CLK_T16_*n* must be configured so that it will keep supplying by writing 0 to the CLGOSC.*xxxx*SLPC bit for the CLK_T16_*n* clock source.
If the CLGOSC.*xxxx*SLPC bit for the CLK_T16_*n* clock source is 1, the CLK_T16_*n* clock source is deactivated during SLEEP mode and T16 stops with the register settings and counter value maintained at those before entering SLEEP mode. After the CPU returns to normal mode, CLK_T16_*n* is supplied and the T16 operation resumes.

10.3.3 Clock Supply in DEBUG Mode

The CLK_T16_*n* supply during DEBUG mode should be controlled using the T16_*n*CLK.DBRUN bit.
The CLK_T16_*n* supply to T16 Ch.*n* is suspended when the CPU enters DEBUG mode if the T16_*n*CLK.DBRUN bit = 0. After the CPU returns to normal mode, the CLK_T16_*n* supply resumes. Although T16 Ch.*n* stops operating when the CLK_T16_*n* supply is suspended, the counter and registers retain the status before DEBUG mode was entered. If the T16_*n*CLK.DBRUN bit = 1, the CLK_T16_*n* supply is not suspended and T16 Ch.*n* will keep operating in DEBUG mode.

10.3.4 Event Counter Clock

The channel that supports the event counter function counts down at the rising edge of the EXCL*m* pin input signal when the T16_*n*CLK.CLKSRC[1:0] bits are set to 0x3.

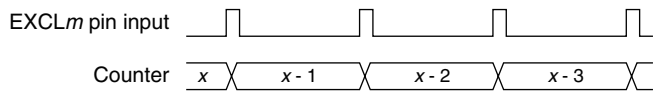


Figure 10.3.4.1 Count Down Timing

Note that the EXOSC clock is selected for the channel that does not support the event counter function.

10.4 Operations

10.4.1 Initialization

T16 Ch.*n* should be initialized and started counting with the procedure shown below.

1. Configure the T16 Ch.*n* operating clock (see "T16 Operating Clock").
2. Set the T16_*n*CTL.MODEN bit to 1. (Enable count operation clock)
3. Set the T16_*n*MOD.TRMD bit. (Select operation mode (Repeat mode or One-shot mode))
4. Set the T16_*n*TR register. (Set reload data (counter preset data))
5. Set the following bits when using the interrupt:
   - Write 1 to the T16_*n*INTF.UFIF bit. (Clear interrupt flag)
   - Set the T16_*n*INTE.UFIE bit to 1. (Enable underflow interrupt)

6. Set the following T16_*n*CTL register bits:
   - Set the T16_*n*CTL.PRESET bit to 1. (Preset reload data to counter)
   - Set the T16_*n*CTL.PRUN bit to 1. (Start counting)

10.4.2 Counter Underflow

Normally, the T16 counter starts counting down from the reload data value preset and generates an underflow signal when an underflow occurs. This signal is used to generate an interrupt and may be output to a specific peripheral circuit as a clock (T16 Ch.*n* must be set to repeat mode to generate a clock). The underflow cycle is determined by the T16 Ch.*n* operating clock setting and reload data (counter initial value) set in the T16_*n*TR register.
The following shows the equations to calculate the underflow cycle and frequency:

$$T = \frac{TR + 1}{f_{CLK\_T16\_n}} \qquad f_T = \frac{f_{CLK\_T16\_n}}{TR + 1} \qquad \text{(Eq. 10.1)}$$

Where

T: Underflow cycle [s]
fT: Underflow frequency [Hz]
TR: T16_*n*TR register setting
$f_{CLK\_T16\_n}$: T16 Ch.*n* operating clock frequency [Hz]

10.4.3 Operations in Repeat Mode

T16 Ch.*n* enters repeat mode by setting the T16_*n*MOD.TRMD bit to 0.
In repeat mode, the count operation starts by writing 1 to the T16_*n*CTL.PRUN bit and continues until 0 is written. A counter underflow presets the T16_*n*TR register value to the counter, so underflow occurs periodically. Select this mode to generate periodic underflow interrupts or when using the timer to output a trigger/clock to the peripheral circuit.

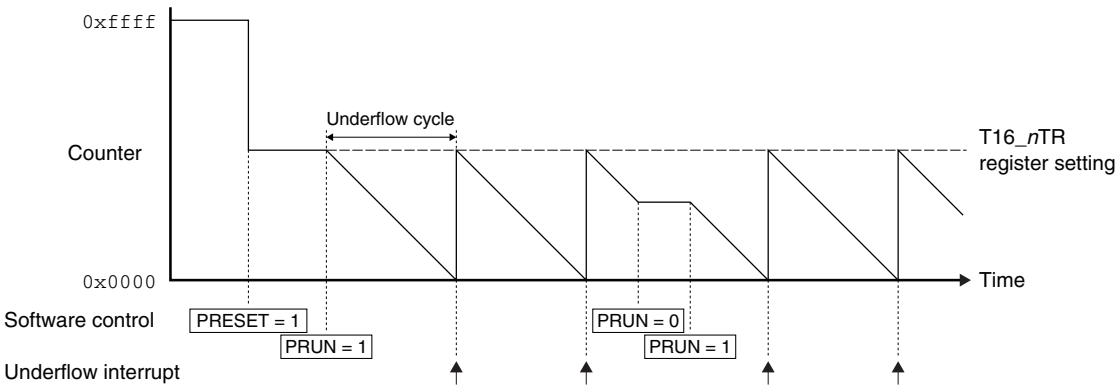


Figure 10.4.3.1 Count Operations in Repeat Mode

10.4.4 Operations in One-shot Mode

T16 Ch.*n* enters one-shot mode by setting the T16_*n*MOD.TRMD bit to 1.
In one-shot mode, the count operation starts by writing 1 to the T16_*n*CTL.PRUN bit and stops after the T16_*n*TR register value is preset to the counter when an underflow has occurred. At the same time the counter stops, the T16_*n*CTL.PRUN bit is cleared automatically. Select this mode to stop the counter after an interrupt has occurred once, such as for checking a specific lapse of time.

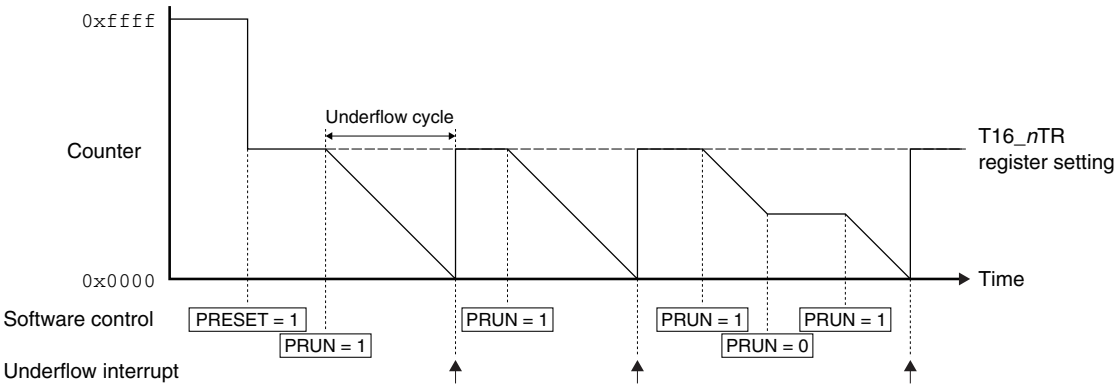


Figure 10.4.4.1 Count Operations in One-shot Mode

10.4.5 Counter Value Read

The counter value can be read out from the T16_*n*TC.TC[15:0] bits. However, since T16 operates on CLK_T16_*n*, one of the operations shown below is required to read correctly by the CPU.

- Read the counter value twice or more and check to see if the same value is read.
- Stop the timer and then read the counter value.

10.5 Interrupt

Each T16 channel has a function to generate the interrupt shown in Table 10.5.1.

Table 10.5.1 T16 Interrupt Function

Interrupt	Interrupt flag	Set condition	Clear condition
Underflow	T16_*n*INTF.UFIF	When the counter underflows	Writing 1

T16 provides interrupt enable bits corresponding to each interrupt flag. An interrupt request is sent to the interrupt controller only when the interrupt flag, of which interrupt has been enabled by the interrupt enable bit, is set. For more information on interrupt control, refer to the "Interrupt Controller" chapter.

10.6 Control Registers

T16 Ch.*n* Clock Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16_*n*CLK	15–9	–	0x00	–	R	–
	8	DBRUN	0	H0	R/W	
	7–4	CLKDIV[3:0]	0x0	H0	R/W	
	3–2	–	0x0	–	R	
	1–0	CLKSRC[1:0]	0x0	H0	R/W	

Bits 15–9 Reserved

Bit 8 DBRUN

This bit sets whether the T16 Ch.*n* operating clock is supplied in DEBUG mode or not.
1 (R/W): Clock supplied in DEBUG mode
0 (R/W): No clock supplied in DEBUG mode

Bits 7–4 CLKDIV[3:0]

These bits select the division ratio of the T16 Ch.*n* operating clock (counter clock).

Bits 3–2 Reserved

Bits 1–0 CLKSRC[1:0]

These bits select the clock source of T16 Ch.*n*.

Table 10.6.1 Clock Source and Division Ratio Settings

T16_*n*CLK.CLKDIV[3:0] bits	T16_*n*CLK.CLKSRC[1:0] bits			
	0x0	0x1	0x2	0x3
	IOSC	OSC1	OSC3	EXOSC/EXCL*m*
0xf	1/32,768	1/1	1/32,768	1/1
0xe	1/16,384		1/16,384	
0xd	1/8,192		1/8,192	
0xc	1/4,096		1/4,096	
0xb	1/2,048		1/2,048	
0xa	1/1,024		1/1,024	
0x9	1/512		1/512	
0x8	1/256	1/256	1/256	
0x7	1/128	1/128	1/128	
0x6	1/64	1/64	1/64	
0x5	1/32	1/32	1/32	
0x4	1/16	1/16	1/16	
0x3	1/8	1/8	1/8	
0x2	1/4	1/4	1/4	
0x1	1/2	1/2	1/2	
0x0	1/1	1/1	1/1	

(Note 1) The oscillation circuits/external input that are not supported in this IC cannot be selected as the clock source.
(Note 2) When the T16_*n*CLK.CLKSRC[1:0] bits are set to 0x3, EXCL*m* is selected for the channel with an event counter function or EXOSC is selected for other channels.

T16 Ch.*n* Mode Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16_*n*MOD	15–8	–	0x00	–	R	–
	7–1	–	0x00	–	R	
	0	TRMD	0	H0	R/W	

Bits 15–1 Reserved

Bit 0 TRMD

This bit selects the T16 operation mode.
1 (R/W): One-shot mode
0 (R/W): Repeat mode

For detailed information on the operation mode, refer to "Operations in One-shot Mode" and "Operations in Repeat Mode."

T16 Ch.*n* Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16_*n*CTL	15–9	–	0x00	–	R	–
	8	PRUN	0	H0	R/W	
	7–2	–	0x00	–	R	
	1	PRESET	0	H0	R/W	
	0	MODEN	0	H0	R/W	

Bits 15–9 Reserved

Bit 8 PRUN

This bit starts/stops the timer.
1 (W): Start timer
0 (W): Stop timer
1 (R): Timer is running
0 (R): Timer is idle

By writing 1 to this bit, the timer starts count operations. However, the T16_*n*CTL.MODEN bit must be set to 1 in conjunction with this bit or it must be set in advance. While the timer is running, writing 0 to this bit stops count operations. When the counter stops due to a counter underflow in one-shot mode, this bit is automatically cleared to 0.

Bits 7–2 Reserved

Bit 1 PRESET

This bit presets the reload data stored in the T16_*n*TR register to the counter.

1 (W): Preset
0 (W): Ineffective
1 (R): Presetting in progress
0 (R): Presetting finished or normal operation

By writing 1 to this bit, the timer presets the T16_*n*TR register value to the counter. However, the T16_*n*CTL.MODEN bit must be set to 1 in conjunction with this bit or it must be set in advance. This bit retains 1 during presetting and is automatically cleared to 0 after presetting has finished.

Bit 0 MODEN

This bit enables the T16 Ch.*n* operations.

1 (R/W): Enable (Start supplying operating clock)
0 (R/W): Disable (Stop supplying operating clock)

T16 Ch.*n* Reload Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16_*n*TR	15–0	TR[15:0]	0xffff	H0	R/W	–

Bits 15–0 TR[15:0]

These bits are used to set the initial value to be preset to the counter.
The value set to this register will be preset to the counter when 1 is written to the T16_*n*CTL.PRESET bit or when the counter underflows.

Notes:
- The T16_*n*TR register cannot be altered while the timer is running (T16_*n*CTL.PRUN bit = 1), as an incorrect initial value may be preset to the counter.
- When one-shot mode is set, the T16_*n*TR.TR[15:0] bits should be set to a value equal to or greater than 0x0001.

T16 Ch.*n* Counter Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16_*n*TC	15–0	TC[15:0]	0xffff	H0	R	–

Bits 15–0 TC[15:0]

The current counter value can be read out from these bits.

T16 Ch.*n* Interrupt Flag Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16_*n*INTF	15–8	–	0x00	–	R	–
	7–1	–	0x00	–	R	
	0	UFIF	0	H0	R/W	Cleared by writing 1.

Bits 15–1 Reserved

Bit 0 UFIF

This bit indicates the T16 Ch.*n* underflow interrupt cause occurrence status.

1 (R): Cause of interrupt occurred
0 (R): No cause of interrupt occurred
1 (W): Clear flag
0 (W): Ineffective

T16 Ch.*n* Interrupt Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16_*n*INTE	15–8	–	0x00	–	R	–
	7–1	–	0x00	–	R	
	0	UFIE	0	H0	R/W	

Bits 15–1 Reserved

Bit 0 UFIE

This bit enables T16 Ch.*n* underflow interrupts.

1 (R/W): Enable interrupts

0 (R/W): Disable interrupts

Note: To prevent generating unnecessary interrupts, the corresponding interrupt flag should be cleared before enabling interrupts.

11 UART (UART3)

11.1 Overview

The UART3 is an asynchronous serial interface. The features of the UART3 are listed below.

- Includes a baud rate generator for generating the transfer clock.
- Supports 7- and 8-bit data length (LSB first).
- Odd parity, even parity, or non-parity mode is selectable.
- The start bit length is fixed at 1 bit.
- The stop bit length is selectable from 1 bit and 2 bits.
- Supports full-duplex communications.
- Includes a 2-byte receive data buffer and a 1-byte transmit data buffer.
- Includes an RZI modulator/demodulator circuit to support IrDA 1.0-compatible infrared communications.
- Can detect parity error, framing error, and overrun error.
- Can generate receive buffer full (1 byte/2 bytes), transmit buffer empty, end of transmission, parity error, framing error, and overrun error interrupts.
- Input pin can be pulled up with an internal resistor.
- The output pin is configurable as an open-drain output.
- Provides the carrier modulation output function.

Figure 11.1.1 shows the UART3 configuration.

Table 11.1.1 UART3 Channel Configuration of S1C17F63

Item	S1C17F63
Number of channels	1 channel (Ch.0)

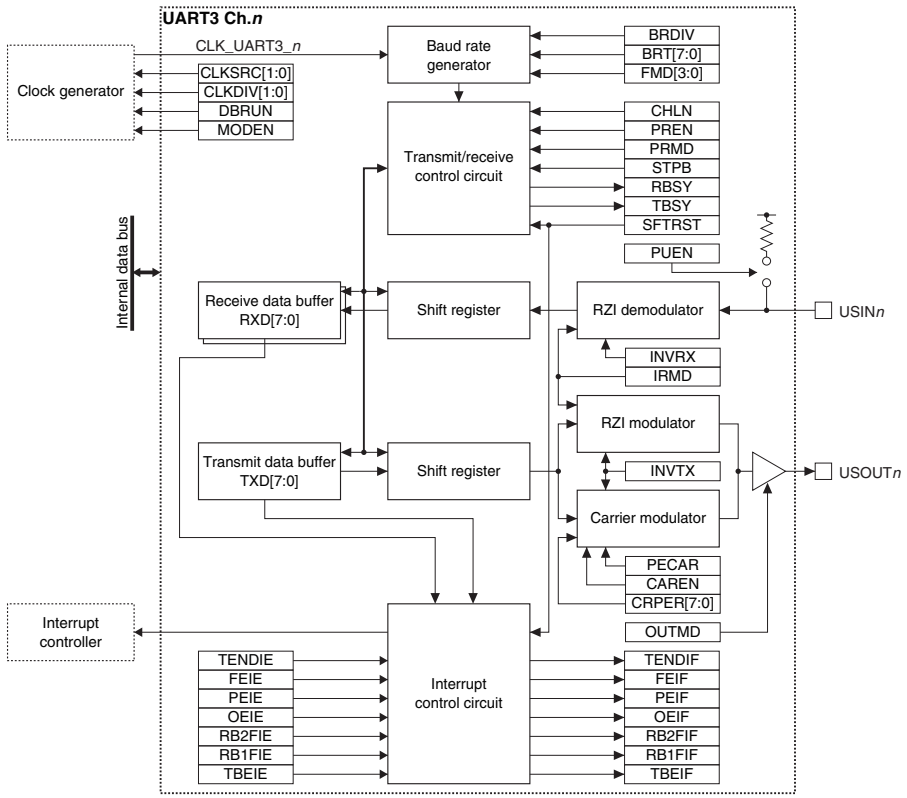


Figure 11.1.1 UART3 Configuration

11.2 Input/Output Pins and External Connections

11.2.1 List of Input/Output Pins

Table 11.2.1.1 lists the UART3 pins.

Table 11.2.1.1 List of UART3 Pins

Pin name	I/O*	Initial status*	Function
USIN*n*	I	I (Hi-Z)	UART3 Ch.*n* data input pin
USOUT*n*	O	O (High)	UART3 Ch.*n* data output pin

* Indicates the status when the pin is configured for the UART3.

If the port is shared with the UART3 pin and other functions, the UART3 input/output function must be assigned to the port before activating the UART3. For more information, refer to the "I/O Ports" chapter.

11.2.2 External Connections

Figure 11.2.2.1 shows a connection diagram between the UART3 in this IC and an external UART device.

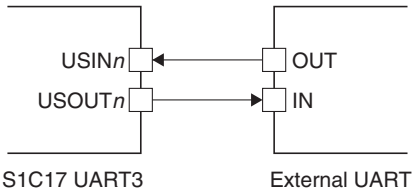


Figure 11.2.2.1 Connections between UART3 and an External UART Device

11.2.3 Input Pin Pull-Up Function

The UART3 includes a pull-up resistor for the USIN*n* pin. Setting the UA*n*MOD.PUEN bit to 1 enables the resistor to pull up the USIN*n* pin.

11.2.4 Output Pin Open-Drain Output Function

The USOUT*n* pin supports the open-drain output function. Default configuration is a push-pull output and it is switched to an open-drain output by setting the UA*n*MOD.OUTMD bit to 1.

11.2.5 Input/Output Signal Inverting Function

The UART3 can invert the signal polarities of the USIN*n* pin input and the USOUT*n* pin output by setting the UA*n*MOD.INVRX bit and the UA*n*MOD.INVTX bit, respectively, to 1.

Note: Unless otherwise specified, this chapter shows input/output signals with non-inverted waveforms (UA*n*MOD.INVRX bit = 0, UA*n*MOD.INVTX bit =0).

11.3 Clock Settings

11.3.1 UART3 Operating Clock

When using the UART3 Ch.*n*, the UART3 Ch.*n* operating clock CLK_UART3_*n* must be supplied to the UART3 Ch.*n* from the clock generator. The CLK_UART3_*n* supply should be controlled as in the procedure shown below.

1. Enable the clock source in the clock generator if it is stopped (refer to "Clock Generator" in the "Power Supply, Reset, and Clocks" chapter).
2. Set the following UA*n*CLK register bits:
   - UA*n*CLK.CLKSRC[1:0] bits (Clock source selection)
   - UA*n*CLK.CLKDIV[1:0] bits (Clock division ratio selection = Clock frequency setting)

   The UART3 operating clock should be selected so that the baud rate generator will be configured easily.

11.3.2 Clock Supply in SLEEP Mode

When using the UART3 during SLEEP mode, the UART3 operating clock CLK_UART3_*n* must be configured so that it will keep supplying by writing 0 to the CLGOSC.*xxxx*SLPC bit for the CLK_UART3_*n* clock source.

11.3.3 Clock Supply in DEBUG Mode

The CLK_UART3_*n* supply during DEBUG mode should be controlled using the UA*n*CLK.DBRUN bit.
The CLK_UART3_*n* supply to the UART3 Ch.*n* is suspended when the CPU enters DEBUG mode if the UA*n*CLK.DBRUN bit = 0. After the CPU returns to normal mode, the CLK_UART3_*n* supply resumes. Although the UART3 Ch.*n* stops operating when the CLK_UART3_*n* supply is suspended, the output pin and registers retain the status before DEBUG mode was entered. If the UA*n*CLK.DBRUN bit = 1, the CLK_UART3_*n* supply is not suspended and the UART3 Ch.*n* will keep operating in DEBUG mode.

11.3.4 Baud Rate Generator

The UART3 includes a baud rate generator to generate the transfer (sampling) clock. The transfer rate is determined by the UA*n*MOD.BRDIV, UA*n*BR.BRT[7:0], and UA*n*BR.FMD[3:0] bit settings. Use the following equations to calculate the setting values for obtaining the desired transfer rate.

$$bps = \frac{CLK\_UART3}{\frac{BRT + 1}{BRDIV} + FMD} \qquad BRT = BRDIV \times \left(\frac{CLK\_UART3}{bps} - FMD\right) - 1 \qquad \text{(Eq. 11.1)}$$

Where

bps:	Transfer rate [bit/s]
CLK_UART3:	UART3 operating clock frequency [Hz]
BRDIV:	Baud rate division ratio (1/16 or 1/4) * Selected by the UA*n*MOD.BRDIV bit
BRT:	UA*n*BR.BRT[7:0] setting value (0 to 255)
FMD:	UA*n*BR.FMD[3:0] setting value (0 to 15)

For the transfer rate range configurable in the UART3, refer to "UART Characteristics, Transfer baud rates U_{BRT1} and U_{BRT2}" in the "Electrical Characteristics" chapter.

11.4 Data Format

The UART3 allows setting of the data length, stop bit length, and parity function. The start bit length is fixed at one bit.

Data length

With the UA*n*MOD.CHLN bit, the data length can be set to seven bits (UA*n*MOD.CHLN bit = 0) or eight bits (UA*n*MOD.CHLN bit = 1).

Stop bit length

With the UA*n*MOD.STPB bit, the stop bit length can be set to one bit (UA*n*MOD.STPB bit = 0) or two bits (UA*n*MOD.STPB bit = 1).

Parity function

The parity function is configured using the UA*n*MOD.PREN and UA*n*MOD.PRMD bits.

Table 11.4.1 Parity Function Setting

UA*n*MOD.PREN bit	UA*n*MOD.PRMD bit	Parity function
1	1	Odd parity
1	0	Even parity
0	*	Non parity

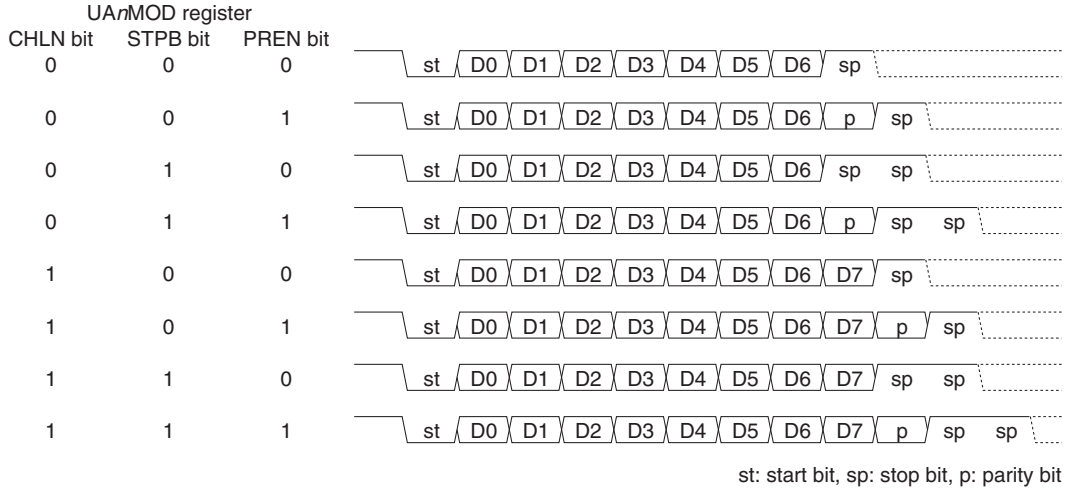


Figure 11.4.1 Data Format

11.5 Operations

11.5.1 Initialization

The UART3 Ch.*n* should be initialized with the procedure shown below.

1. Assign the UART3 Ch.*n* input/output function to the ports. (Refer to the "I/O Ports" chapter.)
2. Set the UA*n*CLK.CLKSRC[1:0] and UA*n*CLK.CLKDIV[1:0] bits. (Configure operating clock)
3. Configure the following UA*n*MOD register bits:
   - UA*n*MOD.BRDIV bit (Select baud rate division ratio (1/16 or 1/4))
   - UAnMOD.INVRX bit (Enable/disable USIN*n* input signal inversion)
   - UAnMOD.INVTX bit (Enable/disable USOUT*n* output signal inversion)
   - UA*n*MOD.PUEN bit (Enable/disable USIN*n* pin pull-up)
   - UA*n*MOD.OUTMD bit (Enable/disable USOUT*n* pin open-drain output)
   - UA*n*MOD.IRMD bit (Enable/disable IrDA interface)
   - UA*n*MOD.CHLN bit (Set data length (7 or 8 bits))
   - UA*n*MOD.PREN bit (Enable/disable parity function)
   - UA*n*MOD.PRMD bit (Select parity mode (even or odd))
   - UA*n*MOD.STPB bit (Set stop bit length (1 or 2 bits))
   - UA*n*MOD.CAREN bit (Enable/disable carrier modulation function)
   - UAnMOD.PECAR bit (Select carrier modulation period (H data period/L data period))
4. Set the UA*n*BR.BRT[7:0] and UA*n*BR.FMD[3:0] bits. (Set transfer rate)
5. Set the UA*n*CAWF.CRPER[7:0] bits. (Set carrier cycle)
6. Set the following UA*n*CTL register bits:
   - Set the UA*n*CTL.SFTRST bit to 1. (Execute software reset)
   - Set the UA*n*CTL.MODEN bit to 1. (Enable UART3 Ch.*n* operations)
7. Set the following bits when using the interrupt:
   - Write 1 to the interrupt flags in the UA*n*INTF register. (Clear interrupt flags)
   - Set the interrupt enable bits in the UA*n*INTE register to 1. * (Enable interrupts)

   * The initial value of the UA*n*INTF.TBEIF bit is 1, therefore, an interrupt will occur immediately after the UA*n*INTE.TBEIE bit is set to 1.

11.5.2 Data Transmission

A data sending procedure and the UART3 Ch.*n* operations are shown below. Figures 11.5.2.1 and 11.5.2.2 show a timing chart and a flowchart, respectively.

Data sending procedure

1. Check to see if the UA*n*INTF.TBEIF bit is set to 1 (transmit buffer empty).
2. Write transmit data to the UA*n*TXD register.
3. Wait for a UART3 interrupt when using the interrupt.
4. Repeat Steps 1 to 3 (or 1 and 2) until the end of transmit data.

UART3 data sending operations

The UART3 Ch.*n* starts data sending operations when transmit data is written to the UA*n*TXD register.
The transmit data in the UA*n*TXD register is automatically transferred to the shift register and the UA*n*INTF.TBEIF bit is set to 1 (transmit buffer empty).
The USOUT*n* pin outputs a start bit and the UA*n*INTF.TBSY bit is set to 1 (transmit busy). The shift register data bits are then output successively from the LSB. Following output of MSB, the parity bit (if parity is enabled) and the stop bit are output.

Even if transmit data is being output from the USOUT*n* pin, the next transmit data can be written to the UA*n*TXD register after making sure the UA*n*INTF.TBEIF bit is set to 1.

If no transmit data remains in the UA*n*TXD register after the stop bit has been output from the USOUT*n* pin, the UA*n*INTF.TBSY bit is cleared to 0 and the UA*n*INTF.TENDIF bit is set to 1 (transmission completed).

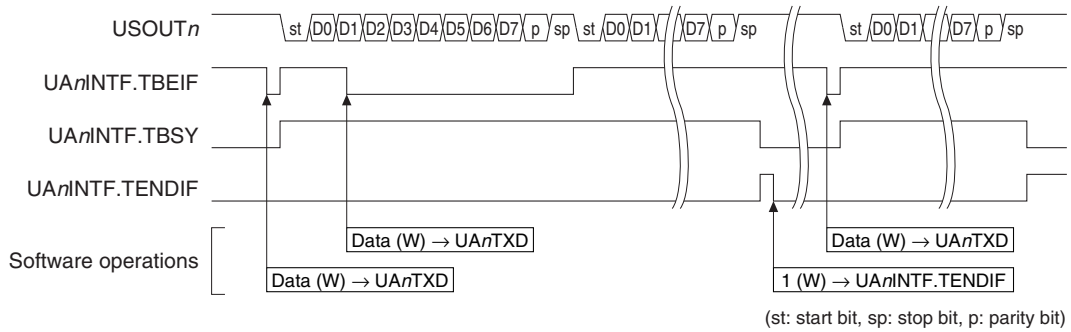


Figure 11.5.2.1 Example of Data Sending Operations

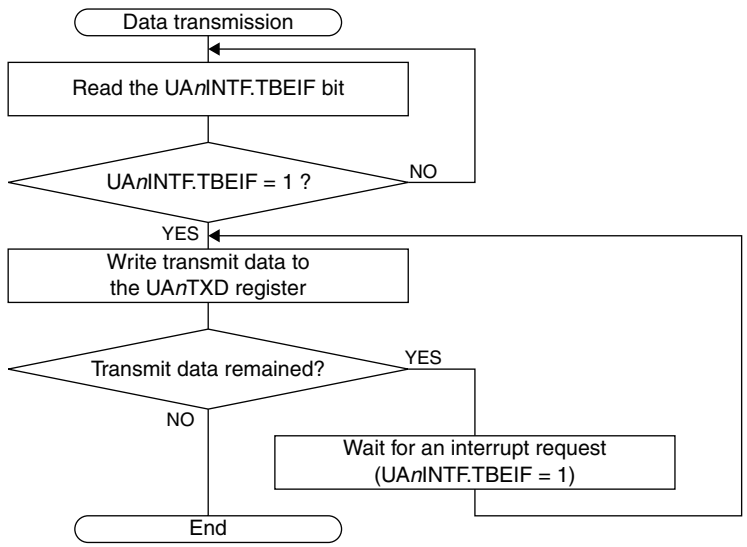


Figure 11.5.2.2 Data Transmission Flowchart

11.5.3 Data Reception

A data receiving procedure and the UART3 Ch.*n* operations are shown below. Figures 11.5.3.1 and 11.5.3.2 show a timing chart and flowcharts, respectively.

Data receiving procedure (read by one byte)

1. Wait for a UART3 interrupt when using the interrupt.
2. Check to see if the UA*n*INTF.RB1FIF bit is set to 1 (receive buffer one byte full).
3. Read the received data from the UA*n*RXD register.
4. Repeat Steps 1 to 3 (or 2 and 3) until the end of data reception.

Data receiving procedure (read by two bytes)

1. Wait for a UART3 interrupt when using the interrupt.
2. Check to see if the UA*n*INTF.RB2FIF bit is set to 1 (receive buffer two bytes full).
3. Read the received data from the UA*n*RXD register twice.
4. Repeat Steps 1 to 3 (or 2 and 3) until the end of data reception.

UART3 data receiving operations

The UART3 Ch.*n* starts data receiving operations when a start bit is input to the USIN*n* pin.
After the receive circuit has detected a low level as a start bit, it starts sampling the following data bits and loads the received data into the receive shift register. The UA*n*INTF.RBSY bit is set to 1 when the start bit is detected.
The UA*n*INTF.RBSY bit is cleared to 0 and the receive shift register data is transferred to the receive data buffer at the stop bit receive timing.
The receive data buffer consists of a 2-byte FIFO and receives data until it becomes full. When the receive data buffer receives the first data, it sets the UA*n*INTF.RB1FIF bit to 1 (receive buffer one byte full). If the second data is received without reading the first data, the UA*n*INTF.RB2FIF bit is set to 1 (receive buffer two bytes full).

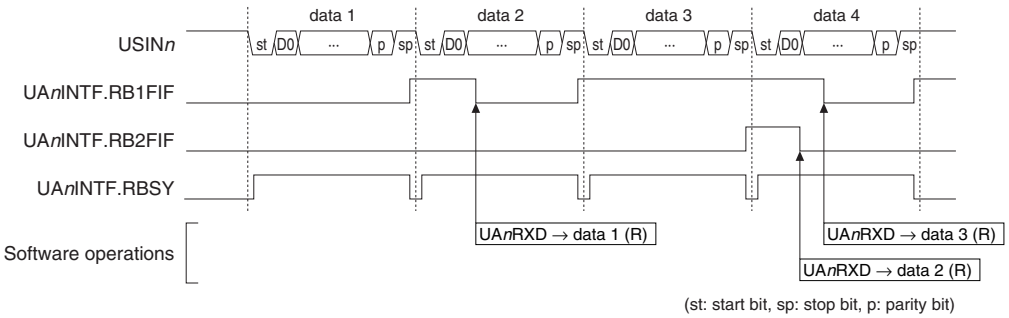


Figure 11.5.3.1 Example of Data Receiving Operations

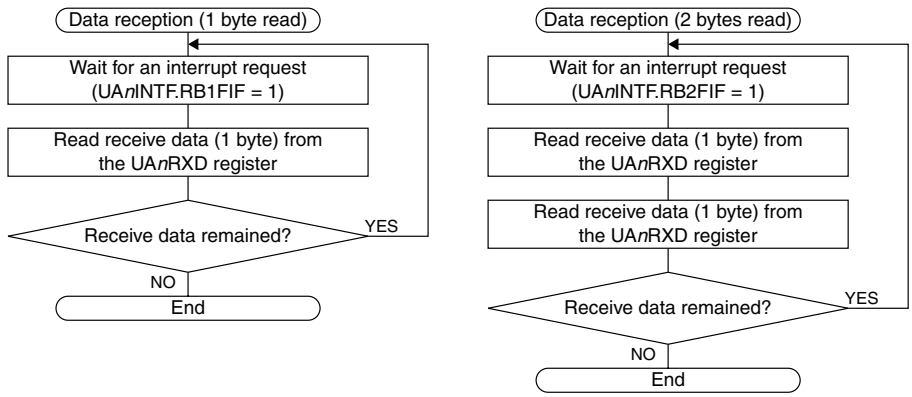


Figure 11.5.3.2 Data Reception Flowcharts

11.5.4 IrDA Interface

This UART3 includes an RZI modulator/demodulator circuit enabling implementation of IrDA 1.0-compatible infrared communication function simply by adding simple external circuits.
Set the UA*n*MOD.IRMD bit to 1 to use the IrDA interface.
Data transfer control is identical to that for normal interface even if the IrDA interface function is enabled.

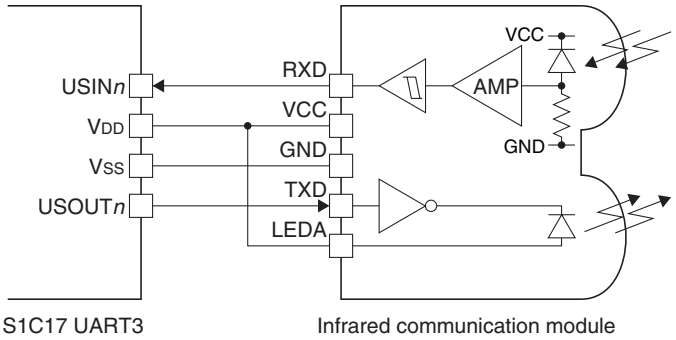


Figure 11.5.4.1 Example of Connections with an Infrared Communication Module

The transmit data output from the UART3 Ch.*n* transmit shift register is output from the USOUT*n* pin after the low pulse width is converted into 3/16 by the RZI modulator in SIR method.

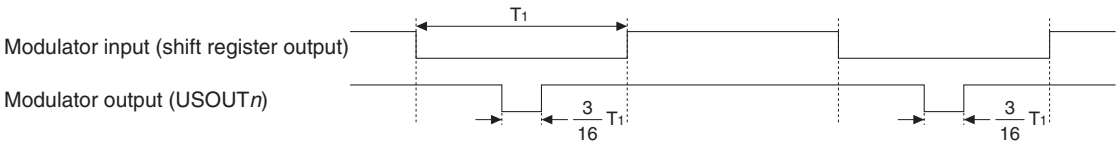


Figure 11.5.4.2 IrDA Transmission Signal Waveform

The received IrDA signal is input to the RZI demodulator and the low pulse width is converted into the normal width before input to the receive shift register.

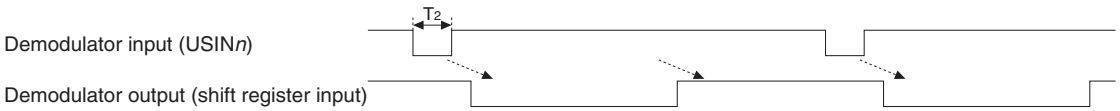


Figure 11.5.4.3 IrDA Receive Signal Waveform

Notes: • Set the baud rate division ratio to 1/16 when using the IrDA interface function.

• The low pulse width (T_2) of the IrDA signal input must be CLK_UART3 × 3 cycles or longer.

11.5.5 Carrier Modulation

The UART3 has a carrier modulation function.
Writing 1 to the UA*n*MOD.CAREN bit enables the carrier modulation function allowing carrier modulation waveforms to be output according to the UA*n*MOD.PECAR bit setting. Data transmit control is identical to that for normal interface even in this case.

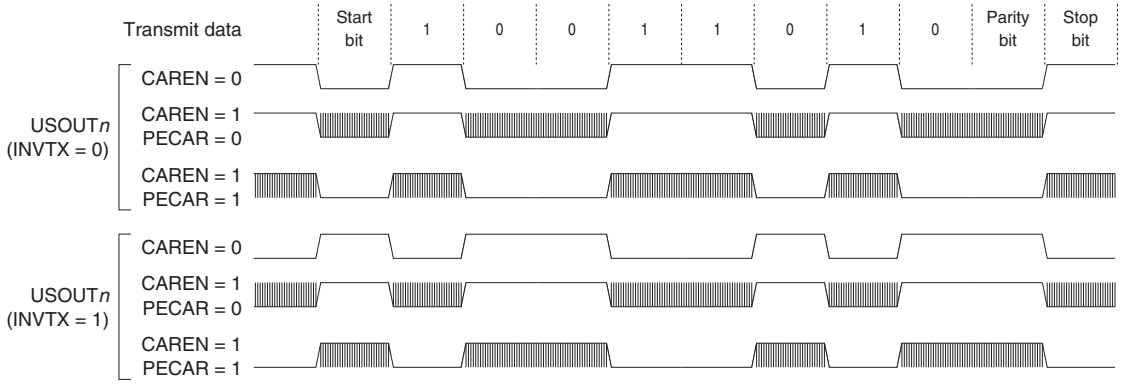


Figure 11.5.5.1 Carrier Modulation Waveform (UA*n*MOD.CHLN = 1, UA*n*MOD.STPB = 0, UA*n*MOD.PREN = 1)

The carrier modulation output frequency is determined by the UA*n*CAWF.CRPER[7:0] bit settings. Use the following equations to calculate the setting values for obtaining the desired frequency.

$$\text{Carrier modulation output frequency} = \frac{\text{CLK\_UART3}}{(\text{CRPER} + 1) \times 2} \text{ [Hz]} \qquad \text{(Eq. 11.2)}$$

Where

CLK_UART3: UART3 operating clock frequency [Hz]
CRPER: UA*n*CAWF.CRPER[7:0] setting value (0 to 255)

11.6 Receive Errors

Three different receive errors, framing error, parity error, and overrun error, may be detected while receiving data. Since receive errors are interrupt causes, they can be processed by generating interrupts.

11.6.1 Framing Error

The UART3 determines loss of sync if a stop bit is not detected (when the stop bit is received as 0) and assumes that a framing error has occurred. The received data that encountered an error is still transferred to the receive data buffer and the UA*n*INTF.FEIF bit (framing error interrupt flag) is set to 1 when the data becomes ready to read from the UA*n*RXD register.

Note: Framing error/parity error interrupt flag set timings
These interrupt flags will be set after the data that encountered an error is transferred to the receive data buffer. Note, however, that the set timing depends on the buffer status at that point.

- When the receive data buffer is empty
  The interrupt flag will be set when the data that encountered an error is transferred to the receive data buffer.
- When the receive data buffer has a one-byte free space
  The interrupt flag will be set when the first data byte already loaded is read out after the data that encountered an error is transferred to the second byte entry of the receive data buffer.

11.6.2 Parity Error

If the parity function is enabled, a parity check is performed when data is received. The UART3 checks matching between the data received in the shift register and its parity bit, and issues a parity error if the result is a non-match. The received data that encountered an error is still transferred to the receive data buffer and the UA*n*INTF.PEIF bit (parity error interrupt flag) is set to 1 when the data becomes ready to read from the UA*n*RXD register (see the Note on framing error).

11.6.3 Overrun Error

If the receive data buffer is still full (two bytes of received data have not been read) when a data reception to the shift register has completed, an overrun error occurs as the data cannot be transferred to the receive data buffer. When an overrun error occurs, the UA*n*INTF.OEIF bit (overrun error interrupt flag) is set to 1.

11.7 Interrupts

The UART3 has a function to generate the interrupts shown in Table 11.7.1.

Table 11.7.1 UART3 Interrupt Function

Interrupt	Interrupt flag	Set condition	Clear condition
End of transmission	UA*n*INTF.TENDIF	When the UA*n*INTF.TBEIF bit = 1 after the stop bit has been sent	Writing 1 or software reset
Framing error	UA*n*INTF.FEIF	Refer to the "Receive Errors."	Writing 1, reading received data that encountered an error, or software reset
Parity error	UA*n*INTF.PEIF	Refer to the "Receive Errors."	Writing 1, reading received data that encountered an error, or software reset
Overrun error	UA*n*INTF.OEIF	Refer to the "Receive Errors."	Writing 1 or software reset
Receive buffer two bytes full	UA*n*INTF.RB2FIF	When the second received data byte is loaded to the receive data buffer in which the first byte is already received	Reading received data or software reset
Receive buffer one byte full	UA*n*INTF.RB1FIF	When the first received data byte is loaded to the emptied receive data buffer	Reading data to empty the receive data buffer or software reset
Transmit buffer empty	UA*n*INTF.TBEIF	When transmit data written to the transmit data buffer is transferred to the shift register	Writing transmit data

The UART3 provides interrupt enable bits corresponding to each interrupt flag. An interrupt request is sent to the interrupt controller only when the interrupt flag, of which interrupt has been enabled by the interrupt enable bit, is set. For more information on interrupt control, refer to the "Interrupt Controller" chapter.

11.8 Control Registers

UART3 Ch.*n* Clock Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
UA*n*CLK	15–9	–	0x00	–	R	–
	8	DBRUN	0	H0	R/W	
	7–6	–	0x0	–	R	
	5–4	CLKDIV[1:0]	0x0	H0	R/W	
	3–2	–	0x0	–	R	
	1–0	CLKSRC[1:0]	0x0	H0	R/W	

Bits 15–9 Reserved

Bit 8 DBRUN

This bit sets whether the UART3 operating clock is supplied in DEBUG mode or not.

1 (R/W): Clock supplied in DEBUG mode

0 (R/W): No clock supplied in DEBUG mode

Bits 7–6 Reserved

Bits 5–4 CLKDIV[1:0]

These bits select the division ratio of the UART3 operating clock.

Bits 3–2 Reserved

Bits 1–0 CLKSRC[1:0]

These bits select the clock source of the UART3.

Table 11.8.1 Clock Source and Division Ratio Settings

UA*n*CLK.CLKDIV[1:0] bits	UA*n*CLK.CLKSRC[1:0] bits			
	0x0	0x1	0x2	0x3
	IOSC	OSC1	OSC3	EXOSC
0x3	1/8	1/1	1/8	1/1
0x2	1/4		1/4	
0x1	1/2		1/2	
0x0	1/1		1/1	

(Note) The oscillation circuits/external input that are not supported in this IC cannot be selected as the clock source.

Note: The UA*n*CLK register settings can be altered only when the UA*n*CTL.MODEN bit = 0.

UART3 Ch.*n* Mode Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
UA*n*MOD	15–13	–	0x0	–	R	–
	12	PECAR	0	H0	R/W	
	11	CAREN	0	H0	R/W	
	10	BRDIV	0	H0	R/W	
	9	INVRX	0	H0	R/W	
	8	INVTX	0	H0	R/W	
	7	–	0	–	R	
	6	PUEN	0	H0	R/W	
	5	OUTMD	0	H0	R/W	
	4	IRMD	0	H0	R/W	
	3	CHLN	0	H0	R/W	
	2	PREN	0	H0	R/W	
	1	PRMD	0	H0	R/W	
	0	STPB	0	H0	R/W	

Bits 15–13 Reserved

Bit 12 PECAR

This bit selects the carrier modulation period.

1 (R/W): Carrier modulation during H data period

0 (R/W): Carrier modulation during L data period

Bit 11 CAREN

This bit enables the carrier modulation function.

1 (R/W): Enable carrier modulation function

0 (R/W): Disable carrier modulation function

Bit 10 BRDIV

This bit sets the UART3 operating clock division ratio for generating the transfer (sampling) clock using the baud rate generator.

1 (R/W): 1/4

0 (R/W): 1/16

Bit 9 INVRX

This bit enables the USIN*n* input inverting function.

1 (R/W): Enable input inverting function

0 (R/W): Disable input inverting function

Bit 8 INVTX

This bit enables the USOUT*n* output inverting function.

1 (R/W): Enable output inverting function

0 (R/W): Disable output inverting function

Bit 7 Reserved

Bit 6 PUEN

This bit enables pull-up of the USIN*n* pin.
1 (R/W): Enable pull-up
0 (R/W): Disable pull-up

Bit 5 OUTMD

This bit sets the USOUT*n* pin output mode.
1 (R/W): Open-drain output
0 (R/W): Push-pull output

Bit 4 IRMD

This bit enables the IrDA interface function.
1 (R/W): Enable IrDA interface function
0 (R/W): Disable IrDA interface function

Bit 3 CHLN

This bit sets the data length.
1 (R/W): 8 bits
0 (R/W): 7 bits

Bit 2 PREN

This bit enables the parity function.
1 (R/W): Enable parity function
0 (R/W): Disable parity function

Bit 1 PRMD

This bit selects either odd parity or even parity when using the parity function.
1 (R/W): Odd parity
0 (R/W): Even parity

Bit 0 STPB

This bit sets the stop bit length.
1 (R/W): 2 bits
0 (R/W): 1 bit

Notes: • The UA*n*MOD register settings can be altered only when the UA*n*CTL.MODEN bit = 0.

• Do not set both the UAnMOD.IRMD and UAnMOD.CAREN bits simultaneously.

UART3 Ch.*n* Baud–Rate Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
UA*n*BR	15–12	–	0x0	–	R	–
	11–8	FMD[3:0]	0x0	H0	R/W	
	7–0	BRT[7:0]	0x00	H0	R/W	

Bits 15–12 Reserved

Bits 11–8 FMD[3:0]
Bits 7–0 BRT[7:0]

These bits set the UART3 transfer rate. For more information, refer to "Baud Rate Generator."

Notes: • The UA*n*BR register settings can be altered only when the UA*n*CTL.MODEN bit = 0.

• Do not set the UA*n*BR.FMD[3:0] bits to a value other than 0 to 3 when the UA*n*MOD.BRDIV bit = 1.

UART3 Ch.*n* Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
UA*n*CTL	15–8	–	0x00	–	R	–
	7–2	–	0x00	–	R	
	1	SFTRST	0	H0	R/W	
	0	MODEN	0	H0	R/W	

Bits 15–2 Reserved

Bit 1 SFTRST

This bit issues software reset to the UART3.

1 (W): Issue software reset
0 (W): Ineffective
1 (R): Software reset is executing.
0 (R): Software reset has finished. (During normal operation)

Setting this bit resets the UART3 transmit/receive control circuit and interrupt flags. This bit is automatically cleared after the reset processing has finished.

Bit 0 MODEN

This bit enables the UART3 operations.

1 (R/W): Enable UART3 operations (The operating clock is supplied.)
0 (R/W): Disable UART3 operations (The operating clock is stopped.)

Note: If the UA*n*CTL.MODEN bit is altered from 1 to 0 while sending/receiving data, the data being sent/received cannot be guaranteed. When setting the UA*n*CTL.MODEN bit to 1 again after that, be sure to write 1 to the UA*n*CTL.SFTRST bit as well.

UART3 Ch.*n* Transmit Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
UA*n*TXD	15–8	–	0x00	–	R	–
	7–0	TXD[7:0]	0x00	H0	R/W	

Bits 15–8 Reserved

Bits 7–0 TXD[7:0]

Data can be written to the transmit data buffer through these bits. Make sure the UA*n*INTF.TBEIF bit is set to 1 before writing data.

UART3 Ch.*n* Receive Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
UA*n*RXD	15–8	–	0x00	–	R	–
	7–0	RXD[7:0]	0x00	H0	R	

Bits 15–8 Reserved

Bits 7–0 RXD[7:0]

The receive data buffer can be read through these bits. The receive data buffer consists of a 2-byte FIFO, and older received data is read first.

UART3 Ch.*n* Status and Interrupt Flag Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
UA*n*INTF	15–10	–	0x00	–	R	–
	9	RBSY	0	H0/S0	R	
	8	TBSY	0	H0/S0	R	
	7	–	0	–	R	
	6	TENDIF	0	H0/S0	R/W	Cleared by writing 1.
	5	FEIF	0	H0/S0	R/W	Cleared by writing 1 or reading the UA*n*RXD register.
	4	PEIF	0	H0/S0	R/W	
	3	OEIF	0	H0/S0	R/W	Cleared by writing 1.
	2	RB2FIF	0	H0/S0	R	Cleared by reading the UA*n*RXD register.
	1	RB1FIF	0	H0/S0	R	
	0	TBEIF	1	H0/S0	R	Cleared by writing to the UA*n*TXD register.

Bits 15–10 Reserved

Bit 9 RBSY

This bit indicates the receiving status. (See Figure 11.5.3.1.)

1 (R): During receiving

0 (R): Idle

Bit 8 TBSY

This bit indicates the sending status. (See Figure 11.5.2.1.)

1 (R): During sending

0 (R): Idle

Bit 7 Reserved

Bit 6 TENDIF

Bit 5 FEIF

Bit 4 PEIF

Bit 3 OEIF

Bit 2 RB2FIF

Bit 1 RB1FIF

Bit 0 TBEIF

These bits indicate the UART3 interrupt cause occurrence status.

1 (R): Cause of interrupt occurred

0 (R): No cause of interrupt occurred

1 (W): Clear flag

0 (W): Ineffective

The following shows the correspondence between the bit and interrupt:

UA*n*INTF.TENDIF bit: End-of-transmission interrupt

UA*n*INTF.FEIF bit: Framing error interrupt

UA*n*INTF.PEIF bit: Parity error interrupt

UA*n*INTF.OEIF bit: Overrun error interrupt

UA*n*INTF.RB2FIF bit: Receive buffer two bytes full interrupt

UA*n*INTF.RB1FIF bit: Receive buffer one byte full interrupt

UA*n*INTF.TBEIF bit: Transmit buffer empty interrupt

UART3 Ch.*n* Interrupt Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
UA*n*INTE	15–8	–	0x00	–	R	–
	7	–	0	–	R	
	6	TENDIE	0	H0	R/W	
	5	FEIE	0	H0	R/W	
	4	PEIE	0	H0	R/W	
	3	OEIE	0	H0	R/W	
	2	RB2FIE	0	H0	R/W	
	1	RB1FIE	0	H0	R/W	
	0	TBEIE	0	H0	R/W	

Bits 15–7 Reserved

Bit 6 TENDIE
Bit 5 FEIE
Bit 4 PEIE
Bit 3 OEIE
Bit 2 RB2FIE
Bit 1 RB1FIE
Bit 0 TBEIE

These bits enable UART3 interrupts.
1 (R/W): Enable interrupts
0 (R/W): Disable interrupts

The following shows the correspondence between the bit and interrupt:
UA*n*INTE.TENDIE bit: End-of-transmission interrupt
UA*n*INTE.FEIE bit: Framing error interrupt
UA*n*INTE.PEIE bit: Parity error interrupt
UA*n*INTE.OEIE bit: Overrun error interrupt
UA*n*INTE.RB2FIE bit: Receive buffer two bytes full interrupt
UA*n*INTE.RB1FIE bit: Receive buffer one byte full interrupt
UA*n*INTE.TBEIE bit: Transmit buffer empty interrupt

UART3 Ch.*n* Carrier Waveform Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
UA*n*CAWF	15–8	–	0x00	–	R	–
	7–0	CRPER[7:0]	0x00	H0	R/W	

Bits 15–8 Reserved

Bits 7–0 CRPER[7:0]

These bits set the carrier modulation output frequency. For more information, refer to "Carrier Modulation."

12 Synchronous Serial Interface (SPIA)

12.1 Overview

SPIA is a synchronous serial interface. The features of SPIA are listed below.

- Supports both master and slave modes.
- Data length: 2 to 16 bits programmable
- Either MSB first or LSB first can be selected for the data format.
- Clock phase and polarity are configurable.
- Supports full-duplex communications.
- Includes separated transmit data buffer and receive data buffer registers.
- Can generate receive buffer full, transmit buffer empty, end of transmission, and overrun interrupts.
- Master mode allows use of a 16-bit timer to set baud rate.
- Slave mode is capable of being operated with the external input clock SPICLK*n* only.
- Slave mode is capable of being operated in SLEEP mode allowing wake-up by an SPIA interrupt.
- Input pins can be pulled up/down with an internal resistor.

Figure 12.1.1 shows the SPIA configuration.

Table 12.1.1 SPIA Channel Configuration of S1C17F63

Item	S1C17F63
Number of channels	2 channels (Ch.0 and Ch.1)
Internal clock input	Ch.0 ← 16-bit timer Ch.1 Ch.1 ← 16-bit timer Ch.3

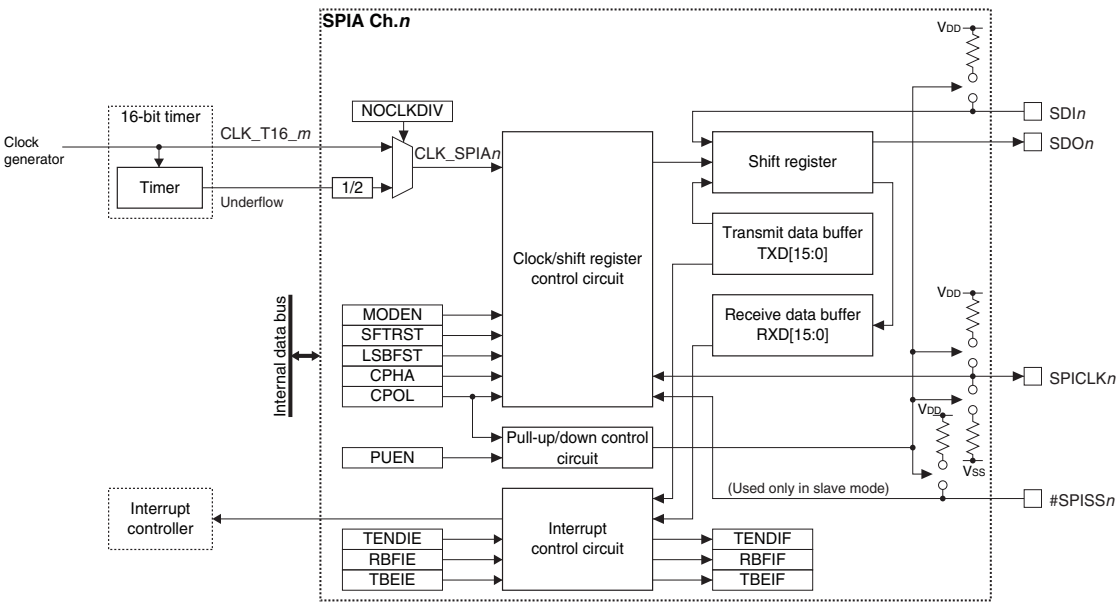


Figure 12.1.1 SPIA Configuration

12.2 Input/Output Pins and External Connections

12.2.1 List of Input/Output Pins

Table 12.2.1.1 lists the SPIA pins.

Table 12.2.1.1 List of SPIA Pins

Pin name	I/O*	Initial status*	Function
SDI*n*	I	I (Hi-Z)	SPIA Ch.*n* data input pin
SDO*n*	O or Hi-Z	Hi-Z	SPIA Ch.*n* data output pin
SPICLK*n*	I or O	I (Hi-Z)	SPIA Ch.*n* external clock input/output pin
#SPISS*n*	I	I (Hi-Z)	SPIA Ch.*n* slave select signal input pin

* Indicates the status when the pin is configured for SPIA.

If the port is shared with the SPIA pin and other functions, the SPIA input/output function must be assigned to the port before activating SPIA. For more information, refer to the "I/O Ports" chapter.

12.2.2 External Connections

SPIA operates in master mode or slave mode. Figures 12.2.2.1 and 12.2.2.2 show connection diagrams between SPIA in each mode and external SPI devices.

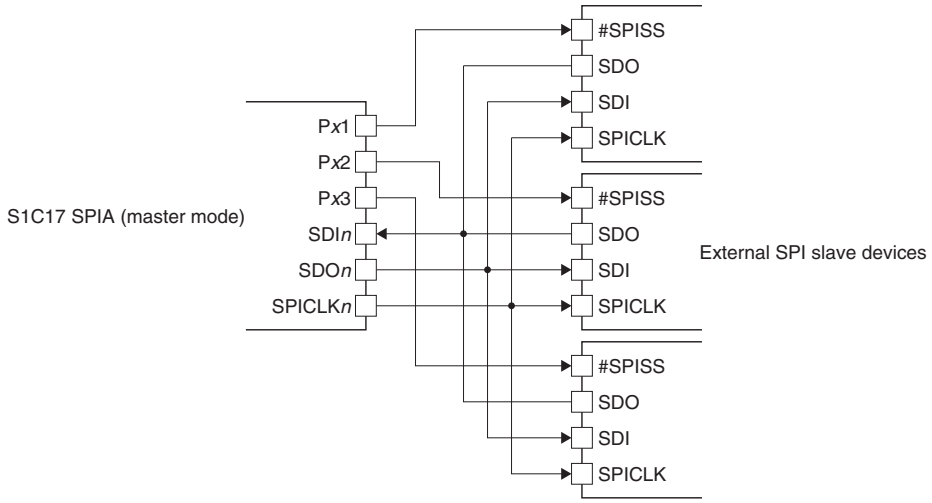


Figure 12.2.2.1 Connections between SPIA in Master Mode and External SPI Slave Devices

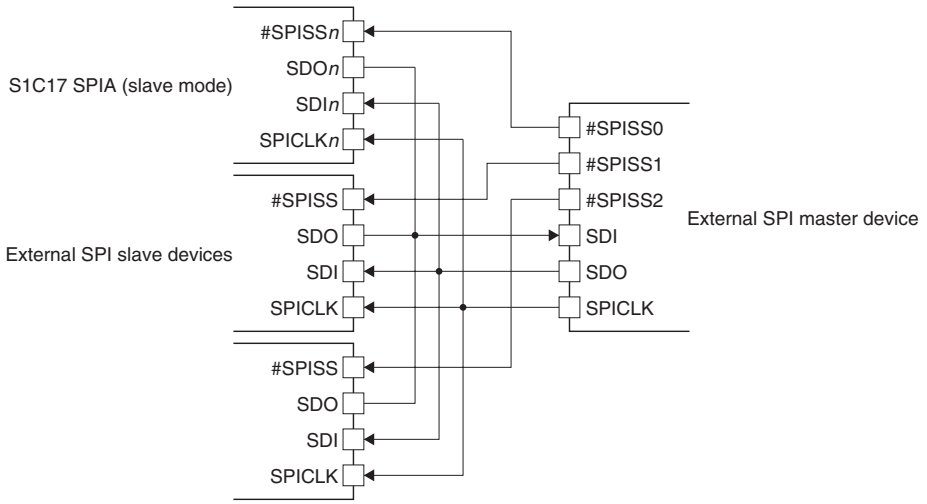


Figure 12.2.2.2 Connections between SPIA in Slave Mode and External SPI Master Device

12.2.3 Pin Functions in Master Mode and Slave Mode

The pin functions are changed according to the master or slave mode selection. The differences in pin functions between the modes are shown in Table 12.2.3.1.

Table 12.2.3.1 Pin Function Differences between Modes

Pin	Function in master mode	Function in slave mode
SDI*n*	Always placed into input state.	
SDO*n*	Always placed into output state.	This pin is placed into output state while a low level is applied to the #SPISS*n* pin or placed into Hi-Z state while a high level is applied to the #SPISS*n* pin.
SPICLK*n*	Outputs the SPI clock to external devices. Output clock polarity and phase can be configured if necessary.	Inputs an external SPI clock. Clock polarity and phase can be designated according to the input clock.
#SPISS*n*	Not used. This input function is not required to be assigned to the port. To output the slave select signal in master mode, use a general-purpose I/O port function.	Applying a low level to the #SPISS*n* pin enables SPIA to transmit/receive data. While a high level is applied to this pin, SPIA is not selected as a slave device. Data input to the SDI*n* pin and the clock input to the SPICLK*n* pin are ignored. When a high level is applied, the transmit/receive bit count is cleared to 0 and the already received bits are discarded.

12.2.4 Input Pin Pull-Up/Pull-Down Function

The SPIA input pins (SDI*n* in master mode or SDI*n*, SPICLK*n*, and #SPISS*n* pins in slave mode) have a pull-up or pull-down function as shown in Table 12.2.4.1. This function is enabled by setting the SPI*n*MOD.PUEN bit to 1.

Table 12.2.4.1 Pull-Up or Pull-Down of Input Pins

Pin	Master mode	Slave mode
SDI*n*	Pull-up	Pull-up
SPICLK*n*	–	SPI*n*MOD.CPOL bit = 1: Pull-up SPI*n*MOD.CPOL bit = 0: Pull-down
#SPISS*n*	–	Pull-up

12.3 Clock Settings

12.3.1 SPIA Operating Clock

Operating clock in master mode

In master mode, the SPIA operating clock is supplied from the 16-bit timer. The following two options are provided for the clock configuration.

Use the 16-bit timer operating clock without dividing

By setting the SPI*n*MOD.NOCLKDIV bit to 1, the operating clock CLK_T16_*m*, which is configured by selecting a clock source and a division ratio, for the 16-bit timer channel corresponding to the SPIA channel is input to SPIA as CLK_SPIA*n*. Since this clock is also used as the SPI clock SPICLK*n* without changing, the CLK_SPIA*n* frequency becomes the baud rate.

To supply CLK_SPIA*n* to SPIA, the 16-bit timer clock source must be enabled in the clock generator. It does not matter how the T16_*m*CTL.MODEN and T16_*m*CTL.PRUN bits of the corresponding 16-bit timer channel are set (1 or 0).

When setting this mode, the timer function of the corresponding 16-bit timer channel may be used for another purpose.

Use the 16-bit timer as a baud rate generator

By setting the SPI*n*MOD.NOCLKDIV bit to 0, SPIA inputs the underflow signal generated by the corresponding 16-bit timer channel and converts it to the SPICLK*n*. The 16-bit timer must be run with an appropriate reload data set. The SPICLK*n* frequency (baud rate) and the 16-bit timer reload data are calculated by the equations shown below.

$$f_{SPICLK} = \frac{f_{CLK\_SPIA}}{2 \times (RLD + 1)} \qquad RLD = \frac{f_{CLK\_SPIA}}{f_{SPICLK} \times 2} - 1 \qquad \text{(Eq. 12.1)}$$

Where

f_{SPICLK}: SPICLK*n* frequency [Hz] (= baud rate [bps])
f_{CLK_SPIA}: SPIA operating clock frequency [Hz]
RLD: 16-bit timer reload data value

For controlling the 16-bit timer, refer to the "16-bit Timers" chapter.

Operating clock in slave mode

SPIA set in slave mode operates with the clock supplied from the external SPI master to the SPICLK*n* pin. The 16-bit timer channel (including the clock source selector and the divider) corresponding to the SPIA channel is not used. Furthermore, the SPI*n*MOD.NOCLKDIV bit setting becomes ineffective.

SPIA keeps operating using the clock supplied from the external SPI master even if all the internal clocks halt during SLEEP mode, so SPIA can receive data and can generate receive buffer full interrupts.

12.3.2 Clock Supply in DEBUG Mode

In master mode, the operating clock supply during DEBUG mode should be controlled using the T16_*m*CLK.DBRUN bit.

The CLK_T16_*m* supply to SPIA Ch.*n* is suspended when the CPU enters DEBUG mode if the T16_*m*CLK.DBRUN bit = 0. After the CPU returns to normal mode, the CLK_T16_*m* supply resumes. Although SPIA Ch.*n* stops operating when the CLK_T16_*m* supply is suspended, the output pins and registers retain the status before DEBUG mode was entered. If the T16_*m*CLK.DBRUN bit = 1, the CLK_T16_*m* supply is not suspended and SPIA Ch.*n* will keep operating in DEBUG mode.

SPIA in slave mode operates with the external SPI master clock input from the SPICLK*n* pin regardless of whether the CPU is placed into DEBUG mode or normal mode.

12.3.3 SPI Clock (SPICLK*n*) Phase and Polarity

The SPICLK*n* phase and polarity can be configured separately using the SPI*n*MOD.CPHA bit and the SPI*n*MOD.CPOL bit, respectively. Figure 12.3.3.1 shows the clock waveform and data input/output timing in each setting.

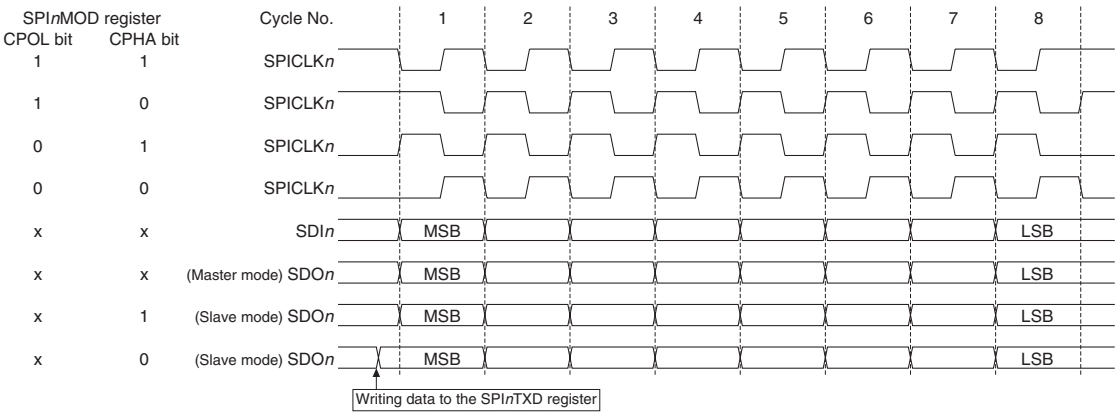


Figure 12.3.3.1 SPI Clock Phase and Polarity (SPI*n*MOD.LSBFST bit = 0, SPI*n*MOD.CHLN[3:0] bits = 0x7)

12.4 Data Format

The SPIA data length can be selected from 2 bits to 16 bits by setting the SPI*n*MOD.CHLN[3:0] bits. The input/output permutation is configurable to MSB first or LSB first using the SPI*n*MOD.LSBFST bit. Figure 12.4.1 shows a data format example when the SPI*n*MOD.CHLN[3:0] bits = 0x7, the SPI*n*MOD.CPOL bit = 0 and the SPI*n*MOD.CPHA bit = 0.

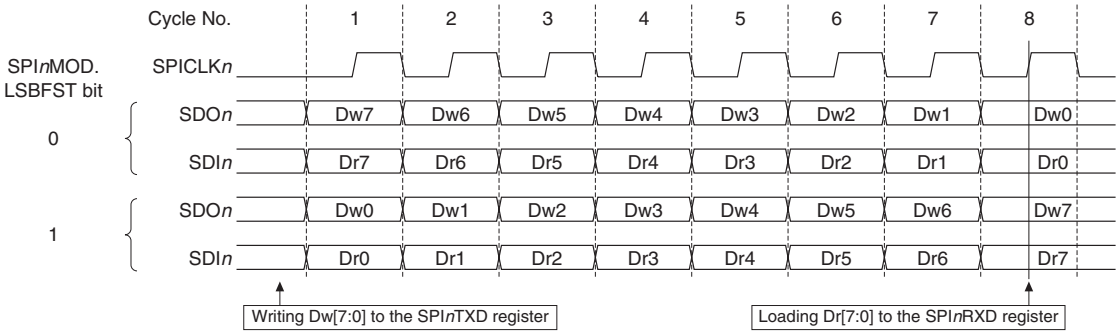


Figure 12.4.1 Data Format Selection Using the SPI*n*MOD.LSBFST Bit
(SPI*n*MOD.CHLN[3:0] bits = 0x7, SPI*n*MOD.CPOL bit = 0, SPI*n*MOD.CPHA bit = 0)

12.5 Operations

12.5.1 Initialization

SPIA Ch.*n* should be initialized with the procedure shown below.

1. <Master mode only> Generate a clock by controlling the 16-bit timer and supply it to SPIA Ch.*n*.
2. Configure the following SPI*n*MOD register bits:
   - SPI*n*MOD.PUEN bit (Enable input pin pull-up/down)
   - SPI*n*MOD.NOCLKDIV bit (Select master mode operating clock)
   - SPI*n*MOD.LSBFST bit (Select MSB first/LSB first)
   - SPI*n*MOD.CPHA bit (Select clock phase)
   - SPI*n*MOD.CPOL bit (Select clock polarity)
   - SPI*n*MOD.MST bit (Select master/slave mode)
3. Assign the SPIA Ch.*n* input/output function to the ports. (Refer to the "I/O Ports" chapter.)
4. Set the following SPI*n*CTL register bits:
   - Set the SPI*n*CTL.SFTRST bit to 1. (Execute software reset)
   - Set the SPI*n*CTL.MODEN bit to 1. (Enable SPIA Ch.*n* operations)
5. Set the following bits when using the interrupt:
   - Write 1 to the interrupt flags in the SPI*n*INTF register. (Clear interrupt flags)
   - Set the interrupt enable bits in the SPI*n*INTE register to 1. * (Enable interrupts)

   * The initial value of the SPI*n*INTF.TBEIF bit is 1, therefore, an interrupt will occur immediately after the SPI*n*INTE.TBEIE bit is set to 1.

12.5.2 Data Transmission in Master Mode

A data sending procedure and operations in master mode are shown below. Figures 12.5.2.1 and 12.5.2.2 show a timing chart and a flowchart, respectively.

Data sending procedure

1. Assert the slave select signal by controlling the general-purpose output port (if necessary).
2. Check to see if the SPI*n*INTF.TBEIF bit is set to 1 (transmit buffer empty).
3. Write transmit data to the SPI*n*TXD register.

4. Wait for an SPIA interrupt when using the interrupt.
5. Repeat Steps 2 to 4 (or 2 and 3) until the end of transmit data.
6. Negate the slave select signal by controlling the general-purpose output port (if necessary).

Data sending operations

SPIA Ch.*n* starts data sending operations when transmit data is written to the SPI*n*TXD register.
The transmit data in the SPI*n*TXD register is automatically transferred to the shift register and the SPI*n*INTF.TBEIF bit is set to 1. If the SPI*n*INTE.TBEIE bit = 1 (transmit buffer empty interrupt enabled), a transmit buffer empty interrupt occurs at the same time.
The SPICLK*n* pin outputs clocks of the number of the bits specified by the SPI*n*MOD.CHLN[3:0] bits and the transmit data bits are output in sequence from the SDO*n* pin in sync with these clocks.

Even if the clock is being output from the SPICLK*n* pin, the next transmit data can be written to the SPI*n*TXD register after making sure the SPI*n*INTF.TBEIF bit is set to 1.

If transmit data has not been written to the SPI*n*TXD register after the last clock is output from the SPICLK*n* pin, the clock output halts and the SPI*n*INTF.TENDIF bit is set to 1. At the same time SPIA issues an end-of-transmission interrupt request if the SPI*n*INTE.TENDIE bit = 1.

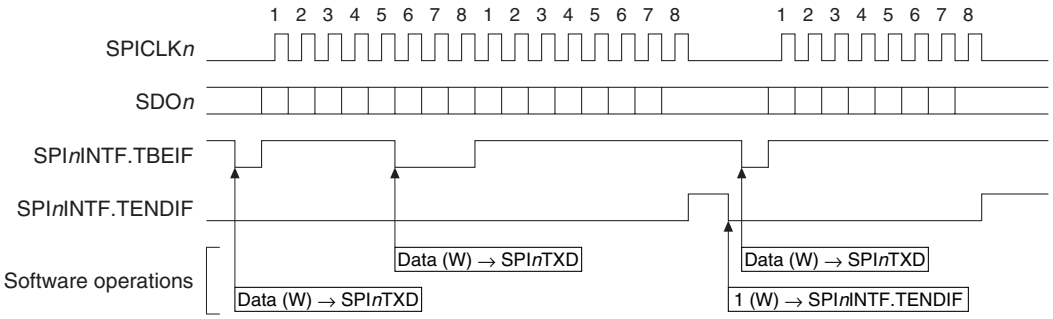


Figure 12.5.2.1 Example of Data Sending Operations in Master Mode (SPI*n*MOD.CHLN[3:0] bits = 0x7)

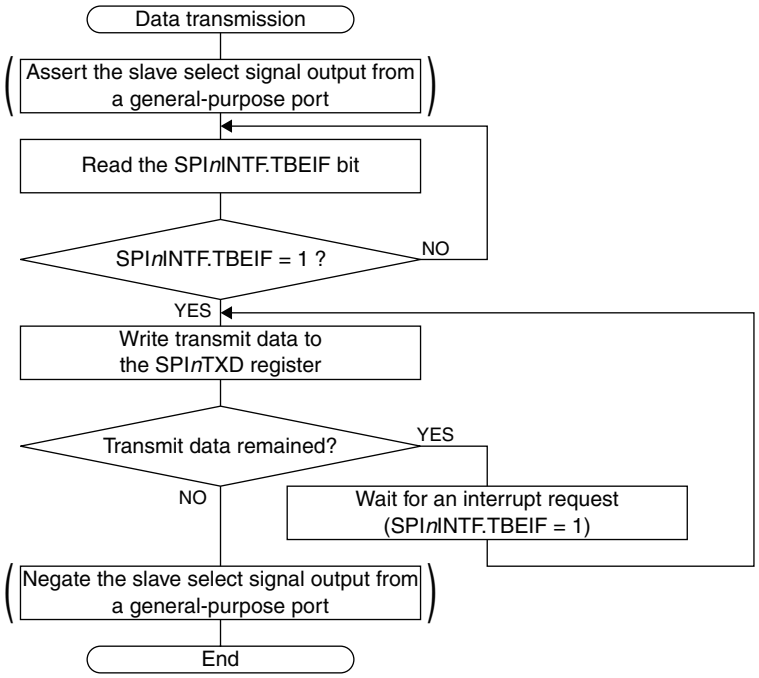


Figure 12.5.2.2 Data Transmission Flowchart in Master Mode

12.5.3 Data Reception in Master Mode

A data receiving procedure and operations in master mode are shown below. Figures 12.5.3.1 and 12.5.3.2 show a timing chart and flowcharts, respectively.

Data receiving procedure

1. Assert the slave select signal by controlling the general-purpose output port (if necessary).
2. Check to see if the SPI*n*INTF.TBEIF bit is set to 1 (transmit buffer empty).
3. Write dummy data (or transmit data) to the SPI*n*TXD register.
4. Wait for a transmit buffer empty interrupt (SPI*n*INTF.TBEIF bit = 1).
5. Write dummy data (or transmit data) to the SPI*n*TXD register.
6. Wait for a receive buffer full interrupt (SPI*n*INTF.RBFIF bit = 1).
7. Read the received data from the SPI*n*RXD register.
8. Repeat Steps 5 to 7 until the end of data reception.
9. Negate the slave select signal by controlling the general-purpose output port (if necessary).

Note: To perform continuous data reception without stopping SPICLK*n*, Steps 7 and 5 operations must be completed within the SPICLK*n* cycles equivalent to "Data bit length - 1" after Step 6.

Data receiving operations

SPIA Ch.*n* starts data receiving operations simultaneously with data sending operations when transmit data (may be dummy data if data transmission is not required) is written to the SPI*n*TXD register.
The SPICLK*n* pin outputs clocks of the number of the bits specified by the SPI*n*MOD.CHLN[3:0] bits. The transmit data bits are output in sequence from the SDO*n* pin in sync with these clocks and the receive data bits input from the SDI*n* pin are shifted into the shift register.
When the last clock is output from the SPICLK*n* pin and receive data bits are all shifted into the shift register, the received data is transferred to the receive data buffer and the SPI*n*INTF.RBFIF bit is set to 1. At the same time SPIA issues a receive buffer full interrupt request if the SPI*n*INTE.RBFIE bit = 1. After that, the received data in the receive data buffer can be read through the SPI*n*RXD register.

Note: If data of the number of the bits specified by the SPI*n*MOD.CHLN[3:0] bits is received when the SPI*n*INTF.RBFIF bit is set to 1, the SPI*n*RXD register is overwritten with the newly received data and the previously received data is lost. In this case, the SPI*n*INTF.OEIF bit is set.

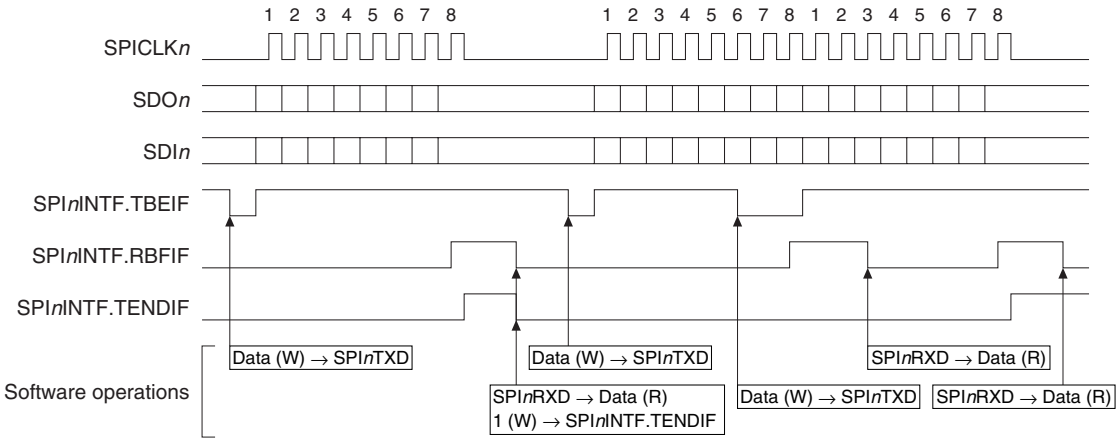


Figure 12.5.3.1 Example of Data Receiving Operations in Master Mode (SPI*n*MOD.CHLN[3:0] bits = 0x7)

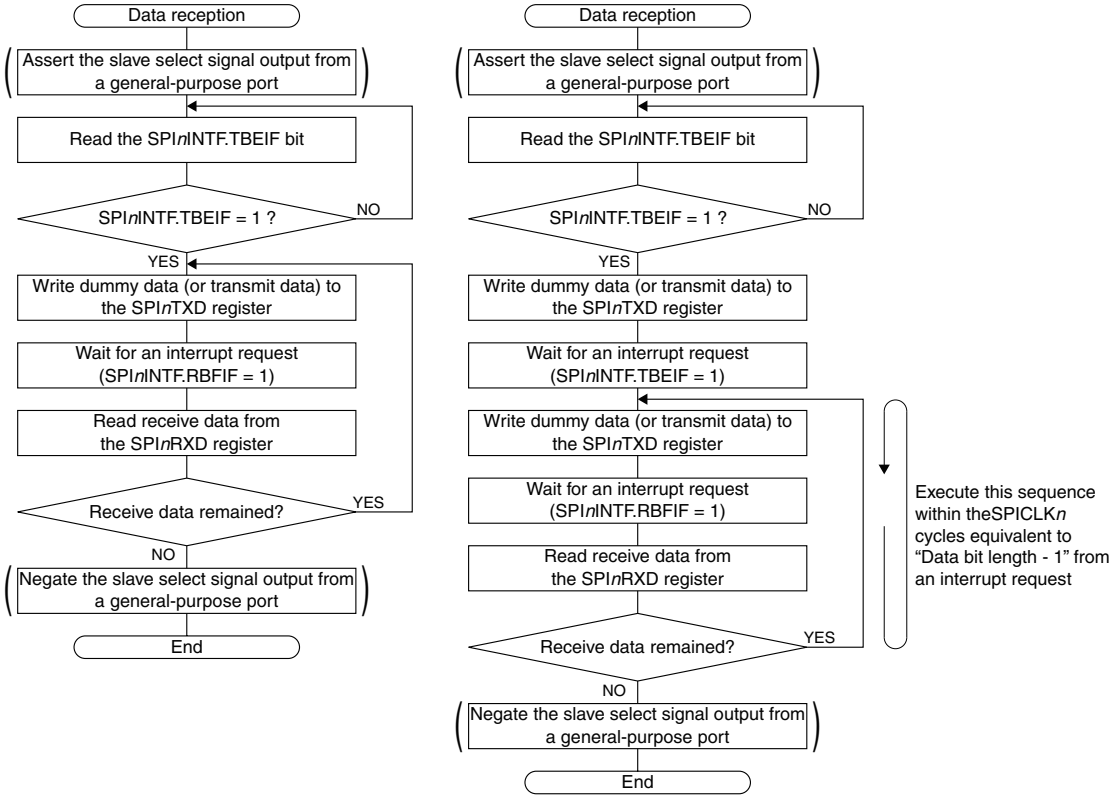


Figure 12.5.3.2 Data Reception Flowcharts in Master Mode

12.5.4 Terminating Data Transfer in Master Mode

A procedure to terminate data transfer in master mode is shown below.

1. Wait for an end-of-transmission interrupt (SPI*n*INTF.TENDIF bit = 1).
2. Set the SPI*n*CTL.MODEN bit to 0 to disable the SPIA Ch.*n* operations.
3. Stop the 16-bit timer to disable the clock supply to SPIA Ch.*n*.

12.5.5 Data Transfer in Slave Mode

A data sending/receiving procedure and operations in slave mode are shown below. Figures 12.5.5.1 and 12.5.5.2 show a timing chart and flowcharts, respectively.

Data sending procedure

1. Check to see if the SPI*n*INTF.TBEIF bit is set to 1 (transmit buffer empty).
2. Write transmit data to the SPI*n*TXD register.
3. Wait for a transmit buffer empty interrupt (SPI*n*INTF.TBEIF bit = 1).
4. Repeat Steps 2 and 3 until the end of transmit data.

Note: Transmit data must be written to the SPI*n*TXD register after the SPI*n*INTF.TBEIF bit is set to 1 by the time the sending SPI*n*TXD register data written is completed. If no transmit data is written during this period, the data bits input from the SDI*n* pin are shifted and output from the SDO*n* pin without being modified.

Data receiving procedure

1. Wait for a receive buffer full interrupt (SPI*n*INTF.RBFIF bit = 1).
2. Read the received data from the SPI*n*RXD register.
3. Repeat Steps 1 and 2 until the end of data reception.

Data transfer operations

The following shows the slave mode operations different from master mode:

- Slave mode operates with the SPI clock supplied from the external SPI master to the SPICLK*n* pin.
  The data transfer rate is determined by the SPICLK*n* frequency. It is not necessary to control the 16-bit timer.
- SPIA can operate as a slave device only when the slave select signal input from the external SPI master to the #SPISS*n* pin is set to the active (low) level.
  If #SPISS*n* = high, the software transfer control, the SPICLK*n* pin input, and the SDI*n* pin input are all ineffective. If the #SPISS*n* signal goes high during data transfer, the transfer bit counter is cleared and data in the shift register is discarded.
- Slave mode starts data transfer when SPICLK*n* is input from the external SPI master after the #SPISS*n* signal is asserted. Writing transmit data is not a trigger to start data transfer. Therefore, it is not necessary to write dummy data to the transmit data buffer when performing data reception only.
- Data transmission/reception can be performed even in SLEEP mode, it makes it possible to wake the CPU up using an SPIA interrupt.

Other operations are the same as master mode.

Notes: • If data of the number of bits specified by the SPI*n*MOD.CHLN[3:0] bits is received when the SPI*n*INTF.RBFIF bit is set to 1, the SPI*n*RXD register is overwritten with the newly received data and the previously received data is lost. In this case, the SPI*n*INTF.OEIF bit is set.

• When the clock for the first bit is input from the SPICLK*n* pin, SPIA starts sending the data currently stored in the shift register even if the SPI*n*INTF.TBEIF bit is set to 1.

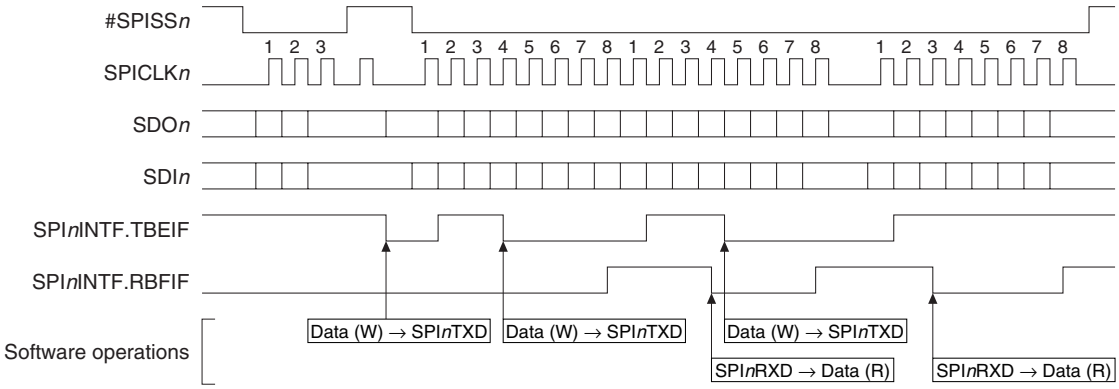


Figure 12.5.5.1 Example of Data Transfer Operations in Slave Mode (SPI*n*MOD.CHLN[3:0] bits = 0x7)

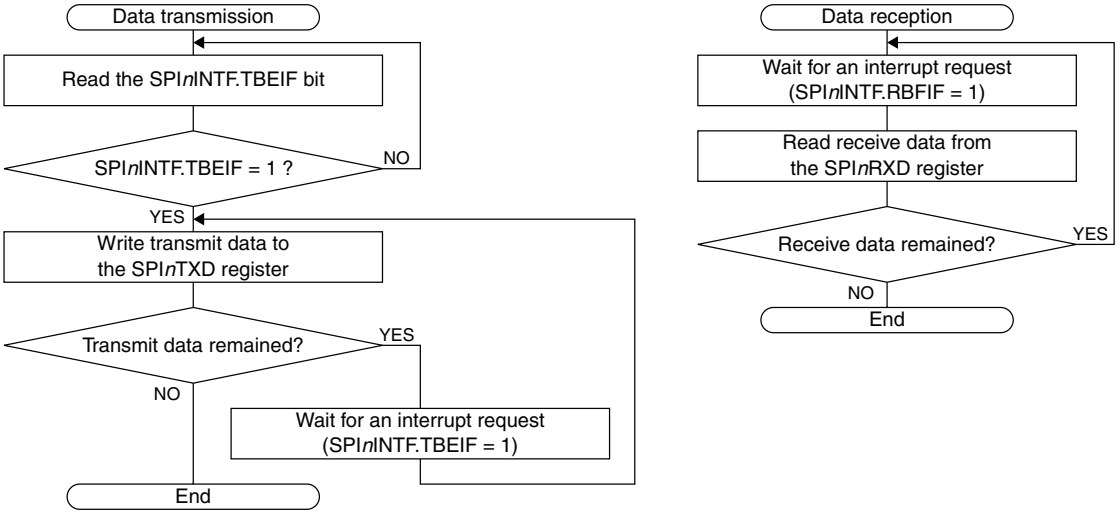


Figure 12.5.5.2 Data Transfer Flowcharts in Slave Mode

12.5.6 Terminating Data Transfer in Slave Mode

A procedure to terminate data transfer in slave mode is shown below.

1. Wait for an end-of-transmission interrupt (SPI*n*INTF.TENDIF bit = 1). Or determine end of transfer via the received data.
2. Set the SPI*n*CTL.MODEN bit to 0 to disable the SPIA Ch.*n* operations.

12.6 Interrupts

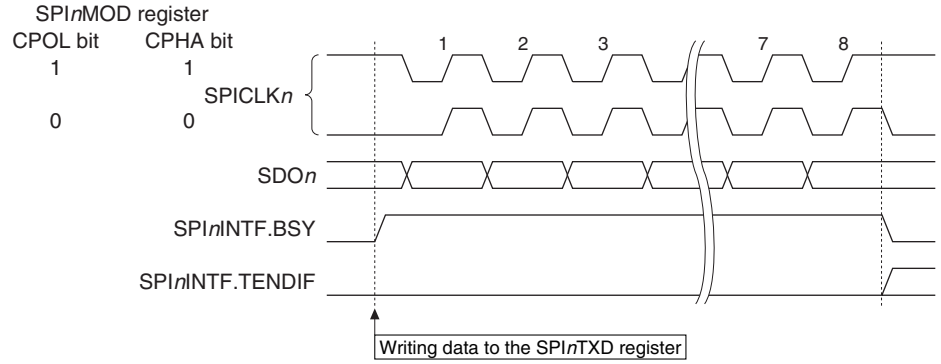
SPIA has a function to generate the interrupts shown in Table 12.6.1.

Table 12.6.1 SPIA Interrupt Function

Interrupt	Interrupt flag	Set condition	Clear condition
End of transmission	SPI*n*INTF.TENDIF	When the SPI*n*INTF.TBEIF bit = 1 after data of the specified bit length (defined by the SPI*n*MOD.CHLN[3:0] bits) has been sent	Writing 1
Receive buffer full	SPI*n*INTF.RBFIF	When data of the specified bit length is received and the received data is transferred from the shift register to the received data buffer	Reading the SPI*n*RXD register
Transmit buffer empty	SPI*n*INTF.TBEIF	When transmit data written to the transmit data buffer is transferred to the shift register	Writing to the SPI*n*TXD register
Overrun error	SPI*n*INTF.OEIF	When the receive data buffer is full (when the received data has not been read) at the point that receiving data to the shift register has completed	Writing 1

SPIA provides interrupt enable bits corresponding to each interrupt flag. An interrupt request is sent to the interrupt controller only when the interrupt flag, of which interrupt has been enabled by the interrupt enable bit, is set. For more information on interrupt control, refer to the "Interrupt Controller" chapter.
The SPI*n*INTF register also contains the BSY bit that indicates the SPIA operating status.
Figure 12.6.1 shows the SPI*n*INTF.BSY and SPI*n*INTF.TENDIF bit set timings.

Master mode



Slave mode

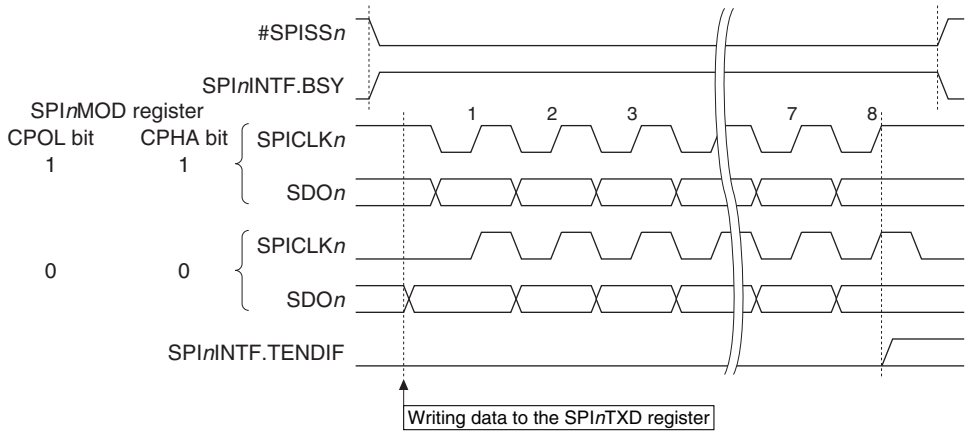


Figure 12.6.1 SPI*n*INTF.BSY and SPI*n*INTF.TENDIF Bit Set Timings (when SPI*n*MOD.CHLN[3:0] bits = 0x7)

12.7 Control Registers

SPIA Ch.*n* Mode Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SPI*n*MOD	15–12	–	0x0	–	R	–
	11–8	CHLN[3:0]	0x7	H0	R/W	
	7–6	–	0x0	–	R	
	5	PUEN	0	H0	R/W	
	4	NOCLKDIV	0	H0	R/W	
	3	LSBFST	0	H0	R/W	
	2	CPHA	0	H0	R/W	
	1	CPOL	0	H0	R/W	
	0	MST	0	H0	R/W	

Bits 15–12 Reserved

Bits 11–8 CHLN[3:0]

These bits set the bit length of transfer data.

Table 12.7.1 Data Bit Length Settings

SPI*n*MOD.CHLN[3:0] bits	Data bit length
0xf	16 bits
0xe	15 bits
0xd	14 bits
0xc	13 bits
0xb	12 bits
0xa	11 bits
0x9	10 bits
0x8	9 bits
0x7	8 bits
0x6	7 bits
0x5	6 bits
0x4	5 bits
0x3	4 bits
0x2	3 bits
0x1	2 bits
0x0	Setting prohibited

Bits 7–6 Reserved

Bit 5 PUEN

This bit enables pull-up/down of the input pins.
1 (R/W): Enable pull-up/down
0 (R/W): Disable pull-up/down

For more information, refer to "Input Pin Pull-Up/Pull-Down Function."

Bit 4 NOCLKDIV

This bit selects SPICLK*n* in master mode. This setting is ineffective in slave mode.
1 (R/W): SPICLK*n* frequency = CLK_SPIA*n* frequency (= 16-bit timer operating clock frequency)
0 (R/W): SPICLK*n* frequency = 16-bit timer output frequency / 2

For more information, refer to "SPIA Operating Clock."

Bit 3 LSBFST

This bit configures the data format (input/output permutation).
1 (R/W): LSB first
0 (R/W): MSB first

Bit 2 CPHA
Bit 1 CPOL

These bits set the SPI clock phase and polarity. For more information, refer to "SPI Clock (SPICLK*n*) Phase and Polarity."

Bit 0 MST

This bit sets the SPIA operating mode (master mode or slave mode).
1 (R/W): Master mode
0 (R/W): Slave mode

Note: The SPI*n*MOD register settings can be altered only when the SPI*n*CTL.MODEN bit = 0.

SPIA Ch.*n* Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SPI*n*CTL	15–8	–	0x00	–	R	–
	7–2	–	0x00	–	R	
	1	SFTRST	0	H0	R/W	
	0	MODEN	0	H0	R/W	

Bits 15–2 Reserved

Bit 1 SFTRST

This bit issues software reset to SPIA.

1 (W): Issue software reset
0 (W): Ineffective
1 (R): Software reset is executing.
0 (R): Software reset has finished. (During normal operation)

Setting this bit resets the SPIA shift register and transfer bit counter. This bit is automatically cleared after the reset processing has finished.

Bit 0 MODEN

This bit enables the SPIA operations.

1 (R/W): Enable SPIA operations (In master mode, the operating clock is supplied.)
0 (R/W): Disable SPIA operations (In master mode, the operating clock is stopped.)

Note: If the SPI*n*CTL.MODEN bit is altered from 1 to 0 while sending/receiving data, the data being sent/received cannot be guaranteed. When setting the SPI*n*CTL.MODEN bit to 1 again after that, be sure to write 1 to the SPI*n*CTL.SFTRST bit as well.

SPIA Ch.*n* Transmit Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SPI*n*TXD	15–0	TXD[15:0]	0x0000	H0	R/W	–

Bits 15–0 TXD[15:0]

Data can be written to the transmit data buffer through these bits.
In master mode, writing to these bits starts data transfer.
Transmit data can be written when the SPI*n*INTF.TBEIF bit = 1 regardless of whether data is being output from the SDO*n* pin or not.
Note that the upper data bits that exceed the data bit length configured by the SPI*n*MOD.CHLN[3:0] bits will not be output from the SDO*n* pin.

Note: Be sure to avoid writing to the SPI*n*TXD register when the SPI*n*INTF.TBEIF bit = 0. Otherwise, transfer data cannot be guaranteed.

SPIA Ch.*n* Receive Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SPI*n*RXD	15–0	RXD[15:0]	0x0000	H0	R	–

Bits 15–0 RXD[15:0]

The receive data buffer can be read through these bits. Received data can be read when the SPI*n*INTF.RBFIF bit = 1 regardless of whether data is being input from the SDI*n* pin or not. Note that the upper bits that exceed the data bit length configured by the SPI*n*MOD.CHLN[3:0] bits become 0.

Note: The SPI*n*RXD.RXD[15:0] bits are cleared to 0x0000 when 1 is written to the SPI*n*CTL.MODEN bit or the SPI*n*CTL.SFTRST bit.

SPIA Ch.*n* Interrupt Flag Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SPI*n*INTF	15–8	–	0x00	–	R	–
	7	BSY	0	H0	R	
	6–4	–	0x0	–	R	
	3	OEIF	0	H0/S0	R/W	Cleared by writing 1.
	2	TENDIF	0	H0/S0	R/W	
	1	RBFIF	0	H0/S0	R	Cleared by reading the SPI*n*RXD register.
	0	TBEIF	1	H0/S0	R	Cleared by writing to the SPI*n*TXD register.

Bits 15–8 Reserved

Bit 7 BSY

This bit indicates the SPIA operating status.

1 (R): Transmit/receive busy (master mode), #SPISS*n* = Low level (slave mode)

0 (R): Idle

Bits 6–4 Reserved

Bit 3 OEIF

Bit 2 TENDIF

Bit 1 RBFIF

Bit 0 TBEIF

These bits indicate the SPIA interrupt cause occurrence status.

1 (R): Cause of interrupt occurred

0 (R): No cause of interrupt occurred

1 (W): Clear flag (OEIF, TENDIF)

0 (W): Ineffective

The following shows the correspondence between the bit and interrupt:

SPI*n*INTF.OEIF bit: Overrun error interrupt

SPI*n*INTF.TENDIF bit: End-of-transmission interrupt

SPI*n*INTF.RBFIF bit: Receive buffer full interrupt

SPI*n*INTF.TBEIF bit: Transmit buffer empty interrupt

SPIA Ch.*n* Interrupt Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SPI*n*INTE	15–8	–	0x00	–	R	–
	7–4	–	0x0	–	R	
	3	OEIE	0	H0	R/W	
	2	TENDIE	0	H0	R/W	
	1	RBFIE	0	H0	R/W	
	0	TBEIE	0	H0	R/W	

Bits 15–4 Reserved

Bit 3 OEIE

Bit 2 TENDIE

Bit 1 RBFIE

Bit 0 TBEIE

These bits enable SPIA interrupts.

1 (R/W): Enable interrupts

0 (R/W): Disable interrupts

The following shows the correspondence between the bit and interrupt:

SPI*n*INTE.OEIE bit: Overrun error interrupt

SPI*n*INTE.TENDIE bit: End-of-transmission interrupt

SPI*n*INTE.RBFIE bit: Receive buffer full interrupt

SPI*n*INTE.TBEIE bit: Transmit buffer empty interrupt

13 I²C (I2C)

13.1 Overview

The I2C is a subset of the I²C bus interface. The features of the I2C are listed below.

- Functions as an I²C bus master (single master) or a slave device.
- Supports standard mode (up to 100 kbit/s) and fast mode (up to 400 kbit/s).
- Supports 7-bit and 10-bit address modes.
- Supports clock stretching.
- Includes a baud rate generator for generating the clock in master mode.
- No clock source is required to run the I2C in slave mode, as it can run with the I²C bus signals only.
- Slave mode is capable of being operated in SLEEP mode allowing wake-up by an interrupt when an address match is detected.
- Master mode supports automatic bus clear sending function.
- Can generate receive buffer full, transmit buffer empty, and other interrupts.
- The input filter for the SDA and SCL inputs does not comply with the standard for removing noise spikes less than 50 ns.

Figure 13.1.1 shows the I2C configuration.

Table 13.1.1 I2C Channel Configuration of S1C17F63

Item	S1C17F63
Number of channels	1 channel (Ch.0)

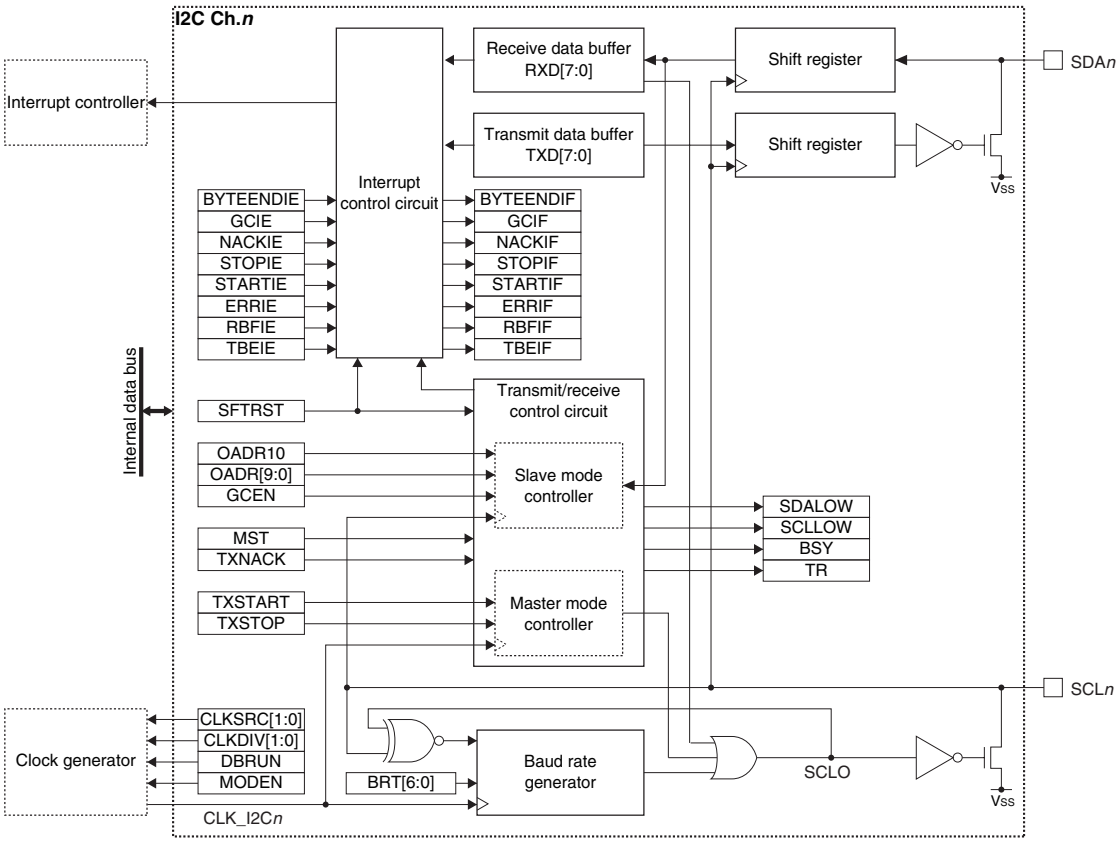


Figure 13.1.1 I2C Configuration

13.2 Input/Output Pins and External Connections

13.2.1 List of Input/Output Pins

Table 13.2.1.1 lists the I2C pins.

Table 13.2.1.1 List of I2C Pins

Pin name	I/O*	Initial status*	Function
SDA*n*	I/O	I	I2C bus serial data input/output pin
SCL*n*	I/O	I	I2C bus clock input/output pin

* Indicates the status when the pin is configured for the I2C.

If the port is shared with the I2C pin and other functions, the I2C input/output function must be assigned to the port before activating the I2C. For more information, refer to the "I/O Ports" chapter.

13.2.2 External Connections

Figure 13.2.2.1 shows a connection diagram between the I2C in this IC and external I2C devices.
The serial data (SDA) and serial clock (SCL) lines must be pulled up with an external resistor.
When the I2C is set into master mode, one or more slave devices that have a unique address may be connected to the I2C bus. When the I2C is set into slave mode, one or more master and slave devices that have a unique address may be connected to the I2C bus.

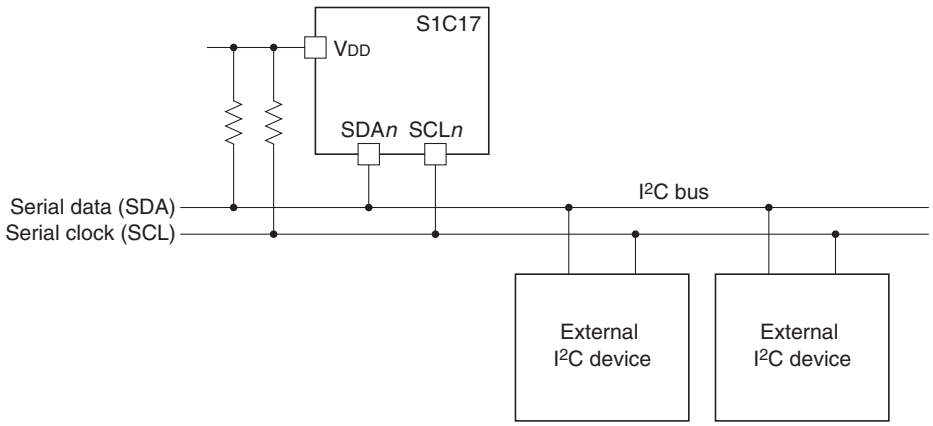


Figure 13.2.2.1 Connections between I2C and External I2C Devices

Notes: • The SDA and SCL lines must be pulled up to a VDD of this IC or lower voltage. However, if the I2C input/output ports are configured with the over voltage tolerant fail-safe type I/O, these lines can be pulled up to a voltage exceeding the VDD of this IC but within the recommended operating voltage range of this IC.

• The internal pull-up resistors for the I/O ports cannot be used for pulling up SDA and SCL.

• When the I2C is set into master mode, no other master device can be connected to the I2C bus.

13.3 Clock Settings

13.3.1 I2C Operating Clock

Master mode operating clock

When using the I2C Ch.*n* in master mode, the I2C Ch.*n* operating clock CLK_I2C*n* must be supplied to the I2C Ch.*n* from the clock generator. The CLK_I2C*n* supply should be controlled as in the procedure shown below.

1. Enable the clock source in the clock generator if it is stopped (refer to "Clock Generator" in the "Power Supply, Reset, and Clocks" chapter).
2. Set the following I2C*n*CLK register bits:
   - I2C*n*CLK.CLKSRC[1:0] bits (Clock source selection)
   - I2C*n*CLK.CLKDIV[1:0] bits (Clock division ratio selection = Clock frequency setting)

   When using the I2C in master mode during SLEEP mode, the I2C Ch.*n* operating clock CLK_I2C*n* must be configured so that it will keep supplying by writing 0 to the CLGOSC.*xxxx*SLPC bit for the CLK_I2C*n* clock source.
   The I2C operating clock should be selected so that the baud rate generator will be configured easily.

Slave mode operating clock

The I2C set to slave mode uses the SCL supplied from the I²C master as its operating clock. The clock setting by the I2C*n*CLK register is ineffective.
The I2C keeps operating using the clock supplied from the external I²C master even if all the internal clocks halt during SLEEP mode, so the I2C can receive data and can generate receive buffer full interrupts.

13.3.2 Clock Supply in DEBUG Mode

In master mode, the CLK_I2C*n* supply during DEBUG mode should be controlled using the I2C*n*CLK.DBRUN bit. The CLK_I2C*n* supply to the I2C Ch.*n* is suspended when the CPU enters DEBUG mode if the I2C*n*CLK.DBRUN bit = 0. After the CPU returns to normal mode, the CLK_I2C*n* supply resumes. Although the I2C Ch.*n* stops operating when the CLK_I2C*n* supply is suspended, the output pin and registers retain the status before DEBUG mode was entered. If the I2C*n*CLK.DBRUN bit = 1, the CLK_I2C*n* supply is not suspended and the I2C Ch.*n* will keep operating in DEBUG mode.
In slave mode, the I2C Ch.*n* operates with the external I²C master clock input from the SCL*n* pin regardless of whether the CPU is placed into DEBUG mode or normal mode.

13.3.3 Baud Rate Generator

The I2C includes a baud rate generator to generate the serial clock SCL used in master mode. The I2C set to slave mode does not use the baud rate generator, as it operates with the serial clock input from the SCL*n* pin.

Setting data transfer rate (for master mode)

The transfer rate is determined by the I2C*n*BR.BRT[6:0] bit settings. Use the following equations to calculate the setting values for obtaining the desired transfer rate.

$$bps = \frac{f_{CLK\_I2Cn}}{(BRT + 3) \times 2} \qquad BRT = \frac{f_{CLK\_I2Cn}}{bps \times 2} - 3 \qquad \text{(Eq. 13.1)}$$

Where
- bps: Data transfer rate [bit/s]
- f_{CLK_I2Cn}: I2C operating clock frequency [Hz]
- BRT: I2C*n*BR.BRT[6:0] bits setting value (1 to 127)

∗ The equations above do not include SCL rising/falling time and delay time by clock stretching (see Figure 13.3.3.1).

Note: The I²C bus transfer rate is limited to 100 kbit/s in standard mode or 400 kbit/s in fast mode. Do not set a transfer rate exceeding the limit.

Baud rate generator clock output and operations for supporting clock stretching

Figure 13.3.3.1 shows the clock generated by the baud rate generator and the clock waveform on the I²C bus.

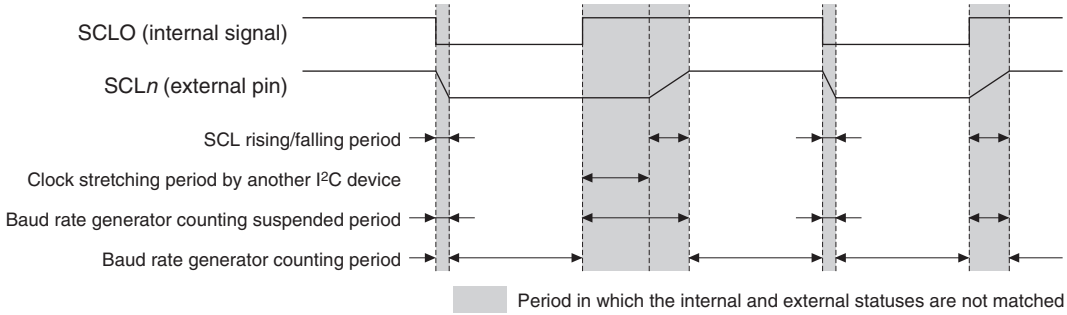


Figure 13.3.3.1 Baud Rate Generator Output Clock and SCL*n* Output Waveform

The baud rate generator output clock SCLO is compared with the SCL*n* pin status and the results are returned to the baud rate generator. If a mismatch has occurred between SCLO and SCL*n* pin levels, the baud rate generator suspends counting. This extends the clock to control data transfer during the SCL signal rising/falling period and clock stretching period in which SCL is fixed at low by a slave device.

13.4 Operations

13.4.1 Initialization

The I2C Ch.*n* should be initialized with the procedure shown below.

When using the I2C in master mode

1. Configure the operating clock and the baud rate generator using the I2C*n*CLK and I2C*n*BR registers.
2. Assign the I2C Ch.*n* input/output function to the ports. (Refer to the "I/O Ports" chapter.)
3. Set the following bits when using the interrupt:
   - Write 1 to the interrupt flags in the I2C*n*INTF register. (Clear interrupt flags)
   - Set the interrupt enable bits in the I2C*n*INTE register to 1. (Enable interrupts)
4. Set the following I2C*n*CTL register bits:
   - Set the I2C*n*CTL.MST bit to 1. (Set master mode)
   - Set the I2C*n*CTL.SFTRST bit to 1. (Execute software reset)
   - Set the I2C*n*CTL.MODEN bit to 1. (Enable I2C Ch.*n* operations)

When using the I2C in slave mode

1. Set the following I2C*n*MOD register bits:
   - I2C*n*MOD.OADR10 bit (Set 10/7-bit address mode)
   - I2C*n*MOD.GCEN bit (Enable response to general call address)
2. Set its own address to the I2C*n*OADR.OADR[9:0] (or OADR[6:0]) bits.
3. Assign the I2C Ch.*n* input/output function to the ports. (Refer to the "I/O Ports" chapter.)
4. Set the following bits when using the interrupt:
   - Write 1 to the interrupt flags in the I2C*n*INTF register. (Clear interrupt flags)
   - Set the interrupt enable bits in the I2C*n*INTE register to 1. (Enable interrupts)
5. Set the following I2C*n*CTL register bits:
   - Set the I2C*n*CTL.MST bit to 0. (Set slave mode)
   - Set the I2C*n*CTL.SFTRST bit to 1. (Execute software reset)
   - Set the I2C*n*CTL.MODEN bit to 1. (Enable I2C Ch.*n* operations)

13.4.2 Data Transmission in Master Mode

A data sending procedure in master mode and the I2C Ch.*n* operations are shown below. Figures 13.4.2.1 and 13.4.2.2 show an operation example and a flowchart, respectively.

Data sending procedure

1. Issue a START condition by setting the I2C*n*CTL.TXSTART bit to 1.
2. Wait for a transmit buffer empty interrupt (I2C*n*INTF.TBEIF bit = 1) or a START condition interrupt (I2C*n*INTF.STARTIF bit = 1).
   Clear the I2C*n*INTF.STARTIF bit by writing 1 after the interrupt has occurred.
3. Write the 7-bit slave address to the I2C*n*TXD.TXD[7:1] bits and 0 that represents WRITE as the data transfer direction to the I2C*n*TXD.TXD0 bit.
4. Wait for a transmit buffer empty interrupt (I2C*n*INTF.TBEIF bit = 1) generated when an ACK is received or a NACK reception interrupt (I2C*n*INTF.NACKIF bit = 1) generated when a NACK is received.
   i. Go to Step 5 if transmit data remains when a transmit buffer empty interrupt has occurred.
   ii. Go to Step 7 or 1 after clearing the I2C*n*INTF.NACKIF bit when a NACK reception interrupt has occurred.
5. Write transmit data to the I2C*n*TXD register.
6. Repeat Steps 4 and 5 until the end of transmit data.
7. Issue a STOP condition by setting the I2C*n*CTL.TXSTOP bit to 1.
8. Wait for a STOP condition interrupt (I2C*n*INTF.STOPIF bit = 1).
   Clear the I2C*n*INTF.STOPIF bit by writing 1 after the interrupt has occurred.

Data sending operations

Generating a START condition

The I2C Ch.*n* starts generating a START condition when the I2C*n*CTL.TXSTART bit is set to 1. When the generating operation has completed, the I2C Ch.*n* clears the I2C*n*CTL.TXSTART bit to 0 and sets both the I2C*n*INTF.STARTIF and I2C*n*INTF.TBEIF bits to 1.

Sending slave address and data

If the I2C*n*INTF.TBEIF bit = 1, a slave address or data can be written to the I2C*n*TXD register. The I2C Ch.*n* pulls down SCL to low and enters standby state until data is written to the I2C*n*TXD register. The writing operation triggers the I2C Ch.*n* to send the data to the shift register automatically and to output eight clock pulses and data bits to the I²C bus.

When the slave device returns an ACK as the response, the I2C*n*INTF.TBEIF bit is set to 1. After this interrupt occurs, the subsequent data may be sent or a STOP/repeated START condition may be issued to terminate transmission. If the slave device returns NACK, the I2C*n*INTF.NACKIF bit is set to 1 without setting the I2C*n*INTF.TBEIF bit.

Generating a STOP/repeated START condition

After the I2C*n*INTF.TBEIF bit is set to 1 (transmit buffer empty) or the I2C*n*INTF.NACKIF bit is set to 1 (NACK received), setting the I2C*n*CTL.TXSTOP bit to 1 generates a STOP condition. When the bus free time (t_{BUF} defined in the I²C Specifications) has elapsed after the STOP condition has been generated, the I2C*n*CTL.TXSTOP bit is cleared to 0 and the I2C*n*INTF.STOPIF bit is set to 1.

When setting the I2C*n*CTL.TXSTART bit to 1 while the I2C*n*INTF.TBEIF bit = 1 (transmit buffer empty) or the I2C*n*INTF.NACKIF bit = 1 (NACK received), the I2C Ch.*n* generates a repeated START condition. When the repeated START condition has been generated, the I2C*n*INTF.STARTIF and I2C*n*INTF.TBEIF bits are both set to 1 same as when a START condition has been generated.

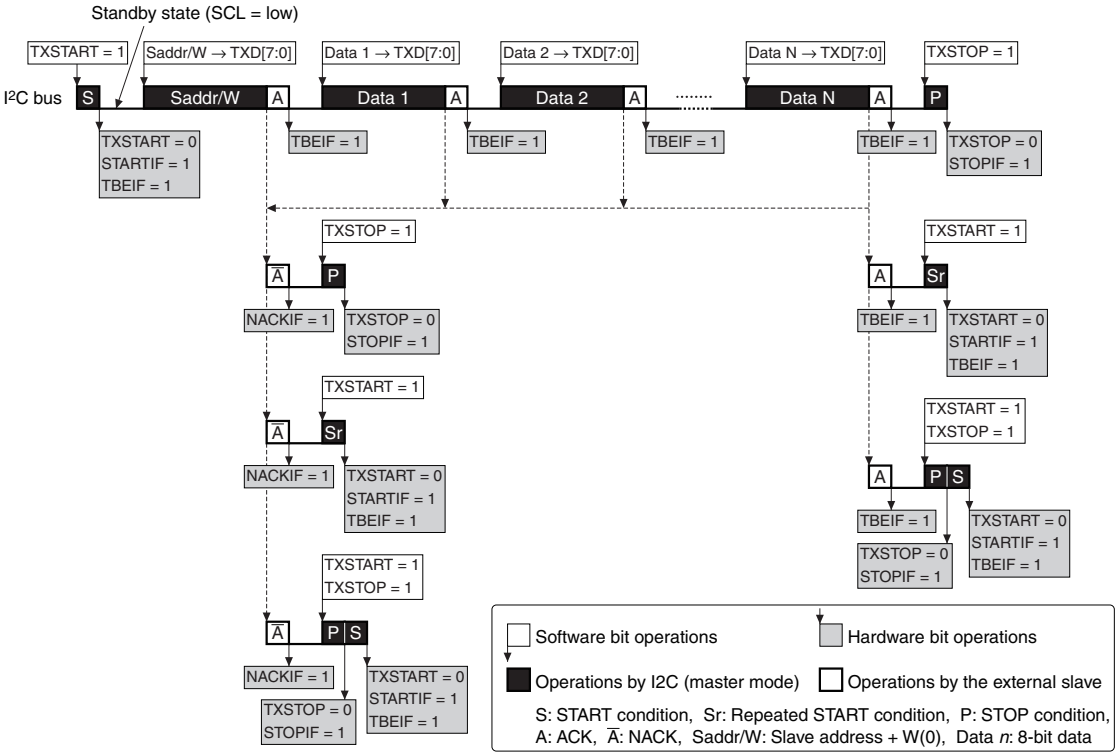


Figure 13.4.2.1 Example of Data Sending Operations in Master Mode

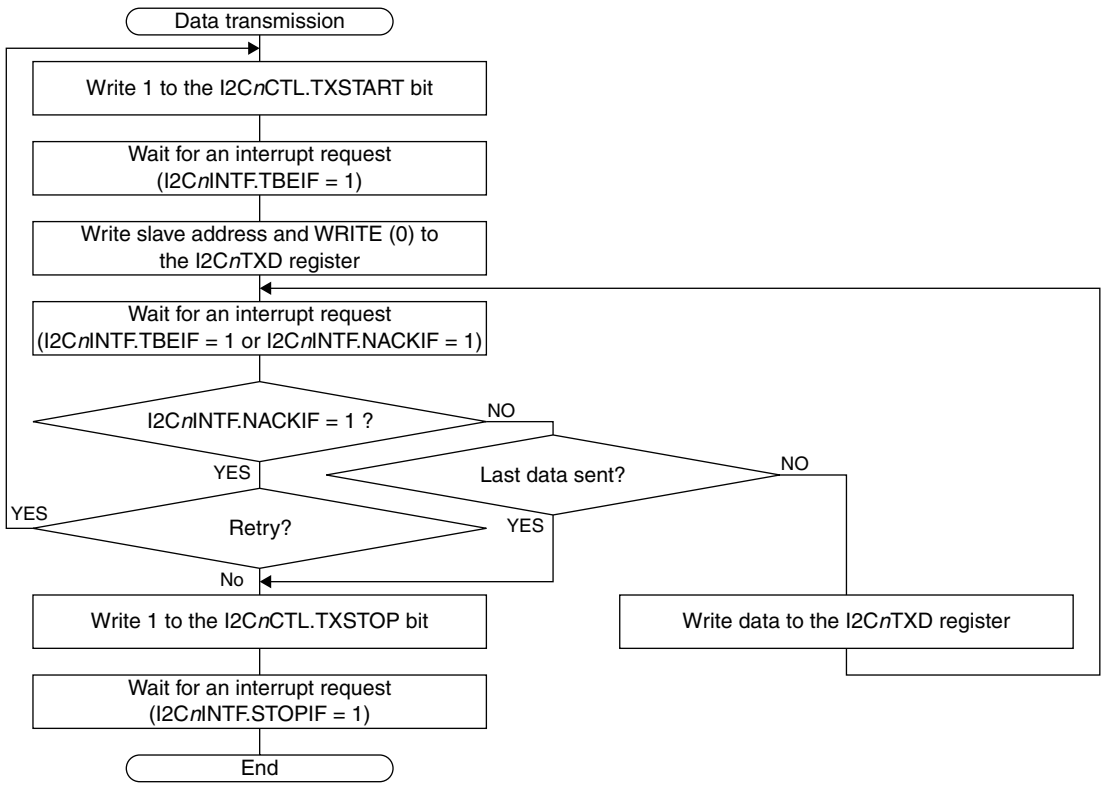


Figure 13.4.2.2 Master Mode Data Transmission Flowchart

13.4.3 Data Reception in Master Mode

A data receiving procedure in master mode and the I2C Ch.*n* operations are shown below. Figures 13.4.3.1 and 13.4.3.2 show an operation example and a flowchart, respectively.

Data receiving procedure

1. When receiving one-byte data, write 1 to the I2C*n*CTL.TXNACK bit.
2. Issue a START condition by setting the I2C*n*CTL.TXSTART bit to 1.
3. Wait for a transmit buffer empty interrupt (I2C*n*INTF.TBEIF bit = 1) or a START condition interrupt (I2C*n*INTF.STARTIF bit = 1).
   Clear the I2C*n*INTF.STARTIF bit by writing 1 after the interrupt has occurred.
4. Write the 7-bit slave address to the I2C*n*TXD.TXD[7:1] bits and 1 that represents READ as the data transfer direction to the I2C*n*TXD.TXD0 bit.
5. Wait for a receive buffer full interrupt (I2C*n*INTF.RBFIF bit = 1) generated when a one-byte reception has completed or a NACK reception interrupt (I2C*n*INTF.NACKIF bit = 1) generated when a NACK is received.
   i. Go to Step 6 when a receive buffer full interrupt has occurred.
   ii. Clear the I2C*n*INTF.NACKIF bit and issue a STOP condition by setting the I2C*n*CTL.TXSTOP bit to 1 when a NACK reception interrupt has occurred. Then go to Step 9 or Step 2 if making a retry.
6. Perform one of the operations below when the last or next-to-last data is received.
   i. When the next-to-last data is received, write 1 to the I2C*n*CTL.TXNACK bit to send a NACK after the last data is received, and then go to Step 7.
   ii. When the last data is received, read the received data from the I2C*n*RXD register and set the I2C*n*CTL.TXSTOP to 1 to generate a STOP condition. Then go to Step 9.
7. Read the received data from the I2C*n*RXD register.
8. Repeat Steps 5 to 7 until the end of data reception.
9. Wait for a STOP condition interrupt (I2C*n*INTF.STOPIF bit = 1).
   Clear the I2C*n*INTF.STOPIF bit by writing 1 after the interrupt has occurred.

Data receiving operations

Generating a START condition

It is the same as the data transmission in master mode.

Sending slave address

It is the same as the data transmission in master mode. Note, however, that the I2C*n*TXD.TXD0 bit must be set to 1 that represents READ as the data transfer direction to issue a request to the slave to send data.

Receiving data

After the slave address has been sent, the slave device sends an ACK and the first data. The I2C Ch.*n* sets the I2C*n*INTF.RBFIF bit to 1 after the data reception has completed. Furthermore, the I2C Ch.*n* returns an ACK. To return a NACK, such as for a response after the last data has been received, write 1 to the I2C*n*CTL.TXNACK bit before the I2C*n*INTF.RBFIF bit is set to 1.

The received data can be read out from the I2C*n*RXD register after a receive buffer full interrupt has occurred. The I2C Ch.*n* pulls down SCL to low and enters standby state until data is read out from the I2C*n*RXD register.

This reading triggers the I2C Ch.*n* to start subsequent data reception.

Generating a STOP or repeated START condition

It is the same as the data transmission in master mode.

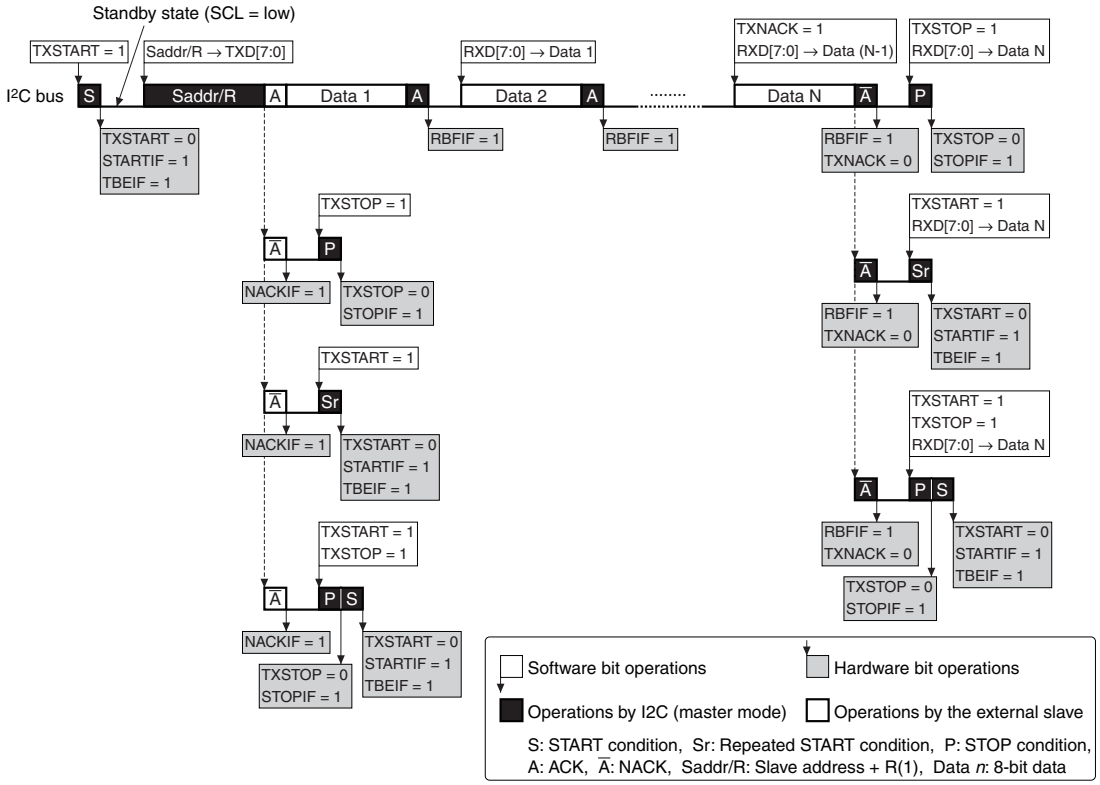


Figure 13.4.3.1 Example of Data Receiving Operations in Master Mode

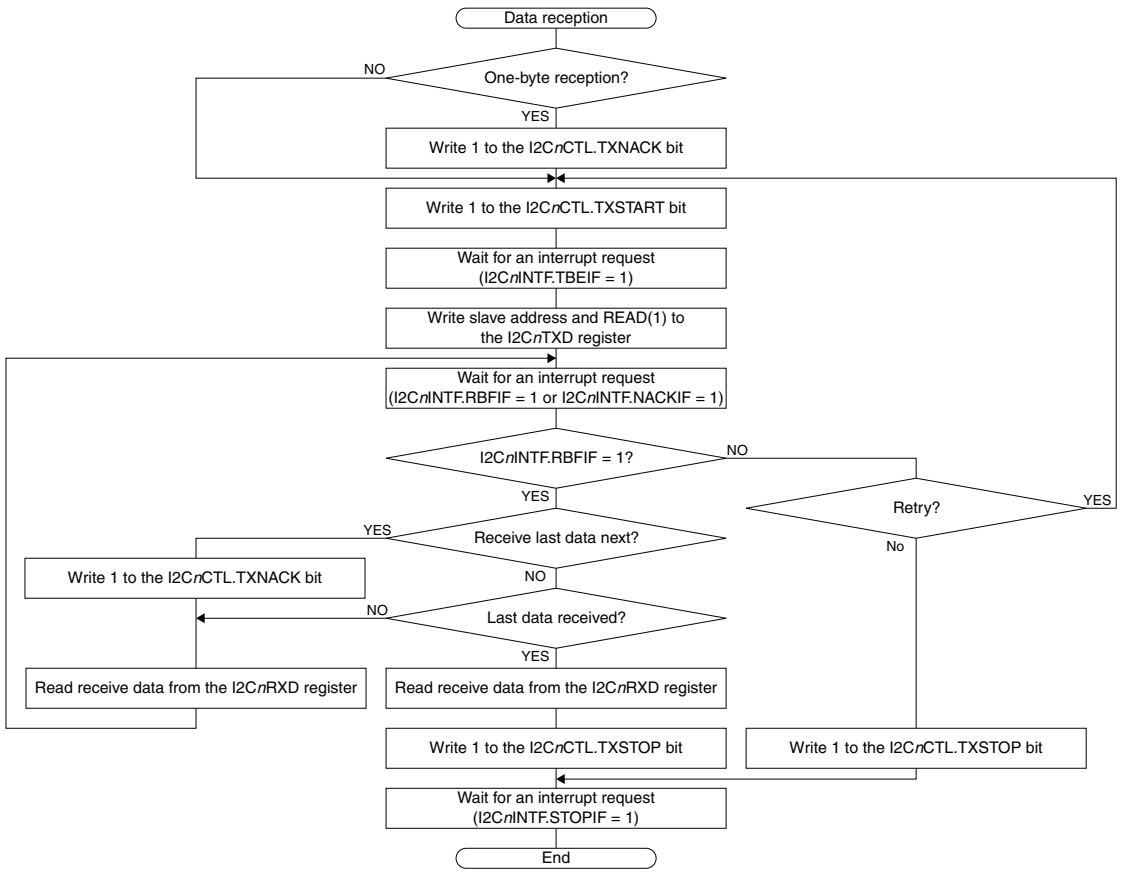


Figure 13.4.3.2 Master Mode Data Reception Flowchart

13.4.4 10-bit Addressing in Master Mode

A 10-bit address consists of the first address that contains two high-order bits and the second address that contains eight low-order bits.

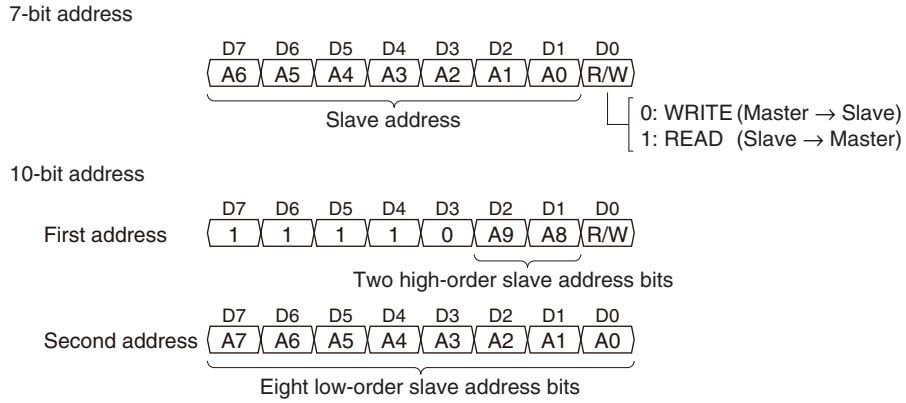


Figure 13.4.4.1 10-bit Address Configuration

The following shows a procedure to start data transfer in 10-bit address mode when the I2C Ch.*n* is placed into master mode (see the 7-bit mode descriptions above for control procedures when a NACK is received or sending/receiving data). Figure 13.4.4.2 shows an operation example.

Starting data transmission in 10-bit address mode

1. Issue a START condition by setting the I2C*n*CTL.TXSTART bit to 1.
2. Wait for a transmit buffer empty interrupt (I2C*n*INTF.TBEIF bit = 1) or a START condition interrupt (I2C*n*INTF.STARTIF bit = 1).
   Clear the I2C*n*INTF.STARTIF bit by writing 1 after the interrupt has occurred.
3. Write the first address to the I2C*n*TXD.TXD[7:1] bits and 0 that represents WRITE as the data transfer direction to the I2C*n*TXD.TXD0 bit.
4. Wait for a transmit buffer empty interrupt (I2C*n*INTF.TBEIF bit = 1).
5. Write the second address to the I2C*n*TXD.TXD[7:0] bits.
6. Wait for a transmit buffer empty interrupt (I2C*n*INTF.TBEIF bit = 1).
7. Perform data transmission.

Starting data reception in 10-bit address mode

1 to 6. These steps are the same as the data transmission starting procedure described above.

7. Issue a repeated START condition by setting the I2C*n*CTL.TXSTART bit to 1.
8. Wait for a transmit buffer empty interrupt (I2C*n*INTF.TBEIF bit = 1) or a START condition interrupt (I2C*n*INTF.STARTIF bit = 1).
   Clear the I2C*n*INTF.STARTIF bit by writing 1 after the interrupt has occurred.
9. Write the first address to the I2C*n*TXD.TXD[7:1] bits and 1 that represents READ as the data transfer direction to the I2C*n*TXD.TXD0 bit.
10. Perform data reception.

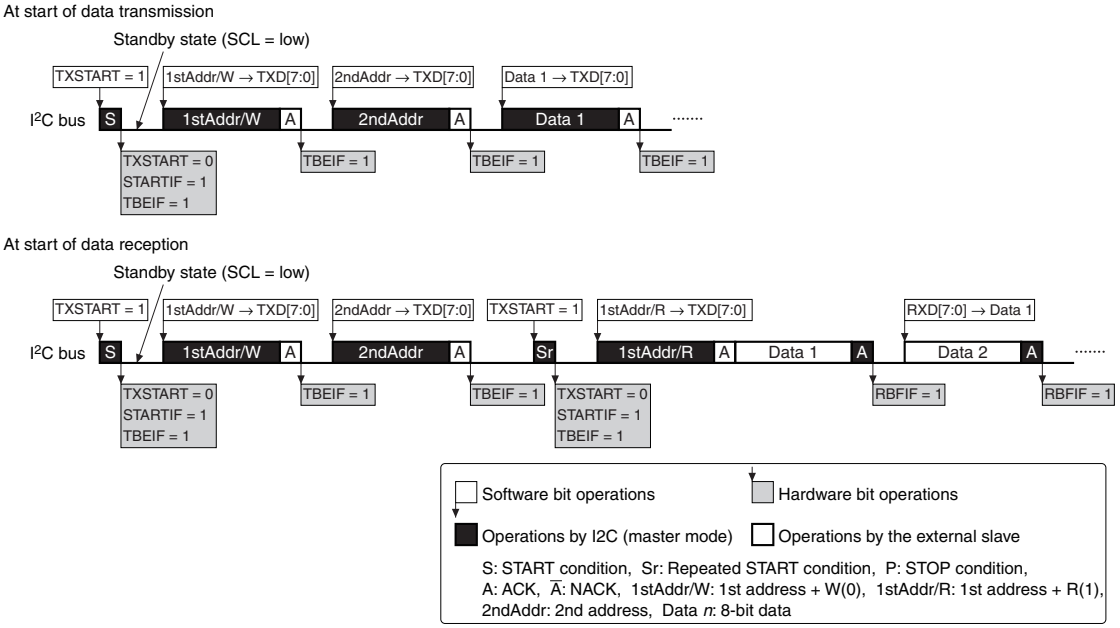


Figure 13.4.4.2 Example of Data Transfer Starting Operations in 10-bit Address Mode (Master Mode)

13.4.5 Data Transmission in Slave Mode

A data sending procedure in slave mode and the I2C Ch.*n* operations are shown below. Figures 13.4.5.1 and 13.4.5.2 show an operation example and a flowchart, respectively.

Data sending procedure

1. Wait for a START condition interrupt (I2C*n*INTF.STARTIF bit = 1).
   Clear the I2C*n*INTF.STARTIF bit by writing 1 after the interrupt has occurred.
2. Check to see if the I2C*n*INTF.TR bit = 1 (transmission mode).
   (Start a data receiving procedure if the I2C*n*INTF.TR bit = 0.)
3. Write transmit data to the I2C*n*TXD register.
4. Wait for a transmit buffer empty interrupt (I2C*n*INTF.TBEIF bit = 1), a NACK reception interrupt (I2C*n*INTF.NACKIF bit = 1), or a STOP condition interrupt (I2C*n*INTF.STOPIF bit = 1).
   i. Go to Step 3 when a transmit buffer empty interrupt has occurred.
   ii. Go to Step 5 after clearing the I2C*n*INTF.NACKIF bit when a NACK reception interrupt has occurred.
   iii. Go to Step 6 when a STOP condition interrupt has occurred.
5. Wait for a STOP condition interrupt (I2C*n*INTF.STOPIF bit = 1) or a START condition interrupt (I2C*n*INTF.STARTIF bit = 1).
   i. Go to Step 6 when a STOP condition interrupt has occurred.
   ii. Go to Step 2 when a START condition interrupt has occurred.
6. Clear the I2C*n*INTF.STOPIF bit and then terminate data sending operations.

Data sending operations

START condition detection and slave address check

While the I2C*n*CTL.MODEN bit = 1 and the I2C*n*CTL.MST bit = 0 (slave mode), the I2C Ch.*n* monitors the I²C bus. When the I2C Ch.*n* detects a START condition, it starts receiving of the slave address sent from the master. If the received address is matched with the own address set to the I2C*n*OADR.OADR[6:0] bits (when the I2C*n*MOD.OADR10 bit = 0 (7-bit address mode)) or the I2C*n*OADR.OADR[9:0] bits (when the I2C*n*MOD.OADR10 bit = 1 (10-bit address mode)), the I2C*n*INTF.STARTIF bit and the I2C*n*INTF.BSY bit are both set to 1. The I2C Ch.*n* sets the I2C*n*INTF.TR bit to the R/W bit value in the received address. If this value is 1, the I2C Ch.*n* sets the I2C*n*INTF.TBEIF bit to 1 and starts data sending operations.

Sending the first data byte

After the valid slave address has been received, the I2C Ch.*n* pulls down SCL to low and enters standby state until data is written to the I2C*n*TXD register. This puts the I²C bus into clock stretching state and the external master into standby state. When transmit data is written to the I2C*n*TXD register, the I2C Ch.*n* clears the I2C*n*INTF.TBEIF bit and sends an ACK to the master. The transmit data written in the I2C*n*TXD register is automatically transferred to the shift register and the I2C*n*INTF.TBEIF bit is set to 1. The data bits in the shift register are output in sequence to the I²C bus.

Sending subsequent data

If the I2C*n*INTF.TBEIF bit = 1, subsequent transmit data can be written during data transmission. If the I2C*n*INTF.TBEIF bit is still set to 1 when the data transmission from the shift register has completed, the I2C Ch.*n* pulls down SCL to low (sets the I²C bus into clock stretching state) until transmit data is written to the I2C*n*TXD register.

If the next transmit data already exists in the I2C*n*TXD register or data has been written after the above, the I2C Ch.*n* sends the subsequent eight-bit data when an ACK from the external master is received. At the same time, the I2C*n*INTF.BYTEENDIF bit is set to 1. If a NACK is received, the I2C*n*INTF.NACKIF bit is set to 1 without sending data.

STOP/repeated START condition detection

While the I2C*n*CTL.MST bit = 0 (slave mode) and the I2C*n*INTF.BSY = 1, the I2C Ch.*n* monitors the I²C bus. When the I2C Ch.*n* detects a STOP condition, it terminates data sending operations. At this time, the I2C*n*INTF.BSY bit is cleared to 0 and the I2C*n*INTF.STOPIF bit is set to 1. Also when the I2C Ch.*n* detects a repeated START condition, it terminates data sending operations. In this case, the I2C*n*INTF.STARTIF bit is set to 1.

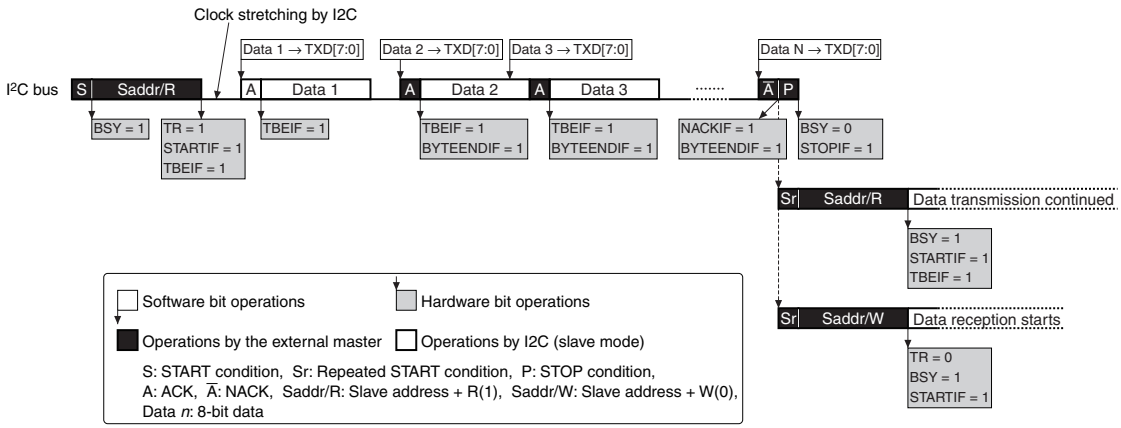


Figure 13.4.5.1 Example of Data Sending Operations in Slave Mode

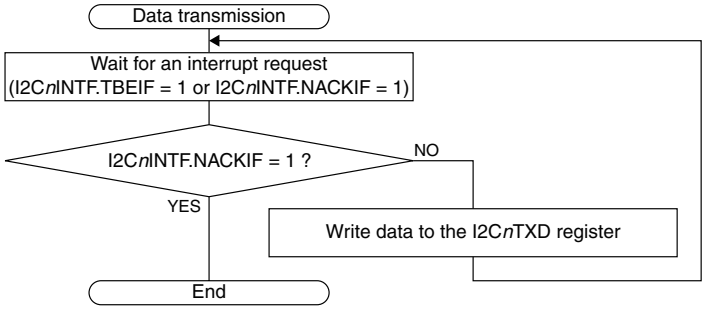


Figure 13.4.5.2 Slave Mode Data Transmission Flowchart

13.4.6 Data Reception in Slave Mode

A data receiving procedure in slave mode and the I2C Ch.*n* operations are shown below. Figures 13.4.6.1 and 13.4.6.2 show an operation example and a flowchart, respectively.

Data receiving procedure

1. When receiving one-byte data, write 1 to the I2C*n*CTL.TXNACK bit.
2. Wait for a START condition interrupt (I2C*n*INTF.STARTIF bit = 1).
3. Check to see if the I2C*n*INTF.TR bit = 0 (reception mode).
   (Start a data sending procedure if I2C*n*INTF.TR bit = 1.)
4. Clear the I2C*n*INTF.STARTIF bit by writing 1.
5. Wait for a receive buffer full interrupt (I2C*n*INTF.RBFIF bit = 1) generated when a one-byte reception has completed or an end of transfer interrupt (I2C*n*INTF.BYTEENDIF bit = 1).
   Clear the I2C*n*INTF.BYTEENDIF bit by writing 1 after the interrupt has occurred.
6. If the next receive data is the last one, write 1 to the I2C*n*CTL.TXNACK bit to send a NACK after it is received.
7. Read the received data from the I2C*n*RXD register.
8. Repeat Steps 5 to 7 until the end of data reception.
9. Wait for a STOP condition interrupt (I2C*n*INTF.STOPIF bit = 1) or a START condition interrupt (I2C*n*INTF.STARTIF bit = 1).
   i. Go to Step 10 when a STOP condition interrupt has occurred.
   ii. Go to Step 3 when a START condition interrupt has occurred.
10. Clear the I2C*n*INTF.STOPIF bit and then terminate data receiving operations.

Data receiving operations

START condition detection and slave address check

It is the same as the data transmission in slave mode.
However, the I2C*n*INTF.TR bit is cleared to 0 and the I2C*n*INTF.TBEIF bit is not set.
If the I2C*n*MOD.GCEN bit is set to 1 (general call address response enabled), the I2C Ch.*n* starts data receiving operations when the general call address is received.
Slave mode can be operated even in SLEEP mode, it makes it possible to wake the CPU up using an interrupt when an address match is detected.

Receiving the first data byte

After the valid slave address has been received, the I2C Ch.*n* sends an ACK and pulls down SCL to low until 1 is written to the I2C*n*INTF.STARTIF bit. This puts the I²C bus into clock stretching state and the external master into standby state. When 1 is written to the I2C*n*INTF.STARTIF bit, the I2C Ch.*n* releases SCL and receives data sent from the external master into the shift register. After eight-bit data has been received, the I2C Ch.*n* sends an ACK and pulls down SCL to low. The received data in the shift register is transferred to the receive data buffer and the I2C*n*INTF.RBFIF and I2C*n*INTF.BYTEENDIF bits are both set to 1. After that, the received data can be read out from the I2C*n*RXD register.

Receiving subsequent data

When the received data is read out from the I2C*n*RXD register after the I2C*n*INTF.RBFIF bit has been set to 1, the I2C Ch.*n* clears the I2C*n*INTF.RBFIF bit to 0, releases SCL, and receives subsequent data sent from the external master. After eight-bit data has been received, the I2C Ch.*n* sends an ACK and pulls down SCL to low. The received data in the shift register is transferred to the receive data buffer and the I2C*n*INTF.RBFIF and I2C*n*INTF.BYTEENDIF bits are both set to 1.

To return a NACK after eight-bit data is received, such as when terminating data reception, write 1 to the I2C*n*CTL.TXNACK bit before the data reception is completed. The I2C*n*CTL.TXNACK bit is automatically cleared to 0 after a NACK has been sent.

STOP/repeated START condition detection

It is the same as the data transmission in slave mode.

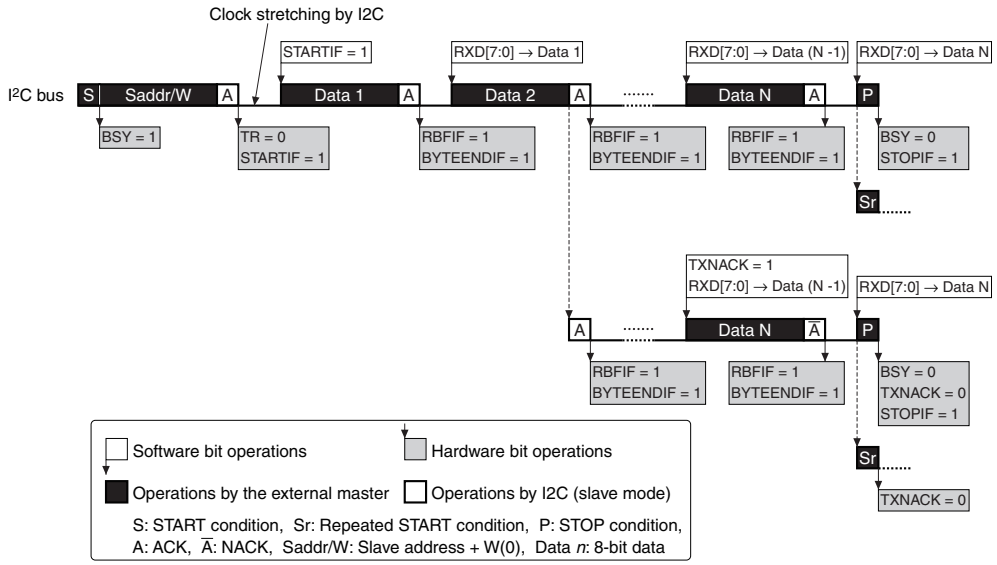


Figure 13.4.6.1 Example of Data Receiving Operations in Slave Mode

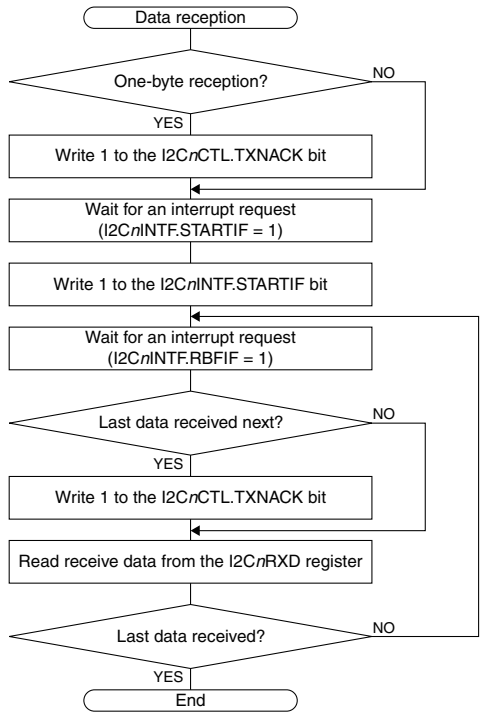


Figure 13.4.6.2 Slave Mode Data Reception Flowchart

13.4.7 Slave Operations in 10-bit Address Mode

The I2C Ch.*n* functions as a slave device in 10-bit address mode when the I2C*n*CTL.MST bit = 0 and the I2C*n*MOD.OADR10 bit = 1.

The following shows the address receiving operations in 10-bit address mode. Figure 13.4.7.1 shows an operation example. See Figure 13.4.4.1 for the 10-bit address configuration.

10-bit address receiving operations

After a START condition is issued, the master sends the first address that includes the two high-order slave address bits and the R/W bit (= 0). If the received two high-order slave address bits are matched with the I2C*n*OADR.OADR[9:8] bits, the I2C Ch.*n* returns an ACK. At this time, other slaves may returns an ACK as the two high-order bits may be matched.

Then the master sends the eight low-order slave address bits as the second address. If this address is matched with the I2C*n*OADR.OADR[7:0] bits, the I2C Ch.*n* returns an ACK and starts data receiving operations.

If the master issues a request to the slave to send data (data reception in the master), the master generates a repeated START condition and sends the first address with the R/W bit set to 1. This reception switches the I2C Ch.*n* to data sending mode.

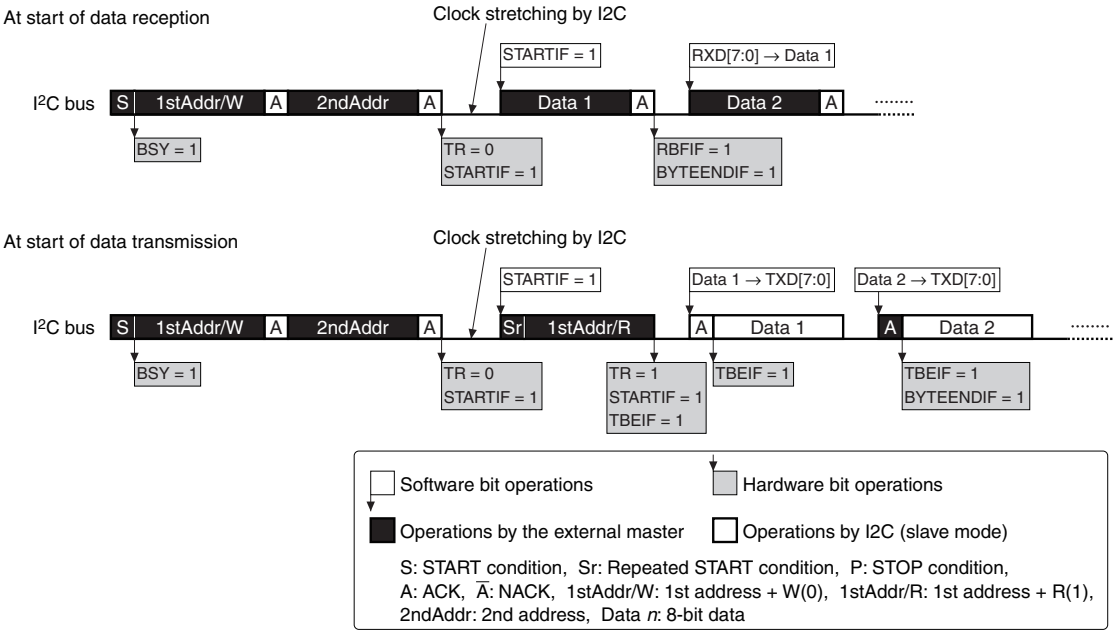


Figure 13.4.7.1 Example of Data Transfer Starting Operations in 10-bit Address Mode (Slave Mode)

13.4.8 Automatic Bus Clearing Operation

The I2C Ch.*n* set into master mode checks the SDA state immediately before generating a START condition. If SDA is set to a low level at this time, the I2C Ch.*n* automatically executes bus clearing operations that output up to ten clocks from the SCL*n* pin with SDA left free state.

When SDA goes high from low within nine clocks, the I2C Ch.*n* issues a START condition and starts normal operations. If SDA does not change from low when the I2C Ch.*n* outputs the ninth clock, it is regarded as an automatic bus clearing failure. In this case, the I2C Ch.*n* clears the I2C*n*CTL.TXSTART bit to 0 and sets both the I2C*n*INTF.ERRIF and I2C*n*INTF.STARTIF bits to 1.

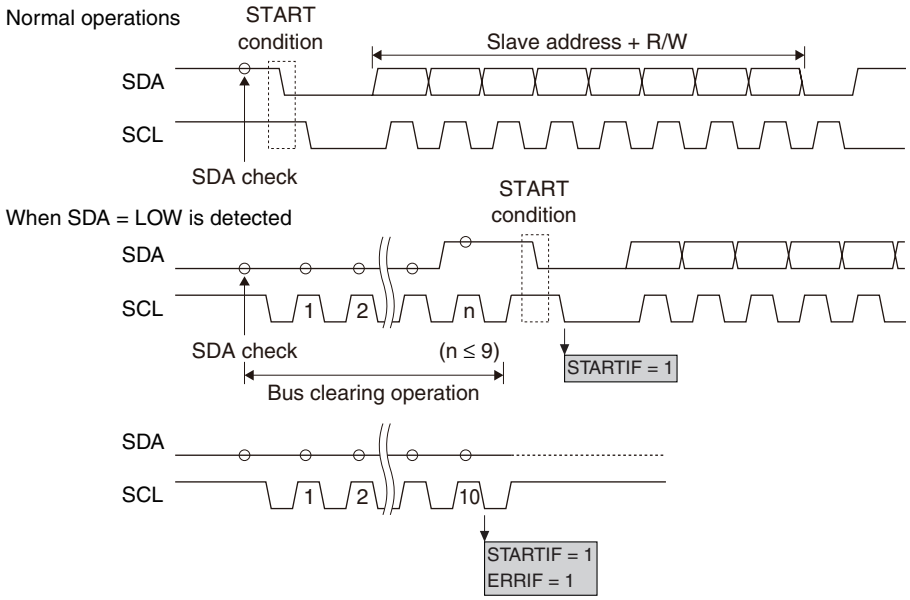


Figure 13.4.8.1 Automatic Bus Clearing Operation

13.4.9 Error Detection

The I2C includes a hardware error detection function.
Furthermore, the I2C*n*INTF.SDALOW and I2C*n*INTF.SCLLOW bits are provided to allow software to check whether the SDA and SCL lines are fixed at low. If unintended low level is detected on SDA or SCL, a software recovery processing, such as I2C Ch.*n* software reset, can be performed.

The table below lists the hardware error detection conditions and the notification method.

Table 13.4.9.1 Hardware Error Detection Function

No.	Error detecting period/timing	I²C bus line monitored and error condition	Notification method
1	While the I2C Ch.*n* controls SDA to high for sending address, data, or a NACK	SDA = low	I2C*n*INTF.ERRIF = 1
2	<Master mode only> When 1 is written to the I2C*n*CTL.TXSTART bit while the I2C*n*INTF.BSY bit = 0	SCL = low	I2C*n*INTF.ERRIF = 1 I2C*n*CTL.TXSTART = 0 I2C*n*INTF.STARTIF = 1
3	<Master mode only> When 1 is written to the I2C*n*CTL.TXSTOP bit while the I2C*n*INTF.BSY bit = 0	SCL = low	I2C*n*INTF.ERRIF = 1 I2C*n*CTL.TXSTOP = 0 I2C*n*INTF.STOPIF = 1
4	<Master mode only> When 1 is written to the I2C*n*CTL.TXSTART bit while the I2C*n*INTF.BSY bit = 0 (Refer to "Automatic Bus Clearing Operation.")	SDA Automatic bus clearing failure	I2C*n*INTF.ERRIF = 1 I2C*n*CTL.TXSTART = 0 I2C*n*INTF.STARTIF = 1

13.5 Interrupts

The I2C has a function to generate the interrupts shown in Table 13.5.1.

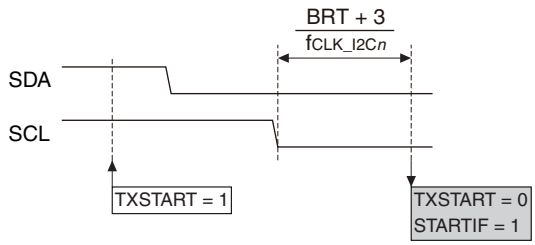
Table 13.5.1 I2C Interrupt Function

Interrupt	Interrupt flag	Set condition	Clear condition
End of data transfer	I2C*n*INTF.BYTEENDIF	When eight-bit data transfer and the following ACK/NACK transfer are completed	Writing 1, software reset
General call address reception	I2C*n*INTF.GCIF	Slave mode only: When the general call address is received	Writing 1, software reset
NACK reception	I2C*n*INTF.NACKIF	When a NACK is received	Writing 1, software reset
STOP condition	I2C*n*INTF. STOPIF	Master mode: When a STOP condition is generated and the bus free time (t_{BUF}) between STOP and START conditions has elapsed Slave mode: When a STOP condition is detected while the I2C Ch.*n* is selected as the slave currently accessed	Writing 1, software reset
START condition	I2C*n*INTF. STARTIF	Master mode: When a START condition is issued Slave mode: When an address match is detected (including general call)	Writing 1, software reset
Error detection	I2C*n*INTF. ERRIF	Refer to "Error Detection."	Writing 1, software reset
Receive buffer full	I2C*n*INTF. RBFIF	When received data is loaded to the receive data buffer	Reading received data (to empty the receive data buffer), software reset
Transmit buffer empty	I2C*n*INTF. TBEIF	Master mode: When a START condition is issued or when an ACK is received from the slave Slave mode: When transmit data written to the transmit data buffer is transferred to the shift register or when an address match is detected with R/W bit set to 1	Writing transmit data

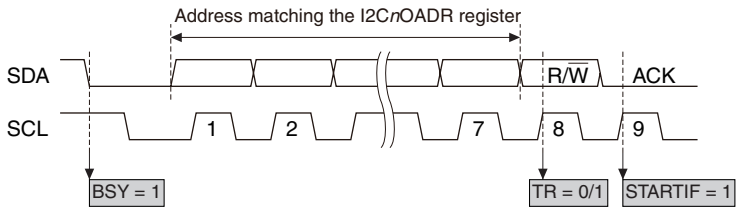
The I2C provides interrupt enable bits corresponding to each interrupt flag. An interrupt request is sent to the interrupt controller only when the interrupt flag, of which interrupt has been enabled by the interrupt enable bit, is set. For more information on interrupt control, refer to the "Interrupt Controller" chapter.

(1) START condition interrupt

Master mode

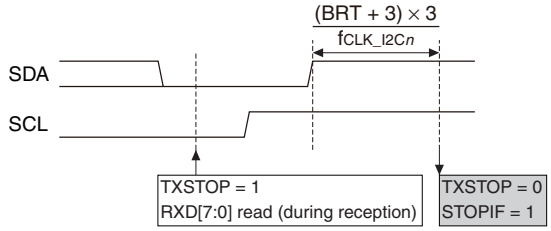


Slave mode

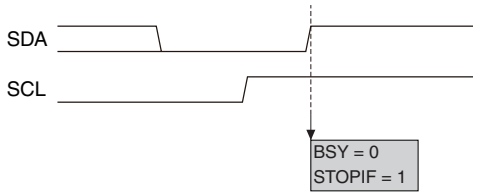


(2) STOP condition interrupt

Master mode



Slave mode



(f_{CLK_I2Cn}: I2C operating clock frequency [Hz], BRT: I2C*n*BR.BRT[6:0] bits setting value (1 to 127))

Figure 13.5.1 START/STOP Condition Interrupt Timings

13.6 Control Registers

I2C Ch.*n* Clock Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
I2C*n*CLK	15–9	–	0x00	–	R	–
	8	DBRUN	0	H0	R/W	
	7–6	–	0x0	–	R	
	5–4	CLKDIV[1:0]	0x0	H0	R/W	
	3–2	–	0	–	R	
	1–0	CLKSRC[1:0]	0x0	H0	R/W	

Bits 15–9 Reserved

Bit 8 DBRUN

This bit sets whether the I2C operating clock is supplied in DEBUG mode or not.

1 (R/W): Clock supplied in DEBUG mode

0 (R/W): No clock supplied in DEBUG mode

Bits 7–6 Reserved

Bits 5–4 CLKDIV[1:0]

These bits select the division ratio of the I2C operating clock.

Bits 3–2 Reserved

Bits 1–0 CLKSRC[1:0]

These bits select the clock source of the I2C.

Table 13.6.1 Clock Source and Division Ratio Settings

I2C*n*CLK.CLKDIV[1:0] bits	I2C*n*CLK.CLKSRC[1:0] bits			
	0x0	0x1	0x2	0x3
	IOSC	OSC1	OSC3	EXOSC
0x3	1/8	1/1	1/8	1/1
0x2	1/4		1/4	
0x1	1/2		1/2	
0x0	1/1		1/1	

(Note) The oscillation circuits/external input that are not supported in this IC cannot be selected as the clock source.

Note: The I2C*n*CLK register settings can be altered only when the I2C*n*CTL.MODEN bit = 0.

I2C Ch.*n* Mode Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
I2C*n*MOD	15–8	–	0x00	–	R	–
	7–3	–	0x00	–	R	
	2	OADR10	0	H0	R/W	
	1	GCEN	0	H0	R/W	
	0	–	0	–	R	

Bits 15–3 Reserved

Bit 2 OADR10

This bit sets the number of own address bits for slave mode.
1 (R/W): 10-bit address
0 (R/W): 7-bit address

Bit 1 GCEN

This bit sets whether to respond to master general calls in slave mode or not.
1 (R/W): Respond to general calls.
0 (R/W): Do not respond to general calls.

Bit 0 Reserved

Note: The I2C*n*MOD register settings can be altered only when the I2C*n*CTL.MODEN bit = 0.

I2C Ch.*n* Baud-Rate Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
I2C*n*BR	15–8	–	0x00	–	R	–
	7	–	0	–	R	
	6–0	BRT[6:0]	0x7f	H0	R/W	

Bits 15–7 Reserved

Bits 6–0 BRT[6:0]

These bits set the I2C Ch.*n* transfer rate for master mode. For more information, refer to "Baud Rate Generator."

Notes: • The I2C*n*BR register settings can be altered only when the I2C*n*CTL.MODEN bit = 0.

• Be sure to avoid setting the I2C*n*BR register to 0.

I2C Ch.*n* Own Address Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
I2C*n*OADR	15–10	–	0x00	–	R	–
	9–0	OADR[9:0]	0x000	H0	R/W	

Bits 15–10 Reserved

Bits 9–0 OADR[9:0]

These bits set the own address for slave mode.
The I2C*n*OADR.OADR[9:0] bits are effective in 10-bit address mode (I2C*n*MOD.OADR10 bit = 1), or the I2C*n*OADR.OADR[6:0] bits are effective in 7-bit address mode (I2C*n*MOD.OADR10 bit = 0).

Note: The I2C*n*OADR register settings can be altered only when the I2C*n*CTL.MODEN bit = 0.

I2C Ch.*n* Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
I2C*n*CTL	15–8	–	0x00	–	R	–
	7–6	–	0x0	–	R	
	5	MST	0	H0	R/W	
	4	TXNACK	0	H0/S0	R/W	
	3	TXSTOP	0	H0/S0	R/W	
	2	TXSTART	0	H0/S0	R/W	
	1	SFTRST	0	H0	R/W	
	0	MODEN	0	H0	R/W	

Bits 15–6 Reserved

Bit 5 MST

This bit selects the I2C Ch.*n* operating mode.

1 (R/W): Master mode

0 (R/W): Slave mode

Bit 4 TXNACK

This bit issues a request for sending a NACK at the next responding.

1 (W): Issue a NACK.

0 (W): Ineffective

1 (R): On standby or during sending a NACK

0 (R): NACK has been sent.

This bit is automatically cleared after a NACK has been sent.

Bit 3 TXSTOP

This bit issues a STOP condition in master mode. This bit is ineffective in slave mode.

1 (W): Issue a STOP condition.

0 (W): Ineffective

1 (R): On standby or during generating a STOP condition

0 (R): STOP condition has been generated.

This bit is automatically cleared when the bus free time (t_{BUF} defined in the I²C Specifications) has elapsed after the STOP condition has been generated.

Bit 2 TXSTART

This bit issues a START condition in master mode. This bit is ineffective in slave mode.

1 (W): Issue a START condition.

0 (W): Ineffective

1 (R): On standby or during generating a START condition

0 (R): START condition has been generated.

This bit is automatically cleared when a START condition has been generated.

Bit 1 SFTRST

This bit issues software reset to the I2C.

1 (W): Issue software reset

0 (W): Ineffective

1 (R): Software reset is executing.

0 (R): Software reset has finished. (During normal operation)

Setting this bit resets the I2C transmit/receive control circuit and interrupt flags. This bit is automatically cleared after the reset processing has finished.

Bit 0 MODEN

This bit enables the I2C operations.

1 (R/W): Enable I2C operations (The operating clock is supplied.)

0 (R/W): Disable I2C operations (The operating clock is stopped.)

Note: If the I2C*n*CTL.MODEN bit is altered from 1 to 0 while sending/receiving data, the data being sent/received cannot be guaranteed. When setting the I2C*n*CTL.MODEN bit to 1 again after that, be sure to write 1 to the I2C*n*CTL.SFTRST bit as well.

I2C Ch.*n* Transmit Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
I2C*n*TXD	15–8	–	0x00	–	R	–
	7–0	TXD[7:0]	0x00	H0	R/W	

Bits 15–8 Reserved

Bits 7–0 TXD[7:0]

Data can be written to the transmit data buffer through these bits. Make sure the I2C*n*INTF.TBEIF bit is set to 1 before writing data.

Note: Be sure to avoid writing to the I2C*n*TXD register when the I2C*n*INTF.TBEIF bit = 0, otherwise transmit data cannot be guaranteed.

I2C Ch.*n* Receive Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
I2C*n*RXD	15–8	–	0x00	–	R	–
	7–0	RXD[7:0]	0x00	H0	R	

Bits 15–8 Reserved

Bits 7–0 RXD[7:0]

The receive data buffer can be read through these bits.

I2C Ch.*n* Status and Interrupt Flag Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
I2C*n*INTF	15–13	–	0x0	–	R	–
	12	SDALOW	0	H0	R	
	11	SCLLOW	0	H0	R	
	10	BSY	0	H0/S0	R	
	9	TR	0	H0	R	
	8	–	0	–	R	
	7	BYTEENDIF	0	H0/S0	R/W	Cleared by writing 1.
	6	GCIF	0	H0/S0	R/W	
	5	NACKIF	0	H0/S0	R/W	
	4	STOPIF	0	H0/S0	R/W	
	3	STARTIF	0	H0/S0	R/W	
	2	ERRIF	0	H0/S0	R/W	
	1	RBFIF	0	H0/S0	R	Cleared by reading the I2C*n*RXD register.
	0	TBEIF	0	H0/S0	R	Cleared by writing to the I2C*n*TXD register.

Bits 15–13 Reserved

Bit 12 SDALOW

This bit indicates that SDA is set to low level.

1 (R): SDA = Low level

0 (R): SDA = High level

Bit 11 SCLLOW

This bit indicates that SCL is set to low level.

1 (R): SCL = Low level

0 (R): SCL = High level

Bit 10 BSY

This bit indicates that the I²C bus is placed into busy status.

1 (R): I²C bus busy

0 (R): I²C bus free

Bit 9 TR

This bit indicates whether the I2C is set in transmission mode or not.

1 (R): Transmission mode

0 (R): Reception mode

Bit 8 Reserved

Bit 7 BYTEENDIF
Bit 6 GCIF
Bit 5 NACKIF
Bit 4 STOPIF
Bit 3 STARTIF
Bit 2 ERRIF
Bit 1 RBFIF
Bit 0 TBEIF

These bits indicate the I2C interrupt cause occurrence status.

1 (R): Cause of interrupt occurred

0 (R): No cause of interrupt occurred

1 (W): Clear flag

0 (W): Ineffective

The following shows the correspondence between the bit and interrupt:

I2C*n*INTF.BYTEENDIF bit: End of transfer interrupt
I2C*n*INTF.GCIF bit: General call address reception interrupt
I2C*n*INTF.NACKIF bit: NACK reception interrupt
I2C*n*INTF.STOPIF bit: STOP condition interrupt
I2C*n*INTF.STARTIF bit: START condition interrupt
I2C*n*INTF.ERRIF bit: Error detection interrupt
I2C*n*INTF.RBFIF bit: Receive buffer full interrupt
I2C*n*INTF.TBEIF bit: Transmit buffer empty interrupt

I2C Ch.*n* Interrupt Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
I2C*n*INTE	15–8	–	0x00	–	R	–
	7	BYTEENDIE	0	H0	R/W	
	6	GCIE	0	H0	R/W	
	5	NACKIE	0	H0	R/W	
	4	STOPIE	0	H0	R/W	
	3	STARTIE	0	H0	R/W	
	2	ERRIE	0	H0	R/W	
	1	RBFIE	0	H0	R/W	
	0	TBEIE	0	H0	R/W	

Bits 15–8 Reserved

Bit 7 BYTEENDIE
Bit 6 GCIE
Bit 5 NACKIE
Bit 4 STOPIE
Bit 3 STARTIE
Bit 2 ERRIE
Bit 1 RBFIE
Bit 0 TBEIE

These bits enable I2C interrupts.
1 (R/W): Enable interrupts
0 (R/W): Disable interrupts

The following shows the correspondence between the bit and interrupt:
I2C*n*INTE.BYTEENDIE bit: End of transfer interrupt
I2C*n*INTE.GCIE bit: General call address reception interrupt
I2C*n*INTE.NACKIE bit: NACK reception interrupt
I2C*n*INTE.STOPIE bit: STOP condition interrupt
I2C*n*INTE.STARTIE bit: START condition interrupt
I2C*n*INTE.ERRIE bit: Error detection interrupt
I2C*n*INTE.RBFIE bit: Receive buffer full interrupt
I2C*n*INTE.TBEIE bit: Transmit buffer empty interrupt

14 Smart Card Interface (SMCIF)

14.1 Overview

SMCIF is an interface circuit that supports smart cards (IC cards) conforming to the ISO7816-3 standard. The features of the SMCIF are listed below.

- Supports both master and slave modes.
- Includes a baud rate generator for generating the transfer rate from the smart card clock.
- Allows stopping the smart card clock output and the selection of pin levels when the clock output is stopped.
- Supports asynchronous half duplex communication (8 data bits and 1 parity bit).
- Includes a 2-byte receive data buffer and a 1-byte transmit data buffer.
- Configurable data input/output level (non-inverted/inverted)
- Configurable data input/output direction (MSB first/LSB first)
- Selectable protocol (T = 0 mode/T = 1 mode)
- Supports guard time and wait time functions.
- Can detect transmit signal error, parity error, and overrun error.
- Can generate transmit buffer empty, end of transmission, transmit error (error signal detection), receive buffer full (1 byte/2 bytes), receive error (parity error/overrun error), and wait time error interrupts
- Configurable output pin (push-pull/open-drain)

Figure 14.1.1 shows the SMCIF configuration.

Table 14.1.1 SMCIF Channel Configuration of S1C17F63

Item	S1C17F63
Number of channels	1 channel (Ch.0)

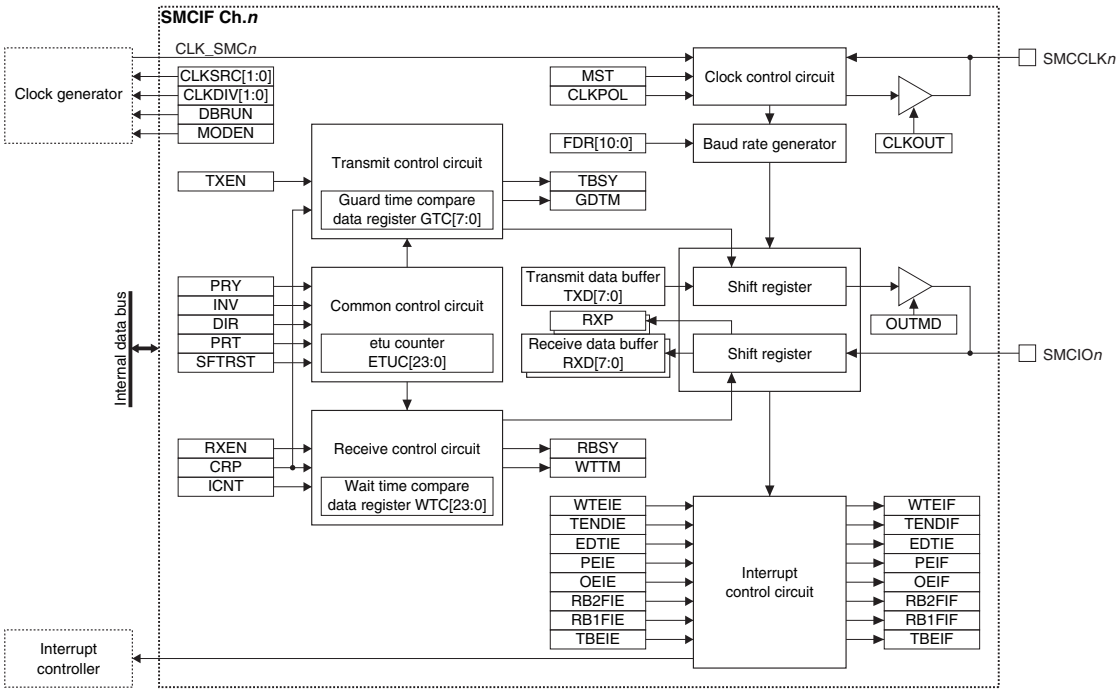


Figure 14.1.1 SMCIF Configuration

14.2 Input/Output Pins and External Connections

14.2.1 List of Input/Output Pins

Table 14.2.1.1 lists the SMCIF pins.

Table 14.2.1.1 List of SMCIF Pins

Pin name	I/O*	Initial status*	Function
SMCCLK*n*	I/O	O (L)	SMCIF Ch.*n* smart card clock input/output pin
SMCIO*n*	I/O	I (Hi-Z)	SMCIF Ch.*n* smart card data input/output pin

* Indicates the status when the pin is configured for SMCIF.

If the port is shared with the SMCIF pin and other functions, the SMCIF input/output function must be assigned to the port before activating SMCIF. For more information, refer to the "I/O Ports" chapter.

14.2.2 External Connections

Figure 14.2.2.1 shows a connection diagram between the SMCIF in this IC and external ISO7816 devices.

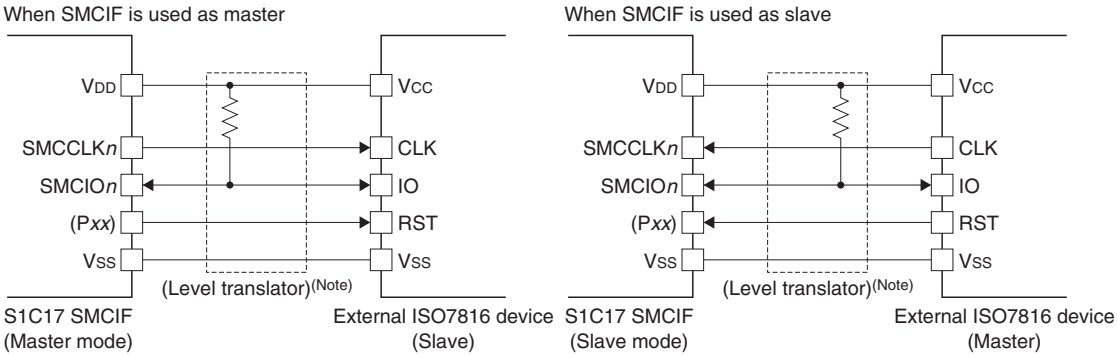


Figure 14.2.2.1 Connections between SMCIF and External ISO7816 Devices

The SMCIO*n* pin should be pulled up to VDD for this IC or a lower voltage using an external resistor. However, if the SMCIO*n* port is configured with the over voltage tolerant fail-safe type I/O, this pin can be pulled up to a voltage exceeding the VDD but within the recommended operating voltage range of this IC. SMCIF has no RST pin, which is defined in the ISO7816-3 specification, therefore, use a general-purpose I/O port to control the RST signal.

Note: If high ESD protection ability is required or if the external device to be connected uses a different interface voltage from SMCIF, connect it through a level translator IC.

14.2.3 Open-Drain/Push-Pull Selection for Output Pin

The SMCIO*n* pin is configured as an open-drain type output by default. It can be reconfigured as a push-pull type output by setting the SMC*n*MOD.OUTMD bit to 0.

14.3 Clock Settings

14.3.1 SMCIF Operating Clock

Operating clock in master mode

When used in master mode, SMCIF Ch.*n* operates with the SMCIF operating clock CLK_SMC*n* supplied from the clock generator. This clock can also be output from the SMCCLK*n* pin as the operating clock for an external ISO7816 slave device.

The CLK_SMC*n* supply should be controlled as in the procedure shown below.

1. Set the SMC*n*MOD.MST bit to 1. (Put SMCIF Ch.*n* into master mode)

2. Enable the clock source in the clock generator if it is stopped (refer to "Clock Generator" in the "Power Supply, Reset, and Clocks" chapter).
3. Set the following SMCnCLK register bits:
   - SMC*n*CLK.CLKSRC[1:0] bits (Clock source selection)
   - SMC*n*CLK.CLKDIV[1:0] bits (Clock division ratio selection = Clock frequency setting)
4. Set the SMC*n*CTL.MODEN bit to 1. (Enable clock supply to SMCIF Ch.*n*)

Operating clock in slave mode

When used in slave mode, SMCIF Ch.*n* operates with the clock supplied to the SMCCLK*n* pin from the external ISO7816 master. This input clock is directly used as the SMCIF operating clock with the clock source and division ratio settings of the SMC*n*CLK register disabled.
The clock supply from the SMCCLK*n* pin should be controlled as in the procedure shown below.

1. Set the SMC*n*MOD.MST bit to 0. (Put SMCIF Ch.*n* into slave mode)
2. Set the SMC*n*CTL.MODEN bit to 1. (Enable clock supply to SMCIF Ch.*n*)

In slave mode, SMCIF Ch.*n* can operate with the external clock even if all clock sources in this IC are inactive such as during SLEEP mode.

14.3.2 Clock Supply in SLEEP Mode

When using SMCIF Ch.*n*, which is placed into master mode, during SLEEP mode, the SMCIF operating clock CLK_SMC*n* must be configured so that it will keep supplying by writing 0 to the CLGOSC.xxxxSLPC bit for the CLK_SMC*n* clock source.
When using SMCIF Ch.*n*, which is placed into slave mode, during SLEEP mode, clock source settings are not necessary, as it operates with the clock supplied to the SMCCLK*n* pin from the external ISO7816 master.

14.3.3 Clock Supply in DEBUG Mode

In master mode, the operating clock supply during DEBUG mode should be controlled using the SMC*n*CLK.DBRUN bit. The CLK_SMC*n* supply to SMCIF Ch.*n* is suspended when the CPU enters DEBUG mode if the SMC*n*CLK.DBRUN bit = 0. After the CPU returns to normal mode, the CLK_SMC*n* supply resumes. Although SMCIF Ch.*n* stops operating when the CLK_SMC*n* supply is suspended, the output pins and registers retain the status before DEBUG mode was entered. If the SMC*n*CLK.DBRUN bit = 1, the CLK_SMC*n* supply is not suspended and SMCIF Ch.*n* will keep operating in DEBUG mode.
SMCIF set to slave mode operates with the clock supplied to the SMCCLK*n* pin from the external ISO7816 master regardless of whether the CPU is placed into DEBUG mode or normal mode.

14.3.4 SMCCLK*n* Pin Output Disabling Function

In master mode, the clock output from the SMCCLK*n* pin can be disabled while SMCIF Ch.*n* is not performing data transfer.
This function should be controlled as in the procedure shown below.

1. Configure the SMC*n*MOD.CLKPOL bit. (Set pin level when clock output is disabled)
2. Set the SMC*n*CTL.CLKOUT bit to 0. (Disable clock output)
3. Set the SMC*n*CTL.CLKOUT bit to 1 to resume clock output.

If CLK_SMC*n* is being supplied, SMCIF Ch.*n* can continue data transmit/receive operations even if the clock output from the SMCCLK*n* pin is disabled. To disable data transmit/receive operations, control it via software.

14.3.5 Baud Rate Generator Settings

SMCIF Ch.*n* includes a baud rate generator that generates the transfer rate using CLK_SMC*n* in master mode or the SMCCLK*n* pin input clock in slave mode as the clock source. In the ISO7816 specification, the baud rate unit is defined as "etu" (Elementary Time Unit), which is the time required for transferring 1-bit characters, and it can be calculated using the parameters shown below.

$$1\ \text{etu} = \frac{F}{D} \times \frac{1}{f} \qquad \text{(Eq. 14.1)}$$

Where

- F: Clock rate conversion factor (integer)
- D: Baud rate adjustment factor (integer)
- f: CLK_SMC*n* clock frequency [Hz] (master mode) or SMCCLK*n* pin input clock frequency [Hz] (slave mode)

Use the SMC*n*BR.FDR[10:0] bits to set the baud rate of SMCIF Ch.*n*. See Table 14.8.2 for the correspondence between the parameters (F, D) and the SMC*n*BR.FDR[10:0] bit settings.

14.4 Data Format

SMCIF Ch.*n* provides the SMC*n*MOD.INV, SMC*n*MOD.DIR, and SMC*n*MOD.PRY bits to configure the data input/output direction, data input/output level, and odd/even parity mode, respectively. Also the SMC*n*MOD.PRT bit is provided to select a protocol from two modes shown below. Figure 14.4.1 shows data format configuration examples.

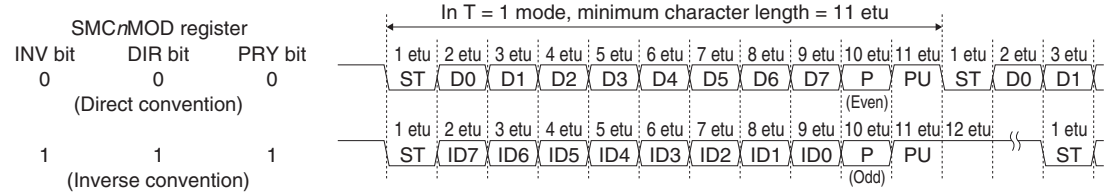
T = 0 mode (SMC*n*MOD.PRT bit = 0)

When the SMC*n*CTL.CRP bit = 1: If a parity error has been detected during data reception, SMCIF Ch.*n* sends an error signal to the transmitter. If an error signal is received during data transmission, SMCIF Ch.*n* retransmits the same data to the receiver.
When the SMC*n*CTL.CRP bit = 0: If a parity error has been detected during data reception, an error signal is not sent. If an error signal is received during data transmission, data is not retransmitted.

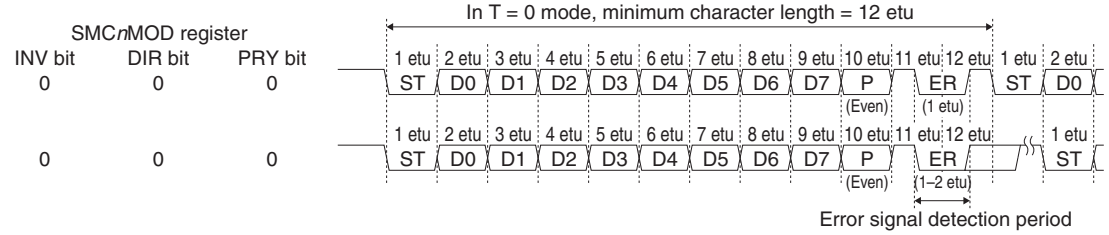
T = 1 mode (SMC*n*MOD.PRT bit = 1)

If a parity error has been detected during data reception, SMCIF Ch.*n* does not send an error signal to the transmitter. If an error signal is received during data transmission, SMCIF Ch.*n* does not retransmit the same data to the receiver.

When SMC*n*MOD.PRT bit = 1 (T = 1 mode)



When SMC*n*MOD.PRT bit = 0 (T = 0 mode)



ST: Start bit, P: Parity bit, PU: Pause state, ER: Error signal, Dx: Non-inverted data, IDx: Inverted data

Figure 14.4.1 Data Format Configuration Example

14.5 Guard Time and Wait Time Settings

The minimum and maximum times (configurable in etu units) between the first characters of a frame and the next frame are defined as guard time (GT) and wait time (WT), respectively. SMCIF Ch.*n* has an embedded etu counter that counts the guard and wait times. Figure 14.5.1 shows the counter operations.

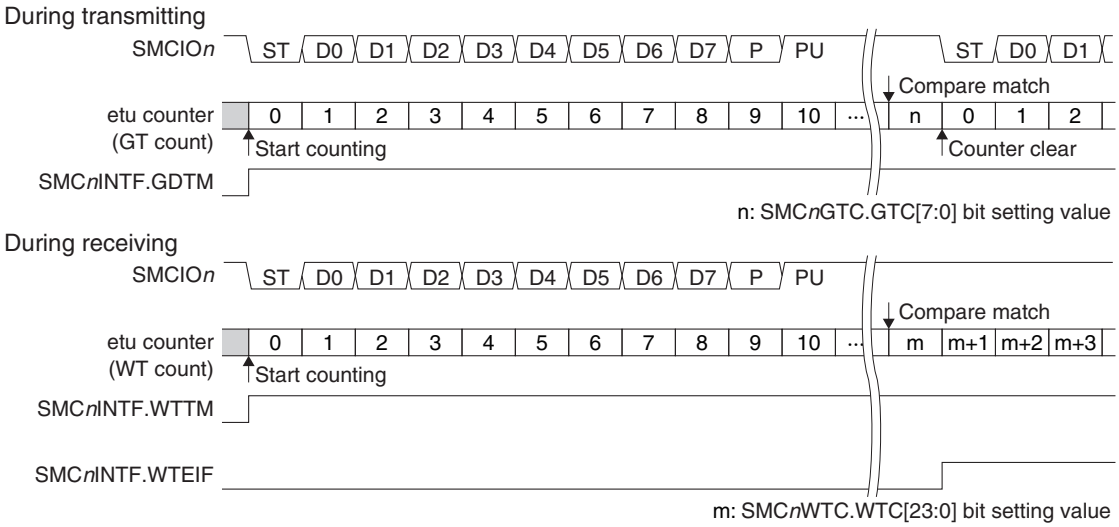


Figure 14.5.1 Guard Time and Wait Time Counter Operations

Guard time function

During data transmission, data of the next frame is transmitted after the time set using the SMC*n*GTC.GTC[7:0] bits has elapsed from the beginning of the current frame.

Wait time function

After data of a frame has been transmitted or received, the SMC*n*INTF.WTEIF bit is set to 1 when the time set using the SMC*n*WTC(0/1).WTC[23:0] bits has elapsed from the beginning of the current frame.

14.6 Operations

14.6.1 Initialization

SMCIF Ch.*n* should be initialized with the procedure shown below.

1. Assign the SMCIF Ch.*n* input/output function to the ports (refer to the "I/O Ports" chapter).
2. Set the SMC*n*MOD.MST bit. (Select master/slave mode)
3. <Master mode only> Set the SMC*n*CLK.CLKSRC[1:0] and SMC*n*CLK.CLKDIV[1:0] bits. (Configure operating clock)
4. Configure the following SMC*n*MOD register bits:
   - SMC*n*MOD.OUTMD bit (Select SMCIO*n* pin open-drain/push-pull output mode)
   - SMC*n*MOD.CLKPOL bit (Select SMCCLK*n* pin level at master clock output disabled)
   - SMC*n*MOD.DIR bit (Select normal (LSB first)/reverse (MSB first) direction)
   - SMC*n*MOD.INV bit (Select non-inverted/inverted level)
   - SMC*n*MOD.PRY bit (Select even/odd parity)
5. Set the SMC*n*WTC(0/1).WTC[23:0] and SMC*n*GTC.GTC[7:0] bits. (Set wait time and guard time)
6. Set the SMC*n*BR.FDR[10:0]bits. (Set transfer rate)

7. Configure the following SMC*n*CTL register bits:
   - SMC*n*CTL.CRP bit (Enable/disable character retransmission requests)
   - Set the SMC*n*CTL.SFTRST bit to 1. (Execute software reset)
   - Set the SMC*n*CTL.MODEN bit to 1. (Enable SMCIF Ch.*n* operations)
8. Set the following bits when using the interrupt:
   - Write 1 to the interrupt flags in the SMC*n*INTF register. (Clear interrupt flags)
   - Set the interrupt enable bits in the SMC*n*INTE register to 1. * (Enable interrupts)

   * The initial value of the SMC*n*INTF.TBEIF bit is 1, therefore, an interrupt will occur immediately after the SMC*n*INTE.TBEIE bit is set to 1.

14.6.2 Data Transmission

A data transmission procedure and the SMCIF Ch.*n* operations are shown below.

Data transmission procedure

1. Set the SMC*n*MOD.PRT bit. (Select protocol mode)
2. Set the SMC*n*CTL.TXEN bit to 1. (Enable data transmission)
3. Check to see if the SMC*n*INTF.TBEIF bit is set to 1 (transmit buffer empty).
4. Write transmit data to the SMC*n*TXD register.
5. Wait for an SMCIF interrupt when using the interrupt.
6. Repeat Steps 3 to 5 (or 3 and 4) until the end of transmit data.

Data transmit operations

SMCIF Ch.*n* starts data transmit operations when transmit data is written to the SMC*n*TXD register.

Operations in T = 0 mode

The transmit data in the SMC*n*TXD register is automatically transferred to the shift register. At this time, the SMC*n*INTF.TBEIF bit still retains 1 (transmit buffer full).

The SMCIOn pin outputs a start bit and the SMC*n*INTF.TBSY bit is set to 1 (transmitter busy). The shift register data bits are then output successively according to the data transfer direction set by the SMC*n*MOD.DIR bit. Following output of data bits, the parity bit is output.

SMCIF Ch.*n* switches the SMCIO*n* pin to input mode for a duration of one etu from 10.5 to 11.5 etu after starting the start bit transmission to check whether the receiver has sent an error signal or not. If an error signal is detected, SMCIF Ch.*n* determines it as a retransmission request from the receiver; if no error signal is detected, SMCIF Ch.*n* determines that no retransmission request has been issued.

The SMC*n*INTF.TBEIF bit retains 0 while transmit data is being output from the SMCIO*n* pin. This indicates that the next transmit data cannot be written to the SMC*n*TXD register.

If no retransmission request has been issued (or regardless of whether a retransmission request has been issued or not when the SMC*n*CTL.CRP bit = 0), the SMC*n*INTF.TBSY bit is cleared to 0, the SMC*n*INTF.TENDIF bit is set to 1 (end of transmission), and the SMC*n*INTF.TBEIF bit is set to 1 (transmit buffer empty) after the error detection that follows the data transmission has finished. If a retransmission request has been issued when the SMC*n*CTL.CRP bit = 1, the transmit data in the SMC*n*TXD register is transferred to the shift register and the same data is transmitted again.

Example: T = 0 mode, GT = 16 (SMC*n*GTC.GTC[7:0] bits = 4), When no error signal is detected

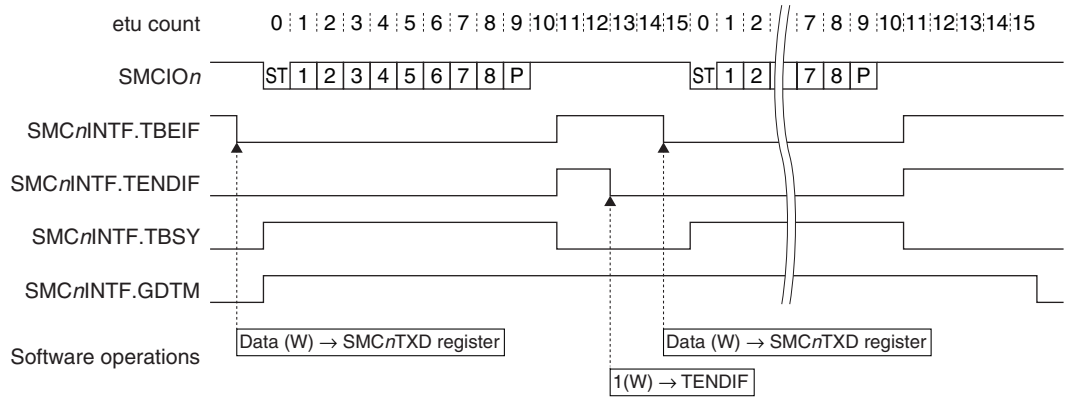
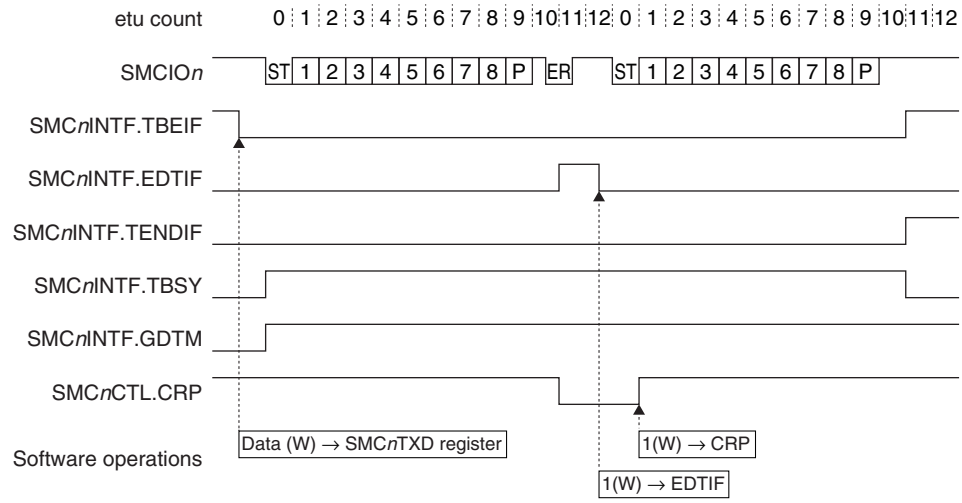


Figure 14.6.2.1 Data Transmit Operations in T = 0 Mode (when no error signal is detected)

Example: T = 0 mode, GT = 16 (SMCnGTC.GTC[7:0] bits = 4)*, Data is retransmitted as an error signal was detected.



* When an error is detected, the retransmission starts after 13 etu regardless of the guard time setting.

Figure 14.6.2.2 Data Transmit Operations in T = 0 Mode (when an error signal is detected)

When the SMC*n*CTL.CRP bit = 1, data is retransmitted if an error is detected after a data transmission has completed. At this time, the SMC*n*CTL.CRP bit is automatically cleared. When using the data retransmission function in the retransmission and subsequent transmissions, set the SMC*n*CTL.CRP bit to 1 again until the next error detection timing (11 etu). If an error has not been detected, the SMC*n*CTL.CRP bit is not cleared.

Operations in T = 1 mode

The transmit data in the SMC*n*TXD register is automatically transferred to the shift register and the SMC*n*INTF.TBEIF bit is set to 1 (transmit buffer empty).

The SMCIO*n* pin outputs a start bit and the SMC*n*INTF.TBSY bit is set to 1 (transmitter busy). The shift register data bits are then output successively according to the data transfer direction set by the SMC*n*MOD.DIR bit. Following output of data bits, the parity bit is output.

Even if transmit data is being output from the SMCIO*n* pin, the next transmit data can be written to the SMC*n*TXD register after making sure that the SMC*n*INTF.TBEIF bit is set to 1.

If no transmit data remains in the SMC*n*TXD register after data has been transmitted, the SMC*n*INTF.TBSY bit is cleared to 0 and the SMC*n*INTF.TENDIF bit is set to 1 (end of transmission).

Example: T = 1 mode, GT = 11 (SMC*n*GTC.GTC[7:0] bits = 255)

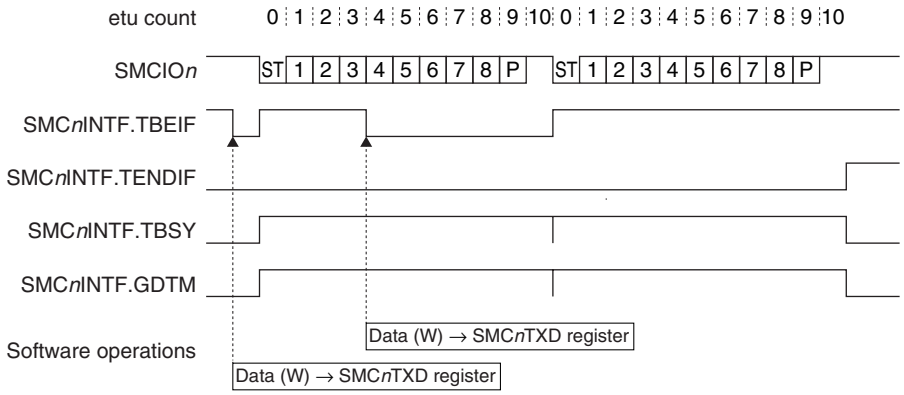


Figure 14.6.2.3 Data Transmission Operations in T = 1 Mode

14.6.3 Data Reception

A data reception procedure and the SMCIF Ch.*n* operations are shown below.

Data reception procedure

1. Set the SMC*n*MOD.PRT bit. (Select protocol mode)
2. Set the SMC*n*CTL.RXEN bit to 1. (Enable data reception)
3. Wait for an SMCIF interrupt when using the interrupt.
4. Check to see if the SMC*n*INTF.RB1FIF bit or SMC*n*INTF.RB2FIF bit is set to 1 (receive buffer full).
5. Read received data from the SMC*n*RXD register.
6. Repeat Steps 3 to 5 (or 4 and 5) until the end of receive data.

Data receive operations

When a start bit is input to the SMCIO*n* pin, SMCIF Ch.*n* detects it and starts data receive operations . At the same time, the SMC*n*INTF.RBSY bit is set to 1 (receiver busy).

The receiver circuit samples the eight data bits that follow the start bit assuming that they were transmitted in the data transfer direction set by the SMC*n*MOD, and loads them successively into the receive shift register. Following data bits, SMCIF Ch.*n* receives the parity bit and performs a parity check that compares the received parity bit with the parity bit generated from the received data.

After the parity bit is received, the received data in the receive shift register is transferred to the receive data buffer.

If a parity error has occurred, the SMC*n*INTF.PEIF bit is then set to 1. When the protocol mode is set to T = 0 and the SMC*n*CTL.CRP bit is set to 1, a low level error signal is output from the SMCIO*n* pin for a duration of one etu from 10.5 to 11.5 etu after the start bit was detected. This informs the transmitter that a parity error has occurred and requests to retransmit the data.

The receive data buffer consists of a 2-byte FIFO and receives data until it becomes full. When the receive data buffer receives the first data, the SMC*n*INTF.RB1FIF bit is set to 1 (receive buffer one byte full). If the second data is received before the first data is read, the SMC*n*INTF.RB2FIF bit is set to 1 (receive buffer two bytes full).

The SMC*n*INTF.RBSY bit is cleared to 0 at the end of the guard time after data has been received and a receive operation is completed. After that, if the start bit of the next data cannot be detected within the period set by the SMC*n*WTC(0/1).WTC[23:0] bits, a wait time error occurs and the SMC*n*INTF.WTEIF bit is set to 1.

Example: T = 0 mode, When no parity error has occurred (or T = 1 mode)

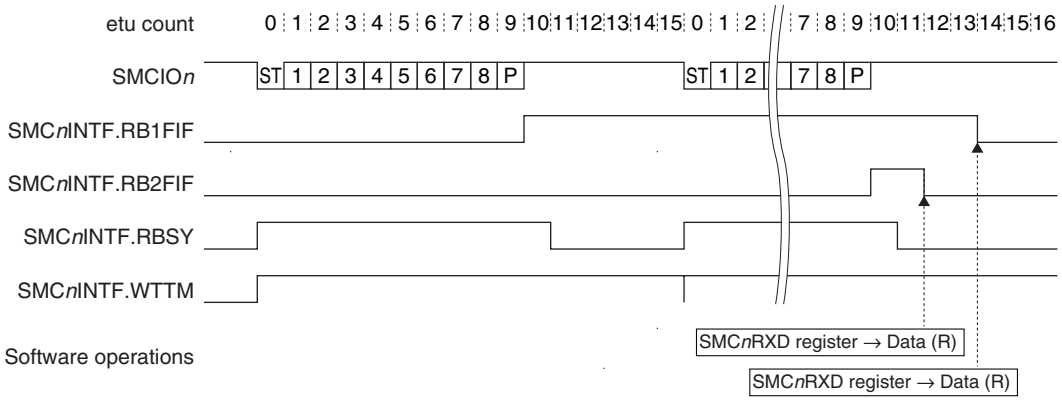


Figure 14.6.3.1 Data Receive Operations (when no error signal is output)

Example: T = 0 mode, A parity error has occurred and retransmitted data is received.

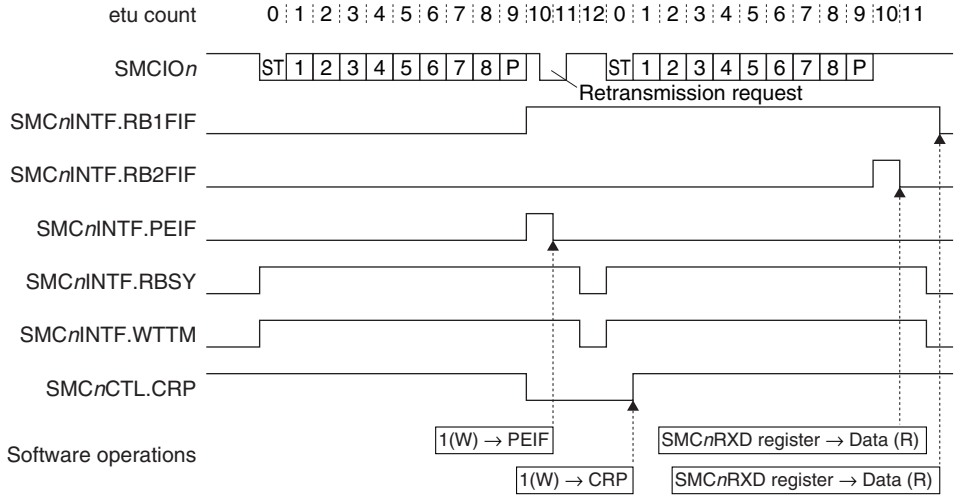


Figure 14.6.3.2 Data Receive Operations (when an error signal is output)

When the SMC*n*CTL.CRP bit = 1, SMCIF Ch.*n* issues a character retransmission request and clears the SMC*n*CTL.CRP bit if a parity error is detected. When using the retransmission request function in the subsequent receptions including the reception for the retransmit data, set the SMC*n*CTL.CRP bit to 1 again until the next parity bit reception timing. If no parity error has been detected, the SMC*n*CTL.CRP bit is not cleared.

14.7 Interrupts

The SMCIF has a function to generate the interrupts shown in Table 14.7.1.

Table 14.7.1 SMCIF Interrupt Function

Interrupt	Interrupt flag	Set condition	Clear condition
Wait time error	SMC*n*INTF.WTEIF	When the time set using the SMC*n*WTC(0/1).WTC[23:0] bits has elapsed Refer to Section 14.5, "Guard Time and Wait Time Settings."	Writing 1 or software reset
End of transmission	SMC*n*INTF.TENDIF	When the transmission is in pause state and the SMC*n*INTE.TBEIF bit = 1	Writing 1 or software reset
Error signal detection	SMC*n*INTF.EDTIF	When an error signal sent from the receiver is detected	Writing 1 or software reset
Parity error	SMC*n*INTF.PEIF	When the parity check determines that the received parity bit is different from the parity bit generated from the received data in the configured parity mode (even or odd)	Writing 1 or software reset
Overrun error	SMC*n*INTF.OEIF	When the receive data buffer is full (the received data has not been read) after data is received in the shift register	Writing 1 or software reset
Receive buffer two bytes full	SMC*n*INTF.RB2FIF	When the second received data byte is loaded to the receive data buffer in which the first byte is already received	Reading the SMC*n*RXD register or software reset
Receive buffer one byte full	SMC*n*INTF.RB1FIF	When the first received data byte is loaded to the emptied receive data buffer	Reading the SMC*n*RXD register to empty the receive data buffer or software reset
Transmit buffer empty	SMC*n*INTF.TBEIF	When transmit data written to the transmit data buffer is transferred to the shift register	Writing to the SMC*n*TXD register

The SMCIF provides interrupt enable bits corresponding to each interrupt flag. An interrupt request is sent to the interrupt controller only when the interrupt flag, of which interrupt has been enabled by the interrupt enable bit, is set. For more information on interrupt control, refer to the "Interrupt Controller" chapter.

14.8 Control Registers

SMCIF Ch.*n* Clock Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SMC*n*CLK	15–9	–	0x00	–	R	–
	8	DBRUN	0	H0	R/W	
	7–6	–	0x0	–	R	
	5–4	CLKDIV[1:0]	0x0	H0	R/W	
	3–2	–	0x0	–	R	
	1–0	CLKSRC[1:0]	0x0	H0	R/W	

Bits 15–9 Reserved

Bit 8 DBRUN

This bit sets whether the SMCIF operating clock is supplied in DEBUG mode or not.

1 (R/W): Clock supplied in DEBUG mode

0 (R/W): No clock supplied in DEBUG mode

Bits 7–6 Reserved

Bits 5–4 CLKDIV[1:0]

These bits select the division ratio of the SMCIF operating clock.

Bits 3–2 Reserved

Bits 1–0 CLKSRC[1:0]

These bits select the clock source of SMCIF.

Table 14.8.1 Clock Source and Division Ratio Settings

SMC*n*CLK. CLKDIV[1:0] bits	SMC*n*CLK.CLKSRC[1:0] bits			
	0x0	0x1	0x2	0x3
	IOSC	OSC1	OSC3	EXOSC
0x3	1/8	1/1	1/8	1/1
0x2	1/4		1/4	
0x1	1/2		1/2	
0x0	1/1		1/1	

(Note) The oscillation circuits/external input that are not supported in this IC cannot be selected as the clock source.

Note: The SMC*n*CLK register settings can be altered only when the SMC*n*CTL.MODEN bit = 0.

SMCIF Ch.*n* Mode Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SMC*n*MOD	15–8	–	0x00	–	R	–
	7	PRT	0	H0	R/W	
	6	PRY	0	H0	R/W	
	5	INV	0	H0	R/W	
	4	DIR	0	H0	R/W	
	3	–	0	–	R	
	2	OUTMD	1	H0	R/W	
	1	CLKPOL	0	H0	R/W	
	0	MST	1	H0	R/W	

Bits 15–8 Reserved

Bit 7 PRT

This bit selects the protocol mode.

1 (R/W): T = 1 mode

0 (R/W): T = 0 mode

Bit 6 PRY

This bit selects the parity mode.

1 (R/W): Odd parity mode

0 (R/W): Even parity mode

Bit 5 INV

This bit sets the SMCIO*n* pin data input/output level.

1 (R/W): Inverted input/output

0 (R/W): Non-inverted input/output

Bit 4 DIR

This bit sets the SMCIO*n* pin data input/output direction.

1 (R/W): MSB first

0 (R/W): LSB first

Bit 3 Reserved

Bit 2 OUTMD

This bit sets the SMCIO*n* pin output mode.

1 (R/W): Open drain output

0 (R/W): Push-pull output

Bit 1 CLKPOL

This bit sets the SMCCLK*n* pin level when the clock output is disabled. This bit is effective only in master mode.

1 (R/W): High level

0 (R/W): Low level

Bit 0 MST

This bit selects master or slave mode.

1 (R/W): Master mode

0 (R/W): Slave mode

Note: Do not alter the SMC*n*MOD register settings when the SMC*n*INTF.RBSY or SMC*n*INTF.TBSY bit is set to 1.

SMCIF Ch.*n* Baud Rate Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SMC*n*BR	15–11	–	0x00	–	R	–
	10–0	FDR[10:0]	0x173	H0	R/W	

Bits 15–11 Reserved

Bits 10–0 FDR[10:0]

These bits set the transfer rate for SMCIF Ch.*n*. Table 14.8.2 lists the SMC*n*MOD.FDR[10:0] bit setting values corresponding to the parameters F and D. For more information, refer to Section 14.3.5, "Baud Rate Generator Settings."

Table 14.8.2 Corresponding Between SMC*n*MOD.FDR[10:0] Bit Settings and Parameters (F, D)

SMC*n*BR.FDR[10:0] bits		D								
		1	2	4	8	16	32	64	12	20
F	**372**	0x173	0x0b9	0x05c	0x02e				0x01e	
	558	0x22d	0x116	0x08b	0x045	0x022			0x02e	0x01b
	744	0x2e7	0x173	0x0b9	0x05c	0x02e			0x03d	
	1,116	0x45b	0x22d	0x116	0x08b	0x045	0x022		0x05c	0x037
	1,488	0x5cf	0x2e7	0x173	0x0b9	0x05c	0x02e		0x07b	0x04a
	1,860	0x743	0x3a1	0x1d0	0x0e8	0x074	0x03a		0x09a	0x05c
	512	0x1ff	0x0ff	0x07f	0x03f	0x01f	0x00f	0x007	0x02a	0x019
	768	0x2ff	0x17f	0x0bf	0x05f	0x02f	0x017	0x00b	0x03f	0x026
	1,024	0x3ff	0x1ff	0x0ff	0x07f	0x03f	0x01f	0x00f	0x055	0x033
	1,536	0x5ff	0x2ff	0x17f	0x0bf	0x05f	0x02f	0x017	0x07f	0x04c
	2,048	0x7ff	0x3ff	0x1ff	0x0ff	0x07f	0x03f	0x01f	0x0aa	0x066

SMCIF Ch.*n* Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SMC*n*CTL	15–12	–	0x0	–	R	–
	11	ICNT	0	H0	R/W	
	10	CLKOUT	0	H0	R/W	
	9	RXEN	0	H0	R/W	
	8	TXEN	0	H0	R/W	
	7–5	–	0x0	–	R	
	4	CRP	0	H0	R/W	
	3–2	–	0x0	–	R	
	1	SFTRST	0	H0	R/W	
	0	MODEN	0	H0	R/W	

Bits 15–12 Reserved

Bit 11 ICNT

This bit starts a clock count operation using the wait time counter.

1 (W): Start counting

0 (W): Stop counting

1 (R): During counting

0 (R): Counting stopped

This bit is provided for slave mode to count clocks at cold reset (at power on). Setting this bit to 1 starts counting the wait time the same as the start bit detection operation. By setting the SMC*n*BR.FDR[10:0] and SMC*n*WTC(0/1).WTC[23:0] bits before setting this bit to 1, a wait time error interrupt occurs when the desired time has elapsed. This bit is effective only when the SMC*n*CTL.RXEN bit = 0.

Bit 10 CLKOUT

This bit controls the clock output from the SMCCLK*n* pin.

1 (R/W): Clock is output.
0 (R/W): Clock is stopped.

Bit 9 RXEN

This bit enables or disables data receive operations.

1 (R/W): Enable data reception
0 (R/W): Disable data reception

Setting this bit to 1 starts the start bit detection operation.

Bit 8 TXEN

This bit enables or disables data transmit operations.

1 (R/W): Enable data transmission
0 (R/W): Disable data transmission

Writing data to the transmit data buffer after setting this bit to 1 starts data transmission from the SMCIO*n* pin.

Bits 7–5 Reserved

Bit 4 CRP

This bit enables or disables the data retransmission and retransmission request functions when an error has been detected. This bit is effective only in T = 0 mode.

For data reception

1 (R/W): Enable data retransmission request signal issuance*1
0 (R/W): Disable data retransmission request signal issuance

*1 If a parity error is detected during data reception, SMCIF Ch.*n* issues a data retransmission request signal. This bit is automatically cleared to 0 after the data retransmission request signal has been issued.

For data transmission

1 (R/W): Enable error signal detection and data retransmission*2
0 (R/W): Disable error signal detection and data retransmission

*2 If an error signal is detected after data has been transmitted, SMCIF Ch.*n* retransmits the same data. This bit is automatically cleared to 0 after the data retransmission has finished.

Bits 3–2 Reserved

Bit 1 SFTRST

This bit issues software reset to SMCIF.

1 (W): Issue software reset
0 (W): Ineffective
1 (R): Software reset is executing.
0 (R): Software reset has finished. (During normal operation)

Setting this bit to 1 resets the SMCIF transmit/receive control circuit and interrupt flags. This bit is automatically cleared to 0 after the reset processing has finished.

Bit 0 MODEN

This bit enables the SMCIF operations.

1 (R/W): Enable SMCIF operations (The operating clock is supplied.)

0 (R/W): Disable SMCIF operations (The operating clock is stopped.)

Note: If the SMC*n*CTL.MODEN bit is altered from 1 to 0 while transmitting/receiving data, the data being transmitted/received cannot be guaranteed. When setting the SMC*n*CTL.MODEN bit to 1 again after that, be sure to write 1 to the SMC*n*CTL.SFTRST bit as well.

SMCIF Ch.*n* Transmit Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SMC*n*TXD	15–8	–	0x00	–	R	–
	7–0	TXD[7:0]	0x00	H0	R/W	

Bits 15–8 Reserved

Bits 7–0 TXD[7:0]

Data can be written to the transmit data buffer through these bits. Make sure the SMC*n*INTF.TBEIF bit is set to 1 before writing data.

Note: Data can be written to this register only when the SMC*n*CTL.MODEN and SMC*n*CTL.TXEN bits are both set to 1.

SMCIF Ch.*n* Receive Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SMC*n*RXD	15–9	–	0x00	–	R	–
	8	RXP	0	H0	R	
	7–0	RXD[7:0]	0x00	H0	R	

Bits 15–9 Reserved

Bit 8 RXP

This bit indicates the parity check results of the received data.

1 (R): Parity error occurred

0 (R): No parity error occurred

Bits 7–0 RXD[7:0]

The receive data buffer can be read through these bits. The receive data buffer consists of a 2-byte FIFO, and older received data is read first.

SMCIF Ch.*n* Wait Time Compare Data Register 0
SMCIF Ch.*n* Wait Time Compare Data Register 1

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SMC*n*WTC0	15–0	WTC[15:0]	0x0000	H0	R/W	–
SMC*n*WTC1	15–8	–	0x00	–	R	–
	7–0	WTC[23:16]	0x00	H0	R/W	

Bits 15–0 (SMC*n*WTC0 register), Bits 7–0 (SMC*n*WTC1 register) WTC[23:0]

These bits set the wait time in etu units.

The value set in these registers is compared with the etu counter value without being changed.

For more information on the wait time, refer to Section 14.5, "Guard Time and Wait Time Settings."

SMCIF Ch.*n* Guard Time Compare Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SMC*n*GTC	15–8	–	0x00	–	R	–
	7–0	GTC[7:0]	0x00	H0	R/W	

Bits 15–8 Reserved

Bits 7–0 GTC[7:0]

These bits set the guard time in etu units.
The guard time is set as shown below.

GT = GTC + 12 [etu] (Eq. 14.2)

Where

GT: Guard time (time between the first characters of a frame and the next frame in etu units)
GTC: SMC*n*GTC.GTC[7:0] bit setting value (0 to 254)

However, when GTC = 255, GT is set to 12 etu in T = 0 mode or is set to 11 etu in T = 1 mode.
For more information on the guard time, refer to Section 14.5, "Guard Time and Wait Time Settings."

SMCIF Ch.*n* Status and Interrupt Flag Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SMC*n*INTF	15–12	–	0x0	–	R	–
	11	WTTM	0	H0/S0	R	
	10	GDTM	0	H0/S0	R	
	9	RBSY	0	H0/S0	R	
	8	TBSY	0	H0/S0	R	
	7	WTEIF	0	H0/S0	R/W	Cleared by writing 1.
	6	TENDIF	0	H0/S0	R/W	
	5	EDTIF	0	H0/S0	R/W	
	4	PEIF	0	H0/S0	R/W	
	3	OEIF	0	H0/S0	R/W	
	2	RB2FIF	0	H0/S0	R	Cleared by reading the SMC*n*RXD register.
	1	RB1FIF	0	H0/S0	R	
	0	TBEIF	1	H0/S0	R	Cleared by writing to the SMC*n*TXD register.

Bits 15–12 Reserved

Bit 11 WTTM

This bit indicates the wait time measurement status of the etu counter.
1 (R): During measurement
0 (R): Idle

Bit 10 GDTM

This bit indicates the guard time measurement status of the etu counter.
1 (R): During measurement
0 (R): Idle

Bit 9 RBSY

This bit indicates the receive operation status. (See Figures 14.6.2.1 to 14.6.2.3.)
1 (R): During receiving
0 (R): Idle

Bit 8 TBSY

This bit indicates the transmit operation status. (See Figures 14.6.3.1 to 14.6.3.2.)
1 (R): During transmitting
0 (R): Idle

Bit 7 WTEIF
Bit 6 TENDIF
Bit 5 EDTIF
Bit 4 PEIF
Bit 3 OEIF
Bit 2 RB2FIF
Bit 1 RB1FIF
Bit 0 TBEIF

These bits indicate the SMCIF interrupt cause occurrence status.
1 (R): Cause of interrupt occurred
0 (R): No cause of interrupt occurred
1 (W): Clear flag
0 (W): Ineffective

The following shows the correspondence between the bit and interrupt:
SMC*n*INTF.WTEIF bit: Wait time error interrupt
SMC*n*INTF.TENDIF bit: End-of-transmission interrupt
SMC*n*INTF.EDTIF bit: Error signal detection interrupt
SMC*n*INTF.PEIF bit: Parity error interrupt
SMC*n*INTF.OEIF bit: Overrun error interrupt
SMC*n*INTF.RB2FIF bit: Receive buffer two bytes full interrupt
SMC*n*INTF.RB1FIF bit: Receive buffer one byte full interrupt
SMC*n*INTF.TBEIF bit: Transmit buffer empty interrupt

SMCIF Ch.*n* Interrupt Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SMC*n*INTE	15–8	–	0x00	–	R	–
	7	WTEIE	0	H0	R/W	
	6	TENDIE	0	H0	R/W	
	5	EDTIE	0	H0	R/W	
	4	PEIE	0	H0	R/W	
	3	OEIE	0	H0	R/W	
	2	RB2FIE	0	H0	R/W	
	1	RB1FIE	0	H0	R/W	
	0	TBEIE	0	H0	R/W	

Bits 15–8 Reserved

Bit 7 WTEIE
Bit 6 TENDIE
Bit 5 EDTIE
Bit 4 PEIE
Bit 3 OEIE
Bit 2 RB2FIE
Bit 1 RB1FIE
Bit 0 TBEIE

These bits enable SMCIF interrupts.
1 (R/W): Enable interrupts
0 (R/W): Disable interrupts

The following shows the correspondence between the bit and interrupt:
SMC*n*INTE.WTEIE bit: Wait time error interrupt
SMC*n*INTE.TENDIE bit: End-of-transmission interrupt
SMC*n*INTE.EDTIE bit: Error signal detection interrupt
SMC*n*INTE.PEIE bit: Parity error interrupt
SMC*n*INTE.OEIE bit: Overrun error interrupt
SMC*n*INTE.RB2FIE bit: Receive buffer two bytes full interrupt
SMC*n*INTE.RB1FIE bit: Receive buffer one byte full interrupt
SMC*n*INTE.TBEIE bit: Transmit buffer empty interrupt

SMCIF Ch.*n* Etu Counter Data Register 0
SMCIF Ch.*n* Etu Counter Data Register 1

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SMC*n*ETU0	15–0	ETUC[15:0]	0xffff	H0/S0	R	–
SMC*n*ETU1	15–8	–	0x00	–	R	–
	7–0	ETUC[23:16]	0xff	H0/S0	R	

Bits 15–0 (SMC*n*ETU0 register), Bits 7–0 (SMC*n*ETU1 register)

ETUC[23:0]

These bits show the current etu counter value.

Read these bits twice or more and determine that the read value is correct when the same value is read twice in succession.

15 16-bit PWM Timers (T16B)

15.1 Overview

T16B is a 16-bit PWM timer with comparator/capture functions. The features of T16B are listed below.

- Counter block
  - 16-bit up/down counter
  - A clock source and a clock division ratio for generating the count clock are selectable in each channel.
  - The count mode is configurable from combinations of up, down, or up/down count operations, and one-shot operations (counting for one cycle configured) or repeat operations (counting continuously until stopped via software).
  - Supports an event counter function using an external clock.
- Comparator/capture block
  - Supports up to six comparator/capture circuits to be included per one channel.
  - The comparator compares the counter value with the values specified via software to generate interrupt signals and a PWM waveform. (Can be used as an interval timer, PWM waveform generator, and external event counter.)
  - The capture circuit captures counter values using external/software trigger signals and generates interrupts. (Can be used to measure external event periods/cycles.)

Figure 15.1.1 shows the T16B configuration.

Table 15.1.1 T16B Channel Configuration of S1C17F63

Item	S1C17F63
Number of channels	2 channels (Ch.0 and Ch.1)
Event counter function	Ch.0: EXCL00 or EXCL01 pin input Ch.1: EXCL10 or EXCL11 pin input
Number of comparator/ capture circuits per channel	2 systems (0 and 1)
Timer generating signal output	Ch.0: TOUT00 and TOUT01 pin outputs (2 systems) Ch.1: TOUT10 and TOUT11 pin outputs (2 systems)
Capture signal input	Ch.0: CAP00 and CAP01 pin inputs (2 systems) Ch.1: CAP10 and CAP11 pin inputs (2 systems)

Note: In this chapter, '*n*' refers to a channel number, and '*m*' refers to an input/output pin number or a comparator/capture circuit number in a channel.

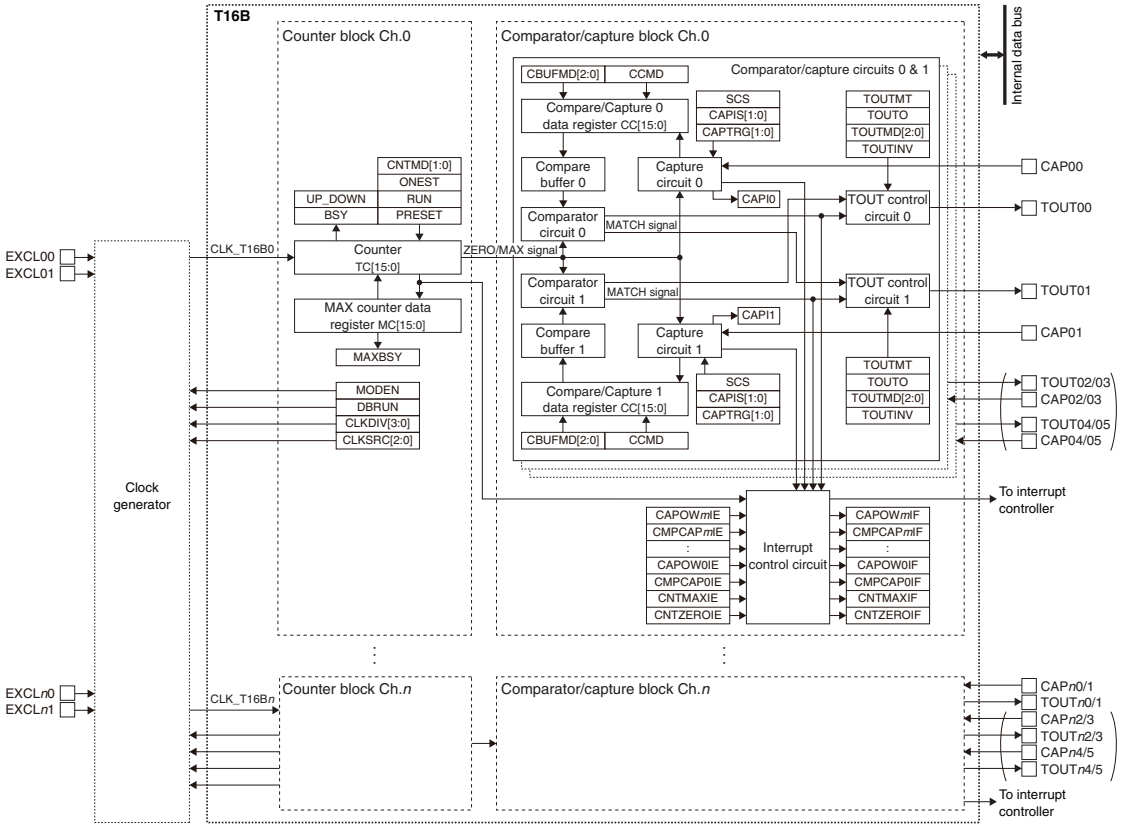


Figure 15.1.1 T16B Configuration

15.2 Input/Output Pins

Table 15.2.1 lists the T16B pins.

Table 15.2.1 List of T16B Pins

Pin name	I/O*	Initial status*	Function
EXCL*nm*	I	I (Hi-Z)	External clock input
TOUT*nm*/CAP*nm*	O or I	O (L)	TOUT signal output (in comparator mode) or capture trigger signal input (in capture mode)

* Indicates the status when the pin is configured for T16B.

If the port is shared with the T16B pin and other functions, the T16B input/output function must be assigned to the port before activating T16B. For more information, refer to the "I/O Ports" chapter.

15.3 Clock Settings

15.3.1 T16B Operating Clock

When using T16B Ch.*n*, the T16B Ch.*n* operating clock CLK_T16B*n* must be supplied to T16B Ch.*n* from the clock generator. The CLK_T16B*n* supply should be controlled as in the procedure shown below.

1. Enable the clock source in the clock generator if it is stopped (refer to "Clock Generator" in the "Power Supply, Reset, and Clocks" chapter).

   When an external clock is used, select the EXCL*nm* pin function (refer to the "I/O Ports" chapter).
2. Set the following T16B*n*CLK register bits:
   - T16B*n*CLK.CLKSRC[2:0] bits (Clock source selection)
   - T16B*n*CLK.CLKDIV[3:0] bits (Clock division ratio selection = Clock frequency setting)

15.3.2 Clock Supply in SLEEP Mode

When using T16B during SLEEP mode, the T16B operating clock CLK_T16B*n* must be configured so that it will keep supplying by writing 0 to the CLGOSC.*xxxx*SLPC bit for the CLK_T16B*n* clock source.
If the CLGOSC.*xxxx*SLPC bit for the CLK_T16B*n* clock source is 1, the CLK_T16B*n* clock source is deactivated during SLEEP mode and T16B stops with the register settings and counter value maintained at those before entering SLEEP mode. After the CPU returns to normal mode, CLK_T16B*n* is supplied and the T16B operation resumes.

15.3.3 Clock Supply in DEBUG Mode

The CLK_T16B*n* supply during DEBUG mode should be controlled using the T16B*n*CLK.DBRUN bit.
The CLK_T16B*n* supply to T16B Ch.*n* is suspended when the CPU enters DEBUG mode if the T16B*n*CLK.DBRUN bit = 0. After the CPU returns to normal mode, the CLK_T16B*n* supply resumes. Although T16B Ch.*n* stops operating when the CLK_T16B*n* supply is suspended, the counter and registers retain the status before DEBUG mode was entered. If the T16B*n*CLK.DBRUN bit = 1, the CLK_T16B*n* supply is not suspended and T16B Ch.*n* will keep operating in DEBUG mode.

15.3.4 Event Counter Clock

When EXCL*nm* is selected as the clock source using the T16B*n*CLK.CLKSRC[2:0] bits, the channel functions as a timer or event counter that counts the EXCL*nm* pin input clocks.
The counter counts rising edges of the input signal. This can be changed so that the counter will count falling edges of the original signal by selecting EXCL*nm* inverted input as the clock source.

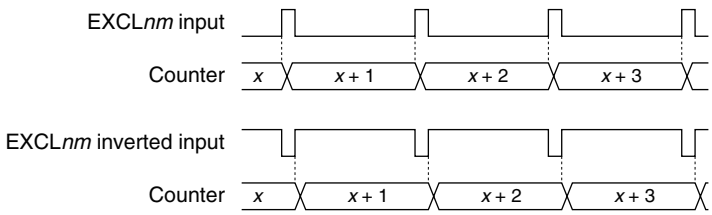


Figure 15.3.4.1 Count Timing (During Count Up Operation)

Note: When running the counter using the event counter clock, two dummy clocks must be input before the first counting up/down can be performed.

15.4 Operations

15.4.1 Initialization

T16B Ch.*n* should be initialized and started counting with the procedure shown below. Perform initial settings for comparator mode when using T16B as an interval timer, PWM waveform generator, or external event counter. Perform initial settings for capture mode when using T16B to measure external event periods/cycles.

Initial settings for comparator mode

1. Configure the T16B Ch.*n* operating clock.
2. Set the T16B*n*CTL.MODEN bit to 1. (Enable T16B operations)
3. Set the following T16B*n*CCCTL0 and T16B*n*CCCTL1 register bits:
   - Set the T16B*n*CCCTL*m*.CCMD bit to 0. * (Set comparator mode)
   - T16B*n*CCCTL*m*.CBUFMD[2:0] bits (Configure compare buffer)

   * Another circuit in the comparator/capture circuit pair (circuits 0 and 1, 2 and 3, 4 and 5) can be set to capture mode.

   Set the following bits when the TOUT*nm* output is used.
   - T16B*n*CCCTL*m*.TOUTMT bit (Select waveform generation signal)
   - T16B*n*CCCTL*m*.TOUTMD[2:0] bits (Select TOUT signal generation mode)
   - T16B*n*CCCTL*m*.TOUTINV bit (Select TOUT signal polarity)
4. Set the T16B*n*MC register. (Set MAX counter data)
5. Set the T16B*n*CCR0 and T16B*n*CCR1 registers. (Set the counter comparison value)
6. Set the following bits when using the interrupt:
   - Write 1 to the interrupt flags in the T16B*n*INTF register. (Clear interrupt flags)
   - Set the interrupt enable bits in the T16B*n*INTE register to 1. (Enable interrupts)
7. Set the following T16B*n*CTL register bits:
   - T16B*n*CTL.CNTMD[1:0] bits (Select count up/down operation)
   - T16B*n*CTL.ONEST bit (Select one-shot/repeat operation)
   - Set the T16B*n*CTL.PRESET bit to 1. (Reset counter)
   - Set the T16B*n*CTL.RUN bit to 1. (Start counting)

Initial settings for capture mode

1. Configure the T16B Ch.*n* operating clock.
2. Set the T16B*n*CTL.MODEN bit to 1. (Enable T16B operations)
3. Set the following T16B*n*CCCTL0 and T16B*n*CCCTL1 register bits:
   - Set the T16B*n*CCCTL*m*.CCMD bit to 1. * (Set capture mode)
   - T16B*n*CCCTL*m*.SCS bit (Set synchronous/asynchronous mode)
   - T16B*n*CCCTL*m*.CAPIS[1:0] bits (Set trigger signal)
   - T16B*n*CCCTL*m*.CAPTRG[1:0] bits (Select trigger edge)

   * Another circuit in the comparator/capture circuit pair (circuits 0 and 1, 2 and 3, 4 and 5) can be set to comparator mode.
4. Set the T16B*n*MC register. (Set MAX counter data)
5. Set the following bits when using the interrupt:
   - Write 1 to the interrupt flags in the T16B*n*INTF register. (Clear interrupt flags)
   - Set the interrupt enable bits in the T16B*n*INTE register to 1. (Enable interrupts)
6. Set the following T16B*n*CTL register bits:
   - T16B*n*CTL.CNTMD[1:0] bits (Select count up/down operation)
   - T16B*n*CTL.ONEST bit (Select one-shot/repeat operation)
   - Set the T16B*n*CTL.PRESET bit to 1. (Reset counter)
   - Set the T16B*n*CTL.RUN bit to 1. (Start counting)

15.4.2 Counter Block Operations

The counter in each counter block channel is a 16-bit up/down counter that counts the selected operating clock (count clock).

Count mode

The T16B*n*CTL.CNTMD[1:0] bits allow selection of up, down, and up/down mode. The T16B*n*CTL.ONEST bit allows selection of repeat and one-shot mode. The counter operates in six counter modes specified with a combination of these modes.

Repeat mode enables the counter to continue counting until stopped via software. Select this mode to generate periodic interrupts at desired intervals or to generate timer output waveforms.

One-shot mode enables the counter to stop automatically. Select this mode to stop the counter after an interrupt has occurred once, such as for measuring pulse width or external event intervals and checking a specific lapse of time.

Up, down, and up/down mode configures the counter as an up counter, down counter and up/down counter, respectively.

MAX counter data register

The MAX counter data register (T16B*n*MC.MC[15:0] bits) is used to set the maximum value of the counter (hereafter referred to as MAX value). This setting limits the count range to 0x0000–MAX value and determines the count and interrupt cycles. When the counter is set to repeat mode, the MAX value can be rewritten in the procedure shown below even if the counter is running.

1. Check to see if the T16B*n*CTL.MAXBSY bit is set to 0.
2. Write the MAX value to the T16B*n*MC.MC[15:0] bits.

Note: When rewriting the MAX value, the new MAX value should be written after the counter has been reset to the previously set MAX value.

Counter reset

Setting the T16B*n*CTL.PRESET bit to 1 resets the counter. This clears the counter to 0x0000 in up or up/down mode, or presets the MAX value to the counter in down mode.

The counter is also cleared to 0x0000 when the counter value exceeds the MAX value during count up operation.

Counting start

To start counting, set the T16B*n*CTL.RUN bit to 1. The counting stop control depends on the count mode set.

Counter value read

The counter value can be read out from the T16B*n*TC.TC[15:0] bits. However, since T16B operates on CLK_T16B*n*, one of the operations shown below is required to read correctly by the CPU.

- Read the counter value twice or more and check to see if the same value is read.
- Stop the timer and then read the counter value.

Counter status check

The counter operating status can be checked using the T16B*n*CS.BSY bit. The T16B*n*CS.BSY bit is set to 1 while the counter is running or 0 while the counter is idle.

The current count direction can also be checked using the T16B*n*CS.UP_DOWN bit. The T16B*n*CS.UP_DOWN bit is set to 1 during count up operation or 0 during count down operation.

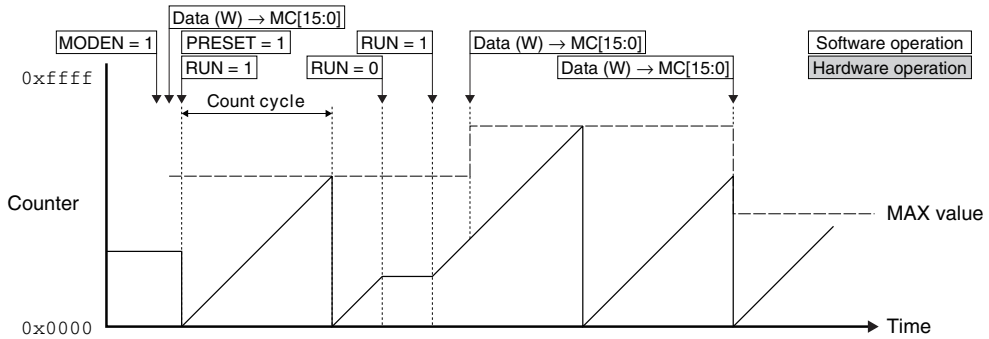
Operations in repeat up count and one-shot up count modes

In these modes, the counter operates as an up counter and counts from 0x0000 (or current value) to the MAX value.

In repeat up count mode, the counter returns to 0x0000 if it exceeds the MAX value and continues counting until the T16B*n*CTL.RUN bit is set to 0. If the MAX value is altered to a value larger than the current counter value during counting, the counter keeps counting up to the new MAX value. If the MAX value is altered to a value smaller than the current counter value, the counter is cleared to 0x0000 and continues counting up to the new MAX value.

In one-shot up count mode, the counter returns to 0x0000 if it exceeds the MAX value and stops automatically at that point.

(1) Repeat up count mode



(2) One-shot up count mode

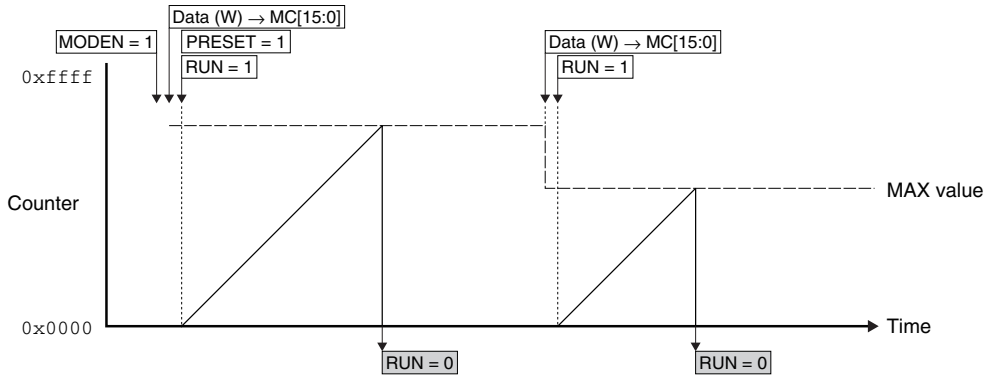


Figure 15.4.2.1 Operations in Repeat Up Count and One-shot Up Count Modes

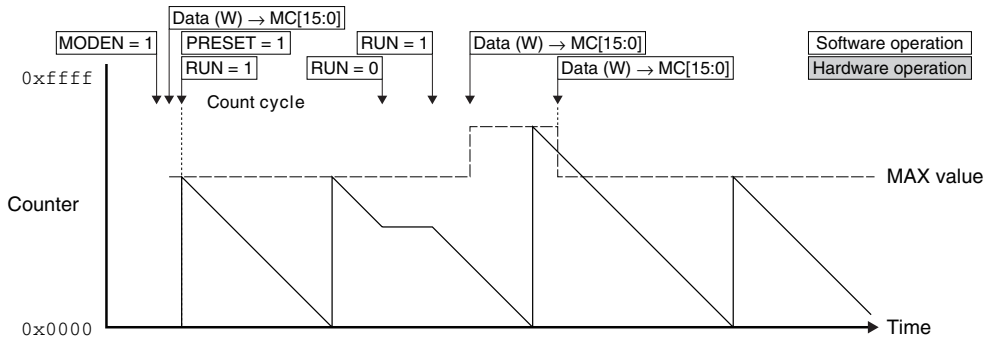
Operations in repeat down count and one-shot down count modes

In these modes, the counter operates as a down counter and counts from the MAX value (or current value) to 0x0000.

In repeat down count mode, the counter returns to the MAX value if a counter underflow occurs and continues counting until the T16B*n*CTL.RUN bit is set to 0. If the MAX value is altered during counting, the counter keeps counting down to 0x0000 and continues counting down from the new MAX value after a counter underflow occurs.

In one-shot down count mode, the counter returns to the MAX value if a counter underflow occurs and stops automatically at that point.

(1) Repeat down count mode



(2) One-shot down count mode

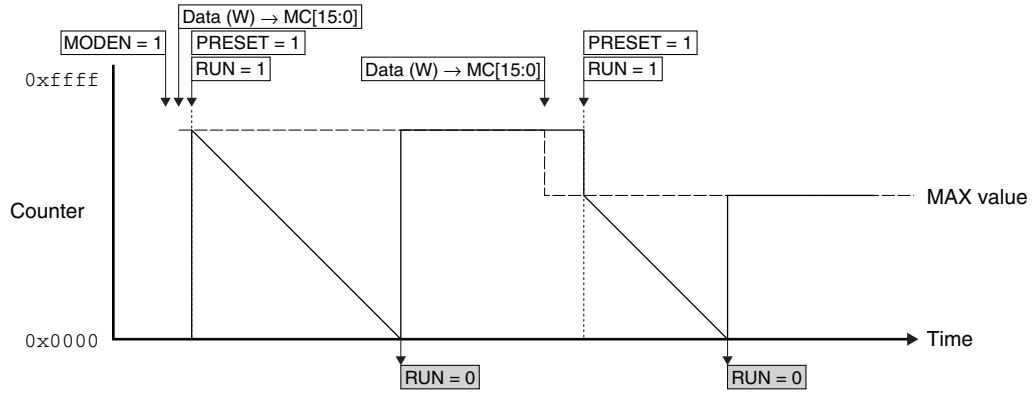


Figure 15.4.2.2 Operations in Repeat Down Count and One-shot Down Count Modes

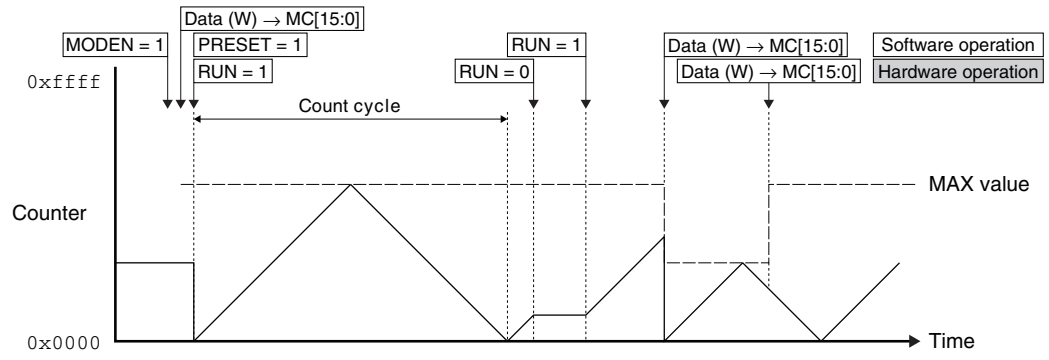
Operations in repeat up/down count and one-shot up/down count modes

In these modes, the counter operates as an up/down counter and counts as 0x0000 (or current value) → the MAX value → 0x0000.

In repeat up/down count mode, the counter repeats counting up from 0x0000 to the MAX value and counting down from the MAX value to 0x0000 until the T16B*n*CTL.RUN bit is set to 0. If the MAX value is altered to a value larger than the current counter value during count up operation, the counter keeps counting up to the new MAX value. If the MAX value is altered to a value smaller than the current counter value, the counter is cleared to 0x0000 and continues counting up to the new MAX value. If the MAX value is altered during count down operation, the counter keeps counting down to 0x0000 and then starts counting up to the new MAX value.

In one-shot up/down count mode, the counter stops automatically when it reaches 0x0000 during count down operation.

(1) Repeat up/down count mode



(2) One-shot up/down count mode

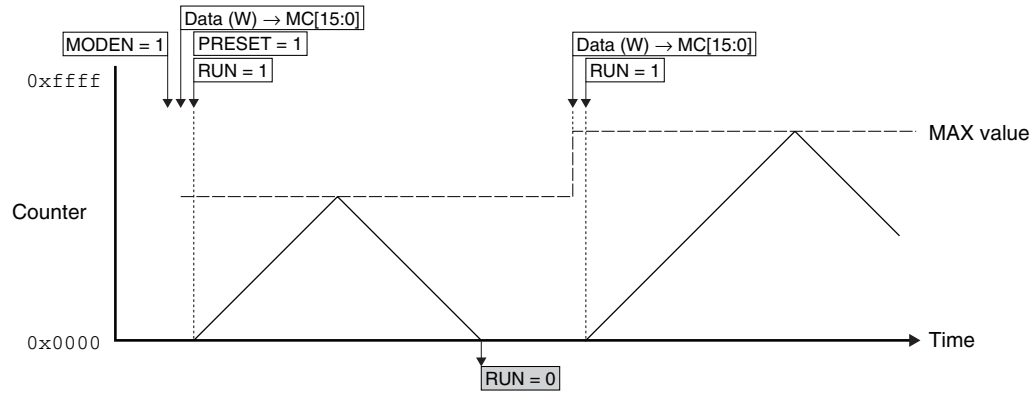


Figure 15.4.2.3 Operations in Repeat Up/Down Count and One-shot Up/Down Count Modes

15.4.3 Comparator/Capture Block Operations

The comparator/capture block functions as a comparator to compare the counter value with the register value set or a capture circuit to capture counter values using the external/software trigger signals.

Comparator/capture block operating mode

The comparator/capture block includes two systems (four or six systems) of comparator/capture circuits and each system can be set to comparator mode or capture mode, individually.

Set the T16B*n*CCCTL*m*.CCMD bit to 0 to set the comparator/capture circuit *m* to comparator mode or 1 to set it to capture mode.

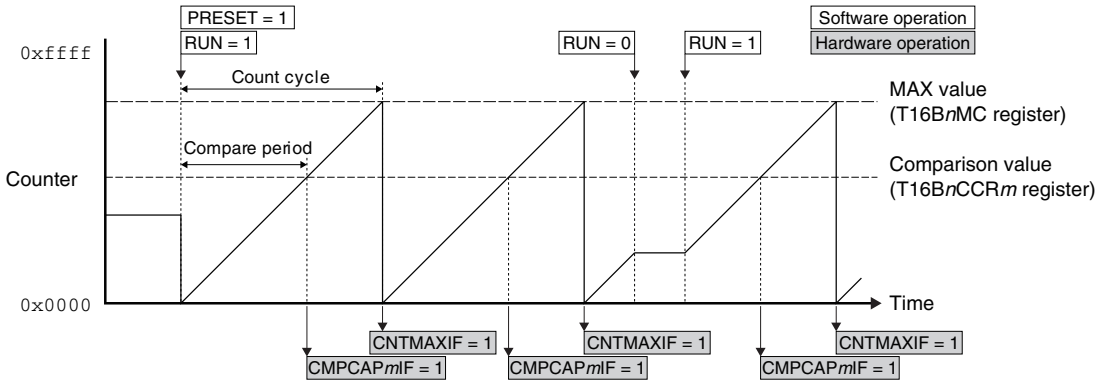
Operations in comparator mode

The comparator mode compares the counter value and the value set via software. It generates an interrupt and toggles the timer output signal level when the values are matched. The T16B*n*CCR*m* register functions as the compare data register used for setting a comparison value in this mode. The TOUT*nm*/CAP*nm* pin is configured to the TOUT*nm* pin.

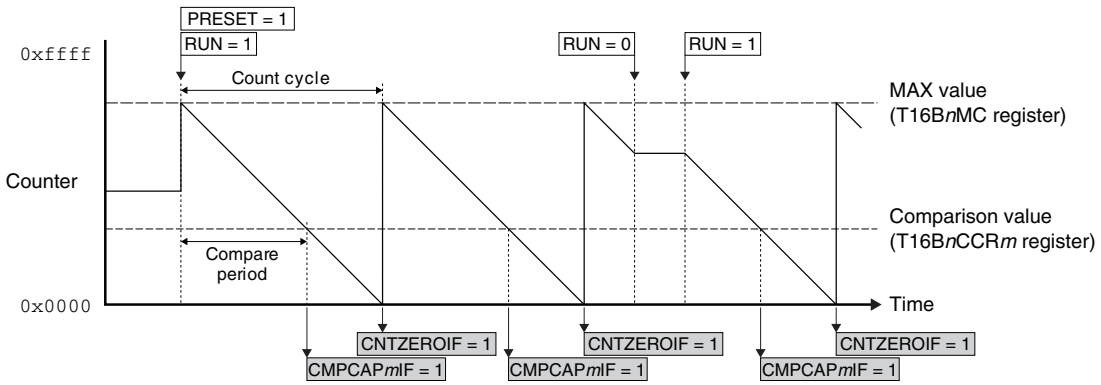
When the counter reaches the value set in the T16B*n*CCR*m* register during counting, the comparator asserts the MATCH signal and sets the T16B*n*INTF.COMPCAP*m*IF bit (compare interrupt flag) to 1.

When the counter reaches the MAX value in comparator mode, the T16B*n*INTF.CNTMAXIF bit (counter MAX interrupt flag) is set to 1. When the counter reaches 0x0000, the T16B*n*INTF.CNTZEROIF bit (counter zero interrupt flag) is set to 1.

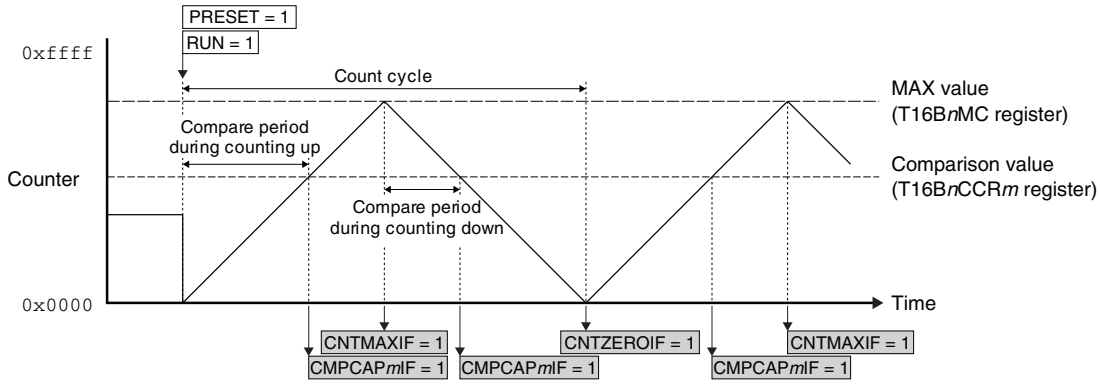
(1) Repeat up count mode



(2) Repeat down count mode



(3) Repeat up/down count mode



(Note that the T16B*n*INTF.CMPCAP*m*IF/CNTMAXIF/CNTZEROIF bit clearing operations via software are omitted from the figure.)

Figure 15.4.3.1 Operation Examples in Comparator Mode

The time from counter = 0x0000 or MAX value to occurrence of a compare interrupt (compare period) and the time to occurrence of a counter MAX or counter zero interrupt (count cycle) can be calculated as follows:

During counting up

$$\text{Compare period} = \frac{(CC + 1)}{f_{CLK\_T16B}} \text{ [s]} \qquad \text{Count cycle} = \frac{(MAX + 1)}{f_{CLK\_T16B}} \text{ [s]} \qquad \text{(Eq. 15.1)}$$

During counting down

$$\text{Compare period} = \frac{(MAX - CC + 1)}{f_{CLK\_T16B}} \text{ [s]} \qquad \text{Count cycle} = \frac{(MAX + 1)}{f_{CLK\_T16B}} \text{ [s]} \qquad \text{(Eq. 15.2)}$$

Where

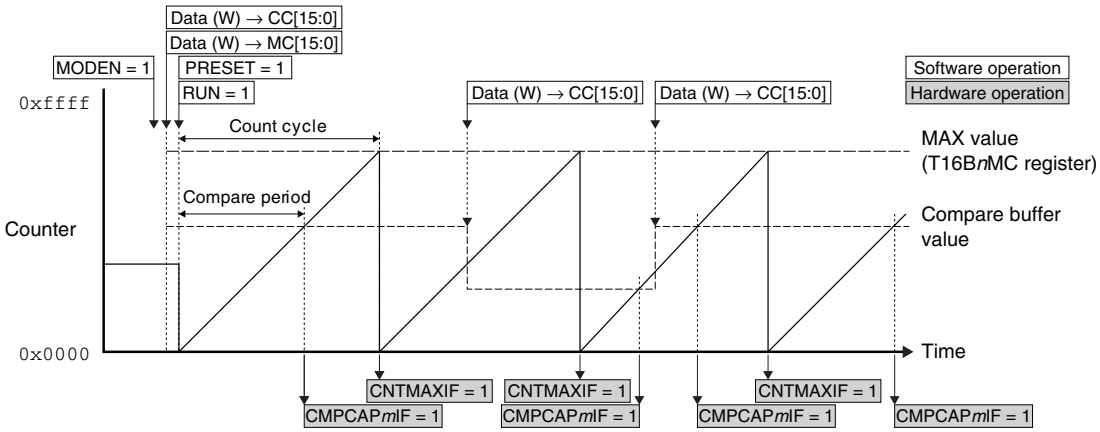
CC: T16B*n*CCR*m* register setting value (0 to 65,535)
MAX: T16B*n*MC register setting value (0 to 65,535)
f_{CLK_T16B}: Count clock frequency [Hz]

The comparator MATCH signal and counter MAX/ZERO signals are also used to generate a timer output waveform (TOUT). Refer to "TOUT Output Control" for more information.

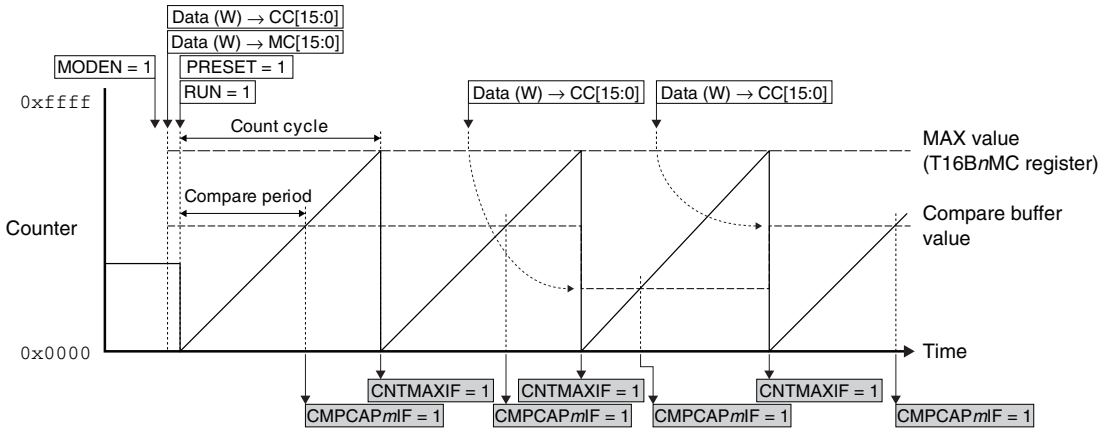
Compare buffer

The comparator loads the comparison value, which has been written to the T16B*n*CCR*m* register, to the compare buffer before comparing it with the counter value. For example, when generating a PWM waveform, the waveform with the desired duty ratio may not be generated if the comparison value is altered asynchronous to the count operation. To avoid this problem, the timing to load the comparison value to the compare buffer can be configured using the T16B*n*CCCTL*m*.CBUFMD[2:0] bits for synchronization with the count operation.

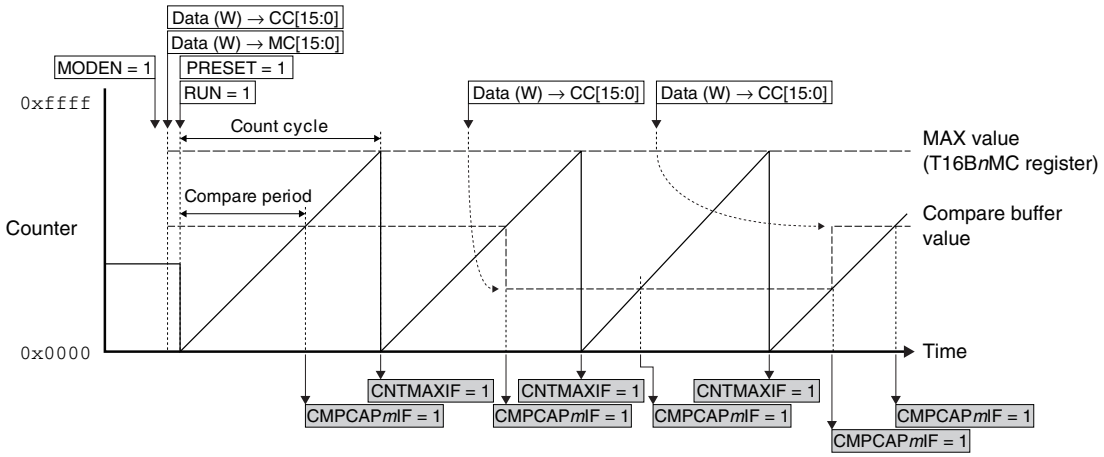
(1) Repeat up count mode
(1.1) T16B*n*CCCTL*m*.CBUFMD[2:0] bits = 0x0



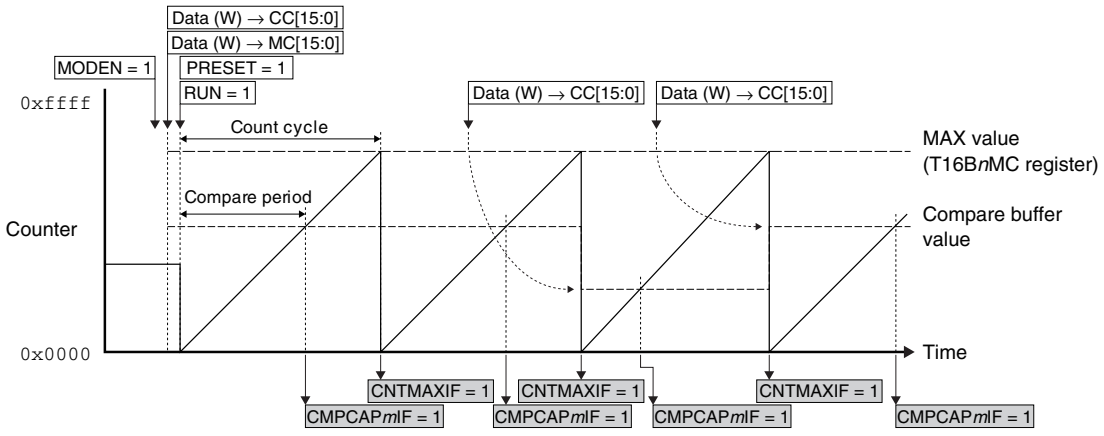
(1.2) T16B*n*CCCTL*m*.CBUFMD[2:0] bits = 0x1



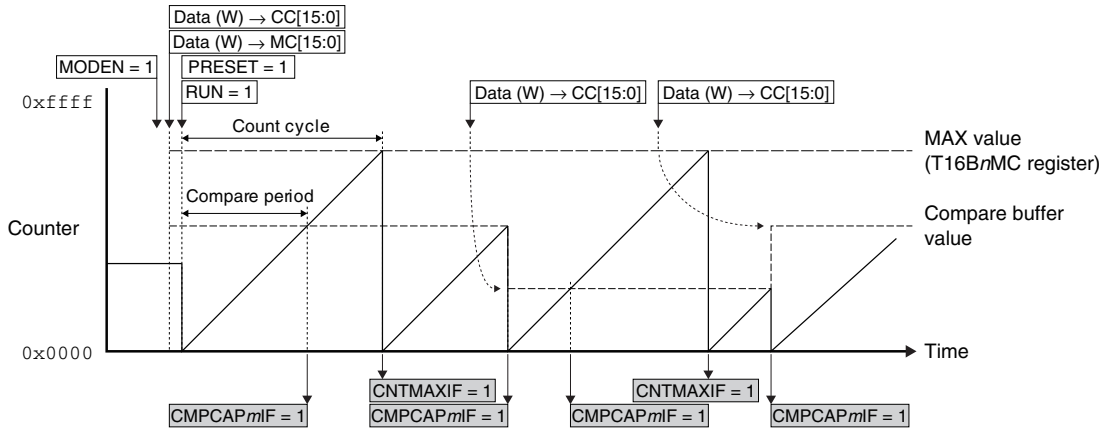
(1.3) T16B*n*CCCTL*m*.CBUFMD[2:0] bits = 0x2



(1.4) T16B*n*CCCTL*m*.CBUFMD[2:0] bits = 0x3

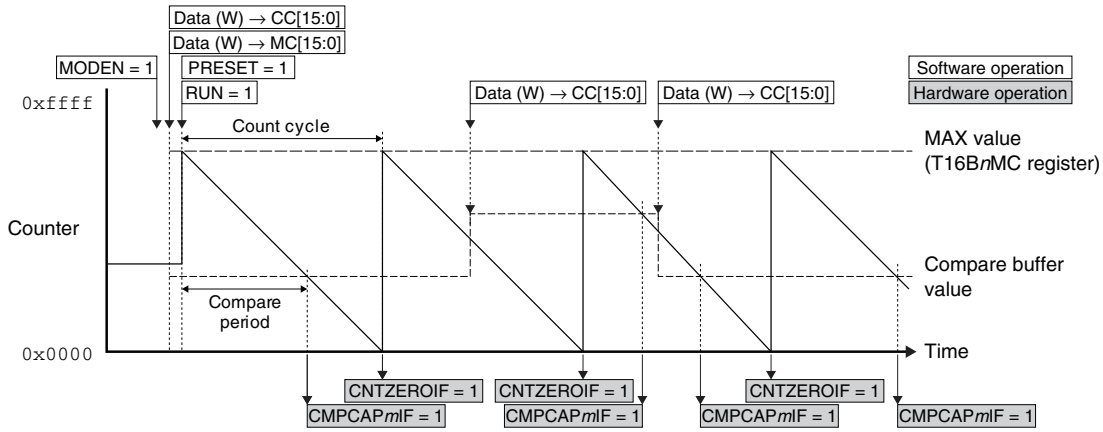


(1.5) T16B*n*CCCTL*m*.CBUFMD[2:0] bits = 0x4

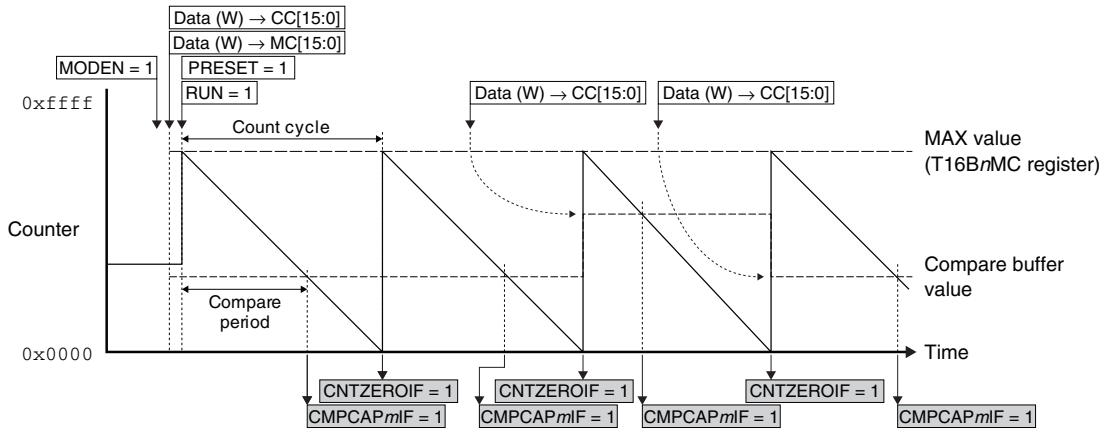


(2) Repeat down count mode

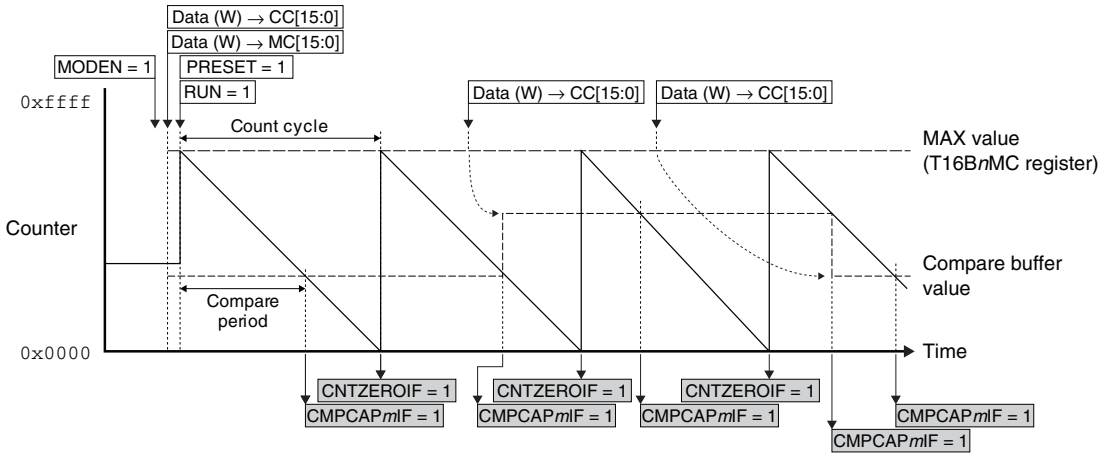
(2.1) T16B*n*CCCTL*m*.CBUFMD[2:0] bits = 0x0



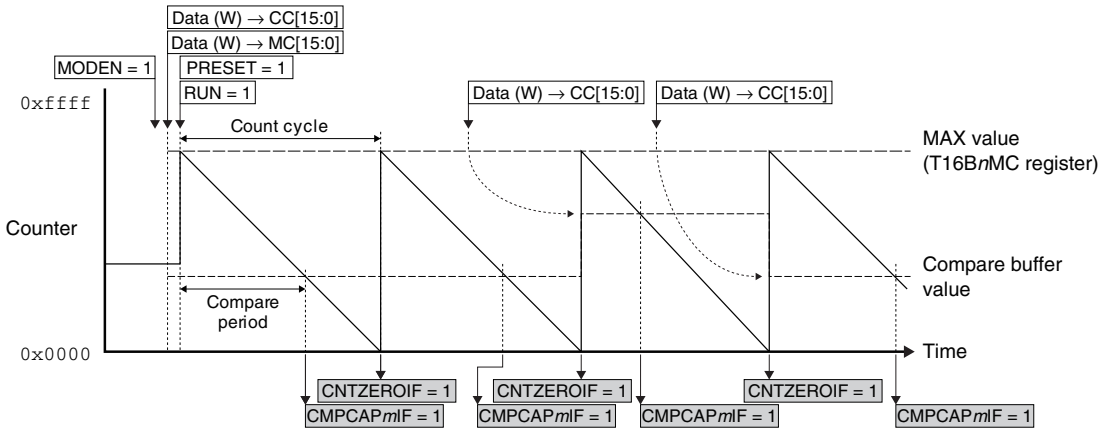
(2.2) T16B*n*CCCTL*m*.CBUFMD[2:0] bits = 0x1



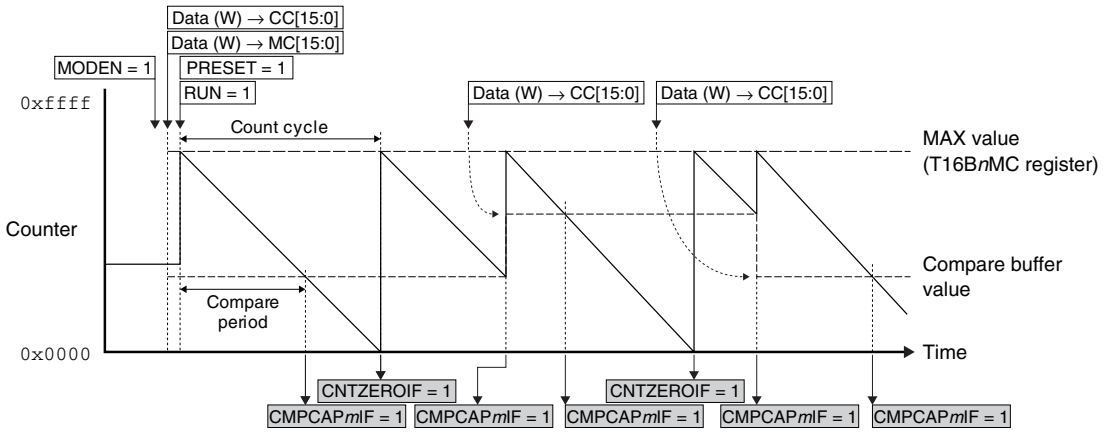
(2.3) T16B*n*CCCTL*m*.CBUFMD[2:0] bits = 0x2



(2.4) T16B*n*CCCTL*m*.CBUFMD[2:0] bits = 0x3

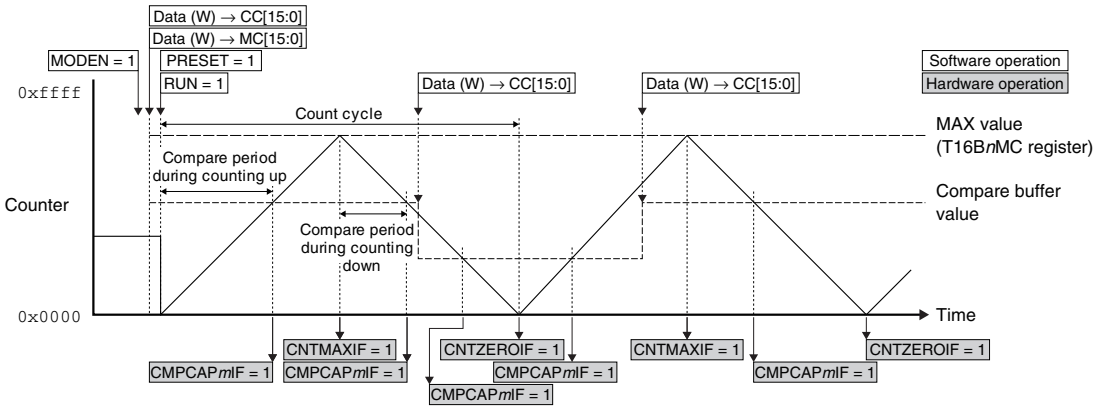


(2.5) T16B*n*CCCTL*m*.CBUFMD[2:0] bits = 0x4

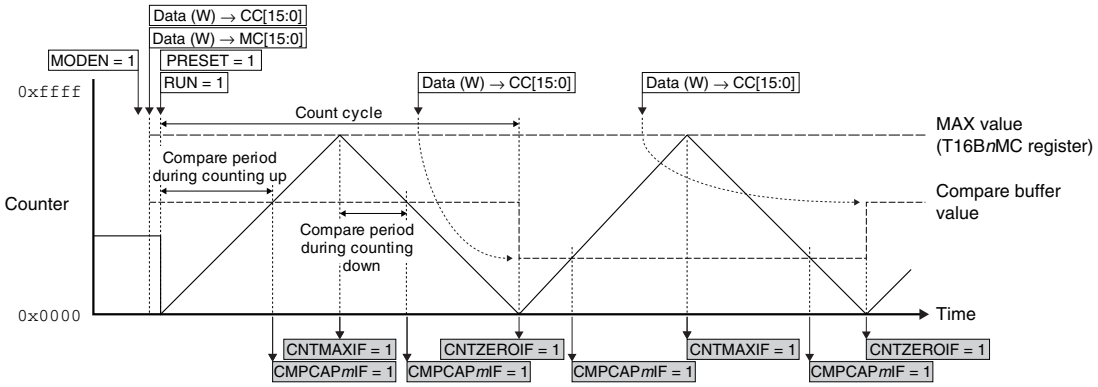


(3) Repeat up/down count mode

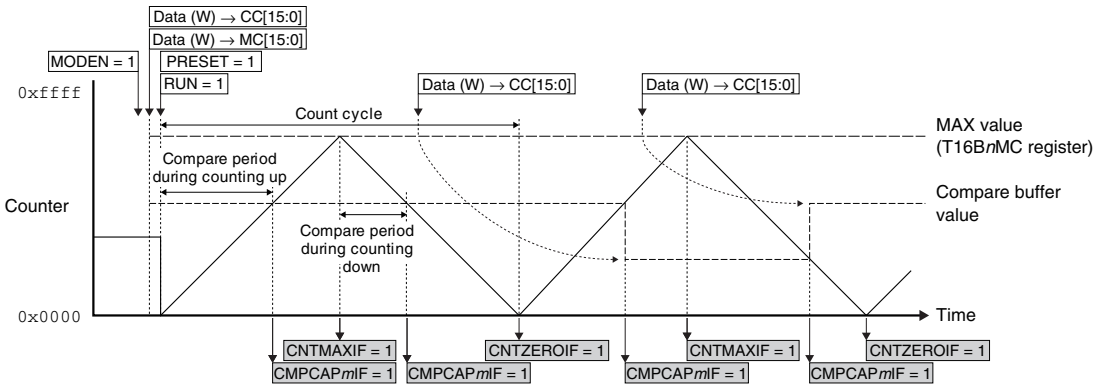
(3.1) T16B*n*CCCTL*m*.CBUFMD[2:0] bits = 0x0

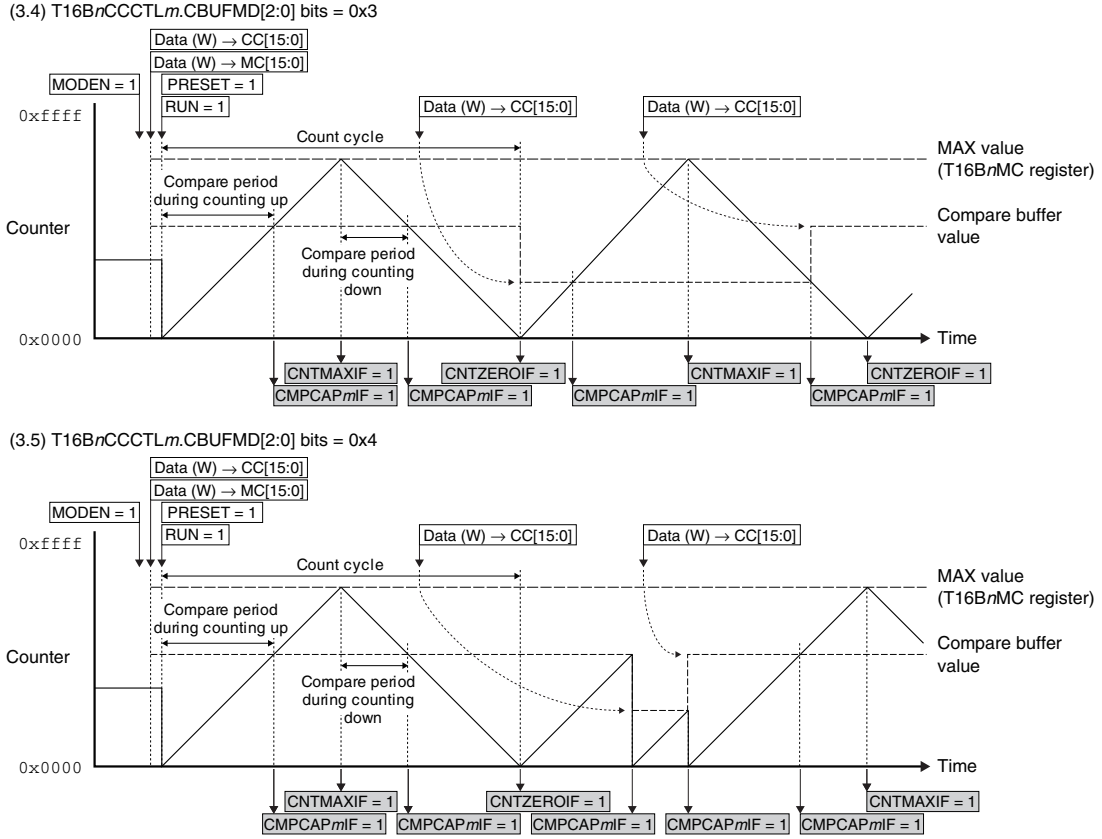


(3.2) T16B*n*CCCTL*m*.CBUFMD[2:0] bits = 0x1



(3.3) T16B*n*CCCTL*m*.CBUFMD[2:0] bits = 0x2





(Note that the T16B*n*INTF.CMPCAP*m*IF/CNTMAXIF/CNTZEROIF bit clearing operations via software are omitted from the figure.)

Figure 15.4.3.2 Compare Buffer Operations

Operations in capture mode

The capture mode captures the counter value when an external event, such as a key entry, occurs (at the specified edge of the external input/software trigger signal). In this mode, the T16B*n*CCR*m* register functions as the capture register from which the captured data is read. Furthermore, the TOUT*nm*/CAP*nm* pin is configured to the CAP*nm* pin.

The trigger signal and the trigger edge to capture the counter value are selected using the T16B*n*CCCTL*m*.CAPIS[1:0] bits and the T16B*n*CCCTL*m*.CAPTRG[1:0] bits, respectively.

When a specified trigger edge is input during counting, the current counter value is loaded to the T16B*n*CCR*m* register. At the same time the T16B*n*INTF.CMPCAP*m*IF bit is set. The interrupt occurred by this bit can be used to read the captured data from the T16B*n*CCR*m* register. For example, external event cycles and pulse widths can be measured from the difference between two captured counter values read.

If the captured data stored in the T16B*n*CCR*m* register is overwritten by the next trigger when the T16B*n*INTF.CMPCAP*m*IF bit is still set, an overwrite error occurs (the T16B*n*INTF.CAPOW*m*IF bit is set).

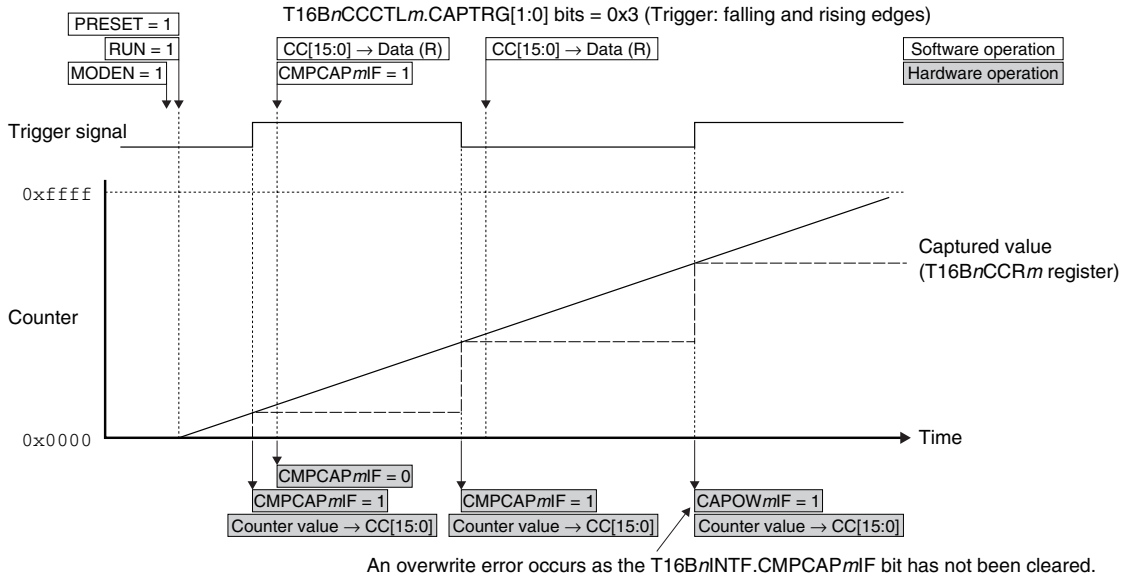


Figure 15.4.3.3 Operations in Capture Mode (Example in One-shot Up Count Mode)

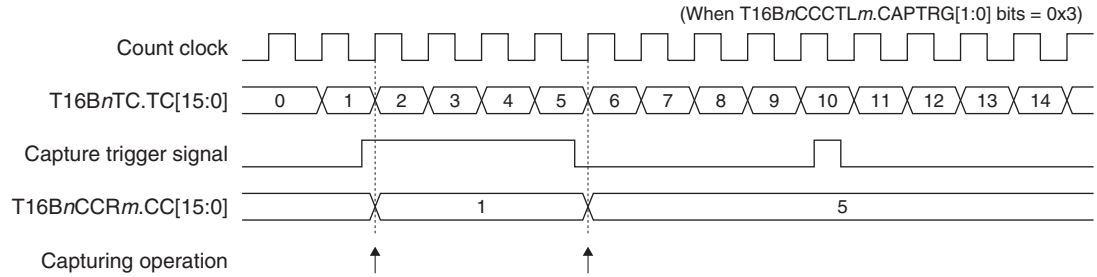
Synchronous capture mode/asynchronous capture mode

The capture circuit can operate in two operating modes: synchronous capture mode and asynchronous capture mode.

Synchronous capture mode is provided to avoid the possibility of invalid data reading by capturing counter data simultaneously with the counter being counted up/down. Set the T16B*n*CCCTL*m*.SCS bit to 1 to set the capture circuit to synchronous capture mode. This mode captures counter data by synchronizing the capture signal with the counter clock.

On the other hand, asynchronous capture mode can capture counter data by detecting a trigger pulse even if the pulse is shorter than the counter clock cycle that becomes invalid in synchronous capture mode. Set the T16B*n*CCCTL*m*.SCS bit to 0 to set the capture circuit to asynchronous capture mode.

(1) Synchronous capture mode



(2) Asynchronous capture mode

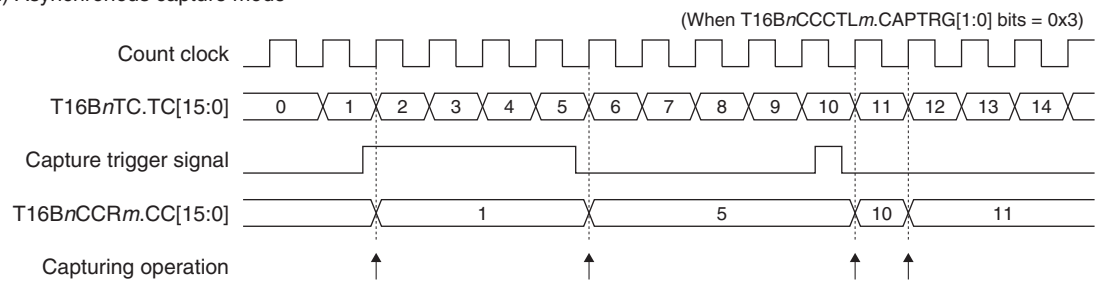


Figure 15.4.3.4 Synchronous Capture Mode/Asynchronous Capture Mode

15.4.4 TOUT Output Control

Comparator mode can generate TOUT signals using the comparator MATCH and counter MAX/ZERO signals. The generated signals can be output to outside the IC. Figure 15.4.4.1 shows the TOUT output circuits (circuits 0 and 1).

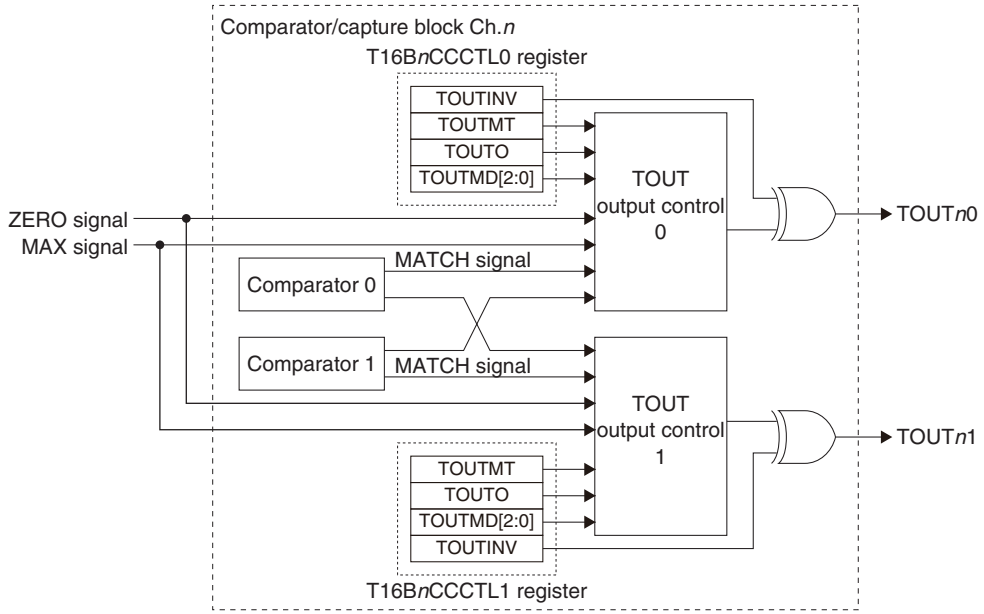


Figure 15.4.4.1 TOUT Output Circuits (Circuits 0 and 1)

Each timer channel includes two (four, or six) TOUT output circuits and their signal generation and output can be controlled individually.

TOUT generation mode

The T16B*n*CCCTL*m*.TOUTMD[2:0] bits are used to set how the TOUT signal waveform is changed by the MATCH and MAX/ZERO signals.

Furthermore, when the T16B*n*CCCTL*m*.TOUTMT bit is set to 1, the TOUT circuit uses the MATCH signal output from another system in the circuit pair (0 and 1, 2 and 3, 4 and 5). This makes it possible to change the signal twice within a counter cycle.

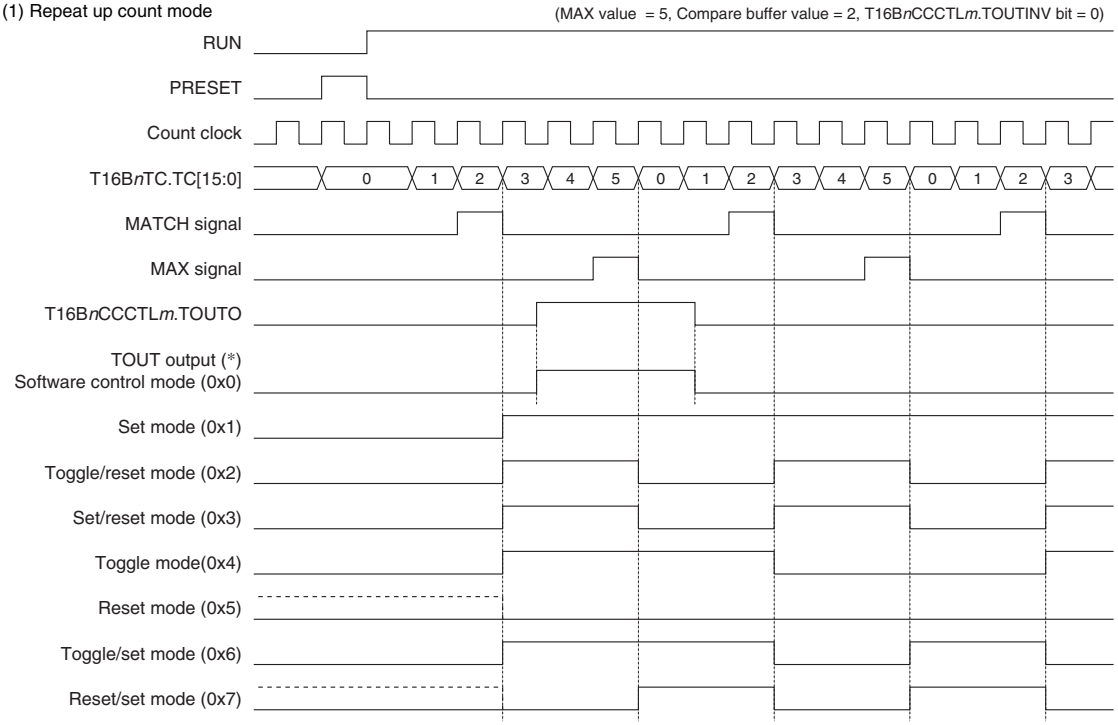
TOUT signal polarity

The TOUT signal polarity (active level) can be set using the T16B*n*CCCTL*m*.TOUTINV bit. It is set to active high by setting the T16B*n*CCCTL*m*.TOUTINV bit to 0 and active low by setting to 1.

Figures 15.4.4.2 and 15.4.4.3 show the TOUT output waveforms.

(1) Repeat up count mode

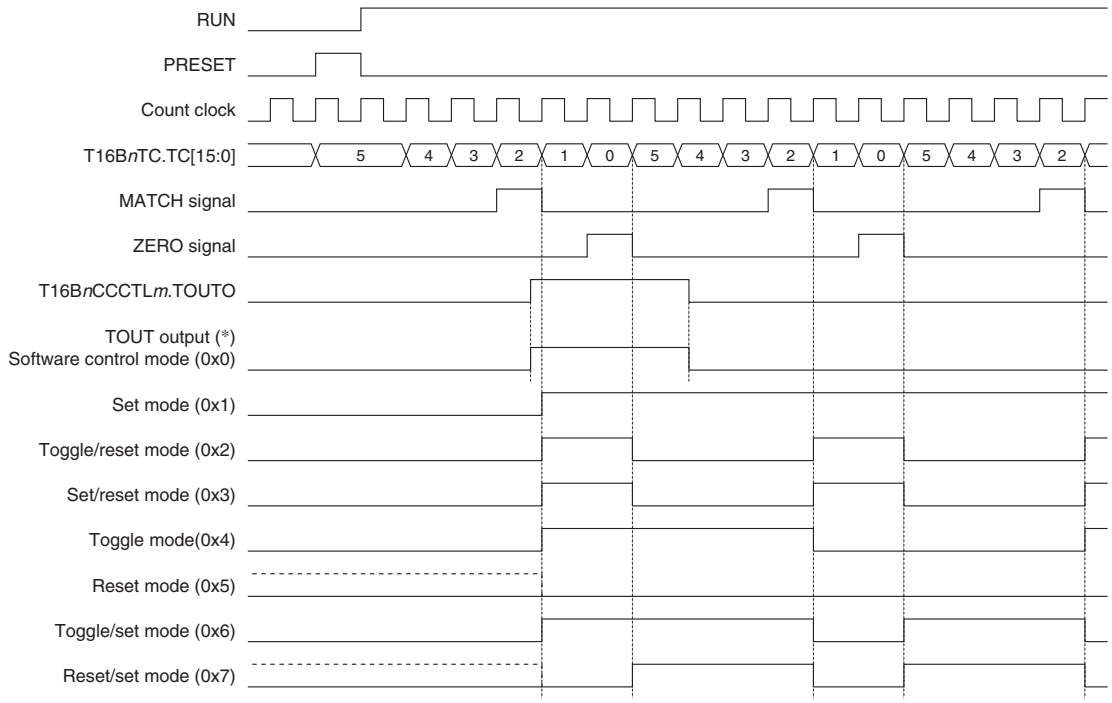
(MAX value = 5, Compare buffer value = 2, T16B*n*CCCTL*m*.TOUTINV bit = 0)



∗ ( ) indicates the T16B*n*CCCTL*m*.TOUTMD[2:0] bit-setting value.

(2) Repeat down count mode

(MAX value = 5, Compare buffer value = 2, T16B*n*CCCTL*m*.TOUTINV bit = 0)



∗ ( ) indicates the T16B*n*CCCTL*m*.TOUTMD[2:0] bit-setting value.

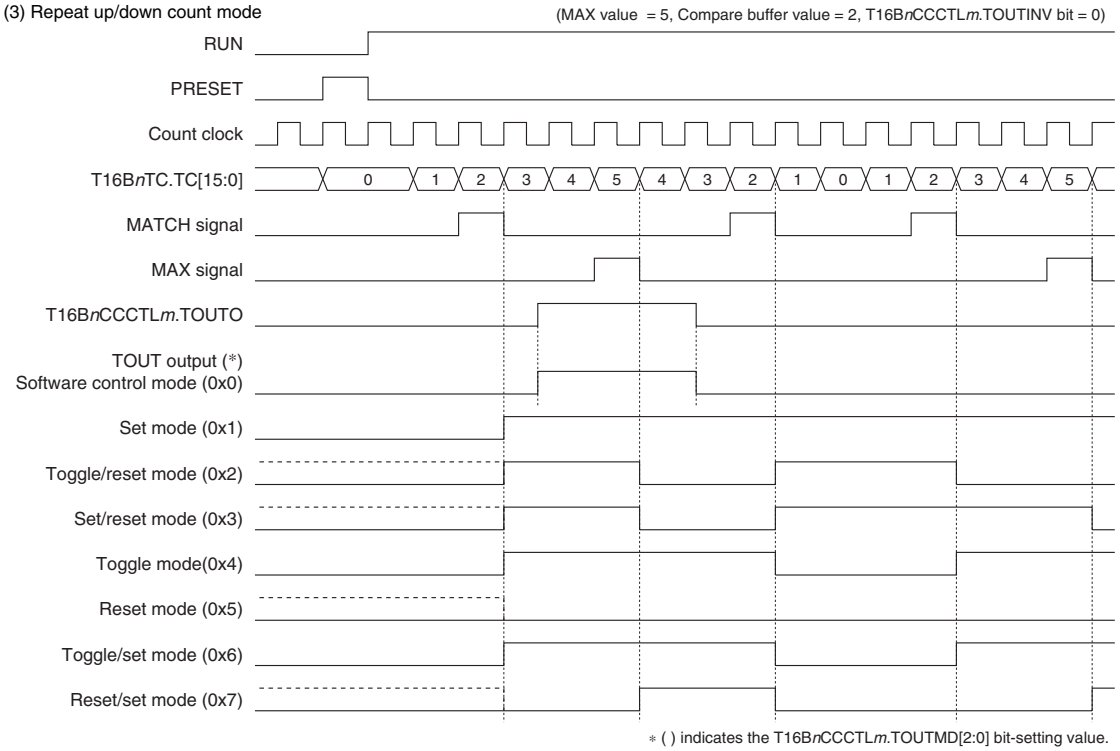
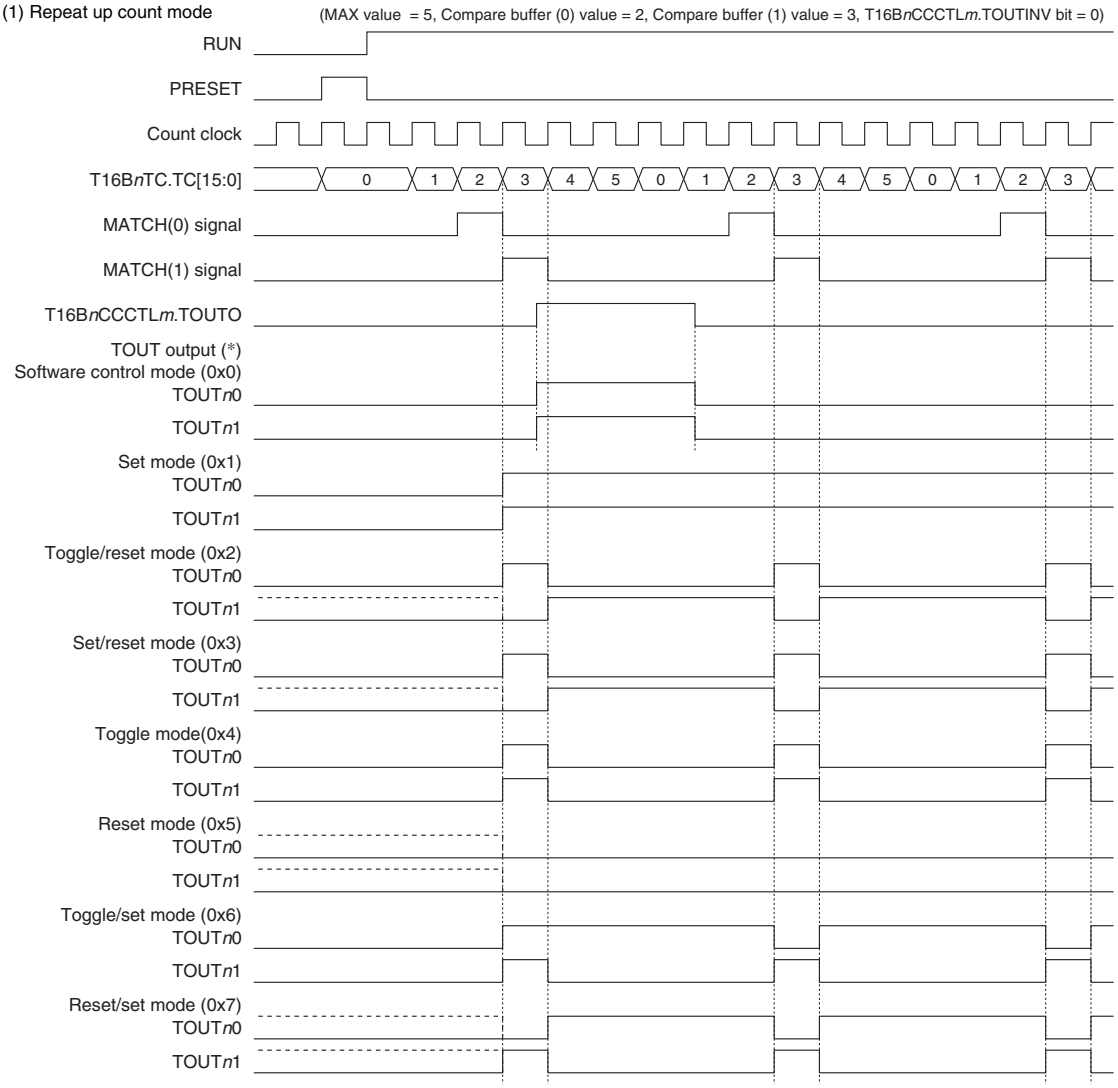


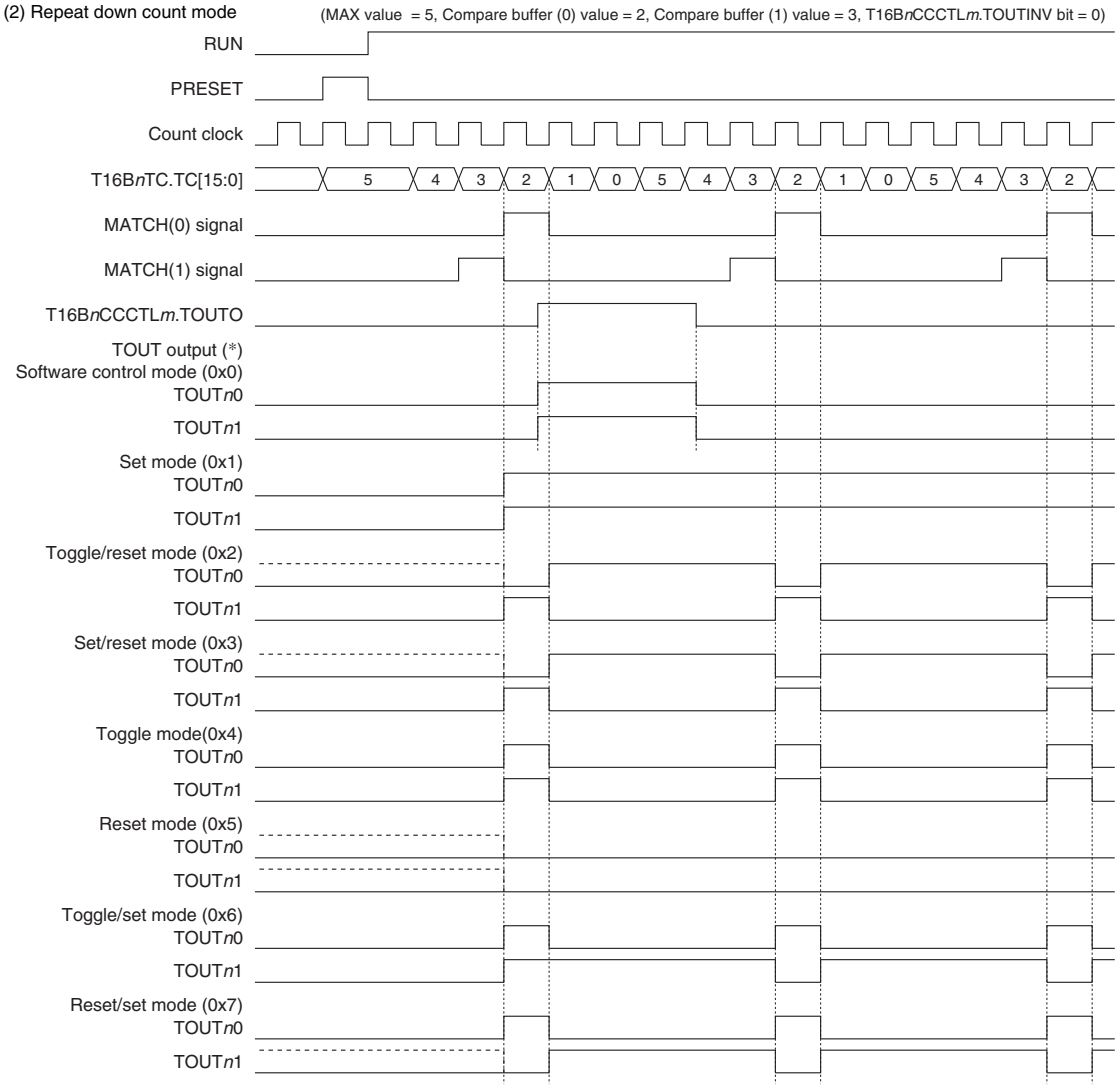
Figure 15.4.4.2 TOUT Output Waveform (T16B*n*CCCTL*m*.TOUTMT bit = 0)

(1) Repeat up count mode



∗ ( ) indicates the T16B*n*CCCTL*m*.TOUTMD[2:0] bit-setting value.

(2) Repeat down count mode



* ( ) indicates the T16B*n*CCCTL*m*.TOUTMD[2:0] bit-setting value.

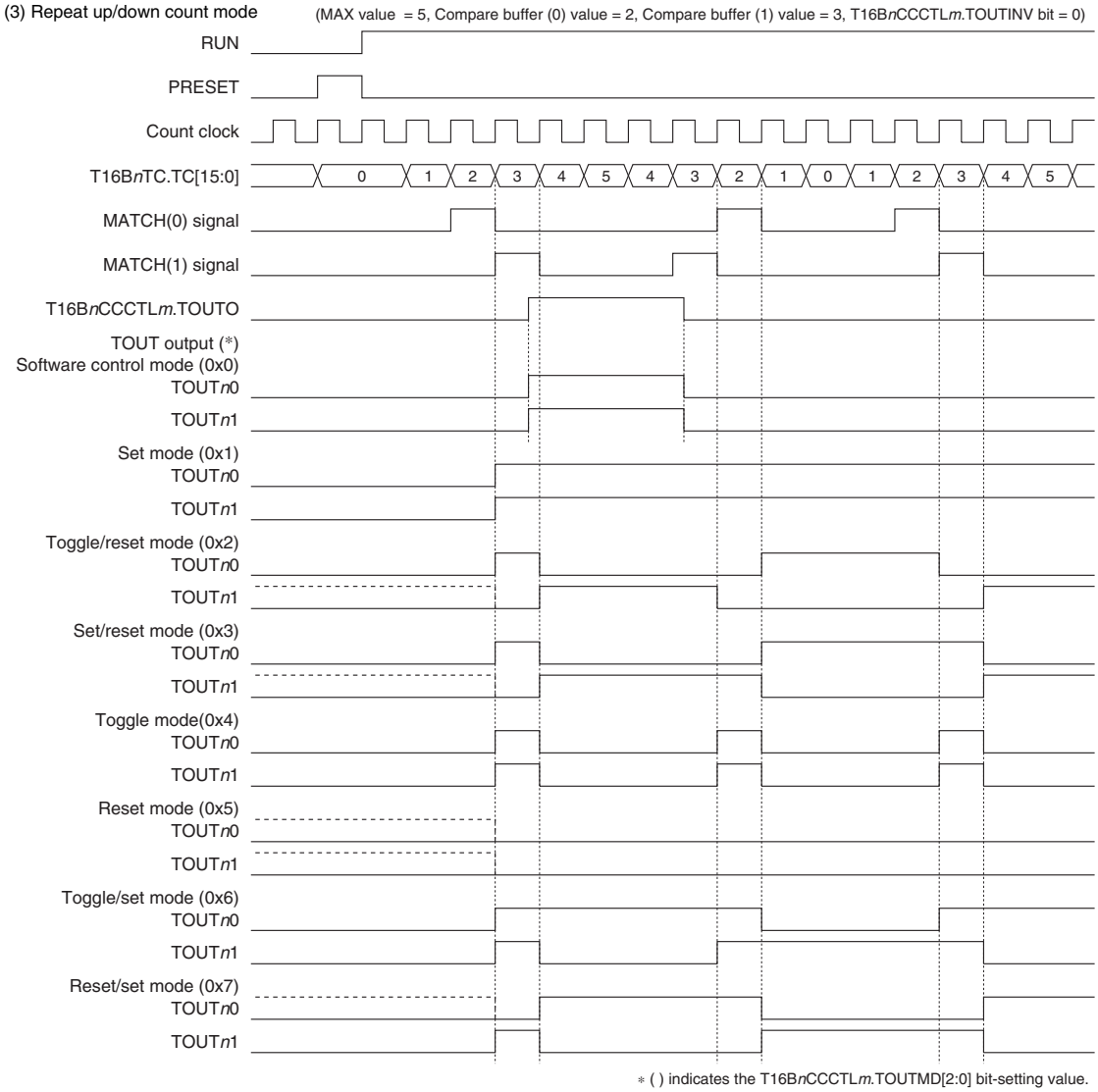


Figure 15.4.4.3 TOUT Output Waveform (T16B*n*CCCTL0.TOUTMT bit = 1, T16B*n*CCCTL1.TOUTMT bit = 0)

15.5 Interrupt

Each T16B channel has a function to generate the interrupt shown in Table 15.5.1.

Table 15.5.1 T16B Interrupt Function

Interrupt	Interrupt flag	Set condition	Clear condition
Capture overwrite	T16B*n*INTF.CAPOW*m*IF	When the T16B*n*INTF.CMPCAP*m*IF bit =1 and the T16B*n* CCR*m* register is overwritten with new captured data in capture mode	Writing 1
Compare/ capture	T16B*n*INTF.CMPCAP*m*IF	When the counter value becomes equal to the compare buffer value in comparator mode When the counter value is loaded to the T16B*n*CCR*m* register by a capture trigger input in capture mode	Writing 1
Counter MAX	T16B*n*INTF.CNTMAXIF	When the counter reaches the MAX value	Writing 1
Counter zero	T16B*n*INTF.CNTZEROIF	When the counter reaches 0x0000	Writing 1

T16B provides interrupt enable bits corresponding to each interrupt flag. An interrupt request is sent to the interrupt controller only when the interrupt flag, of which interrupt has been enabled by the interrupt enable bit, is set. For more information on interrupt control, refer to the "Interrupt Controller" chapter.

15.6 Control Registers

T16B Ch.*n* Clock Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16B*n*CLK	15–9	–	0x00	–	R	–
	8	DBRUN	0	H0	R/W	
	7–4	CLKDIV[3:0]	0x0	H0	R/W	
	3	–	0	–	R	
	2–0	CLKSRC[2:0]	0x0	H0	R/W	

Bits 15–9 Reserved

Bit 8 DBRUN

This bit sets whether the T16B Ch.*n* operating clock is supplied in DEBUG mode or not.

1 (R/W): Clock supplied in DEBUG mode

0 (R/W): No clock supplied in DEBUG mode

Bits 7–4 CLKDIV[3:0]

These bits select the division ratio of the T16B Ch.*n* operating clock (counter clock).

Bit 3 Reserved

Bits 2–0 CLKSRC[2:0]

These bits select the clock source of T16B Ch.*n*.

Table 15.6.1 Clock Source and Division Ratio Settings

T16B*n*CLK.CLKDIV[3:0] bits	T16B*n*CLK.CLKSRC[2:0] bits							
	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7
	IOSC	OSC1	OSC3	EXOSC	EXCL*n*0	EXCL*n*1	EXCL*n*0 inverted input	EXCL*n*1 inverted input
0xf	1/32,768	1/1	1/32,768	1/1	1/1	1/1	1/1	1/1
0xe	1/16,384		1/16,384					
0xd	1/8,192		1/8,192					
0xc	1/4,096		1/4,096					
0xb	1/2,048		1/2,048					
0xa	1/1,024		1/1,024					
0x9	1/512		1/512					
0x8	1/256	1/256	1/256					
0x7	1/128	1/128	1/128					
0x6	1/64	1/64	1/64					
0x5	1/32	1/32	1/32					
0x4	1/16	1/16	1/16					
0x3	1/8	1/8	1/8					
0x2	1/4	1/4	1/4					
0x1	1/2	1/2	1/2					
0x0	1/1	1/1	1/1					

(Note) The oscillator circuits/external inputs that are not supported in this IC cannot be selected as the clock source.

T16B Ch.*n* Counter Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16B*n*CTL	15–9	–	0x00	–	R	–
	8	MAXBSY	0	H0	R	
	7–6	–	0x0	–	R	
	5–4	CNTMD[1:0]	0x0	H0	R/W	
	3	ONEST	0	H0	R/W	
	2	RUN	0	H0	R/W	
	1	PRESET	0	H0	R/W	
	0	MODEN	0	H0	R/W	

Bits 15–9 Reserved

Bit 8 MAXBSY

This bit indicates whether data can be written to the T16B*n*MC register or not.

1 (R): Busy status (cannot be written)

0 (R): Idle (can be written)

While this bit is 1, the T16B*n*MC register is loading the MAX value. Data writing is prohibited during this period.

Bits 7–6 Reserved

Bits 5–4 CNTMD[1:0]

These bits select the counter up/down mode. The count mode is configured with this selection and the T16B*n*CTL.ONEST bit setting (see Table 15.6.2).

Bit 3 ONEST

This bit selects the counter repeat/one-shot mode. The count mode is configured with this selection and the T16B*n*CTL.CNTMD[1:0] bit settings (see Table 15.6.2).

Table 15.6.2 Count Mode

T16B*n*CTL.CNTMD[1:0] bits	Count mode	
	T16B*n*CTL.ONEST bit = 1	T16B*n*CTL.ONEST bit = 0
0x3	Reserved	
0x2	One-shot up/down count mode	Repeat up/down count mode
0x1	One-shot down count mode	Repeat down count mode
0x0	One-shot up count mode	Repeat up count mode

Bit 2 RUN

This bit starts/stops counting.

1 (W): Start counting
0 (W): Stop counting
1 (R): Counting
0 (R): Idle

By writing 1 to this bit, the counter block starts count operations. However, the T16B*n*CTL.MODEN bit must be set to 1 in conjunction with this bit or it must be set in advance. While the timer is running, writing 0 to the T16B*n*CTL.RUN bit stops count operations. When the counter stops by the counter MAX/ZERO signal in one-shot mode, this bit is automatically cleared to 0.

Bit 1 PRESET

This bit resets the counter.

1 (W): Reset
0 (W): Ineffective
1 (R): Resetting in progress
0 (R): Resetting finished or normal operation

In up mode or up/down mode, the counter is cleared to 0x0000 by writing 1 to this bit. In down mode, the MAX value, which has been set to the T16B*n*MC register, is preset to the counter. However, the T16B*n*CTL.MODEN bit must be set to 1 in conjunction with this bit or it must be set in advance.

Bit 0 MODEN

This bit enables the T16B Ch.*n* operations.

1 (R/W): Enable (Start supplying operating clock)
0 (R/W): Disable (Stop supplying operating clock)

Note: The counter reset operation using the T16B*n*CTL.PRESET bit and the counting start operation using the T16B*n*CTL.RUN bit take effect only when the T16B*n*CTL.MODEN bit = 1.

T16B Ch.*n* Max Counter Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16B*n*MC	15–0	MC[15:0]	0xffff	H0	R/W	–

Bits 15–0 MC[15:0]

These bits are used to set the MAX value to preset to the counter. For more information, refer to "Counter Block Operations - MAX counter data register."

Notes:
- When one-shot mode is selected, do not alter the T16B*n*MC.MC[15:0] bits (MAX value) during counting.
- Make sure the T16B*n*CTL.MODEN bit is set to 1 before writing data to the T16B*n*MC.MC[15:0] bits. If the T16B*n*CTL.MODEN bit = 0 when writing to the T16B*n*MC.MC[15:0] bits, set the T16B*n*CTL.MODEN bit to 1 until the T16B*n*CS.BSY bit is set to 0 from 1.
- Do not set the T16B*n*MC.MC[15:0] bits to 0x0000.

T16B Ch.*n* Timer Counter Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16B*n*TC	15–0	TC[15:0]	0x0000	H0	R	–

Bits 15–0 TC[15:0]

The current counter value can be read out through these bits.

T16B Ch.*n* Counter Status Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16B*n*CS	15–8	–	0x00	–	R	–
	7	CAPI5	0	H0	R	
	6	CAPI4	0	H0	R	
	5	CAPI3	0	H0	R	
	4	CAPI2	0	H0	R	
	3	CAPI1	0	H0	R	
	2	CAPI0	0	H0	R	
	1	UP_DOWN	1	H0	R	
	0	BSY	0	H0	R	

Bits 15–8 Reserved

Bit 7 CAPI5
Bit 6 CAPI4
Bit 5 CAPI3
Bit 4 CAPI2
Bit 3 CAPI1
Bit 2 CAPI0

These bits indicate the signal level currently input to the CAP*nm* pin.
1 (R): Input signal = High level
0 (R): Input signal = Low level

The following shows the correspondence between the bit and the CAP*nm* pin:
T16B*n*CS.CAPI5 bit: CAP*n*5 pin
T16B*n*CS.CAPI4 bit: CAP*n*4 pin
T16B*n*CS.CAPI3 bit: CAP*n*3 pin
T16B*n*CS.CAPI2 bit: CAP*n*2 pin
T16B*n*CS.CAPI1 bit: CAP*n*1 pin
T16B*n*CS.CAPI0 bit: CAP*n*0 pin

Note: The configuration of the T16B*n*CS.CAPI*m* bits depends on the model. The bits corresponding to the CAP*nm* pins that do not exist are read-only bits and are always fixed at 0.

Bit 1 UP_DOWN

This bit indicates the currently set count direction.
1 (R): Count up
0 (R): Count down

Bit 0 BSY

This bit indicates the counter operating status.
1 (R): Running
0 (R): Idle

T16B Ch.*n* Interrupt Flag Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16B*n*INTF	15–14	–	0x0	–	R	–
	13	CAPOW5IF	0	H0	R/W	Cleared by writing 1.
	12	CMPCAP5IF	0	H0	R/W	
	11	CAPOW4IF	0	H0	R/W	
	10	CMPCAP4IF	0	H0	R/W	
	9	CAPOW3IF	0	H0	R/W	
	8	CMPCAP3IF	0	H0	R/W	
	7	CAPOW2IF	0	H0	R/W	
	6	CMPCAP2IF	0	H0	R/W	
	5	CAPOW1IF	0	H0	R/W	
	4	CMPCAP1IF	0	H0	R/W	
	3	CAPOW0IF	0	H0	R/W	
	2	CMPCAP0IF	0	H0	R/W	
	1	CNTMAXIF	0	H0	R/W	
	0	CNTZEROIF	0	H0	R/W	

Bits 15–14 Reserved

Bit 13 CAPOW5IF
Bit 12 CMPCAP5IF
Bit 11 CAPOW4IF
Bit 10 CMPCAP4IF
Bit 9 CAPOW3IF
Bit 8 CMPCAP3IF
Bit 7 CAPOW2IF
Bit 6 CMPCAP2IF
Bit 5 CAPOW1IF
Bit 4 CMPCAP1IF
Bit 3 CAPOW0IF
Bit 2 CMPCAP0IF
Bit 1 CNTMAXIF
Bit 0 CNTZEROIF

These bits indicate the T16B Ch.*n* interrupt cause occurrence status.
1 (R): Cause of interrupt occurred
0 (R): No cause of interrupt occurred
1 (W): Clear flag
0 (W): Ineffective

The following shows the correspondence between the bit and interrupt:
T16B*n*INTF.CAPOW5IF bit: Capture 5 overwrite interrupt
T16B*n*INTF.CMPCAP5IF bit: Compare/capture 5 interrupt
T16B*n*INTF.CAPOW4IF bit: Capture 4 overwrite interrupt
T16B*n*INTF.CMPCAP4IF bit: Compare/capture 4 interrupt
T16B*n*INTF.CAPOW3IF bit: Capture 3 overwrite interrupt
T16B*n*INTF.CMPCAP3IF bit: Compare/capture 3 interrupt
T16B*n*INTF.CAPOW2IF bit: Capture 2 overwrite interrupt
T16B*n*INTF.CMPCAP2IF bit: Compare/capture 2 interrupt
T16B*n*INTF.CAPOW1IF bit: Capture 1 overwrite interrupt
T16B*n*INTF.CMPCAP1IF bit: Compare/capture 1 interrupt
T16B*n*INTF.CAPOW0IF bit: Capture 0 overwrite interrupt
T16B*n*INTF.CMPCAP0IF bit: Compare/capture 0 interrupt
T16B*n*INTF.CNTMAXIF bit: Counter MAX interrupt
T16B*n*INTF.CNTZEROIF bit: Counter zero interrupt

Note: The configuration of the T16B*n*INTF.CAPOW*m*IF and T16B*n*INTF.CMPCAP*m*IF bits depends on the model. The bits corresponding to the comparator/capture circuits that do not exist are read-only bits and are always fixed at 0.

T16B Ch.*n* Interrupt Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16B*n*INTE	15–14	–	0x0	–	R	–
	13	CAPOW5IE	0	H0	R/W	
	12	CMPCAP5IE	0	H0	R/W	
	11	CAPOW4IE	0	H0	R/W	
	10	CMPCAP4IE	0	H0	R/W	
	9	CAPOW3IE	0	H0	R/W	
	8	CMPCAP3IE	0	H0	R/W	
	7	CAPOW2IE	0	H0	R/W	
	6	CMPCAP2IE	0	H0	R/W	
	5	CAPOW1IE	0	H0	R/W	
	4	CMPCAP1IE	0	H0	R/W	
	3	CAPOW0IE	0	H0	R/W	
	2	CMPCAP0IE	0	H0	R/W	
	1	CNTMAXIE	0	H0	R/W	
	0	CNTZEROIE	0	H0	R/W	

Bits 15–14 Reserved

Bit 13 CAPOW5IE
Bit 12 CMPCAP5IE
Bit 11 CAPOW4IE
Bit 10 CMPCAP4IE
Bit 9 CAPOW3IE
Bit 8 CMPCAP3IE
Bit 7 CAPOW2IE
Bit 6 CMPCAP2IE
Bit 5 CAPOW1IE
Bit 4 CMPCAP1IE
Bit 3 CAPOW0IE
Bit 2 CMPCAP0IE
Bit 1 CNTMAXIE
Bit 0 CNTZEROIE

These bits enable T16B Ch.*n* interrupts.
1 (R/W): Enable interrupts
0 (R/W): Disable interrupts

The following shows the correspondence between the bit and interrupt:
T16B*n*INTE.CAPOW5IE bit: Capture 5 overwrite interrupt
T16B*n*INTE.CMPCAP5IE bit: Compare/capture 5 interrupt
T16B*n*INTE.CAPOW4IE bit: Capture 4 overwrite interrupt
T16B*n*INTE.CMPCAP4IE bit: Compare/capture 4 interrupt
T16B*n*INTE.CAPOW3IE bit: Capture 3 overwrite interrupt
T16B*n*INTE.CMPCAP3IE bit: Compare/capture 3 interrupt
T16B*n*INTE.CAPOW2IE bit: Capture 2 overwrite interrupt
T16B*n*INTE.CMPCAP2IE bit: Compare/capture 2 interrupt
T16B*n*INTE.CAPOW1IE bit: Capture 1 overwrite interrupt
T16B*n*INTE.CMPCAP1IE bit: Compare/capture 1 interrupt
T16B*n*INTE.CAPOW0IE bit: Capture 0 overwrite interrupt
T16B*n*INTE.CMPCAP0IE bit: Compare/capture 0 interrupt
T16B*n*INTE.CNTMAXIE bit: Counter MAX interrupt
T16B*n*INTE.CNTZEROIE bit: Counter zero interrupt

Notes: • The configuration of the T16B*n*INTE.CAPOW*m*IE and T16B*n*INTE.CMPCAP*m*IE bits depends on the model. The bits corresponding to the comparator/capture circuits that do not exist are read-only bits and are always fixed at 0.

• To prevent generating unnecessary interrupts, the corresponding interrupt flag should be cleared before enabling interrupts.

T16B Ch.*n* Comparator/Capture *m* Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16B*n*CCCTL*m*	15	SCS	0	H0	R/W	–
	14–12	CBUFMD[2:0]	0x0	H0	R/W	
	11–10	CAPIS[1:0]	0x0	H0	R/W	
	9–8	CAPTRG[1:0]	0x0	H0	R/W	
	7	–	0	–	R	
	6	TOUTMT	0	H0	R/W	
	5	TOUTO	0	H0	R/W	
	4–2	TOUTMD[2:0]	0x0	H0	R/W	
	1	TOUTINV	0	H0	R/W	
	0	CCMD	0	H0	R/W	

Bit 15 SCS

This bit selects either synchronous capture mode or asynchronous capture mode.

1 (R/W): Synchronous capture mode

0 (R/W): Asynchronous capture mode

For more information, refer to "Comparator/Capture Block Operations - Synchronous capture mode/ asynchronous capture mode." The T16B*n*CCCTL*m*.SCS bit is control bit for capture mode and is ineffective in comparator mode.

Bits 14–12 CBUFMD[2:0]

These bits select the timing to load the comparison value written in the T16B*n*CCR*m* register to the compare buffer. The T16B*n*CCCTL*m*.CBUFMD[2:0] bits are control bits for comparator mode and are ineffective in capture mode.

Table 15.6.3 Timings to Load Comparison Value to Compare Buffer

T16B*n*CCCTL*m*. CBUFMD[2:0] bits	Count mode	Comparison Value load timing
0x7–0x5	Reserved	
0x4	Up mode	When the counter becomes equal to the comparison value set previously Also the counter is reset to 0x0000 simultaneously.
	Down mode	When the counter becomes equal to the comparison value set previously Also the counter is reset to the MAX value simultaneously.
	Up/down mode	When the counter becomes equal to the comparison value set previously Also the counter is reset to 0x0000 simultaneously.
0x3	Up mode	When the counter reverts to 0x0000
	Down mode	When the counter reverts to the MAX value
	Up/down mode	When the counter becomes equal to the comparison value set previously or when the counter reverts to 0x0000
0x2	Up mode	When the counter becomes equal to the comparison value set previously
	Down mode	
	Up/down mode	
0x1	Up mode	When the counter reaches the MAX value
	Down mode	When the counter reaches 0x0000
	Up/down mode	When the counter reaches 0x0000 or the MAX value
0x0	Up mode	At the CLK_T16B*n* rising edge after writing to the T16B*n*CCR*m* register
	Down mode	
	Up/down mode	

Bits 11–10 CAPIS[1:0]

These bits select the trigger signal for capturing (see Table 15.6.4). The T16B*n*CCCTL*m*.CAPIS[1:0] bits are control bits for capture mode and are ineffective in comparator mode.

Bits 9–8 CAPTRG[1:0]

These bits select the trigger edge(s) of the trigger signal at which the counter value is captured in the T16B*n*CCR*m* register in capture mode (see Table 15.6.4). The T16B*n*CCCTL*m*.CAPTRG[1:0] bits are control bits for capture mode and are ineffective in comparator mode.

Table 15.6.4 Trigger Signal/Edge for Capturing Counter Value

T16B*n*CCCTL*m*. CAPTRG[1:0] bits (Trigger edge)	Trigger condition		
	T16B*n*CCCTL*m*.CAPIS[1:0] bits (Trigger signal)		
	0x0 (External trigger signal)	0x2 (Software trigger signal = L)	0x3 (Software trigger signal = H)
0x3 (↑ & ↓)	Rising or falling edge of the CAP*nm* pin input signal	Altering the T16B*n*CCCTL*m*.CAPIS[1:0] bits from 0x2 to 0x3, or from 0x3 to 0x2	
0x2 (↓)	Falling edge of the CAP*nm* pin input signal	Altering the T16B*n*CCCTL*m*.CAPIS[1:0] bits from 0x3 to 0x2	
0x1 (↑)	Rising edge of the CAP*nm* pin input signal	Altering the T16B*n*CCCTL*m*.CAPIS[1:0] bits from 0x2 to 0x3	
0x0	Not triggered (disable capture function)		

Bit 7 Reserved

Bit 6 TOUTMT

This bit selects whether the comparator MATCH signal of another system is used for generating the TOUT*nm* signal or not.

1 (R/W): Generate TOUT using two comparator MATCH signals of the comparator circuit pair (0 and 1, 2 and 3, 4 and 5)

0 (R/W): Generate TOUT using one comparator MATCH signal of comparator *m* and the counter MAX or ZERO signals

The T16B*n*CCCTL*m*.TOUTMT bit is control bit for comparator mode and is ineffective in capture mode.

Bit 5 TOUTO

This bit sets the TOUT*nm* signal output level when software control mode (T16B*n*CCCTL*m*.TOUTMD[2:0] = 0x0) is selected for the TOUT*nm* output.

1 (R/W): High level output

0 (R/W): Low level output

The T16B*n*CCCTL*m*.TOUTO bit is control bit for comparator mode and is ineffective in capture mode.

Bits 4–2 TOUTMD[2:0]

These bits configure how the TOUT*nm* signal waveform is changed by the comparator MATCH and counter MAX/ZERO signals.

The T16B*n*CCCTL*m*.TOUTMD[2:0] bits are control bits for comparator mode and are ineffective in capture mode.

Table 15.6.5 TOUT Generation Mode

T16B*n*CCCTL*m*. TOUTMD[2:0] bits	TOUT generation mode and operations			
	T16B*n*CCCTL*m*. TOUTMT bit	Count mode	Output signal	Change in the signal
0x7	**Reset/set mode**			
	0	Up count mode Up/down count mode	TOUT*nm*	The signal becomes inactive by the MATCH signal and it becomes active by the MAX signal.
		Down count mode	TOUT*nm*	The signal becomes inactive by the MATCH signal and it becomes active by the ZERO signal.
	1	All count modes	TOUT*nm*	The signal becomes inactive by the MATCH*m* signal and it becomes active by the MATCH*m*+1 signal.
			TOUT*nm*+1	The signal becomes inactive by the MATCH*m*+1 signal and it becomes active by the MATCH*m* signal.
0x6	**Toggle/set mode**			
	0	Up count mode Up/down count mode	TOUT*nm*	The signal is inverted by the MATCH signal and it becomes active by the MAX signal.
		Down count mode	TOUT*nm*	The signal is inverted by the MATCH signal and it becomes active by the ZERO signal.
	1	All count modes	TOUT*nm*	The signal is inverted by the MATCH*m* signal and it becomes active by the MATCH*m*+1 signal.
			TOUT*nm*+1	The signal is inverted by the MATCH*m*+1 signal and it becomes active by the MATCH*m* signal.
0x5	**Reset mode**			
	0	All count modes	TOUT*nm*	The signal becomes inactive by the MATCH signal.
	1	All count modes	TOUT*nm*	The signal becomes inactive by the MATCH*m* or MATCH*m*+1 signal.
			TOUT*nm*+1	The signal becomes inactive by the MATCH*m*+1 or MATCH*m* signal.

T16B*n*CCCTL*m*. TOUTMD[2:0] bits	TOUT generation mode and operations			
	T16B*n*CCCTL*m*. TOUTMT bit	Count mode	Output signal	Change in the signal
0x4	**Toggle mode**			
	0	All count modes	TOUT*nm*	The signal is inverted by the MATCH signal.
	1	All count modes	TOUT*nm*	The signal is inverted by the MATCH*m* or MATCH*m*+1 signal.
			TOUT*nm*+1	The signal is inverted by the MATCH*m*+1 or MATCH*m* signal.
0x3	**Set/reset mode**			
	0	Up count mode Up/down count mode	TOUT*nm*	The signal becomes active by the MATCH signal and it becomes inactive by the MAX signal.
		Down count mode	TOUT*nm*	The signal becomes active by the MATCH signal and it becomes inactive by the ZERO signal.
	1	All count modes	TOUT*nm*	The signal becomes active by the MATCH*m* signal and it becomes inactive by the MATCH*m*+1 signal.
			TOUT*nm*+1	The signal becomes active by the MATCH*m*+1 signal and it becomes inactive by the MATCH*m* signal.
0x2	**Toggle/reset mode**			
	0	Up count mode Up/down count mode	TOUT*nm*	The signal is inverted by the MATCH signal and it becomes inactive by the MAX signal.
		Down count mode	TOUT*nm*	The signal is inverted by the MATCH signal and it becomes inactive by the ZERO signal.
	1	All count modes	TOUT*nm*	The signal is inverted by the MATCH*m* signal and it becomes inactive by the MATCH*m*+1 signal.
			TOUT*nm*+1	The signal is inverted by the MATCH*m*+1 signal and it becomes inactive by the MATCH*m* signal.
0x1	**Set mode**			
	0	All count modes	TOUT*nm*	The signal becomes active by the MATCH signal.
	1	All count modes	TOUT*nm*	The signal becomes active by the MATCH*m* or MATCH*m*+1 signal.
			TOUT*nm*+1	The signal becomes active by the MATCH*m*+1 or MATCH*m* signal.
0x0	**Software control mode**			
	*	All count modes	TOUT*nm*	The signal becomes active by setting the T16B*n*CCCTL*m*. TOUTO bit to 1 and it becomes inactive by setting to 0.

Bit 1 TOUTINV

This bit selects the TOUT*nm* signal polarity.

1 (R/W): Inverted (active low)

0 (R/W): Normal (active high)

The T16B*n*CCCTL*m*.TOUTINV bit is control bit for comparator mode and is ineffective in capture mode.

Bit 0 CCMD

This bit selects the operating mode of the comparator/capture circuit *m*.

1 (R/W): Capture mode (T16B*n*CCR*m* register = capture register)

0 (R/W): Comparator mode (T16B*n*CCR*m* register = compare data register)

T16B Ch.*n* Compare/Capture *m* Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16B*n*CCR*m*	15–0	CC[15:0]	0x0000	H0	R/W	–

Bits 15–0 CC[15:0]

In comparator mode, this register is configured as the compare data register and used to set the comparison value to be compared with the counter value.

In capture mode, this register is configured as the capture register and the counter value captured by the capture trigger signal is loaded.

16 Sound Generator (SNDA)

16.1 Overview

SNDA is a sound generator that generates melodies and buzzer signals. The features of the SNDA are listed below.

- Sound output mode is selectable from three types.
  1. Normal buzzer mode (for normal buzzer output of which the output duration is controlled via software)
     - Output frequency: Can be set within the range of 512 Hz to 16,384 Hz.
     - Duty ratio: Can be set within the range of 0% to 100%.
  2. One-shot buzzer mode (for short buzzer output such as a clicking sound)
     - Output frequency: Can be set within the range of 512 Hz to 16,384 Hz.
     - Duty ratio: Can be set within the range of 0% to 100%.
     - One-shot output duration: Can be set within the range of 15.6 ms to 250 ms. (16 types)
  3. Melody mode (for playing single note melody)
     - Pitch: Can be set within the range of 128 Hz to 16,384 Hz. (Scale: 3 octave from C3 to C6 with reference to A4 = 443 Hz)
     - Duration: Can be set within the range of half note/rest to thirty-second note/rest. (7 types)
     - Tempo: Can be set within the range of 30 to 480. (16 types)
     - Other: Tie and slur can be specified.
- A piezoelectric buzzer can be driven with the inverted and non-inverted output pins.
- Can control the non-inverted output pin status while sound stops.

Figure 16.1.1 shows the SNDA configuration.

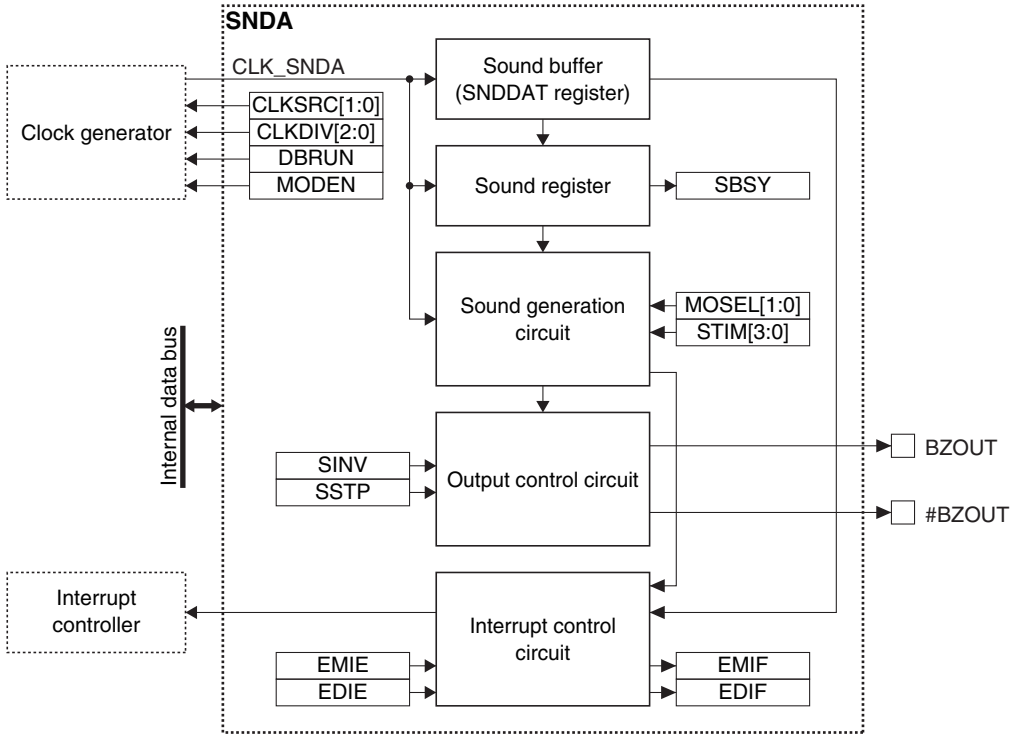


Figure 16.1.1 SNDA Configuration

16.2 Output Pins and External Connections

16.2.1 List of Output Pins

Table 16.2.1.1 lists the SNDA pins.

Table 16.2.1.1 List of SNDA Pins

Pin name	I/O*	Initial status*	Function
BZOUT	O	O (Low)	Non-inverted buzzer output pin
#BZOUT	O	O (Low)	Inverted buzzer output pin

* Indicates the status when the pin is configured for SNDA

If the port is shared with the SNDA pin and other functions, the SNDA output function must be assigned to the port before activating the SNDA. For more information, refer to the "I/O Ports" chapter.

16.2.2 Output Pin Drive Mode

The drive mode of the BZOUT and #BZOUT pins can be set to one of the two types shown below using the SNDSEL.SINV bit.

Direct drive mode (SNDSEL.SINV bit = 0)

This mode drives both the BZOUT and #BZOUT pins to low while the buzzer signal output is off to prevent the piezoelectric buzzer from applying unnecessary bias.

Normal drive mode (SNDSEL.SINV bit = 1)

In this mode, the #BZOUT pin always outputs the inverted signal of the BZOUT pin even when the buzzer output is off.

16.2.3 External Connections

Figures 16.2.2.1 and 16.2.2.2 show connection diagrams between SNDA and a piezoelectric buzzer.

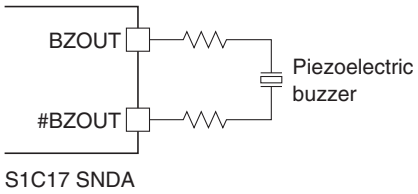


Figure 16.2.2.1 Connection between SNDA and Piezoelectric Buzzer (Direct Drive)

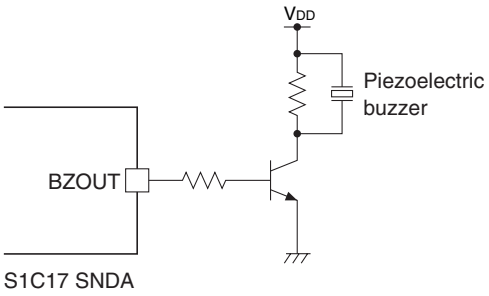


Figure 16.2.2.2 Connection between SNDA and Piezoelectric Buzzer (Single Pin Drive)

16.3 Clock Settings

16.3.1 SNDA Operating Clock

When using SNDA, the SNDA operating clock CLK_SNDA must be supplied to SNDA from the clock generator. The CLK_SNDA supply should be controlled as in the procedure shown below.

1. Enable the clock source in the clock generator if it is stopped (refer to "Clock Generator" in the "Power Supply, Reset, and Clocks" chapter).
2. Set the following SNDCLK register bits:
   - SNDCLK.CLKSRC[1:0] bits (Clock source selection)
   - SNDCLK.CLKDIV[2:0] bits (Clock division ratio selection = Clock frequency setting)

The CLK_SNDA frequency should be set to around 32,768 Hz.

16.3.2 Clock Supply in SLEEP Mode

When using SNDA during SLEEP mode, the SNDA operating clock CLK_SNDA must be configured so that it will keep supplying by writing 0 to the CLGOSC.*xxxx*SLPC bit for the CLK_SNDA clock source.
If the CLGOSC.*xxxx*SLPC bit for the CLK_SNDA clock source is 1, the CLK_SNDA clock source is deactivated during SLEEP mode and SNDA stops with the register settings maintained at those before entering SLEEP mode. After the CPU returns to normal mode, CLK_SNDA is supplied and the SNDA operation resumes.

16.3.3 Clock Supply in DEBUG Mode

The CLK_SNDA supply during DEBUG mode should be controlled using the SNDCLK.DBRUN bit.
The CLK_SNDA supply to SNDA is suspended when the CPU enters DEBUG mode if the SNDCLK.DBRUN bit = 0. After the CPU returns to normal mode, the CLK_SNDA supply resumes. Although SNDA stops operating when the CLK_SNDA supply is suspended, the output pin and registers retain the status before DEBUG mode was entered. If the SNDCLK.DBRUN bit = 1, the CLK_SNDA supply is not suspended and SNDA will keep operating in DEBUG mode.

16.4 Operations

16.4.1 Initialization

SNDA should be initialized with the procedure shown below.

1. Assign the SNDA output function to the ports. (Refer to the "I/O Ports" chapter.)
2. Configure the SNDA operating clock.
3. Set the SNDCTL.MODEN bit to 1. (Enable SNDA operations)
4. Set the SNDSEL.SINV bit. (Set output pin drive mode)
5. Set the following bits when using the interrupt:
   - Write 1 to the interrupt flags in the SNDINTF register. (Clear interrupt flags)
   - Set the interrupt enable bits in the SNDINTE register to 1. (Enable interrupts)

16.4.2 Buzzer Output in Normal Buzzer Mode

Normal buzzer mode generates a buzzer signal with the software specified frequency and duty ratio, and outputs the generated signal to outside the IC. The buzzer output duration can also be controlled via software.
An output start/stop procedure and the SNDA operations are shown below.

Normal buzzer output start/stop procedure

1. Set the SNDSEL.MOSEL[1:0] bits to 0x0. (Set normal buzzer mode)

2. Write data to the following sound buffer (SNDDAT register) bits. (Start buzzer output)
   - SNDDAT.SLEN[5:0] bits (Set buzzer output signal duty ratio)
   - SNDDAT.SFRQ[7:0] bits (Set buzzer output signal frequency)
3. Write 1 to the SNDCTL.SSTP bit after the output period has elapsed. (Stop buzzer output)

Normal buzzer output operations

When data is written to the sound buffer (SNDDAT register), SNDA clears the SNDINTF.EMIF bit (sound buffer empty interrupt flag) to 0 and starts buzzer output operations.
The data written to the sound buffer is loaded into the sound register in sync with the CLK_SNDA clock. At the same time, the SNDINTF.EMIF bit and SNDINTF.SBSY bit are both set to 1. The output pin outputs the buzzer signal with the frequency/duty ratio specified.
Writing 1 to the SNDCTL.SSTP bit stops buzzer output and sets the SNDINTF.EDIF bit (sound output completion interrupt flag) to 1. The SNDINTF.SBSY bit is cleared to 0.
Figure 16.4.2.1 shows a buzzer output timing chart in normal buzzer mode.

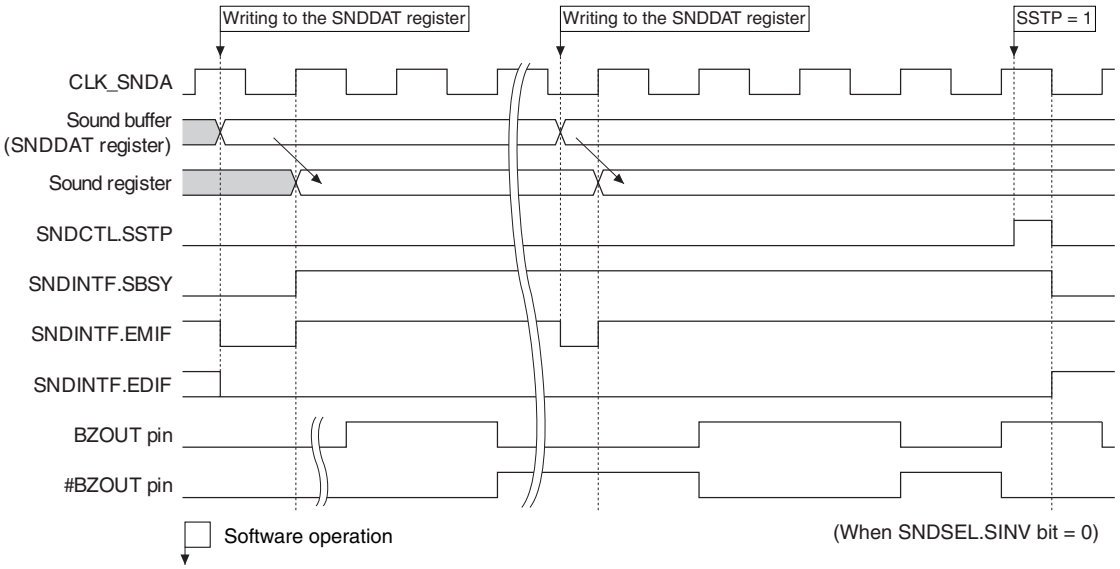


Figure 16.4.2.1 Buzzer Output Timing Chart in Normal Buzzer Mode

Buzzer output waveform configuration (normal buzzer mode/one-shot buzzer mode)

Set the buzzer signal frequency and duty ratio (high period/cycle) using the SNDDAT.SFRQ[7:0] and SNDDAT.SLEN[5:0] bits, respectively. Use the following equations to calculate these setting values.

$$\text{SNDDAT.SFRQ[7:0] bits} = \frac{f_{CLK\_SNDA}}{f_{BZOUT}} - 1 \qquad \text{(Eq. 16.1)}$$

$$\text{SNDDAT.SLEN[5:0] bits} = \left(\frac{f_{CLK\_SNDA}}{f_{BZOUT}} \times \frac{DUTY}{100}\right) - 1 \qquad \text{(Eq. 16.2)}$$

Where
f_{CLK_SNDA}: CLK_SNDA frequency [Hz]
f_{BZOUT}: Buzzer signal frequency [Hz]
DUTY: Buzzer signal duty ratio [%]

However, the following settings are prohibited:
- Settings as SNDDAT.SFRQ[7:0] bits ≤ SNDDAT.SLEN[5:0] bits
- Settings as SNDDAT.SFRQ[7:0] bits = 0x00

Table 16.4.2.1 Buzzer Frequency Settings (when f_{CLK_SNDA} = 32,768 Hz)

SNDDAT. SFRQ[7:0] bits	Frequency [Hz]	SNDDAT. SFRQ[7:0] bits	Frequency [Hz]	SNDDAT. SFRQ[7:0] bits	Frequency [Hz]	SNDDAT. SFRQ[7:0] bits	Frequency [Hz]
0x3f	512.0	0x2f	682.7	0x1f	1,024.0	0x0f	2,048.0
0x3e	520.1	0x2e	697.2	0x1e	1,057.0	0x0e	2,184.5
0x3d	528.5	0x2d	712.3	0x1d	1,092.3	0x0d	2,340.6
0x3c	537.2	0x2c	728.2	0x1c	1,129.9	0x0c	2,520.6
0x3b	546.1	0x2b	744.7	0x1b	1,170.3	0x0b	2,730.7
0x3a	555.4	0x2a	762.0	0x1a	1,213.6	0x0a	2,978.9
0x39	565.0	0x29	780.2	0x19	1,260.3	0x09	3,276.8
0x38	574.9	0x28	799.2	0x18	1,310.7	0x08	3,640.9
0x37	585.1	0x27	819.2	0x17	1,365.3	0x07	4,096.0
0x36	595.8	0x26	840.2	0x16	1,424.7	0x06	4,681.1
0x35	606.8	0x25	862.3	0x15	1,489.5	0x05	5,461.3
0x34	618.3	0x24	885.6	0x14	1,560.4	0x04	6,553.6
0x33	630.2	0x23	910.2	0x13	1,638.4	0x03	8,192.0
0x32	642.5	0x22	936.2	0x12	1,724.6	0x02	10,922.7
0x31	655.4	0x21	963.8	0x11	1,820.4	0x01	16,384.0
0x30	668.7	0x20	993.0	0x10	1,927.5	0x00	Cannot be set

Table 16.4.2.2 Buzzer Duty Ratio Setting Examples (when f_{CLK_SNDA} = 32,768 Hz)

SNDDAT. SLEN[5:0] bits	Duty ratio by buzzer frequency					
	16,384 Hz	8,192 Hz	4,096 Hz	2,048 Hz	1,024 Hz	512 Hz
0x3f	–	–	–	–	–	–
0x3e	–	–	–	–	–	98.4
0x3d	–	–	–	–	–	96.9
0x3c	–	–	–	–	–	95.3
0x3b	–	–	–	–	–	93.8
0x3a	–	–	–	–	–	92.2
0x39	–	–	–	–	–	90.6
0x38	–	–	–	–	–	89.1
0x37	–	–	–	–	–	87.5
0x36	–	–	–	–	–	85.9
0x35	–	–	–	–	–	84.4
0x34	–	–	–	–	–	82.8
0x33	–	–	–	–	–	81.3
0x32	–	–	–	–	–	79.7
0x31	–	–	–	–	–	78.1
0x30	–	–	–	–	–	76.6
0x2f	–	–	–	–	–	75.0
0x2e	–	–	–	–	–	73.4
0x2d	–	–	–	–	–	71.9
0x2c	–	–	–	–	–	70.3
0x2b	–	–	–	–	–	68.8
0x2a	–	–	–	–	–	67.2
0x29	–	–	–	–	–	65.6
0x28	–	–	–	–	–	64.1
0x27	–	–	–	–	–	62.5
0x26	–	–	–	–	–	60.9
0x25	–	–	–	–	–	59.4
0x24	–	–	–	–	–	57.8
0x23	–	–	–	–	–	56.3
0x22	–	–	–	–	–	54.7
0x21	–	–	–	–	–	53.1
0x20	–	–	–	–	–	51.6
0x1f	–	–	–	–	–	50.0
0x1e	–	–	–	–	96.9	48.4
0x1d	–	–	–	–	93.8	46.9
0x1c	–	–	–	–	90.6	45.3
0x1b	–	–	–	–	87.5	43.8
0x1a	–	–	–	–	84.4	42.2
0x19	–	–	–	–	81.3	40.6
0x18	–	–	–	–	78.1	39.1
0x17	–	–	–	–	75.0	37.5
0x16	–	–	–	–	71.9	35.9
0x15	–	–	–	–	68.8	34.4
0x14	–	–	–	–	65.6	32.8
0x13	–	–	–	–	62.5	31.3
0x12	–	–	–	–	59.4	29.7

SNDDAT. SLEN[5:0] bits	Duty ratio by buzzer frequency					
	16,384 Hz	8,192 Hz	4,096 Hz	2,048 Hz	1,024 Hz	512 Hz
0x11	–	–	–	–	56.3	28.1
0x10	–	–	–	–	53.1	26.6
0x0f	–	–	–	–	50.0	25.0
0x0e	–	–	–	93.8	46.9	23.4
0x0d	–	–	–	87.5	43.8	21.9
0x0c	–	–	–	81.3	40.6	20.3
0x0b	–	–	–	75.0	37.5	18.8
0x0a	–	–	–	68.8	34.4	17.2
0x09	–	–	–	62.5	31.3	15.6
0x08	–	–	–	56.3	28.1	14.1
0x07	–	–	–	50.0	25.0	12.5
0x06	–	–	87.5	43.8	21.9	10.9
0x05	–	–	75.0	37.5	18.8	9.4
0x04	–	–	62.5	31.3	15.6	7.8
0x03	–	–	50.0	25.0	12.5	6.3
0x02	–	75.0	37.5	18.8	9.4	4.7
0x01	–	50.0	25.0	12.5	6.3	3.1
0x00	50.0	25.0	12.5	6.3	3.1	1.6

16.4.3 Buzzer Output in One-shot Buzzer Mode

One-shot buzzer mode is provided for clicking sound and short-duration buzzer output. This mode generates a buzzer signal with the software specified frequency and duty ratio, and outputs the generated signal for the short duration specified.

An output start procedure and the SNDA operations are shown below. For the buzzer output waveform, refer to "Buzzer Output in Normal Buzzer Mode."

One-shot buzzer output start procedure

1. Set the following SNDSEL register bits:
   - Set the SNDSEL.MOSEL[1:0] bits to 0x1. (Set one-shot buzzer mode)
   - SNDSEL.STIM[3:0] bits (Set output duration)
2. Write data to the following sound buffer (SNDDAT register) bits. (Start buzzer output)
   - SNDDAT.SLEN[5:0] bits (Set buzzer output signal duty ratio)
   - SNDDAT.SFRQ[7:0] bits (Set buzzer output signal frequency)

One-shot buzzer output operations

When data is written to the sound buffer (SNDDAT register), SNDA clears the SNDINTF.EMIF bit (sound buffer empty interrupt flag) to 0 and starts buzzer output operations.

The data written to the sound buffer is loaded into the sound register in sync with the CLK_SNDA clock. At the same time, the SNDINTF.EMIF bit and SNDINTF.SBSY bit are both set to 1. The output pin outputs the buzzer signal with the frequency/duty ratio specified.

The buzzer output automatically stops when the duration specified by the SNDSEL.STIM[3:0] bits has elapsed. At the same time, the SNDINTF.EDIF bit (sound output completion interrupt flag) is set to 1 and the SNDINTF.SBSY bit is cleared to 0.

Figure 16.4.3.1 shows a buzzer output timing chart in one-shot buzzer mode.

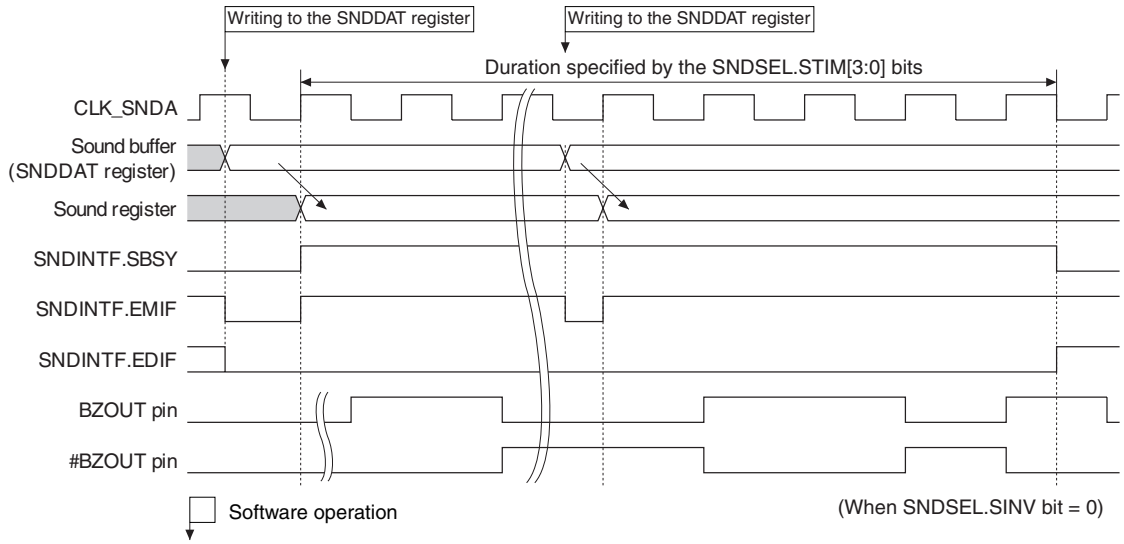


Figure 16.4.3.1 Buzzer Output Timing Chart in One-shot Buzzer Mode

16.4.4 Output in Melody Mode

Melody mode generates the buzzer signal with a melody according to the data written to the sound buffer (SNDDAT register) successively, and outputs the generated signal to outside the IC. An output start procedure and the SNDA operations are shown below.

Melody output start procedure

1. Set the following SNDSEL register bits:
   - Set the SNDSEL.MOSEL[1:0] bits to 0x2. (Set melody mode)
   - SNDSEL.STIM[3:0] bits (Set tempo)
2. Write data to the following sound buffer (SNDDAT register) bits. (Start sound output)
   - SNDDAT.MDTI bit (Set tie/slur)
   - SNDDAT.MDRS bit (Set note/rest)
   - SNDDAT.SLEN[5:0] bits (Set duration)
   - SNDDAT.SFRQ[7:0] bits (Set scale)
3. Check to see if the SNDINTF.EMIF bit is set to 1 (an interrupt can be used).
4. Repeat Steps 2 and 3 until the end of the melody.

Melody output operations

When data is written to the sound buffer (SNDDAT register), SNDA clears the SNDINTF.EMIF bit (sound buffer empty interrupt flag) to 0 and starts sound output operations.

The data written to the sound buffer is loaded into the sound register by the internal trigger signal. At the same time, the SNDINTF.EMIF bit and SNDINTF.SBSY bit are both set to 1. The output pin outputs the sound specified.

The sound output stops if data is not written to the sound buffer (SNDDAT register) until the next trigger is issued. At the same time, the SNDINTF.EDIF bit (sound output completion interrupt flag) is set to 1 and the SNDINTF.SBSY bit is cleared to 0.

Figure 16.4.4.1 shows a melody mode operation timing chart.

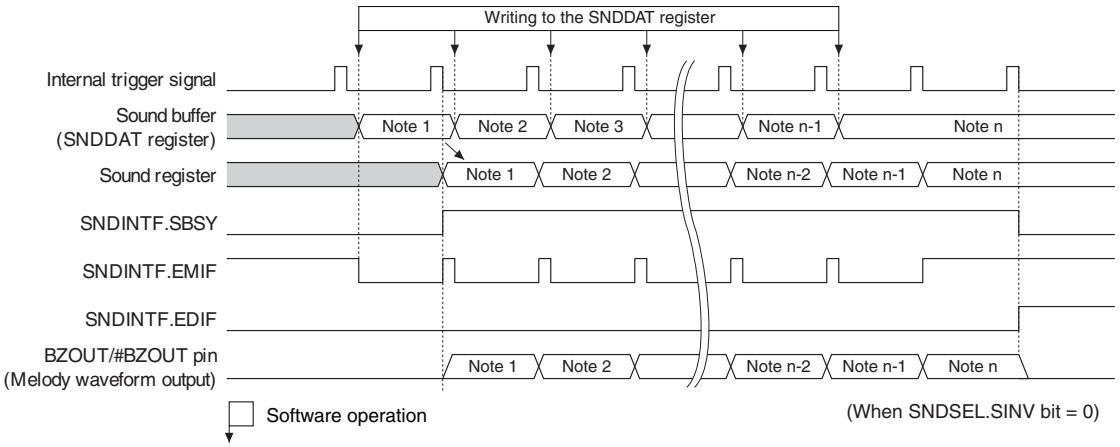


Figure 16.4.4.1 Melody Mode Operation Timing Chart

Melody output waveform configuration

Note/rest (duration) specification

Notes and rests can be specified using the SNDDAT.MDRS and SNDDAT.SLEN[5:0] bits.

Table 16.4.4.1 Note/Rest Specification (when f_{CLK_SNDA} = 32,768 Hz)

SNDDAT.SLEN[5:0] bits	SNDDAT.MDRS bit	
	0: Note	1: Rest
0x0f	Half note	Half rest
0x0b	Dotted quarter note	Dotted quarter rest
0x07	Quarter note	Quarter rest
0x05	Dotted eighth note	Dotted eighth rest
0x03	Eighth note	Eighth rest
0x01	Sixteenth note	Sixteenth rest
0x00	Thirty-second note	Thirty-second rest
Other	Setting prohibited	

Tie/slur specification

A tie or slur takes effect by setting the SNDDAT.MDTI bit to 1 and the previous note and the current note are played continuously.

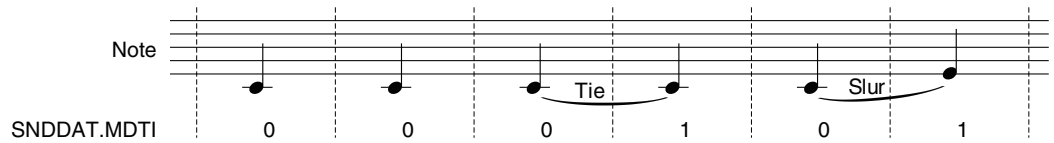


Figure 16.4.4.2 Tie and Slur

Scale specification

Scales can be specified using the SNDDAT.SFRQ[7:0] bits.

Table 16.4.4.2 Scale Specification (when f_{CLK_SNDA} = 32,768 Hz)

SNDDAT.SFRQ[7:0] bits	Scale	Frequency [Hz]
0xf8	C3	131.60
0xea	C#3	139.44
0xdd	D3	147.60
0xd1	D#3	156.04
0xc5	E3	165.49
0xba	F3	175.23
0xaf	F#3	186.18
0xa5	G3	197.40
0x9c	G#3	208.71
0x93	A3	221.41
0x8b	A#3	234.06

SNDDAT.SFRQ[7:0] bits	Scale	Frequency [Hz]
0x83	B3	248.24
0x7c	C4	262.14
0x75	C#4	277.69
0x6e	D4	295.21
0x68	D#4	312.08
0x62	E4	330.99
0x5c	F4	352.34
0x57	F#4	372.36
0x52	G4	394.80
0x4e	G#4	414.78
0x49	A4	442.81
0x45	A#4	468.11
0x41	B4	496.48
0x3d	C5	528.52
0x3a	C#5	555.39
0x37	D5	585.14
0x33	D#5	630.15
0x30	E5	668.73
0x2e	F5	697.19
0x2b	F#5	744.73
0x29	G5	780.19
0x26	G#5	840.21
0x24	A5	885.62
0x22	A#5	936.23
0x20	B5	992.97
0x1e	C6	1057.03

16.5 Interrupts

SNDA has a function to generate the interrupts shown in Table 16.5.1.

Table 16.5.1 SNDA Interrupt Function

Interrupt	Interrupt flag	Set condition	Clear condition
Sound buffer empty	SNDINTF.EMIF	When data in the sound buffer (SNDDAT register) is transferred to the sound register or 1 is written to the SNDCTL.SSTP bit	Writing to the SNDDAT register
Sound output completion	SNDINTF.EDIF	When a sound output has completed	Writing 1 or writing to the SNDDAT register

SNDA provides interrupt enable bits corresponding to each interrupt flag. An interrupt request is sent to the interrupt controller only when the interrupt flag, of which interrupt has been enabled by the interrupt enable bit, is set. For more information on interrupt control, refer to the "Interrupt Controller" chapter.

16.6 Control Registers

SNDA Clock Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SNDCLK	15–9	–	0x00	–	R	–
	8	DBRUN	0	H0	R/W	
	7	–	0	–	R	
	6–4	CLKDIV[2:0]	0x0	H0	R/W	
	3–2	–	0x0	–	R	
	1–0	CLKSRC[1:0]	0x0	H0	R/W	

Bits 15–9 Reserved

Bit 8 DBRUN

This bit sets whether the SNDA operating clock is supplied in DEBUG mode or not.

1 (R/W): Clock supplied in DEBUG mode

0 (R/W): No clock supplied in DEBUG mode

Bit 7 Reserved

Bits 6–4 CLKDIV[2:0]

These bits select the division ratio of the SNDA operating clock.

Bits 3–2 Reserved

Bits 1–0 CLKSRC[1:0]

These bits select the clock source of SNDA.

Table 16.6.1 Clock Source and Division Ratio Settings

SNDCLK. CLKDIV[2:0] bits	SNDCLK.CLKSRC[1:0] bits			
	0x0	0x1	0x2	0x3
	IOSC	OSC1	OSC3	EXOSC
0x7	Reserved	1/1	Reserved	1/1
0x6				
0x5	1/128		1/512	
0x4	1/64		1/256	
0x3	1/32		1/128	
0x2	1/16		1/64	
0x1	1/8		1/32	
0x0	1/4		1/16	

(Note) The oscillation circuits/external input that are not supported in this IC cannot be selected as the clock source.

Note: The SNDCLK register settings can be altered only when the SNDCTL.MODEN bit = 0.

SNDA Select Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SNDSEL	15–12	–	0x0	–	R	–
	11–8	STIM[3:0]	0x0	H0	R/W	
	7–3	–	0x00	–	R	
	2	SINV	0	H0	R/W	
	1–0	MOSEL[1:0]	0x0	H0	R/W	

Bits 15–12 Reserved

Bits 11–8 STIM[3:0]

These bits select a tempo (when melody mode is selected) or a one-shot buzzer output duration (when one-shot buzzer mode is selected).

Table 16.6.2 Tempo/One-shot Buzzer Output Duration Selections (when f_{CLK_SNDA} = 32,768 Hz)

SNDSEL. STIM[3:0] bits	Tempo (= Quarter note/minute)	One-shot buzzer output duration [ms]
0xf	30	250.0
0xe	32	234.4
0xd	34.3	218.8
0xc	36.9	203.1
0xb	40	187.5
0xa	43.6	171.9
0x9	48	156.3
0x8	53.3	140.6
0x7	60	125.0
0x6	68.6	109.4
0x5	80	93.8
0x4	96	78.1
0x3	120	62.5
0x2	160	46.9
0x1	240	31.3
0x0	480	15.6

Note: Be sure to avoid altering these bits when SNDINTF.SBSY bit = 1.

Bits 7–3 Reserved

Bit 2 SINV

This bit selects an output pin drive mode.
1 (R/W): Normal drive mode
0 (R/W): Direct drive mode

For more information, refer to "Output Pin Drive Mode."

Bits 1–0 MOSEL[1:0]

These bits select a sound output mode.

Table 16.6.3 Sound Output Mode Selection

SNDSEL.MOSEL[1:0] bits	Sound output mode
0x3	Reserved
0x2	Melody mode
0x1	One-shot buzzer mode
0x0	Normal buzzer mode

SNDA Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SNDCTL	15–9	–	0x00	–	R	–
	8	SSTP	0	H0	R/W	
	7–1	–	0x00	–	R	
	0	MODEN	0	H0	R/W	

Bits 15–9 Reserved

Bit 8 SSTP

This bit stops sound output.
1 (W): Stop sound output
0 (W): Ineffective
1 (R): In stop process
0 (R): Stop process completed/Idle

The SNDCTL.SSTP bit is used to stop buzzer output in normal buzzer mode. After 1 is written, this bit is cleared to 0 when the sound output has completed. Also in one-shot buzzer mode/melody mode, writing 1 to this bit can forcibly terminate the sound output.

Bits 7–1 Reserved

Bit 0 MODEN

This bit enables the SNDA operations.
1 (R/W): Enable SNDA operations (The operating clock is supplied.)
0 (R/W): Disable SNDA operations (The operating clock is stopped.)

SNDA Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SNDDAT	15	MDTI	0	H0	R/W	–
	14	MDRS	0	H0	R/W	
	13–8	SLEN[5:0]	0x00	H0	R/W	
	7–0	SFRQ[7:0]	0xff	H0	R/W	

This register functions as a sound buffer. Writing data to this register starts sound output. For detailed information on the setting data, refer to "Buzzer output waveform configuration (normal buzzer mode/one-shot buzzer mode)" and "Melody output waveform configuration."

Bit 15 MDTI

This bit specifies a tie or slur (continuous play with the previous note) in melody mode.
1 (R/W): Enable tie/slur
0 (R/W): Disable tie/slur

This bit is ignored in normal buzzer mode/one-shot buzzer mode.

Bit 14 MDRS

This bit selects the output type in melody mode from a note or a rest .

1 (R/W): Rest

0 (R/W): Note

When a rest is selected, the BZOUT pin goes low and the #BZOUT pin goes high during the output duration. This bit is ignored in normal buzzer mode/one-shot buzzer mode.

Bits 13–8 SLEN[5:0]

These bits select a duration (when melody mode is selected) or a buzzer signal duty ratio (when normal buzzer mode/one-shot buzzer mode is selected).

Bits 7–0 SFRQ[7:0]

These bits select a scale (when melody mode is selected) or a buzzer signal frequency (when normal buzzer mode/one-shot buzzer mode is selected).

Notes: • In normal buzzer mode/one-shot buzzer mode, only the low-order 6 bits (SNDDAT.SFRQ[5:0] bits) are effective within the SNDDAT.SFRQ[7:0] bits. Always set the SNDDAT.SFRQ[7:6] bits to 0x0.

• The SNDDAT register allows 16-bit data writing only. Data writings in 8-bit size will be ignored.

SNDA Interrupt Flag Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SNDINTF	15–9	–	0x00	–	R	–
	8	SBSY	0	H0	R	
	7–2	–	0x00	–	R	
	1	EMIF	1	H0	R	Cleared by writing to the SNDDAT register.
	0	EDIF	0	H0	R/W	Cleared by writing 1 or writing to the SNDDAT register.

Bits 15–9 Reserved

Bit 8 SBSY

This bit indicates the sound output status. (See Figures 16.4.2.1, 16.4.3.1, and 16.4.4.1.)

1 (R): Outputting

0 (R): Idle

Bits 7–2 Reserved

Bit 1 EMIF

Bit 0 EDIF

These bits indicate the SNDA interrupt cause occurrence status.

1 (R): Cause of interrupt occurred

0 (R): No cause of interrupt occurred

1 (W): Clear flag

0 (W): Ineffective

The following shows the correspondence between the bit and interrupt:

SNDINTF.EMIF bit: Sound buffer empty interrupt

SNDINTF.EDIF bit: Sound output completion interrupt

SNDA Interrupt Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SNDINTE	15–8	–	0x00	–	R	–
	7–2	–	0x00	–	R	
	1	EMIE	0	H0	R/W	
	0	EDIE	0	H0	R/W	

Bits 15–2 Reserved

Bit 1 EMIE
Bit 0 EDIE

These bits enable SNDA interrupts.
1 (R/W): Enable interrupts
0 (R/W): Disable interrupts

The following shows the correspondence between the bit and interrupt:
SNDINTE.EMIE bit: Sound buffer empty interrupt
SNDINTE.EDIE bit: Sound output completion interrupt

17 12-bit A/D Converter (ADC12A)

17.1 Overview

The ADC12A is a successive approximation type 12-bit A/D converter.
The features of the ADC12A are listed below.

- Conversion method: Successive approximation type
- Resolution: 12 bits
- Analog input voltage range: Reference voltage VREFA to Vss
- Supports two conversion modes: 1. One-time conversion mode
  2. Continuous conversion mode
- Supports three conversion triggers: 1. Software trigger
  2. 16-bit timer underflow trigger
  3. External trigger
- Can convert multiple analog input signals sequentially.
- Can generate conversion completion and overwrite error interrupts.

Figure 17.1.1 shows the ADC12A configuration.

Table 17.1.1 ADC12A Configuration of S1C17F63

Item	S1C17F63
Number of channels	1 channel (Ch.0)
Number of analog signal inputs per channel	Ch.0: 8 inputs (ADIN00–ADIN06, (ADIN07 *1))
16-bit timer used as conversion clock and trigger sources	Ch.0 ← 16-bit timer Ch.2
VREFA pin (reference voltage input)	Can be input externally or generated internally *2

*1 ADIN07 is connected to the internal temperature sensor output.
*2 The reference voltage generator output can be input as the reference voltage.
For more information, refer to the "Temperature Sensor/Reference Voltage Generator" chapter.

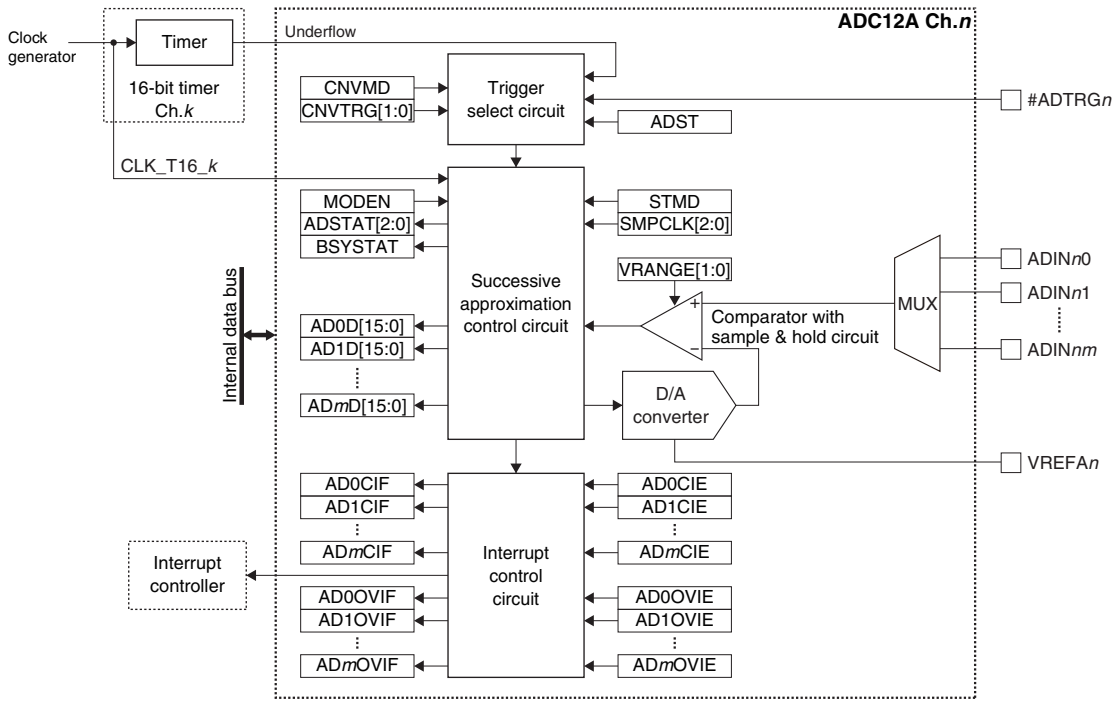


Figure 17.1.1 ADC12A Configuration

Note: In this chapter, *n*, *m*, and *k* refer to an ADC12A channel number, an analog input pin number, and a 16-bit timer channel number, respectively.

17.2 Input Pins and External Connections

17.2.1 List of Input Pins

Table 17.2.1.1 lists the ADC12A pins.

Table 17.2.1.1 List of ADC12A Pins

Pin name	I/O*	Initial status*	Function
ADIN*nm*	A	Hi-Z	Analog signal input
#ADTRG*n*	I	I	External trigger input
VREFA*n*	A	Hi-Z	Reference voltage input

* Indicates the status when the pin is configured for the ADC12A.

If the port is shared with the ADC12A pin and other functions, the ADC12A input function must be assigned to the port before activating the ADC12A. For more information, refer to the "I/O Ports" chapter.

17.2.2 External Connections

Figure 17.2.2.1 shows a connection diagram between the ADC12A and external devices.

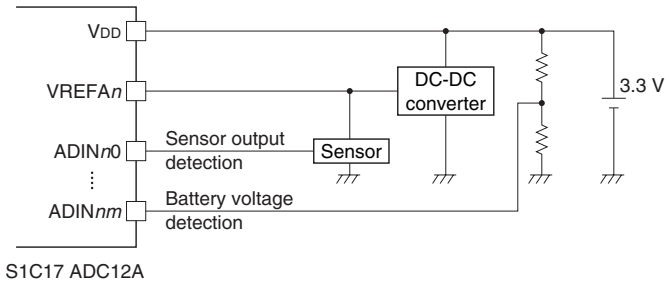


Figure 17.2.2.1 Connections between ADC12A and External Devices

17.3 Clock Settings

17.3.1 ADC12A Operating Clock

The 16-bit timer Ch.*k* operating clock CLK_T16_*k* is also used as the ADC12A operating clock. For more information on the CLK_T16_*k* settings and clock supply in SLEEP and DEBUG modes, refer to "Clock Settings" in the "16-bit Timers" chapter.

Note: When the CLK_T16_*k* supply stops during A/D conversion (e.g., when the CPU enters SLEEP or DEBUG mode), correct conversion results cannot be obtained even if the clock supply is resumed after that. In this case, perform A/D conversion again.

17.3.2 Sampling Time

The ADC12A includes a sample and hold circuit. The sampling time must be set so that it will satisfy the time required for acquiring input voltage (t_{ACQ}: acquisition time). Figure 17.3.2.1 shows an equivalent circuit of the analog input portion.

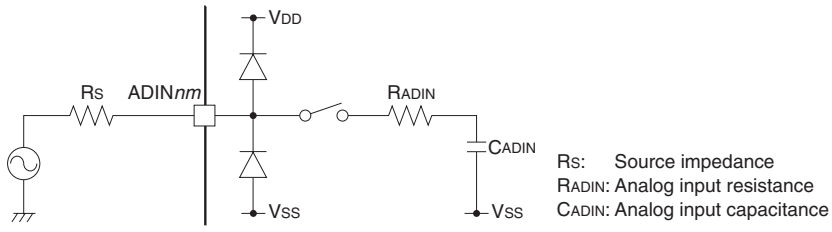


Figure 17.3.2.1 Equivalent Circuit of Analog Input Portion

For the RADIN and CADIN values in the equivalent circuit, refer to "12-bit A/D Converter Characteristics" in the "Electrical Characteristics" chapter. Based on these values, configure the ADC12A operating clock CLK_T16_*k* and the ADC12_*n*TRG.SMPCLK[2:0] bits that set the sampling time so that these settings will satisfy the equations shown below.

$$t_{ACQ} = 8 \times (R_S + R_{ADIN}) \times C_{ADIN} \quad \text{(Eq. 17.1)}$$

$$\frac{1}{f_{CLK\_ADC}} \times SMPCLK > t_{ACQ} \quad \text{(Eq. 17.2)}$$

Where

f_{CLK_ADC}: CLK_T16_*k* frequency [Hz]

SMPCLK: Sampling time = ADC12_*n*TRG.SMPCLK[2:0] bit-setting (4 to 11 CLK_T16_*k* cycles)

The following shows the relationship between the sampling time and the maximum sampling rate.

$$\text{Maximum sampling rate [sps]} = \frac{f_{CLK\_ADC}}{SMPCLK + 13} \quad \text{(Eq. 17.3)}$$

17.4 Operations

17.4.1 Initialization

The ADC12A should be initialized with the procedure shown below.

1. Assign the ADC12A input function to the ports. (Refer to the "I/O Ports" chapter.)
2. Configure the 16-bit timer Ch.*k* operating clock so that it will satisfy the sampling time.
3. Set the ADC12_*n*CTL.MODEN bit to 1. (Enable ADC12A operations)
4. Configure the following ADC12_*n*TRG register bits:
   - ADC12_*n*TRG.SMPCLK[2:0] bits (Set sampling time)
   - ADC12_*n*TRG.CNVTRG[1:0] bits (Select conversion start trigger source)
   - ADC12_*n*TRG.CNVMD bit (Set conversion mode)
   - ADC12_*n*TRG.STMD bit (Set data storing mode)
   - ADC12_*n*TRG.STAAIN[2:0] bits (Set analog input pin to be A/D converted first)
   - ADC12_*n*TRG.ENDAIN[2:0] bits (Set analog input pin to be A/D converted last)
5. Set the ADC12_*n*CFG.VRANGE[1:0] bits. (Set operating voltage range according to VDD)
6. Set the following bits when using the interrupt:
   - Write 1 to the interrupt flags in the ADC12_*n*INTF register. (Clear interrupt flags)
   - Set the interrupt enable bits in the ADC12_*n*INTE register to 1. (Enable interrupts)

17.4.2 Conversion Start Trigger Source

The trigger source, which starts A/D conversion, can be selected from the three types shown below using the ADC12_*n*TRG.CNVTRG[1:0] bits.

External trigger (#ADTRG*n* pin)

Writing 1 to the ADC12_*n*CTL.ADST bit enables the ADC12A to accept trigger inputs. After that, the falling edge of the signal input to the #ADTRG*n* pin starts A/D conversion.

16-bit timer Ch.*k* underflow trigger

Writing 1 to the ADC12_*n*CTL.ADST bit enables the ADC12A to accept trigger inputs. After that, A/D conversion is started when an underflow occurs in the 16-bit timer Ch.*k*.

Software trigger

Writing 1 to the ADC12_*n*CTL.ADST bit starts A/D conversion.

Trigger inputs can be accepted while the ADC12_*n*CTL.BSYSTAT bit is set to 0 and are ignored while set to 1.
A/D conversion is actually started in sync with CLK_T16_*k* after a trigger is accepted.
Writing 0 to the ADC12_*n*CTL.ADST bit stops A/D conversion after the one currently being executed has completed.

17.4.3 Conversion Mode and Analog Input Pin Settings

The ADC12A can be put into two conversion modes shown below using the ADC12_*n*TRG.CNVMD bit. Each mode allows setting of analog input pin range to be A/D converted. The analog input pin range can be set using the ADC12_*n*TRG.STAAIN[2:0] bits for specifying the first analog input pin and the ADC12_*n*TRG.ENDAIN[2:0] bits for specifying the last analog input pin. The analog input signals within the specified range are A/D converted successively in ascending order of the pin numbers.

One-time conversion mode

Once the ADC12A executes A/D conversion for all the analog input signals within the specified range, it is automatically stopped.

Continuous conversion mode

The ADC12A repeatedly executes A/D conversion within the specified range until 0 is written to the ADC12_*n*CTL.ADST bit.

17.4.4 A/D Conversion Operations and Control Procedures

The following shows A/D conversion control procedures and the ADC12A operations.

Control procedure in one-time conversion mode

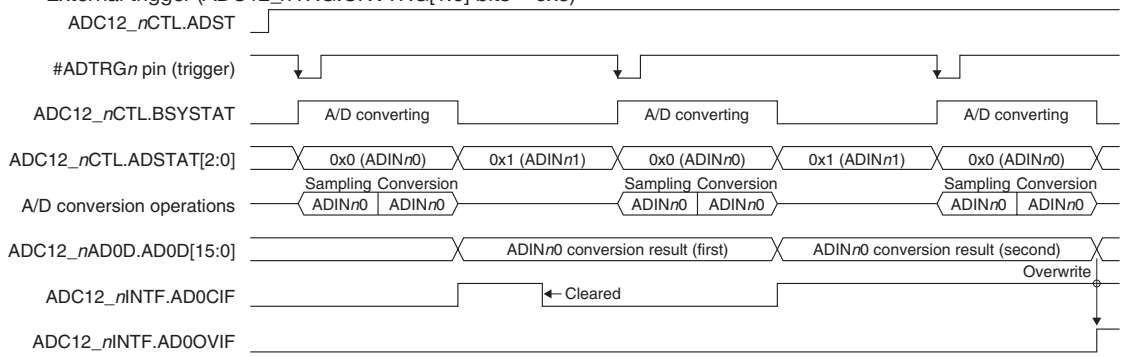
1. Write 1 to the ADC12_*n*CTL.ADST bit.
2. Wait for an ADC12A interrupt.
   i. If the ADC12_*n*INTF.AD*m*CIF bit = 1 (analog input signal *m* A/D conversion completion interrupt), clear the ADC12_*n*INTF.AD*m*CIF bit and then go to Step 3.
   ii. If the ADC12_*n*INTF.AD*m*OVIF bit = 1 (analog input signal *m* A/D conversion result overwrite error interrupt), clear the ADC12_*n*INTF.AD*m*OVIF bit and terminate as an error or retry A/D conversion.
3. Read the A/D conversion result of the analog input *m* (ADC12_*n*AD*m*D.AD*m*D[15:0] bits).
   * The 12-bit conversion results are located at the low-order 12 bits or high-order 12-bits within the ADC12_*n*AD*m*D.AD*m*D[15:0] bits according to the ADC12_*n*TRG.STMD bit setting.
4. Repeat Steps 2 and 3 until A/D conversion for all the analog input pins within the specified range is completed.
5. To forcefully terminate the A/D conversion being executed, write 0 to the ADC12_*n*CTL.ADST bit.
   The ADC12A stops operating after the A/D conversion currently being executed has completed.

   The ADC12_*n*CTL.ADST bit must be cleared by writing 0 even if A/D conversion is completed and automatically stopped.

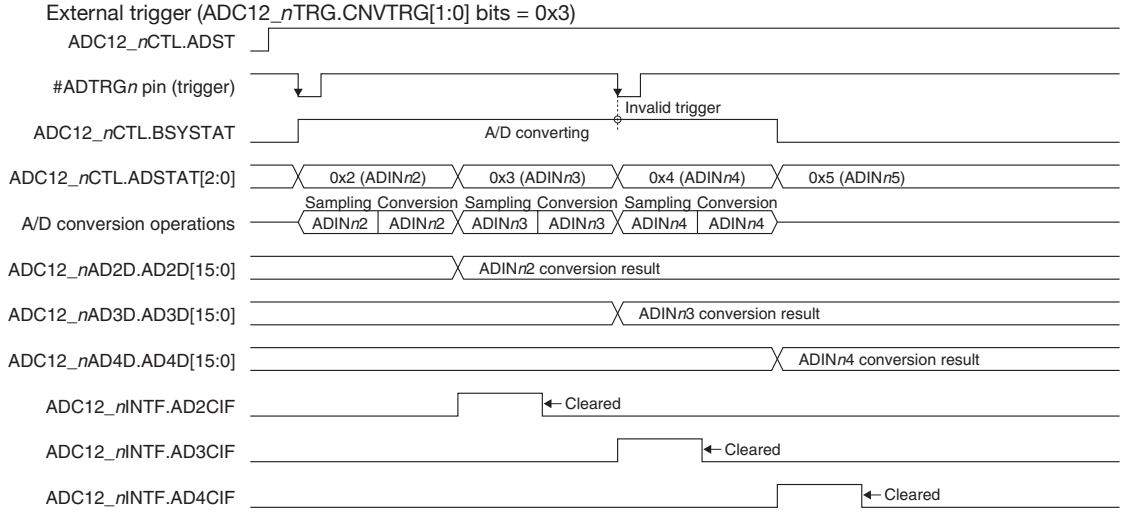
Control procedure in continuous conversion mode

1. Write 1 to the ADC12_*n*CTL.ADST bit.
2. Wait for an ADC12A interrupt.
   i. If the ADC12_*n*INTF.AD*m*CIF bit = 1 (analog input signal *m* A/D conversion completion interrupt), clear the ADC12_*n*INTF.AD*m*CIF bit and then go to Step 3.
   ii. If the ADC12_*n*INTF.AD*m*OVIF bit = 1 (analog input signal *m* A/D conversion result overwrite error interrupt), clear the ADC12_*n*INTF.AD*m*OVIF bit and terminate as an error or retry A/D conversion.
3. Read the A/D conversion result of the analog input *m* (ADC12_*n*AD*m*D.AD*m*D[15:0] bits).
4. Repeat Steps 2 and 3 until terminating A/D conversion.
5. Write 0 to the ADC12_*n*CTL.ADST bit.
   The ADC12A stops operating after the A/D conversion currently being executed has completed.

(1) One-time conversion mode (ADC12_*n*TRG.CNVMD bit = 0)
A/D conversion for ADIN*n*0 (ADC12_*n*TRG.STAAIN[2:0] bits = 0x0, ADC12_*n*TRG.ENDAIN[2:0] bits = 0x0)
External trigger (ADC12_*n*TRG.CNVTRG[1:0] bits = 0x3)



(2) One-time conversion mode (ADC12_*n*TRG.CNVMD bit = 0)
A/D conversion for ADIN*n*2–4 (ADC12_*n*TRG.STAAIN[2:0] bits = 0x2, ADC12_*n*TRG.ENDAIN[2:0] bits = 0x4)
External trigger (ADC12_*n*TRG.CNVTRG[1:0] bits = 0x3)



(3) Continuous conversion mode (ADC12_*n*TRG.CNVMD bit = 1)
A/D conversion for ADIN*n*3–4 (ADC12_*n*TRG.STAAIN[2:0] bits = 0x3, ADC12_*n*TRG.ENDAIN[2:0] bits = 0x4)
Software trigger (ADC12_*n*TRG.CNVTRG[1:0] bits = 0x0)

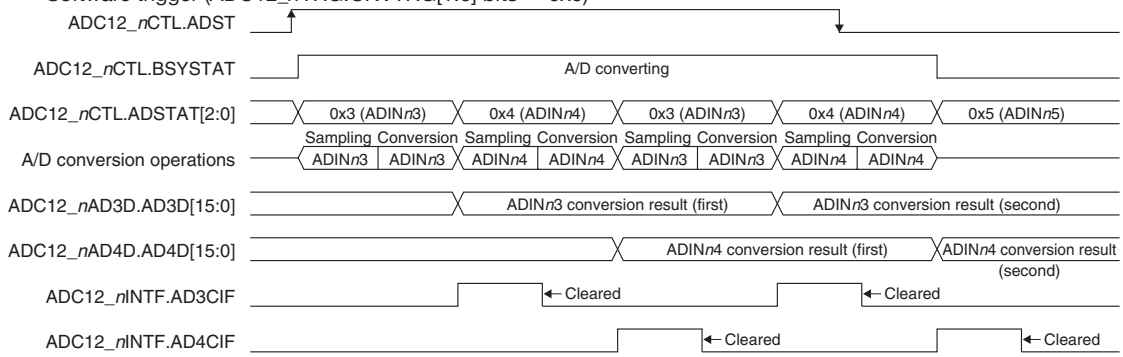


Figure 17.4.4.1 A/D Conversion Operations

17.5 Interrupts

The ADC12A has a function to generate the interrupts shown in Table 17.5.1.

Table 17.5.1 ADC12A Interrupt Function

Interrupt	Interrupt flag	Set condition	Clear condition
Analog input signal *m* A/D conversion completion	ADC12_*n*INTF.AD*m*CIF	When an analog input signal *m* A/D conversion result is loaded to the ADC12_*n*AD*m*D register	Writing 1
Analog input signal *m* A/D conversion result overwrite error	ADC12_*n*INTF.AD*m*OVIF	When a new A/D conversion result is loaded to the ADC12_*n*AD*m*D register while the ADC12_*n*INTF.AD*m*CIF bit = 1	Writing 1

Note that the A/D conversion continues even if an A/D conversion result overwrite error has occurred. A/D conversion result overwrite errors are decided regardless of whether the ADC12_*n*AD*m*D register has been read or not.

The ADC12A provides interrupt enable bits corresponding to each interrupt flag. An interrupt request is sent to the interrupt controller only when the interrupt flag, of which interrupt has been enabled by the interrupt enable bit, is set. For more information on interrupt control, refer to the "Interrupt Controller" chapter.

17.6 Control Registers

ADC12A Ch.*n* Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
ADC12_*n*CTL	15	–	0	–	R	–
	14–12	ADSTAT[2:0]	0x0	H0	R	
	11	–	0	–	R	
	10	BSYSTAT	0	H0	R	
	9–8	–	0x0	–	R	
	7–2	–	0x00	–	R	
	1	ADST	0	H0	R/W	
	0	MODEN	0	H0	R/W	

Bit 15 Reserved

Bits 14–12 ADSTAT[2:0]

These bits indicate the analog input pin number *m* being A/D converted.

Table 17.6.1 Relationship Between Control Bit Value and Analog Input Pin

ADC12_*n*CTL.ADSTAT[2:0] bits ADC12_*n*TRG.STAAIN[2:0] bits ADC12_*n*TRG.ENDAIN[2:0] bits	Analog input pin
0x7	ADIN*n*7
0x6	ADIN*n*6
0x5	ADIN*n*5
0x4	ADIN*n*4
0x3	ADIN*n*3
0x2	ADIN*n*2
0x1	ADIN*n*1
0x0	ADIN*n*0

These bits indicate the last converted analog input pin number after A/D conversion is forcefully terminated by writing 0 to the ADC12_*n*CTL.ADST bit or automatically terminated in one-time conversion mode (ADC12_*n*TRG.CNVMD = 0). If A/D conversion is stopped after the maximum analog input pin number (different in each model) has been completed, these bits indicate ADIN*n*0.

Bit 11 Reserved

Bit 10 BSYSTAT

This bit indicates whether the ADC12A is executing A/D conversion or not.
1 (R/W): A/D converting
0 (R/W): Idle

Bits 9–2 Reserved

Bit 1 ADST

This bit starts A/D conversion or enables to accept triggers.
1 (R/W): Start sampling and conversion (software trigger)/
Enable trigger acceptance (external trigger, 16-bit timer underflow trigger)
0 (R/W): Terminate conversion

This bit does not revert to 0 automatically after A/D conversion has completed. Write 0 to this bit once and write 1 again to start another A/D conversion. After 0 is written to this bit to forcefully terminate conversion, the ADC12A stops after the A/D conversion being executed is completed. Therefore, this bit cannot be used to determine whether the ADC12A is executing A/D conversion or not.

Note: The data written to the ADC12_*n*CTL.ADST bit must be retained for one or more CLK_T16_*k* clock cycles when 1 is written or two or more CLK_T16_*k* clock cycles when 0 is written.

Bit 0 MODEN

This bit enables the ADC12A operations.
1 (R/W): Enable ADC12A operations (The operating clock is supplied.)
0 (R/W): Disable ADC12A operations (The operating clock is stopped.)

Note: After 0 is written to the ADC12_*n*CTL.MODEN bit, the ADC12A executes a terminate processing. Before the clock source is deactivated, read the ADC12_*n*CTL.MODEN bit to make sure that it is set to 0.

ADC12A Ch.*n* Trigger/Analog Input Select Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
ADC12_*n*TRG	15–14	–	0x0	–	R	–
	13–11	ENDAIN[2:0]	0x0	H0	R/W	
	10–8	STAAIN[2:0]	0x0	H0	R/W	
	7	STMD	0	H0	R/W	
	6	CNVMD	0	H0	R/W	
	5–4	CNVTRG[1:0]	0x0	H0	R/W	
	3	–	0	–	R	
	2–0	SMPCLK[2:0]	0x7	H0	R/W	

Note: Make sure that the ADC12_*n*CTL.BSYSTAT bit is set to 0 before altering the ADC12_*n*TRG register.

Bits 15–14 Reserved

Bits 13–11 ENDAIN[2:0]

These bits set the analog input pin to be A/D converted last.
See Table 17.6.1 for the relationship between analog input pins and bit setting values.

Note: The analog input pin range to perform A/D conversion must be set as ADC12_*n*TRG.ENDAIN[2:0] bits ≥ ADC12_*n*TRG.STAAIN[2:0] bits.

Bits 10–8 STAAIN[2:0]

These bits set the analog input pin to be A/D converted first.
See Table 17.6.1 for the relationship between analog input pins and bit setting values.

Bit 7 STMD

This bit selects the data alignment when the conversion results are loaded into the A/D conversion result registers (ADC12_*n*AD*m*D.AD*m*D[15:0] bits).

1 (R/W): Left justify

0 (R/W): Right justify

All the A/D conversion result registers change their data alignment immediately after this bit is altered. This does not affect the conversion results.

ADC12_*n*AD*m*D.AD*m*D[15:0] bits

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Left justified (ADC12_*n*TRG.STMD bit = 1)	(MSB)											(LSB)	0	0	0	0
Right justified (ADC12_*n*TRG.STMD bit = 0)	0	0	0	0	(MSB)											(LSB)

Figure 17.6.1 Conversion Data Alignment

Bit 6 CNVMD

This bit sets the A/D conversion mode.

1 (R/W): Continuous conversion mode

0 (R/W): One-time conversion mode

Bits 5–4 CNVTRG[1:0]

These bits select a trigger source to start A/D conversion.

Table 17.6.2 Trigger Source Selection

ADC12_*n*TRG.CNVTRG[1:0] bits	Trigger source
0x3	#ADTRG*n* pin (external trigger)
0x2	Reserved
0x1	16-bit timer Ch.*k* underflow
0x0	ADC12_*n*CTL.ADST bit (software trigger)

Bit 3 Reserved

Bits 2–0 SMPCLK[2:0]

These bits set the analog input signal sampling time.

Table 17.6.3 Sampling Time Settings

ADC12_*n*TRG.SMPCLK[2:0] bits	Sampling time (Number of CLK_T16_*k* cycles)
0x7	11 cycles
0x6	10 cycles
0x5	9 cycles
0x4	8 cycles
0x3	7 cycles
0x2	6 cycles
0x1	5 cycles
0x0	4 cycles

ADC12A Ch.*n* Configuration Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
ADC12_*n*CFG	15–8	–	0x00	–	R	–
	7–2	–	0x00	–	R	
	1–0	VRANGE[1:0]	0x0	H0	R/W	

Note: Make sure that the ADC12_*n*CTL.BSYSTAT bit is set to 0 before altering the ADC12_*n*CFG register.

Bits 15–2 Reserved

Bits 1–0 VRANGE[1:0]

These bits set the A/D converter operating voltage range.

Table 17.6.4 A/D Converter Operating Voltage Range Setting

ADC12_*n*CFG.VRANGE[1:0] bits	A/D converter operating voltage range
0x3	1.8 to 5.5 V
0x2	3.6 to 5.5 V
0x1	4.8 to 5.5 V
0x0	Conversion disabled

Notes: • A/D conversion will not be performed if the ADC12_*n*CFG.VRANGE[1:0] bits = 0x0. Set these bits to the value according to the operating voltage to perform A/D conversion.

• Be aware that ADC circuit current I_{ADC} flows if the ADC12_*n*CFG.VRANGE[1:0] bits are set to a value other than 0x0 when the ADC12_*n*CTL.BSYSTAT bit = 1.

ADC12A Ch.*n* Interrupt Flag Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
ADC12_*n*INTF	15	AD7OVIF	0	H0	R/W	Cleared by writing 1.
	14	AD6OVIF	0	H0	R/W	
	13	AD5OVIF	0	H0	R/W	
	12	AD4OVIF	0	H0	R/W	
	11	AD3OVIF	0	H0	R/W	
	10	AD2OVIF	0	H0	R/W	
	9	AD1OVIF	0	H0	R/W	
	8	AD0OVIF	0	H0	R/W	
	7	AD7CIF	0	H0	R/W	
	6	AD6CIF	0	H0	R/W	
	5	AD5CIF	0	H0	R/W	
	4	AD4CIF	0	H0	R/W	
	3	AD3CIF	0	H0	R/W	
	2	AD2CIF	0	H0	R/W	
	1	AD1CIF	0	H0	R/W	
	0	AD0CIF	0	H0	R/W	

Bits 15–8 AD*m*OVIF
Bits 7–0 AD*m*CIF

These bits indicate the ADC12A interrupt cause occurrence status.
1 (R): Cause of interrupt occurred
0 (R): No cause of interrupt occurred
1 (W): Clear flag
0 (W): Ineffective

The following shows the correspondence between the bit and interrupt:
ADC12_*n*INTF.AD*m*OVIF bit: Analog input signal *m* A/D conversion result overwrite error interrupt
ADC12_*n*INTF.AD*m*CIF bit: Analog input signal *m* A/D conversion completion interrupt

ADC12A Ch.*n* Interrupt Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
ADC12_*n*INTE	15	AD7OVIE	0	H0	R/W	–
	14	AD6OVIE	0	H0	R/W	
	13	AD5OVIE	0	H0	R/W	
	12	AD4OVIE	0	H0	R/W	
	11	AD3OVIE	0	H0	R/W	
	10	AD2OVIE	0	H0	R/W	
	9	AD1OVIE	0	H0	R/W	
	8	AD0OVIE	0	H0	R/W	
	7	AD7CIE	0	H0	R/W	
	6	AD6CIE	0	H0	R/W	
	5	AD5CIE	0	H0	R/W	
	4	AD4CIE	0	H0	R/W	
	3	AD3CIE	0	H0	R/W	
	2	AD2CIE	0	H0	R/W	
	1	AD1CIE	0	H0	R/W	
	0	AD0CIE	0	H0	R/W	

Bits 15–8 AD*m*OVIE
Bits 7–0 AD*m*CIE

These bits enable ADC12A interrupts.
1 (R/W): Enable interrupts
0 (R/W): Disable interrupts

The following shows the correspondence between the bit and interrupt:
ADC12_*n*INTE.AD*m*OVIE bit: Analog input signal *m* A/D conversion result overwrite error interrupt
ADC12_*n*INTE.AD*m*CIE bit: Analog input signal *m* A/D conversion completion interrupt

ADC12A Ch.*n* Result Register *m*

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
ADC12_*n*AD*m*D	15–0	AD*m*D[15:0]	0x0000	H0	R	–

Bits 15–0 AD*m*D[15:0]

These bits are the A/D conversion results of the analog input signal *m*.

18 Temperature Sensor/Reference Voltage Generator (TSRVR)

18.1 Overview

The TSRVR is a peripheral circuit for the internal A/D converter that outputs the internal temperature sensor detection values and generates the reference voltage. The features of the TSRVR are listed below.

- Includes a temperature sensor that has a linear output characteristic and the sensor output can be measured using the internal A/D converter without external components being attached.
- Can supply a reference voltage (2.0 V, 2.5 V, or VDD selectable) to the internal A/D converter.
- Can supply the reference voltage generated in this circuit to external devices if this IC has the VREFA exclusive pin.

Figure 18.1.1 shows the TSRVR configuration.

Table 18.1.1 TSRVR Configuration of S1C17F63

Item	S1C17F63
Number of channels	1 channel (Ch.0)
Correspondence between TSRVR and internal A/D converter channels	TSRVR Ch.0 → ADC12A Ch.0
A/D converter input connected to temperature sensor	ADIN07
Reference voltage output to external devices	Unavailable

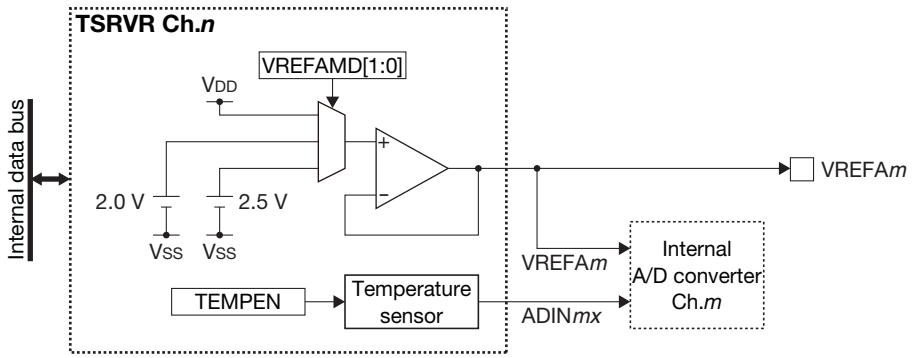


Figure 18.1.1 TSRVR Configuration

Note: In this chapter, *n* and *m* refer to a TSRVR channel number and an internal A/D converter channel number, respectively.

18.2 Output Pin and External Connections

18.2.1 Output Pin

Table 18.2.1.1 shows the TSRVR pin.

Table 18.2.1.1 TSRVR Pin

Pin name	I/O	Initial status	Function
VREFA*m*	A	Hi-Z	Reference voltage output

If the port is shared with the TSRVR pin and other functions, the TSRVR output function must be assigned to the port before activating the TSRVR. For more information, refer to the "I/O Ports" chapter.

18.2.2 External Connections

Figure 18.2.2.1 shows connection diagrams between the TSRVR and external components.

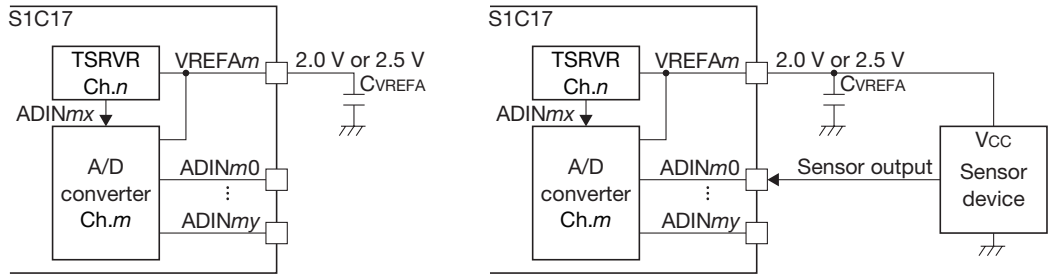


Figure 18.2.2.1 Connections between TSRVR and External Components

18.3 Operations

TSRVR should be configured before starting measurements using the internal A/D converter.

18.3.1 Reference Voltage Setting

The TSRVR output voltage can be supplied to the internal A/D converter as the reference voltage VREFA*m* when it is not supplied externally. The output voltage can be selected using the TSRVR*n*VCTL.VREFAMD[1:0] bits. Connect CVREFA to the VREFA*m* pin when supplying the reference voltage from TSRVR. A/D conversion by the internal A/D converter should be started after the reference voltage stabilization time tVREFA has elapsed from the time when the output voltage is selected.

18.3.2 Temperature Sensor Setting

The temperature sensor output voltage can be directly measured using the internal A/D converter. The measurement should be started after the temperature sensor output stabilization time tTEMP has elapsed from writing 1 to the TSRVR*n*TCTL.TEMPEN bit to activate the temperature sensor.
From the temperature sensor output voltage, the measured temperature can be calculated by the equations shown below.

$$T_{SEN} = \frac{(V_{TSEN} - V_{TREF}) \times 1{,}000}{\Delta V_{TEMP}} + T_{REF} \qquad \text{(Eq. 18.1)}$$

Where

- T_{SEN}: Actual temperature [°C]
- V_{TSEN}: Temperature sensor output voltage at temperature T_{SEN} [V]
- T_{REF}: Reference temperature for calibration [°C]
- V_{TREF}: Temperature sensor output voltage at temperature T_{REF} [V]
- ΔV_{TEMP}: Temperature sensor output voltage temperature coefficient [mV/°C] (Refer to the "Electrical Characteristics" chapter.)

Convert the digital values corresponding to the respective temperatures, that are obtained by the internal A/D converter, into voltage values and assign them to VTSEN and VTREF.

$$V_{(TSEN,\,TREF)} = \frac{ADD}{4{,}096} \times V_{REFA} \qquad \text{(Eq. 18.2)}$$

Where

- ADD: A/D conversion result at temperature T_{SEN} or T_{REF} (decimal)
- V_{REFA}: A/D converter reference voltage [V]

For details of the internal A/D converter, refer to the "12-bit A/D Converter" chapter.

18.4 Control Registers

TSRVR Ch.*n* Temperature Sensor Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
TSRVR*n*TCTL	15–8	–	0x00	–	R	–
	7–1	–	0x00	H0	R	
	0	TEMPEN	0	H0	R/W	

Bits 15–1 Reserved

Bit 0 TEMPEN

This bit enables the temperature sensor operation.

1 (R/W): Enable temperature sensor output

0 (R/W): Disable temperature sensor output

TSRVR Ch.*n* Reference Voltage Generator Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
TSRVR*n*VCTL	15–8	–	0x00	–	R	–
	7–2	–	0x00	H0	R	
	1–0	VREFAMD[1:0]	0x0	H0	R/W	

Bits 15–2 Reserved

Bits 1–0 VREFAMD[1:0]

These bits set the reference voltage generator output voltage.

Table 18.4.1 Output Voltage Settings

TSRVR*n*VCTL.VREFAMD[1:0] bits	Output voltage
0x3	2.5 V output
0x2	2.0 V output
0x1	V_{DD} level output
0x0	Hi-Z (An external voltage can be applied.)

Notes: • Be aware that VREFA operating current I_{VREFA} flows when the TSRVR*n*VCTL.VREFAMD[1:0] bits are set to 0x2 or 0x3.

• When the TSRVR*n*VCTL.VREFAMD[1:0] bits are not set to 0x0, do not apply an external voltage to the VREFA*m* pin.

19 EPD Controller/Driver (EPDC)

19.1 Overview

The EPDC is an EPD controller/driver to implement EPD display control functions.
The features of the EPDC are listed below.

- EPD drive power control function.
- Includes an EPD display waveform memory (programmable drive waveform).
- Includes a display data memory.
- Contrast adjustment function.
- Supports reverse, all white, and all black display functions.
- Can generate an interrupt at the end of the drive waveform output.
- Allows the software to direct control the outputs from the segment, back plane, and top plane pins.
- A trigger signal and clock can be output to an external Seiko Epson EPD driver.
- The segment, top plane, and back plane output pin assignments are selectable from four configurations.

Figure 19.1.1 shows the EPDC configuration.

Table 19.1.1 EPDC Configuration of S1C17F63

Item	S1C17F63
Number of driver outputs	42 segments + 1 back plane + 1 top plane outputs
EPD drive voltages	Two voltage values, V_{EPD} and V_{SS}

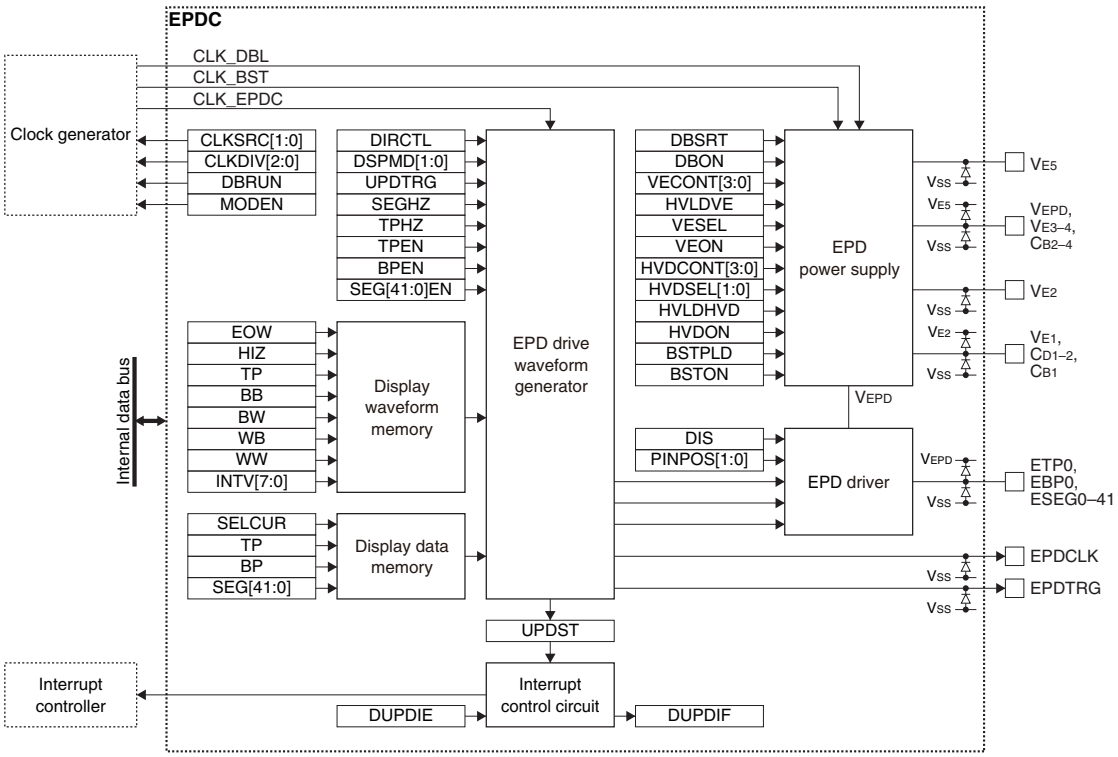


Figure 19.1.1 EPDC Configuration

19.2 Input/Output Pins and External Connections

19.2.1 List of Input/Output Pins

Table 19.2.1.1 lists the EPDC input/output pins.

Table 19.2.1.1 List of EPDC Pins

Pin name	I/O*	Initial status*	Function
ETP0	O	Hi-Z	EPD top plane/back plane/segment output
EBP0	O	Hi-Z	EPD back plane/segment output
ESEG0	O	Hi-Z	EPD segment/back plane/top plane output
ESEG1	O	Hi-Z	EPD segment/back plane output
ESEG2–41	O	Hi-Z	EPD segment outputs
V_{EPD}	P	–	EPD drive voltage output
$V_{E1–5}$	P	–	EPD power voltage booster outputs
$C_{D1–2}$	A	–	EPD power voltage booster capacitor connecting pins
$C_{B1–4}$	A	–	EPD power voltage booster capacitor connecting pins
EPDCLK	O	Hi-Z	EPD clock output for external EPD driver
EPDTRG	O	Hi-Z	EPD trigger output for external EPD driver

* Indicates the status when the pin is configured for the EPDC.

If the port is shared with the EPDC pin and other functions, the EPDC input function must be assigned to the port before activating the EPDC. For more information, refer to the "I/O Ports" chapter.

Notes: • Be sure to avoid using the V_{E1} to V_{E5} pin outputs for driving external circuits.

• The V_{EPD} pin does not allow the input of an external EPD drive voltage.

19.2.2 EPD Driver Output Pin Assignment

The EPD driver output (top plane, back plane, and segment) pin assignment is selectable from four configurations using the EPDPOS.PINPOS[1:0] bits.
Table 19.2.2.1 lists the correspondence between the EPDPOS.PINPOS[1:0] bit settings and the pin assignments.

Table 19.2.2.1 EPD Driver Output Pin Assignment

Output pin name	Driver output pin assignment			
	EPDPOS.PINPOS[1:0] bits			
	0x0	0x1	0x2	0x3
ESEG0	SEG0	BP	TP	TP
ESEG1	SEG1	SEG0	SEG0	BP
ESEG2	SEG2	SEG1	SEG1	SEG0
…	…	…	…	…
ESEG39	SEG39	SEG38	SEG38	SEG37
ESEG40	SEG40	SEG39	SEG39	SEG38
ESEG41	SEG41	SEG40	SEG40	SEG39
EBP0	BP	SEG41	SEG41	SEG40
ETP0	TP	TP	BP	SEG41

19.2.3 External Connections

Figure 19.2.3.1 shows a connection diagram between the EPDC and external devices.

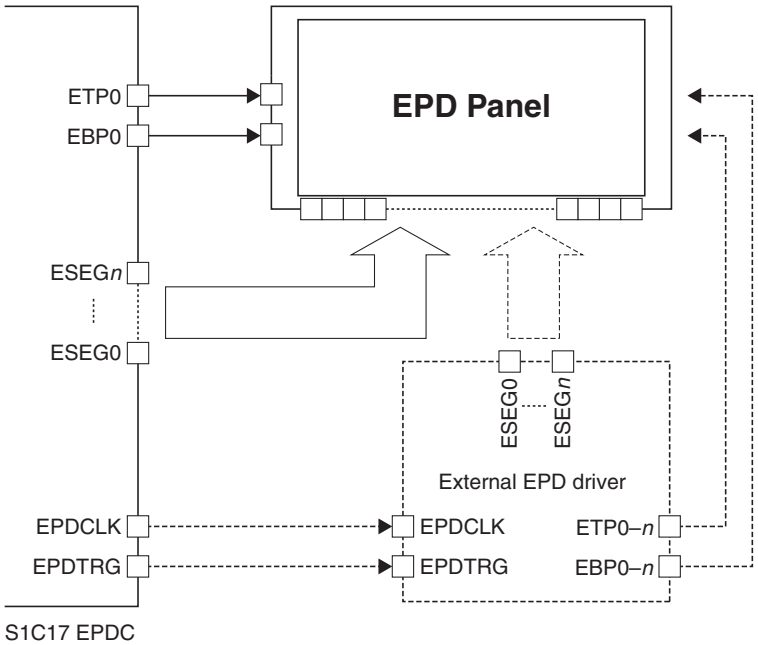


Figure 19.2.3.1 Connections between EPDC and External Devices

19.3 Clock Settings

19.3.1 EPDC Operating Clock

When using the EPDC, the timing clock CLK_EPDC must be supplied to the EPDC from the clock generator. The clocks for the voltage booster circuits (doubler and booster), CLK_DBL and CLK_BST, are also required to operate the EPD power supply circuit.
The CLK_EPDC, CLK_DBL, and CLK_BST supplies should be controlled as in the procedure shown below.

1. Enable the clock source in the clock generator if it is stopped (refer to "Clock Generator" in the "Power Supply, Reset, and Clocks" chapter).
2. Configure CLK_EPDC using the following EPDTIMCLK register bits:
   - EPDTIMCLK.CLKSRC[1:0] bits (Timing clock source selection)
   - EPDTIMCLK.CLKDIV[2:0] bits (Timing clock division ratio selection = Clock frequency setting)
3. Configure CLK_DBL using the following EPDDBLCLK register bits:
   - EPDDBLCLK.CLKSRC[1:0] bits (Doubler clock source selection)
   - EPDDBLCLK.CLKDIV[2:0] bits (Doubler clock division ratio selection = Clock frequency setting)

   The CLK_DBL frequency should be set within the range from 8 kHz to 32 kHz. It is not necessary to configure CLK_DBL if the doubler is not used.
4. Configure CLK_BST using the following EPDBSTCLK register bits:
   - EPDBSTCLK.CLKSRC[1:0] bits (Booster clock source selection)
   - EPDBSTCLK.CLKDIV[2:0] bits (Booster clock division ratio selection = Clock frequency setting)

   The CLK_BST frequency should be set within the range from 4 kHz to 16 kHz. It is not necessary to configure CLK_BST if the embedded EPD power supply circuit is not used.

19.3.2 Clock Supply in SLEEP Mode

When using EPDC during SLEEP mode, CLK_EPDC, CLK_DBL, and CLK_BST must be configured so that they will keep supplying by writing 0 to the CLGOSC.*xxxx*SLPC bit for the respective clock source.

19.3.3 Clock Supply in DEBUG Mode

The CLK_EPDC, CLK_DBL, and CLK_BST supplies during DEBUG mode should be controlled using the EPDTIMCLK.DBRUN bit, EPDDBLCLK.DBRUN bit, and EPDBSTCLK.DBRUN bit, respectively.
The EPDC operating clock supply is suspended when the CPU enters DEBUG mode if the EPD*xxx*CLK.DBRUN bit = 0. After the CPU returns to normal mode, the clock supply resumes. The registers retain the status before DEBUG mode was entered even if the clock supply is suspended. If the EPD*xxx*CLK.DBRUN bit = 1, the clock supply is not suspended and EPDC will keep operating in DEBUG mode.

19.4 EPD Power Supply

19.4.1 Configuration of EPD Power Supply Circuit

The EPD power supply circuit generates the EPD drive voltage VEPD and supplies it to the EPD driver. Figure 19.4.1.1 shows the configuration of the EPD power supply circuit.

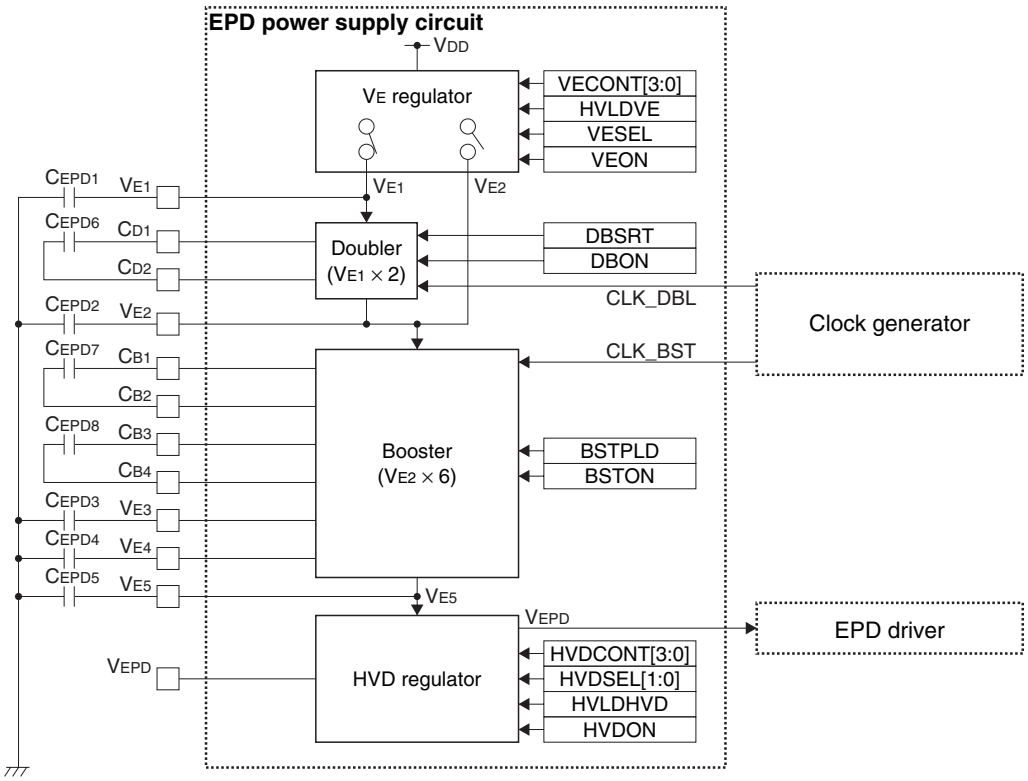


Figure 19.4.1.1 EPD Power Supply Circuit Configuration

The EPD power supply circuit consists of a VE regulator, two voltage boosters (doubler and booster), and a HVD regulator that can be controlled via software individually. For the EPD drive voltage (VEPD) value, refer to the "Electrical Characteristics" chapter.

V_E regulator

The V_E regulator generates the reference voltage for boosting (V_{E1} or V_{E2}) from V_{DD} according to the EPDPWR0.VESEL bit setting. This selection determines the path to generate V_{EPD} as follows:

1. Reference voltage = V_{E1}
   V_{DD} → [V_E regulator] → V_{E1} (reference voltage) → [Doubler] → V_{E2} (= $2V_{E1}$) → [Booster] → V_{E5} (= $6V_{E2}$) → [HVD regulator] → V_{EPD}
2. Reference voltage = V_{E2}
   V_{DD} → [V_E regulator] → V_{E2} (reference voltage) → [Booster] → V_{E5} (= $6V_{E2}$) → [HVD regulator] → V_{EPD}

Doubler

The doubler generates V_{E2} by doubling the V_{E1} generated by the V_E regulator. When V_{E2} is generated by the V_E regulator, the doubler is not required.
Between the doubler input and output can be short-circuited so that the doubler circuit cannot affect the V_E regulator output when V_{E2} is generated.

Booster

The booster multiplies the V_{E2} input from the V_E regulator or doubler by a factor of six to generate V_{E5}.
The booster output can be pulled down to V_{SS} to set the EPD drive voltage to an off level.

HVD regulator

The HVD regulator inputs the V_{E5} generated by the booster and generates the EPD drive voltage V_{EPD}. V_{EPD} is supplied to the EPD driver to generate EPD drive waveforms. The V_{EPD} output value can be selected from the three levels in accordance with the EPD specification.

19.4.2 EPD Contrast Adjustment

The V_E regulator and HVD regulator allow software to switch the output voltage in 16 steps for adjusting the EPD contrast. For the voltage values, refer to the "Electrical Characteristics" chapter.

19.4.3 Heavy Load Protection Mode

In order to ensure a stable EPD display quality even if the power supply voltage fluctuates due to driving an external load, the regulators have a heavy load protection function.
The V_E and HVD regulators should be placed into heavy load protection mode when the display has inconsistencies in density.

Note: Current consumption increases in heavy load protection mode, therefore do not set heavy load protection mode via software if unnecessary.

19.5 Operations

19.5.1 Initialization

The EPDC should be initialized with the procedure shown below.

1. Assign the EPDC output function to the ports as necessary. (Refer to the "I/O Ports" chapter.)
2. Supply the operating clocks from the clock generator. (Refer to Section 19.3.1.)
3. Configure the following EPDPWR0 register bits:

   When generating V_{E1} by the V_E regulator
   - Set the EPDPWR0.DBSRT bit to 0. (Open between doubler input and output)
   - Set the EPDPWR0.DBON bit to 1. (Turn doubler ON)
   - EPDPWR0.VECONT[3:0] bits (Set contrast initial value (V_{E1} voltage adjustment))
   - EPDPWR0.HVLDVE bit (V_E regulator heavy load protection mode)
   - Set the EPDPWR0.VESEL bit to 0. (Specify V_{E1} generation)
   - Set the EPDPWR0.VEON bit to 1. (Turn V_E regulator ON)

   When generating V_{E2} by the V_E regulator
   - Set the EPDPWR0.DBSRT bit to 1. (Short-circuit between doubler input and output)
   - Set the EPDPWR0.DBON bit to 0. (Turn doubler OFF)
   - EPDPWR0.VECONT[3:0] bits (Set contrast initial value (V_{E2} voltage adjustment))
   - EPDPWR0.HVLDVE bit (V_E regulator heavy load protection mode)
   - Set the EPDPWR0.VESEL bit to 1. (Specify V_{E2} generation)
   - Set the EPDPWR0.VEON bit to 1. (Turn V_E regulator ON)
4. Configure the following EPDPWR1 register bits:
   - EPDPWR1.HVDCONT[3:0] bits (Set contrast initial value (V_{EPD} voltage adjustment))
   - EPDPWR1.HVDSEL[1:0] bits (Select V_{EPD} voltage value)
   - EPDPWR1.HVLDHVD bit (HVD regulator heavy load protection mode)
   - Set the EPDPWR1.HVDON bit to 0. (Turn HVD regulator OFF)
   - EPDPWR1.BSTPLD bit (Select pull down of booster output)
   - Set the EPDPWR1.BSTON bit to 1. (Turn booster ON)
5. Wait for 35 ms or more. (Wait for booster output to stabilize)
6. Set the EPDPWR1.HVDON bit to 1. (Turn HVD regulator ON)
7. Wait for 5 ms or more. (Wait for V_{EPD} output to stabilize)
8. Configure the following EPDCTL register bits:
   - EPDCTL.DIS bit (Enable/disable discharging of drive pins)
   - Set the EPDCTL.MODEN bit to 1. (Enable EPDC operations)
9. Set the EPDDSP.DIRCTL bit. (Select waveform mode or direct mode)
10. Set the EPDPOS.PINPOS[1:0] bits. (Select driver output pin assignment)
11. Set the EPDTPBPEN.TPEN and EPDTPBPEN.BPEN bits to 1. (Enable TP/BP pin outputs)
12. Set the EPDSEGEN*x*.SEG[41:0]EN bits. (Enable/disable ESEG pin outputs)
13. Set the following bits when using the interrupt:
    - Write 1 to the EPDINTF.DUPDIF bit. (Clear interrupt flag)
    - Set the EPDINTE.DUPDIE bit to 1. (Enable EPDC interrupt)

19.5.2 Operating Mode

The EPDC supports two operating modes (waveform mode and direct mode) that can be selected using the EPDDSP.DIRCTL bit.

Waveform mode (EPDDSP.DIRCTL bit = 0)

When a display update trigger is issued, the EPDC outputs the drive waveforms programmed in the display waveform memory. In this mode, no CPU power is required for generating drive waveforms. For more information on the waveform programming, refer to Section 19.5.3.

Direct mode (EPDDSP.DIRCTL bit = 1)

This mode is provided to control the segment, top plane, and back plane pin outputs directly via software. The program must control the waveform generation in real time.

19.5.3 Display Waveform Memory

The display waveform memory stores the settings for the EPDC to generate drive waveforms in waveform mode.
The display waveform memory is capable of storing up to 32 timing sets (Timing set 0 to Timing set 31) that consist of 15 bits. Timing set 0 represents the initial state and its period generated immediately after a display update trigger is issued. The changes in the waveforms should be programmed one by one in the subsequent timing sets (1 to n = Max. 31).
A timing set consists of the bits shown below.

Table 19.5.3.1 Contents of a Timing Set

Bit	Bit name	Contents
15	EOW (End Of Waveform)	Specifies the end of waveform. The waveform generation is completed at the timing set in which EOW is set to 1. The pins are set into high-impedance state until the subsequent display update trigger is issued. The timing sets other than the last must be programmed with EOW set to 0.
14	–	Fixed at 0.
13	HIZ (High Impedance)	Sets the segment and back plane pins into high-impedance state. When this bit is set to 1, the segment and back plane pins are placed into high-impedance state for the period specified in the timing set (BB/BW/WB/WW settings are ignored). When this bit is set to 0, the pins go to the level specified by BB/BW/WB/WW.
12	TP (Top Plane)	Sets the waveform output from the top plane pins. When this bit is set to 1, the top plane pins go to the V_{EPD} level for the period specified in the timing set. When this bit is set to 0, the pins go to the V_{SS} level.
11	BB (Black to Black)	Sets the waveform output from the segment and back plane pins to maintain black display during update (black to black). When this bit is set to 1, the segment and back plane pins go to the V_{EPD} level for the period specified in the timing set. When this bit is set to 0, the pins go to the V_{SS} level.
10	BW (Black to White)	Sets the waveform output from the segment and back plane pins to switch black display to white during update. When this bit is set to 1, the segment and back plane pins go to the V_{EPD} level for the period specified in the timing set. When this bit is set to 0, the pins go to the V_{SS} level.
9	WB (White to Black)	Sets the waveform output from the segment and back plane pins to switch white display to black during update. When this bit is set to 1, the segment and back plane pins go to the V_{EPD} level for the period specified in the timing set. When this bit is set to 0, the pins go to the V_{SS} level.
8	WW (White to White)	Sets the waveform output from the segment and back plane pins to maintain white display during update (white to white). When this bit is set to 1, the segment and back plane pins go to the V_{EPD} level for the period specified in the timing set. When this bit is set to 0, the pins go to the V_{SS} level.
7–0	INTV[7:0] (Interval)	Specifies the timing set period in a number of CLK_EPDC clocks. Time [s] = (INTV[7:0] + 1)/CLK_EPDC frequency

The conditions above can be set using the EPDWAVE0 to EPDWAVE31 registers provided for the timing sets individually. The registers consist of the bits with the names shown above.

The following simple example shows the correspondence between the settings in the timing sets and the waveforms generated.

Table 19.5.3.2 Setting Example of Timing Sets

Timing set number (register)	EOW	–	HIZ	TP	BB	BW	WB	WW	INTV[7:0]
0 (EPDWAVE0)	0	0	0	0	0	0	0	0	0x1
1 (EPDWAVE1)	0	0	0	1	0	1	0	1	0x2
2 (EPDWAVE2)	0	0	0	0	0	0	1	1	0x0
3 (EPDWAVE3)	0	0	1	1	*	*	*	*	0x1
4 (EPDWAVE4)	1	0	0	0	0	0	0	0	0x3

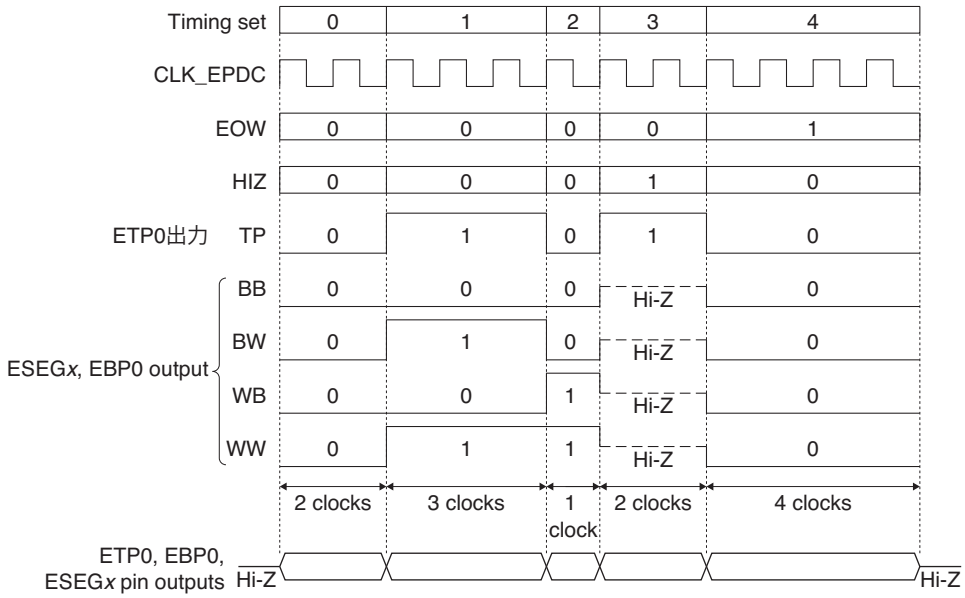


Figure 19.5.3.1 Example of Display Waveforms (by settings in Table 19.5.3.2)

Note: Table 19.5.3.2 and Figure 19.5.3.1 show merely an example to explain relationships between the settings and waveforms, not those that can be used for actual EPD driving.

19.5.4 Display Data Memory

The EPDC includes a display data memory that consists of 42 bits (for segment outputs) + 2 bits (for top plane and back plane outputs).
Segment output data should be set to the EPDSEG*x*.SEG[41:0] bits (*x* = 0 to 2). Back plane output data should be set to EPDTPBP.BP bit. Writing 1 to the bit specifies black display in waveform mode or high (V_{EPD}) level output in direct mode; writing 0 specifies white display in waveform mode or low (V_{SS}) level output in direct mode.
Top plane output data should be set to EPDTPBP.TP bit. This bit is effective only in direct mode. Writing 1 specifies high (V_{EPD}) level output; writing 0 specifies low (V_{SS}) level output. In waveform mode, the top plane output is controlled according to the contents of the display waveform memory.
The EPDC has two display data, data currently displayed and data to be displayed next, that are used to determine the waveform to be output from each ESEG pin. Either the current or next display data can be specified to be read/written using the EPDDSP.SELCUR bit only in waveform mode and when the display is not being updated.
The display data memory settings take effect when a display update trigger (described later) is issued. Writing to the display data memory does not update the screen.
After an initial reset, the display data memory is cleared to 0.

19.5.5 Display Control (Waveform Mode)

This section describes the display control method in waveform mode. The drive waveforms must be programmed in the display waveform memory before starting display (refer to Section 19.5.3).
Control the display as the flowchart shown in Figure 19.5.5.1.

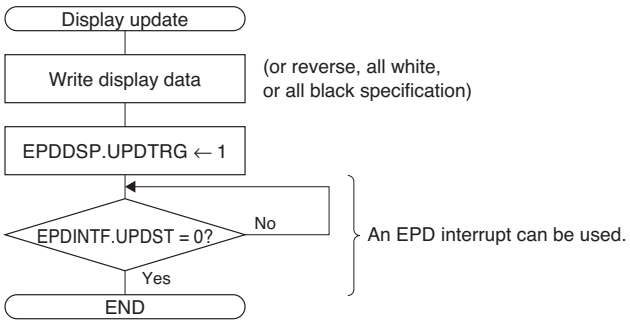


Figure 19.5.5.1 Display Control in Waveform Mode

Normal display control

Display can be updated in the procedure shown below.

1. Set the EPDDSP.SELCUR bit to 0. (Specify to access to next updating data)
2. Check if the EPDINTF.UPDST bit = 0. (Ready to display update?)
3. Set the EPDTPBP.BP bit. (Set back plane data)
4. Set the EPDSEG*x*.SEG[41:0] bits. (Set segment data)
5. Write 1 to the EPDDSP.UPDTRG bit. (Issue display update trigger)

   The EPDC outputs the drive waveforms programmed in the display waveform memory to the segment, top plane and back plane pins according to the contents of the display data memory and the current display data.
4. Wait for changing the EPDINTF.UPDST bit from 1 to 0 or a display update interrupt (EPDINTF.DUPDIF bit = 1).

   The EPDINTF.UPDST bit goes 1 by a display update trigger and reverts to 0 upon completion of the programmed drive waveform output.

Notes: • The EPDC generates the drive waveforms with the current display data regarded as 0 in the first display update after an initial reset.

• When direct mode is switched to waveform mode, fluctuations on screen may occur only in the first display update.

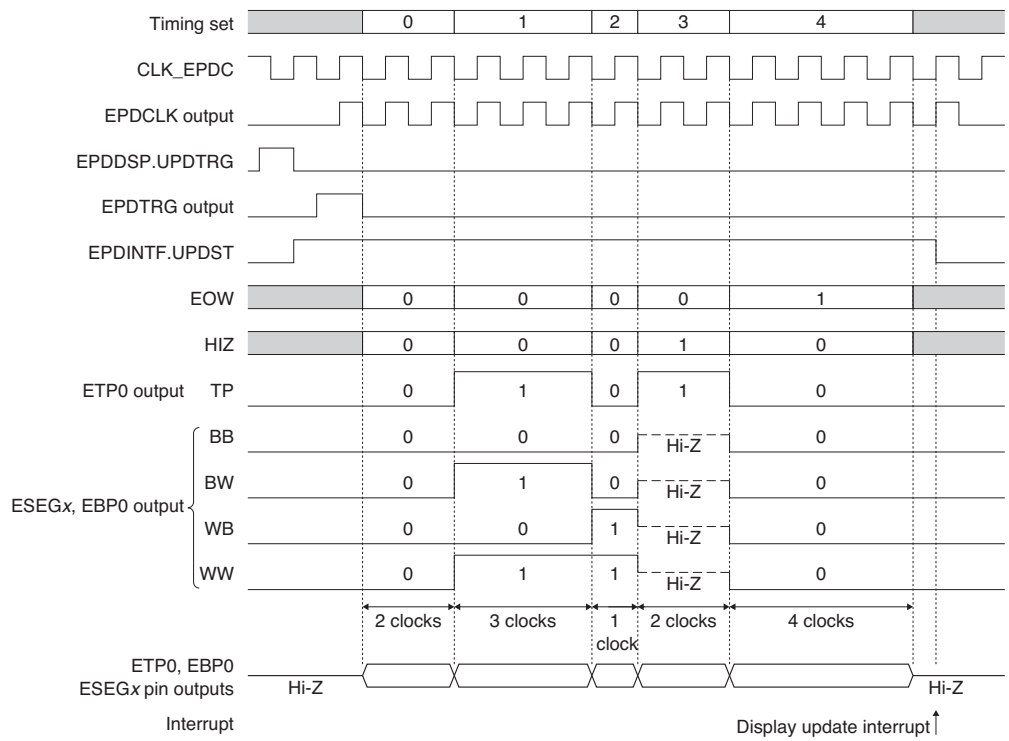


Figure 19.5.5.2 Timing Chart of Waveform Output Example (by settings in Table 19.5.3.2)

Reverse, all white, and all black display control

In waveform mode, the screen can be reversed or turned to all white or black without rewriting the display data memory via software. The following shows the operation procedure:

1. Check if the EPDINTF.UPDST bit = 0. (Ready to display update?)
2. Set the EPDDSP.DSPMD[1:0] bits. (Specify display mode)
3. Write 1 to the EPDDSP.UPDTRG bit. (Issue display update trigger)

   By writing 1 to the EPDDSP.UPDTRG bit, the drive waveforms are output to change the display.

Table 19.5.5.1 Display Mode

EPDDSP. DSPMD[1:0] bits	Display mode	Display status
0x3	All black display mode	Writing 1 to the EPDDSP.UPDTRG bit updates the display so that the all segments will turn to black regardless of the display memory contents.
0x2	All white display mode	Writing 1 to the EPDDSP.UPDTRG bit updates the display so that the all segments will turn to white regardless of the display memory contents.
0x1	Reverse display mode	Meaning of the display memory bits are swapped between 1 and 0. In other words, writing 1 to the EPDDSP.UPDTRG bit in this mode updates the display so that the segments/back plane corresponding to the bits set to 1 will turn to white, and those corresponding to the bits set to 0 will turn to black.
0x0	Normal display mode	Writing 1 to the EPDDSP.UPDTRG bit updates the display according to the display memory contents.

19.5.6 Display Control (Direct Mode)

This section describes the display control method in direct mode.
Update the display as the flowchart shown in Figure 19.5.6.1.

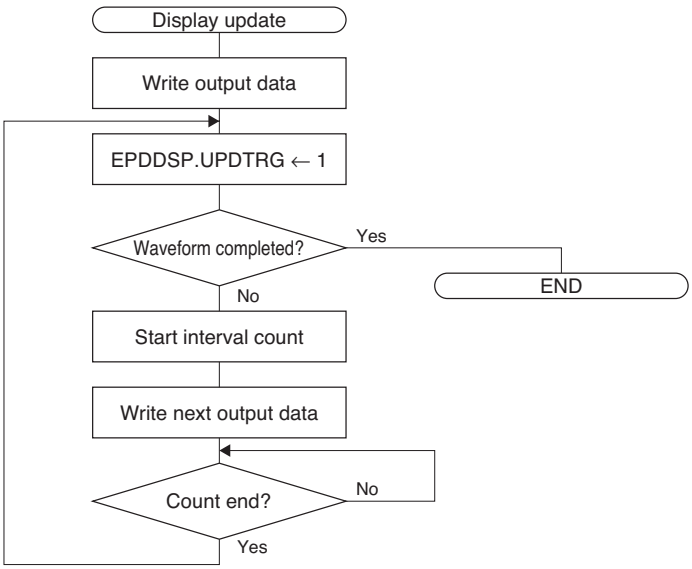


図19.5.6.1 Display Control in Direct Mode

1. Check if the EPDINTF.UPDST bit = 0. (Ready to display update?)
2. Set the EPDTPBP.TP bit. (Set top plane output level)
3. Set the EPDTPBP.BP bit. (Set back plane output level)
4. Set the EPDSEG*x*.SEG[41:0] bits. (Set segment output levels)

   ∗ To set the top plane and segment/back plane pins into high-impedance, write 1 to the EPDTPBP.TPHZ bit and the EPDTPBP.SEGHZ bit, respectively. Settings in the display data memory are ineffective in this case.
5. Write 1 to the EPDDSP.UPDTRG bit. (Issue display update trigger)

   The EPDC outputs the contents of the display data memory to the segment, top plane and back plane pins.

6. Start counting the current level output period using a timer.
7. Write the subsequent output data to the display data memory during counting. (Steps 1 to 4)
8. Wait for the end of counting such as a timer interrupt.
9. Terminate the processing when the display update waveforms have been output.
   Return to Step 5 if the display update waveforms have not been output completely.

19.5.7 Outputs for External Driver

The EPDC is able to output the timing clock (EPDCLK) and the display update trigger signal (EPDTRG) allowing use of an external EPD driver. The clock is output from the EPDCLK pin and the trigger signal is output from the EPDTRG pin. No output control is required, note, however, that the output pins must be switched for EPD outputs using the port function select bits. For the trigger signal output timing, see Figure 19.5.5.2.

19.6 Interrupt

The EPDC has a function to generate the interrupt shown in Table 19.6.1.

Table 19.6.1 EPDC Interrupt Function

Interrupt	Interrupt flag	Set condition	Clear condition
Display update	EPDINTF.DUPDIF	When the drive waveform output by a display update trigger in waveform mode (output of the timing set in which EOW is set) has finished	Writing 1

The EPDC provides an interrupt enable bit corresponding to the interrupt flag. An interrupt request is sent to the interrupt controller only when the interrupt flag is set while the interrupt enable bit = 1 (interrupt enabled). For more information on interrupt control, refer to the “Interrupt Controller” chapter.

19.7 Control Registers

EPDC Timing Clock Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
EPDTIMCLK	15–9	–	0x00	–	R	–
	8	DBRUN	1	H0	R/W	
	7	–	0	–	R	
	6–4	CLKDIV[2:0]	0x0	H0	R/W	
	3–2	–	0x0	–	R	
	1–0	CLKSRC[1:0]	0x0	H0	R/W	

Bit 15–9 Reserved

Bit 8 DBRUN

This bit sets whether the EPDC timing clock is supplied in DEBUG mode or not.
1 (R/W): Clock supplied in DEBUG mode
0 (R/W): No clock supplied in DEBUG mode

Bit 7 Reserved

Bits 6–4 CLKDIV[2:0]

These bits select the division ratio of the EPDC timing clock.

Bits 3–2 Reserved

Bits 1–0 CLKSRC[1:0]

These bits select the EPDC timing clock source.

Table 19.7.1 EPDC Timing Clock Source and Division Ratio Settings

EPDTIMCLK. CLKDIV[2:0] bits	EPDTIMCLK.CLKSRC[1:0] bits			
	0x0	0x1	0x2	0x3
	IOSC	OSC1	OSC3	EXOSC
0x7	1/16,384	1/128	1/16,384	1/1
0x6	1/8,192	1/64	1/8,192	
0x5	1/4,096	1/32	1/4,096	
0x4	1/2,048	1/16	1/2,048	
0x3	1/1,024	1/8	1/1,024	
0x2	1/512	1/4	1/512	
0x1	1/256	1/2	1/256	
0x0	1/128	1/1	1/128	

(Note) The oscillation circuits/external input that are not supported in this IC cannot be selected as the clock source.

EPDC Doubler Clock Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
EPDDBLCLK	15–9	–	0x00	–	R	–
	8	DBRUN	1	H0	R/W	
	7	–	0	–	R	
	6–4	CLKDIV[2:0]	0x0	H0	R/W	
	3–2	–	0x0	–	R	
	1–0	CLKSRC[1:0]	0x0	H0	R/W	

Bits 15–9 Reserved

Bit 8 DBRUN

This bit sets whether the operating clock of the doubler in the EPD power supply circuit is supplied in DEBUG mode or not.

1 (R/W): Clock supplied in DEBUG mode

0 (R/W): No clock supplied in DEBUG mode

Bit 7 Reserved

Bits 6–4 CLKDIV[2:0]

These bits select the operating clock division ratio of the doubler in the EPD power supply circuit.

Bits 3–2 Reserved

Bits 1–0 CLKSRC[1:0]

These bits select the clock source of the doubler in the EPD power supply circuit.

Table 19.7.2 Doubler Clock Source and Division Ratio Settings

EPDDBLCLK. CLKDIV[2:0] bits	EPDDBLCLK.CLKSRC[1:0] bits			
	0x0	0x1	0x2	0x3
	IOSC	OSC1	OSC3	EXOSC
0x7	Reserved	Reserved	Reserved	1/1
0x6				
0x5				
0x4	1/256		1/256	
0x3	1/128	1/8	1/128	
0x2	1/64	1/4	1/64	
0x1	1/32	1/2	1/32	
0x0	1/16	1/1	1/16	

(Note) The oscillation circuits/external input that are not supported in this IC cannot be selected as the clock source.

EPDC Booster Clock Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
EPDBSTCLK	15–9	–	0x00	–	R	–
	8	DBRUN	1	H0	R/W	
	7	–	0	–	R	
	6–4	CLKDIV[2:0]	0x0	H0	R/W	
	3–2	–	0x0	–	R	
	1–0	CLKSRC[1:0]	0x0	H0	R/W	

Bits 15–9 Reserved

Bit 8 DBRUN

This bit sets whether the operating clock of the booster in the EPD power supply circuit is supplied in DEBUG mode or not.

1 (R/W): Clock supplied in DEBUG mode

0 (R/W): No clock supplied in DEBUG mode

Bit 7 Reserved

Bits 6–4 CLKDIV[2:0]

These bits select the operating clock division ratio of the booster in the EPD power supply circuit.

Bits 3–2 Reserved

Bits 1–0 CLKSRC[1:0]

These bits select the clock source of the booster in the EPD power supply circuit.

Table 19.7.3 Booster Clock Source and Division Ratio Settings

EPDBSTCLK. CLKDIV[2:0] bits	EPDBSTCLK.CLKSRC[1:0] bits			
	0x0	0x1	0x2	0x3
	IOSC	OSC1	OSC3	EXOSC
0x7	Reserved	Reserved	Reserved	1/1
0x6				
0x5				
0x4	1/256		1/256	
0x3	1/128	1/8	1/128	
0x2	1/64	1/4	1/64	
0x1	1/32	1/2	1/32	
0x0	1/16	1/1	1/16	

(Note) The oscillation circuits/external input that are not supported in this IC cannot be selected as the clock source.

EPDC Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
EPDCTL	15–8	–	0x00	–	R	–
	7–2	–	0x00	–	R	
	1	DIS	0	H0	R/W	
	0	MODEN	0	H0	R/W	

Bits 15–2 Reserved

Bit 1 DIS

This bit enables the EPD drive output pin discharge operation.

1 (R/W): Enable discharge operation

0 (R/W): Disable discharge operation

Setting this bit to 1 puts the EPD drive output pins into discharging state by pulling the pins down except when the display on the EPD is being updated. Setting this bit to 0 puts the EPD drive output pins into high-impedance state except when the display on the EPD is being updated. While the display is being updated, the pull-down is cancelled regardless of how this bit is set.

Bit 0 MODEN

This bit enables the EPDC operations.
1 (R/W): Enable EPDC operations (The timing clock is supplied.)
0 (R/W): Disable EPDC operations (The timing clock is stopped.)

EPDC Power Supply Control Register 0

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
EPDPWR0	15–10	–	0x00	–	R	–
	9	DBSRT	0	H0	R/W	
	8	DBON	0	H0	R/W	
	7–4	VECONT[3:0]	0x0	H0	R/W	
	3	–	0	–	R	
	2	HVLDVE	0	H0	R/W	
	1	VESEL	0	H0	R/W	
	0	VEON	0	H0	R/W	

Bits 15–10 Reserved

Bit 9 DBSRT

This bit short-circuits between the doubler input and output.
1 (R/W): Short
0 (R/W): Open

When the doubler is not used, set this bit to 1 to short-circuit between the doubler input and output. When the doubler is activated (EPDPWR0.DBON bit = 1), the input and output are not short-circuited even if this bit is set to 1.

Bit 8 DBON

This bit turns the doubler on or off.
1 (R/W): Doubler On
0 (R/W): Doubler Off

Bits 7–4 VECONT[3:0]

These bits switch the V_E regulator output voltage value to adjust the EPD contrast.

Table 19.7.4 Setting V_E Regulator Output Level (EPD Contrast Adjustment Function)

EPDPWR0.VECONT[3:0] bits	V_E regulator output level
0xf	Level 15 (high contrast)
:	:
0x0	Level 0 (low contrast)

Refer to the "Electrical Characteristics" chapter for the voltage values.

Bit 3 Reserved

Bit 2 HVLDVE

This bit sets the V_E regulator into heavy load protection mode.
1 (R/W): Heavy load protection On
0 (R/W): Heavy load protection Off

Bit 1 VESEL

This bit selects the V_E regulator output voltage (reference voltage for boosting).
1 (R/W): V_{E2}
0 (R/W): V_{E1}

Select either V_{E1} or V_{E2} to be generated by the V_E regulator according to the V_{DD} value.

Table 19.7.5 V_E Regulator Output Selection

Power supply voltage V_{DD}	EPDPWR0.VESEL bit	V_E regulator output
$V_{DD} \geq V_{E1} + 0.3$ V	0	V_{E1}
$V_{DD} \geq V_{E2} + 0.2$ V	1	V_{E2}

Bit 0 VEON

This bit turns the VE regulator on or off.

1 (R/W): VE regulator On

0 (R/W): VE regulator Off

EPDC Power Supply Control Register 1

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
EPDPWR1	15–12	HVDCONT[3:0]	0x0	H0	R/W	–
	11–10	HVDSEL[1:0]	0x0	H0	R/W	
	9	HVLDHVD	0	H0	R/W	
	8	HVDON	0	H0	R/W	
	7–2	–	0x00	–	R	
	1	BSTPLD	0	H0	R/W	
	0	BSTON	0	H0	R/W	

Bits 15–12 HVDCONT[3:0]

These bits switch the HVD regulator output voltage value to adjust the EPD contrast.

Table 19.7.6 Setting HVD Regulator Output Level (EPD Contrast Adjustment Function)

EPDPWR1.HVDCONT[3:0] bits	HVD regulator output level
0xf	Level 15 (high contrast)
:	:
0x0	Level 0 (low contrast)

Refer to the "Electrical Characteristics" chapter for the voltage values.

Bits 11–10 HVDSEL[1:0]

These bits select the HVD regulator output voltage value (VEPD) in accordance with the EPD specification.

Table 19.7.7 VEPD Voltage Value

EPDPWR1.HVDSEL[1:0] bits	VEPD voltage
0x3	Reserved
0x2	9 V type
0x1	12 V type
0x0	15 V type

Bit 9 HVLDHVD

This bit sets the HVD regulator into heavy load protection mode.

1 (R/W): Heavy load protection On

0 (R/W): Heavy load protection Off

Bit 8 HVDON

This bit turns the HVD regulator on or off.

1 (R/W): HVD regulator On

0 (R/W): HVD regulator Off

Note: After the HVD regulator is turned on, the VEPD output voltage requires about 5 ms to stabilize. Do not start display on the EPD in this unstable period.

Bits 7–2 Reserved

Bit 1 BSTPLD

This bit pulls down the booster output to VSS.

1 (R/W): Pull-down On

0 (R/W): Pull-down Off

This bit allows software to set the EPD drive voltage to an off level.

Bit 0 BSTON

This bit turns the booster on or off.

1 (R/W): Booster On

0 (R/W): Booster Off

Note: After the booster is turned on, the V_{E5} output voltage requires about 35 ms to stabilize. Do not activate the HVD regulator in this unstable period.

EPDC Display Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
EPDDSP	15–8	–	0x00	–	R	–
	7–6	–	0x0	–	R	
	5	SELCUR	0	H0	R/W	
	4	DIRCTL	0	H0	R/W	
	3–2	DSPMD[1:0]	0x0	H0	R/W	
	1	–	0	–	R	
	0	UPDTRG	0	H0	W	

Bits 15–6 Reserved

Bit 5 SELCUR (waveform mode)

This bit selects the access destination through the display data register.

1 (R/W): Current display data

0 (R/W): Next display data

Access to the current display data is effective only in waveform mode with the EPDINTF.UPDST bit set to 0.

Bit 4 DIRCTL

This bit sets the EPD controller into waveform or direct mode.

1 (R/W): Direct mode

0 (R/W): Waveform mode

Bits 3–2 DSPMD[1:0] (waveform mode)

These bits select a display mode in waveform mode.

Table 19.7.8 Display Control

EPDDSP.DSPMD[1:0] bits	Display mode
0x3	All black display
0x2	All white display
0x1	Reverse display
0x0	Normal display

(Default: 0x0)

The display mode switches when a display update trigger (EPDDSP.UPDTRG bit = 1) is issued.

Bit 1 Reserved

Bit 0 UPDTRG

This bit starts display update sequence.

1 (W): Display update trigger

0 (W): Ineffective

Note: Writing 1 to the EPDDSP.UPDTRG bit is ineffective while the EPDINTF.UPDST bit is set to 1.

EPDC Pin Assignment Select Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
EPDPOS	15–8	–	0x00	–	R	–
	7–2	–	0x00	–	R	
	1–0	PINPOS[1:0]	0x0	H0	R/W	

Bits 15–2 Reserved

Bits 1–0 PINPOS[1:0]

These bits select the driver output pin assignment (see Table 19.2.2.1).

EPDC Interrupt Flag/Status Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
EPDINTF	15–9	–	0x00	–	R	–
	8	UPDST	0	H0	R	
	7–1	–	0x00	–	R	
	0	DUPDIF	0	H0	R/W	Cleared by writing 1.

Bits 15–9 Reserved

Bit 8 UPDST (waveform mode)

This bit indicates the display update status in waveform mode.

1 (R): Display is being updated

0 (R): Idle

The EPDINTF.UPDST bit goes 1 when a display update operation is started by writing 1 to the EPDDSP.UPDTRG bit, and reverts to 0 upon completion of the programmed drive waveform output (output of the timing set in which EOW is set).

The EPDINTF.UPDST bit is ineffective in direct mode and is always read as 0.

Note: Be sure to avoid rewriting the display data memory and altering the EPDDSP.DSPMD[1:0] bits while the The EPDINTF.UPDST bit is set to 1.

Bits 7–1 Reserved

Bit 0 DUPDIF

This bit indicates the EPDC display update interrupt cause occurrence status.

1 (R): Cause of interrupt occurred

0 (R): No cause of interrupt occurred

1 (W): Clear flag

0 (W): Ineffective

EPDC Interrupt Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
EPDINTE	15–8	–	0x00	–	R	–
	7–1	–	0x00	–	R	
	0	DUPDIE	0	H0	R/W	

Bits 15–1 Reserved

Bit 0 DUPDIE

This bit enables the EPDC display update interrupt.

1 (R/W): Enable interrupt

0 (R/W): Disable interrupt

EPDC Top/Back Plane Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
EPDTPBP	15–10	–	0x00	–	R	–
	9	SEGHZ	0	H0	R/W	Effective only in direct mode
	8	TPHZ	0	H0	R/W	–
	7–5	–	0x0	–	R	
	4	TP	0	H0	R/W	Effective only in direct mode
	3–1	–	0x0	–	R	–
	0	BP	0	H0	R/W	

Bits 15–10 Reserved

Bit 9 SEGHZ (direct mode)

This bit sets the segment/back plane outputs into high-impedance state.

1 (R/W): High-impedance

0 (R/W): Normal output

Bit 8 TPHZ (direct mode)

This bit sets the top plane outputs into high-impedance state.

1 (R/W): High-impedance

0 (R/W): Normal output

Bits 7–5 Reserved

Bit 4 TP (direct mode)

This bit sets the top plane output level.

1 (R/W): High level

0 (R/W): Low level

Bits 3–1 Reserved

Bit 0 BP

This bit sets the back plane display data/output level.

1 (R/W): Black (waveform mode)/High level (direct mode)

0 (R/W): White (waveform mode)/Low level (direct mode)

Note: Setting this register does not update the display. A display update trigger using the EPDDSP. UPDTRG bit is required.

EPDC Segment Data Registers 0–2

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
EPDSEG0	15–0	SEG[15:0]	0x0000	H0	R/W	–
EPDSEG1	15–0	SEG[31:16]	0x0000	H0	R/W	–
EPDSEG2	15–10	–	0x00	–	R	–
	9–0	SEG[41:32]	0x00	H0	R/W	

Bits 15–10 Reserved (EPDSEG2)

Bits 15(9)–0 SEG*xx*

These bits set the segment display data/output level.

1 (R/W): Black (waveform mode)/High level (direct mode)

0 (R/W): White (waveform mode)/Low level (direct mode)

Note: Setting the data registers do not update the display. A display update trigger using the EPDDSP. UPDTRG bit is required.

EPDC Top/Back Plane Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
EPDTPBPEN	15–8	–	0x00	–	R	–
	7–5	–	0x0	–	R	
	4	TPEN	1	H0	R/W	
	3–1	–	0x0	–	R	
	0	BPEN	1	H0	R/W	

Bits 15–5 Reserved

Bit 4 TPEN

This bit enables the top plane pin output.
1 (R/W): Enable top plane pin output
0 (R/W): Disable top plane pin output

Bits 3–1 Reserved

Bit 0 BPEN

This bit enables the back plane pin output.
1 (R/W): Enable back plane pin output
0 (R/W): Disable back plane pin output

When the top plane/back plane pin output is disabled, the pins are always put into high-impedance state.

EPDC Segment Enable Registers 0–2

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
EPDSEGEN0	15–0	SEG[15:0]EN	0x0000	H0	R/W	–
EPDSEGEN1	15–0	SEG[31:16]EN	0x0000	H0	R/W	–
EPDSEGEN2	15–10	–	0x00	–	R	–
	9–0	SEG[41:32]EN	0x00	H0	R/W	

Bits 15–10 Reserved (EPDSEGEN2)

Bits 15(9)–0 SEG*xx*EN

These bits enable the ESEG*xx* pin outputs.
1 (R/W): Enable ESEG*xx* output
0 (R/W): Disable ESEG*xx* pin output

The ESEG*xx* pin to be used should be enabled to output drive waveforms. When the unused ESEG*xx* pin outputs are disabled, the pins are always put into high-impedance state. This makes it possible to suppress useless power consumption.

EPDC Waveform Timing Set Registers 0–31

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
EPDWAVE0	15	EOW	0	H0	R/W	–
|	14	–	0	–	R	
EPDWAVE31	13	HIZ	0	H0	R/W	
	12	TP	0	H0	R/W	
	11	BB	0	H0	R/W	
	10	BW	0	H0	R/W	
	9	WB	0	H0	R/W	
	8	WW	0	H0	R/W	
	7–0	INTV[7:0]	0x00	H0	R/W	

These registers are used to set the display waveform memory for waveform mode. For more information, refer to Section 19.5.3, "Display Waveform Memory."

Bit 15 EOW

This bit specifies the end of waveform.
1 (R/W): End
0 (R/W): Continued

The waveform generation is completed at the timing set in which the EOW bit is set to 1. The pins are set into high-impedance state until the subsequent display update trigger is issued. The timing sets other than the last must be programmed with the EOW bit set to 0.

Bit 14 Reserved

Bit 13 HIZ

This bit sets the segment and back plane pins into high-impedance state.
1 (R/W): High-impedance
0 (R/W): High/low output

When this bit is set to 1, the segment and back plane pins are placed into high-impedance state for the period specified in the timing set (BB/BW/WB/WW settings are ignored). When this bit is set to 0, the pins go to the level specified by BB/BW/WB/WW.

Bit 12 TP

This bit sets the waveform output from the top plane pins.
1 (R/W): High
0 (R/W): Low

Bit 11 BB

This bit sets the waveform output from the segment and back plane pins to maintain black display during update (black to black).
1 (R/W): High
0 (R/W): Low

Bit 10 BW

This bit sets the waveform output from the segment and back plane pins to switch black display to white during update.
1 (R/W): High
0 (R/W): Low

Bit 9 WB

This bit sets the waveform output from the segment and back plane pins to switch white display to black during update.
1 (R/W): High
0 (R/W): Low

Bit 8 WW

This bit sets the waveform output from the segment and back plane pins to maintain white display during update (white to white).
1 (R/W): High
0 (R/W): Low

Bits 7–0 INTV[7:0]

These bits specify the timing set period in a number of CLK_EPDC clocks.

Time [s] = (INTV[7:0] + 1)/CLK_EPDC frequency

20 Multiplier/Divider (COPRO2)

20.1 Overview

COPRO2 is the coprocessor that provides multiplier/divider functions. The features of COPRO2 are listed below.

- Multiplication: Supports signed/unsigned multiplications.
  (16 bits × 16 bits = 32 bits)
  Can be executed in 1 cycle.
- Multiplication and accumulation (MAC): Supports signed/unsigned MAC operations with overflow detection function. (16 bits × 16 bits + 32 bits = 32 bits)
  Can be executed in 1 cycle.
- Division: Supports signed/unsigned divisions.
  (32 bits ÷ 32 bits = 32 bits with 32-bit reminder)
  Can be executed in 17 to 20 cycles.
  Overflow detection and division by zero processing are not supported.

Figure 20.1.1 shows the COPRO2 configuration.

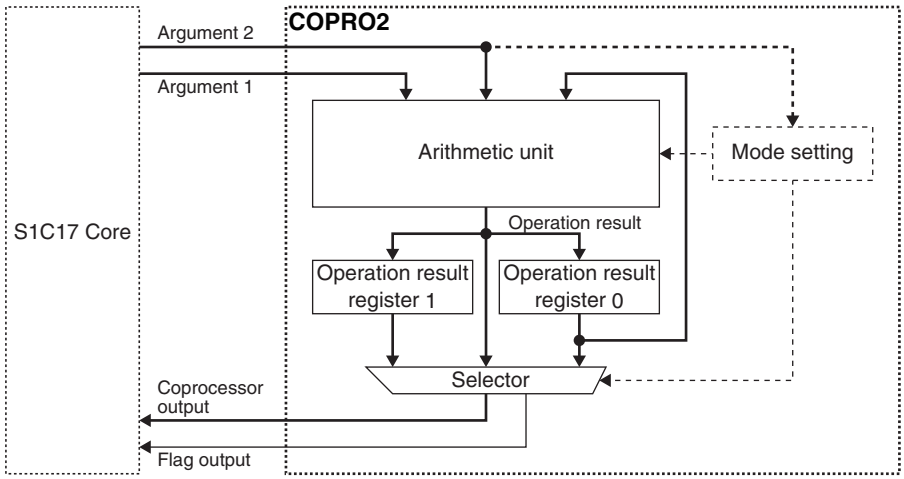


Figure 20.1.1 COPRO2 Configuration

20.2 Operation Mode and Output Mode

COPRO2 operates according to the operation mode specified by the application program. As listed in Table 20.2.1, COPRO2 supports 11 operations.
The multiplication, division and MAC results are 32-bit data, therefore, the S1C17 Core cannot read them in one access cycle. The output mode is provided to specify the high-order 16 bits or low-order 16 bits of the operation result register 0 or 1 to be read from COPRO2.
The operation and output modes can be specified with a 7-bit data by writing it to the mode setting register in COPRO2. Use a "`ld.cw`" instruction for this writing.

`ld.cw %rd,%rs` %rs[6:0] is written to the mode setting register. (%rd: not used)
`ld.cw %rd,`*`imm7`* *imm7*[6:0] is written to the mode setting register. (%rd: not used)

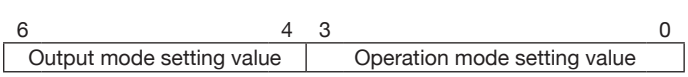


Figure 20.2.1 Mode Setting Register

Table 20.2.1 Mode Settings

Setting value (D[6:4])	Output mode	Setting value (D[3:0])	Operation mode
0x0	**16 low-order bits output mode 0** The low-order 16 bits of the operation result register 0 can be read as the coprocessor output.	0x0	**Initialize mode 0** Clears the operation result registers 0 and 1 to 0x0.
0x1	**16 high-order bits output mode 0** The high-order 16 bits of the operation result register 0 can be read as the coprocessor output.	0x1	**Initialize mode 1** Loads the 16-bit augend into the low-order 16 bits of the operation result register 0.
0x2	**16 low-order bits output mode 1** The low-order 16 bits of the operation result register 1 can be read as the coprocessor output.	0x2	**Initialize mode 2** Loads the 32-bit data into the operation result register 0.
0x3	**16 high-order bits output mode 1** The high-order 16 bits of the operation result register 1 can be read as the coprocessor output.	0x3	**Operation result read mode** Outputs the data in the operation result registers 0 and 1 without computation.
0x4–0x7	Reserved	0x4	**Unsigned multiplication mode** Performs unsigned multiplication.
		0x5	**Signed multiplication mode** Performs signed multiplication.
		0x6	**Unsigned MAC mode** Performs unsigned MAC operation.
		0x7	**Signed MAC mode** Performs signed MAC operation.
		0x8	**Unsigned division mode** Performs unsigned division.
		0x9	**Signed division mode** Performs signed division.
		0xa	**Initialize mode 3** Loads the 32-bit data into the operation result register 1.
		0xb–0xf	Reserved

20.3 Multiplication

The multiplication function performs "A (32 bits) = B (16 bits) × C (16 bits)."
The following shows a procedure to perform a multiplication:

1. Set the mode to 0x04 (unsigned multiplication, 16 low-order bits output mode 0) or 0x05 (signed multiplication, 16 low-order bits output mode 0).
2. Send the 16-bit multiplicand (B) and 16-bit multiplier (C) to COPRO2 using a "`ld.ca`" instruction.
3. Read the one-half result (16 low-order bits = A[15:0]) and the flag status.
4. Set the mode to 0x13 (operation result read, 16 high-order bits output mode 0).
5. Read another one-half result (16 high-order bits = A[31:16]).

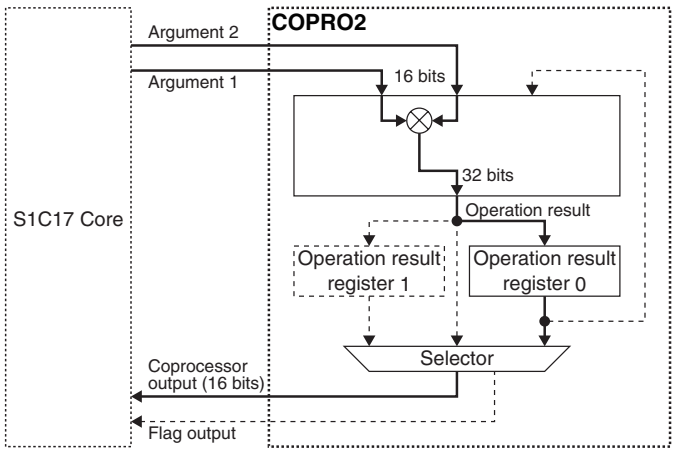


Figure 20.3.1 Data Path in Multiplication Mode

Table 20.3.1 Operation in Multiplication Mode

Mode setting value	Instruction	Operations	Flags	Remarks
0x04 or 0x05	`ld.ca %rd,%rs`	res0[31:0] ← %rd × %rs %rd ← res0[15:0]	psr (CVZN) ← 0b0000	The operation result register 0 keeps the operation result until it is rewritten by other operation.
	(`ext` *imm9*) `ld.ca %rd,`*imm7*	res0[31:0] ← %rd × *imm7/16* %rd ← res0[15:0]		
0x14 or 0x15	`ld.ca %rd,%rs`	res0[31:0] ← %rd × %rs %rd ← res0[31:16]		
	(`ext` *imm9*) `ld.ca %rd,`*imm7*	res0[31:0] ← %rd × *imm7/16* %rd ← res0[31:16]		

res0: operation result register 0

Example:

```
ld.cw %r0,0x04 ; Sets the mode (unsigned multiplication mode and 16 low-order bits output mode 0).
ld.ca %r0,%r1  ; Performs "res0[31:0] = %r0[15:0] × %r1[15:0]" and loads the 16 low-order bits of the
                 result to %r0.
ld.cw %r0,0x13 ; Sets the mode (operation result read mode and 16 high-order bits output mode 0).
ld.ca %r1,%r0  ; Loads the 16 high-order bits of the result to %r1.
```

20.4 Division

The division function performs "A (32 bits) = B (32 bits) ÷ C (32 bits), D (32 bits) = remainder."
The following shows a procedure to perform a division:

1. Set the mode to 0x02 (initialize mode 2).
2. Set the 32-bit dividend (B) to the operation result register 0 using a "`ld.cf`" instruction.
3. Set the mode to 0x08 (unsigned division, 16 low-order bits output mode 0) or 0x09 (signed division, 16 low-order bits output mode 0).
4. Send the 32-bit divisor (C) to COPRO2 using a "`ld.ca`" instruction.
5. Read the one-half result (16 low-order bits = A[15:0]) of the operation result register 0 (quotient) and the flag status.
6. Set the mode to 0x13 (operation result read, 16 high-order bits output mode 0).
7. Read another one-half result (16 high-order bits = A[31:16]) of the operation result register 0 (quotient).
8. Set the mode to 0x23 (operation result read, 16 low-order bits output mode 1).
9. Read the one-half result (16 low-order bits = D[15:0]) of the operation result register 1 (remainder).
10. Set the mode to 0x33 (operation result read, 16 high-order bits output mode 1).
11. Read another one-half result (16 high-order bits = D[31:16]) of the operation result register 1 (remainder).

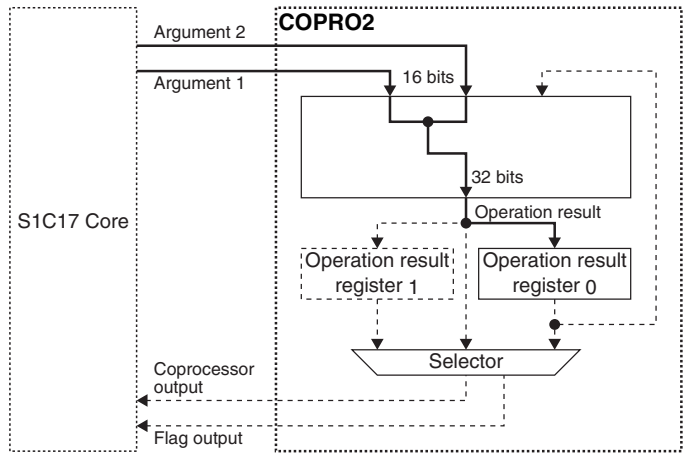


Figure 20.4.1 Data Path in Initialize Mode 2

Table 20.4.1 Initializing the Operation Result Register 0 (32 bits)

Mode setting value	Instruction	Operations	Remarks
0x02	`ld.cf %rd,%rs`	res0[31:16] ← %rd res0[15:0] ← %rs	
	(`ext` *imm9*) `ld.cf %rd,`*imm7*	res0[31:16] ← %rd res0[15:0] ← *imm7/16*	

res0: operation result register 0

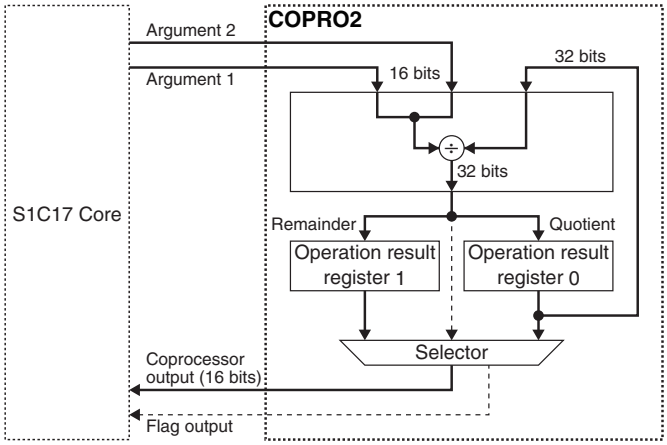


Figure 20.4.2 Data Path in Division Mode

Table 20.4.2 Operation in Division Mode

Mode setting value	Instruction	Operations	Flags	Remarks
0x08 or 0x09	`ld.ca %rd,%rs`	res0[31:0] ÷ {%rd, %rs} res0[31:0] ← Quotient res1[31:0] ← Remainder %rd ← res0[15:0] (Quotient)	psr (CVZN) ← 0b0000	The operation result registers 0 and 1 keep the operation results until they are rewritten by other operation. COPRO2 does not support 0 ÷ 0 division.
	(`ext` *imm9*) `ld.ca %rd,`*imm7*	res0[31:0] ÷ {%rd, *imm7/16*} res0[31:0] ← Quotient res1[31:0] ← Remainder %rd ← res0[15:0] (Quotient)		
0x18 or 0x19	`ld.ca %rd,%rs`	res0[31:0] ÷ {%rd, %rs} res0[31:0] ← Quotient res1[31:0] ← Remainder %rd ← res0[31:16] (Quotient)		
	(`ext` *imm9*) `ld.ca %rd,`*imm7*	res0[31:0] ÷ {%rd, *imm7/16*} res0[31:0] ← Quotient res1[31:0] ← Remainder %rd ← res0[31:16] (Quotient)		
0x28 or 0x29	`ld.ca %rd,%rs`	res0[31:0] ÷ {%rd, %rs} res0[31:0] ← Quotient res1[31:0] ← Remainder %rd ← res1[15:0] (Remainder)		
	(`ext` *imm9*) `ld.ca %rd,`*imm7*	res0[31:0] ÷ {%rd, *imm7/16*} res0[31:0] ← Quotient res1[31:0] ← Remainder %rd ← res1[15:0] (Remainder)		
0x38 or 0x39	`ld.ca %rd,%rs`	res0[31:0] ÷ {%rd, %rs} res0[31:0] ← Quotient res1[31:0] ← Remainder %rd ← res1[31:16] (Remainder)		
	(`ext` *imm9*) `ld.ca %rd,`*imm7*	res0[31:0] ÷ {%rd, *imm7/16*} res0[31:0] ← Quotient res1[31:0] ← Remainder %rd ← res1[31:16] (Remainder)		

res0: operation result register 0, res1: operation result register 1

Example:

```
ld.cw %r0,0x02 ; Sets the mode (initialize mode 2).
ld.cf %r0,%r1  ; Set the dividend {%r0, %r1} to the operation result register 0.
ld.cw %r0,0x08 ; Sets the mode (unsigned division mode and 16 low-order bits output mode 0).
ld.ca %r0,%r1  ; Performs "res0[31:0] (quotient), res1[31:0] (remainder) = res0[31:0] ÷ {%r0[15:0],
                 %r1[15:0]}" and loads the 16 low-order bits of the result (quotient) to %r0.
ld.ca %r1,%r0  ; Loads the 16 low-order bits of the result (quotient) to %r1.
ld.cw %r0,0x13 ; Sets the mode (operation result read mode and 16 high-order bits output mode 0).
ld.ca %r2,%r0  ; Loads the 16 high-order bits of the result (quotient) to %r2.
ld.cw %r0,0x23 ; Sets the mode (operation result read mode and 16 low-order bits output mode 1).
ld.ca %r3,%r0  ; Loads the 16 low-order bits of the result (remainder) to %r3.
ld.cw %r0,0x33 ; Sets the mode (operation result read mode and 16 high-order bits output mode 1).
ld.ca %r4,%r0  ; Loads the 16 high-order bits of the result (remainder) to %r4.
```

20.5 MAC

The MAC (multiplication and accumulation) function performs "A (32 bits) = B (16 bits) × C (16 bits) + A (32 bits)."
The following shows a procedure to perform a MAC operation:

1. Set the initial value (A) to the operation result register 0.
   - To clear the operation result registers (A = 0):
     Set the mode to 0x00 (initialize mode 0). (It is not necessary to send 0x00 to COPRO2 with another instruction.)
   - To load a 16-bit value to the operation result register 0:
     Set the operation mode to 0x01 (initialize mode 1) and then send the initial value (16 bits) to COPRO2 using a "`ld.cf`" instruction.
   - To load a 32-bit value to the operation result register 0:
     Set the operation mode to 0x02 (initialize mode 2) and then send the initial value (32 bits) to COPRO2 using a "`ld.cf`" instruction.
2. Set the mode to 0x06 (unsigned MAC, 16 low-order bits output mode 0) or 0x07 (signed MAC, 16 low-order bits output mode 0).
3. Repeat sending the 16-bit multiplicand (B) and 16-bit multiplier (C) to COPRO2 the number of times required using a "`ld.ca`" instruction.
4. Read the one-half result (16 low-order bits = A[15:0]) and the flag status.
5. Set the mode to 0x13 (operation result read, 16 high-order bits output mode).
6. Read another one-half result (16 high-order bits = A[31:16]).

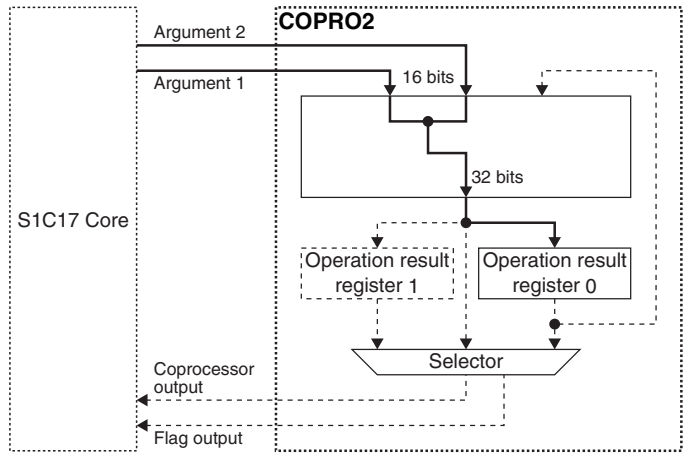


Figure 20.5.1 Data Path in Initialize Mode

Table 20.5.1 Initializing the Operation Result Register 0

Mode setting value	Instruction	Operations	Remarks
0x00	–	res0[31:0] ← 0x0 res1[31:0] ← 0x0	Setting the operating mode executes the initialization without sending data.
0x01	`ld.cf %rd,%rs`	res0[31:16] ← 0x0 res0[15:0] ← %rs	
	(`ext` *imm9*) `ld.cf %rd,`*imm7*	res0[31:16] ← 0x0 res0[15:0] ← *imm7/16*	
0x02	`ld.cf %rd,%rs`	res0[31:16] ← %rd res0[15:0] ← %rs	
	(`ext` *imm9*) `ld.cf %rd,`*imm7*	res0[31:16] ← %rd res0[15:0] ← *imm7/16*	

res0: operation result register 0, res1: operation result register 1

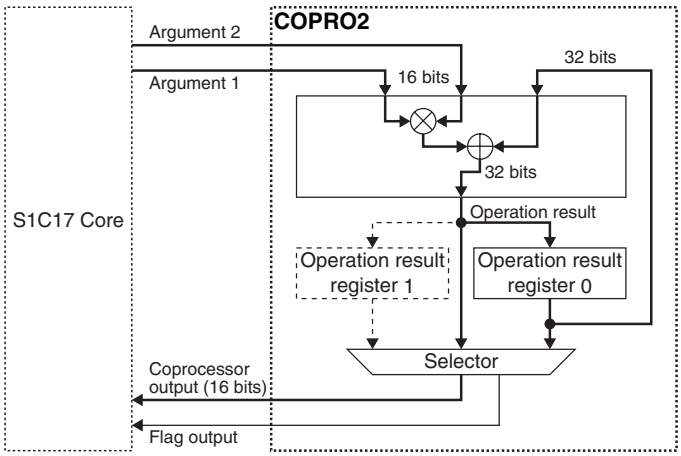


Figure 20.5.2 Data Path in MAC Mode

Table 20.5.2 Operation in MAC Mode

Mode setting value	Instruction	Operations	Flags	Remarks
0x06 or 0x07	`ld.ca %rd,%rs`	res0[31:0] ← %rd × %rs + res0[31:0] %rd ← res0[15:0]	psr (CVZN) ← 0b0100 if an overflow has occurred Otherwise psr (CVZN) ← 0b0000	The operation result register 0 keeps the operation result until it is rewritten by other operation. Overflow can be detected only in signed MAC mode (it does not occur in unsigned MAC mode).
	(`ext` *imm9*) `ld.ca %rd,`*imm7*	res0[31:0] ← %rd × *imm7/16* + res0[31:0] %rd ← res0[15:0]		
0x16 or 0x17	`ld.ca %rd,%rs`	res0[31:0] ← %rd × %rs + res0[31:0] %rd ← res0[31:16]		
	(`ext` *imm9*) `ld.ca %rd,`*imm7*	res0[31:0] ← %rd × *imm7/16* + res0[31:0] %rd ← res0[31:16]		

res0: operation result register 0

Example:

```
ld.cw %r0,0x00 ; Sets the mode (initialize mode 0) to clear the operation result register 0 to 0x0000.
ld.cw %r0,0x07 ; Sets the mode (signed MAC mode and 16 low-order bits output mode 0).
ld.ca %r0,%r1  ; Performs "res0[31:0] = %r0[15:0] × %r1[15:0] + res0[31:0]" and loads the 16 low-
                 order bits of the result to %r0.
ld.cw %r0,0x13 ; Sets the mode (operation result read mode and 16 high-order bits output mode 0).
ld.ca %r1,%r0  ; Loads the 16 high-order bits of the result to %r1.
```

Conditions to set the overflow (V) flag

An overflow occurs in a signed MAC operation and the overflow (V) flag is set to 1 when the signs of the multiplication result, operation result register value, and multiplication & accumulation result match the following conditions:

Table 20.5.3 Conditions to Set the Overflow (V) Flag

Mode setting value	Sign of multiplication result	Sign of operation result register value	Sign of multiplication & accumulation result
0x07	0 (positive)	0 (positive)	1 (negative)
0x07	1 (negative)	1 (negative)	0 (positive)

An overflow occurs when a MAC operation performs addition of positive values and a negative value results, or it performs addition of negative values and a positive value results. The coprocessor holds the operation result until the overflow (V) flag is cleared.

Conditions to clear the overflow (V) flag

The overflow (V) flag that has been set will be cleared when an overflow has not been occurred during execution of the "`ld.ca`" instruction for MAC operation or when the "`ld.ca`" or "`ld.cf`" instruction is executed in an operation mode other than operation result read mode.

20.6 Reading Operation Results

The "`ld.ca`" instruction cannot load a 32-bit operation result to a CPU register, so a multiplication, division or MAC operation returns the one-half (16 bits according to the output mode) result (A[15:0] or A[31:16]) and the flag status to the CPU registers. Another one-half should be read by setting COPRO2 into operation result read mode. The operation result register keeps the loaded operation result until it is rewritten by other operation.

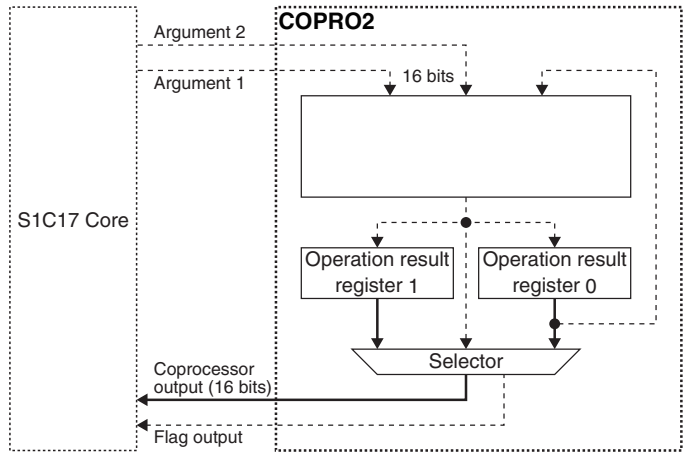


Figure 20.6.1 Data Path in Operation Result Read Mode

Table 20.6.1 Operation in Operation Result Read Mode

Mode setting value	Instruction	Operations	Flags	Remarks
0x03	`ld.ca %rd,%rs`	%rd ← res[15:0]	psr (CVZN) ← 0b0000	This operation mode does not affect the operation result registers 0 and 1.
	`ld.ca %rd,`*`imm7`*	%rd ← res[15:0]		
0x13	`ld.ca %rd,%rs`	%rd ← res[31:16]		
	`ld.ca %rd,`*`imm7`*	%rd ← res[31:16]		
0x23	`ld.ca %rd,%rs`	%rd ← res1[15:0]		
	`ld.ca %rd,`*`imm7`*	%rd ← res1[15:0]		
0x33	`ld.ca %rd,%rs`	%rd ← res1[31:16]		
	`ld.ca %rd,`*`imm7`*	%rd ← res1[31:16]		

res0: operation result register 0, res1: operation result register 1

21 Independent Low-Power Real-Time Clock (RTCLP)

21.1 Overview

The RTCLP is a peripheral circuit that operates independently from the CPU core and other peripheral circuits (hereinafter referred to as MCU core). The main features are outlined below.

- Includes a real-time clock with a dedicated low-power oscillator.
- Includes a 128-byte backup RAM.
- Includes two bits of I/O ports.
- Power consumption can be reduced by stopping power supply to the MCU core except for the RTCLP.
- Interrupts that occur in the RTCLP can resume supplying power to the MCU core.
- The RTCLP control registers are accessible via the synchronous serial interface (SPIA).

Figure 21.1.1 shows the relationship between the RTCLP and the MCU core. Figure 21.1.2 shows the configuration of the real-time clock.

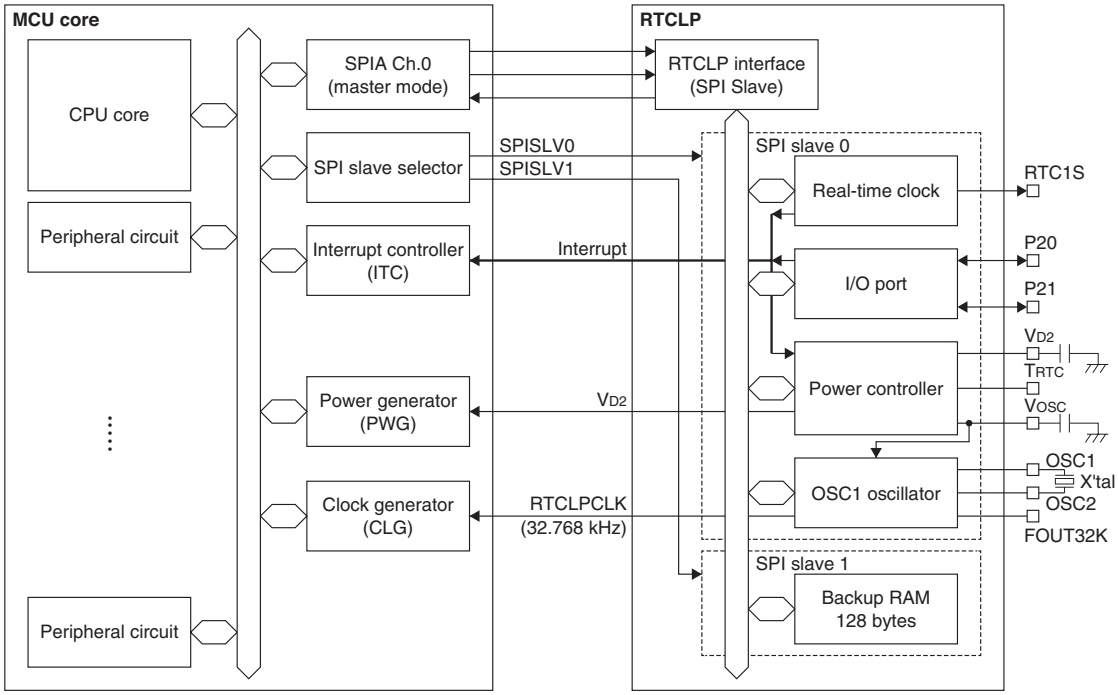


Figure 21.1.1 RTCLP and MCU Core

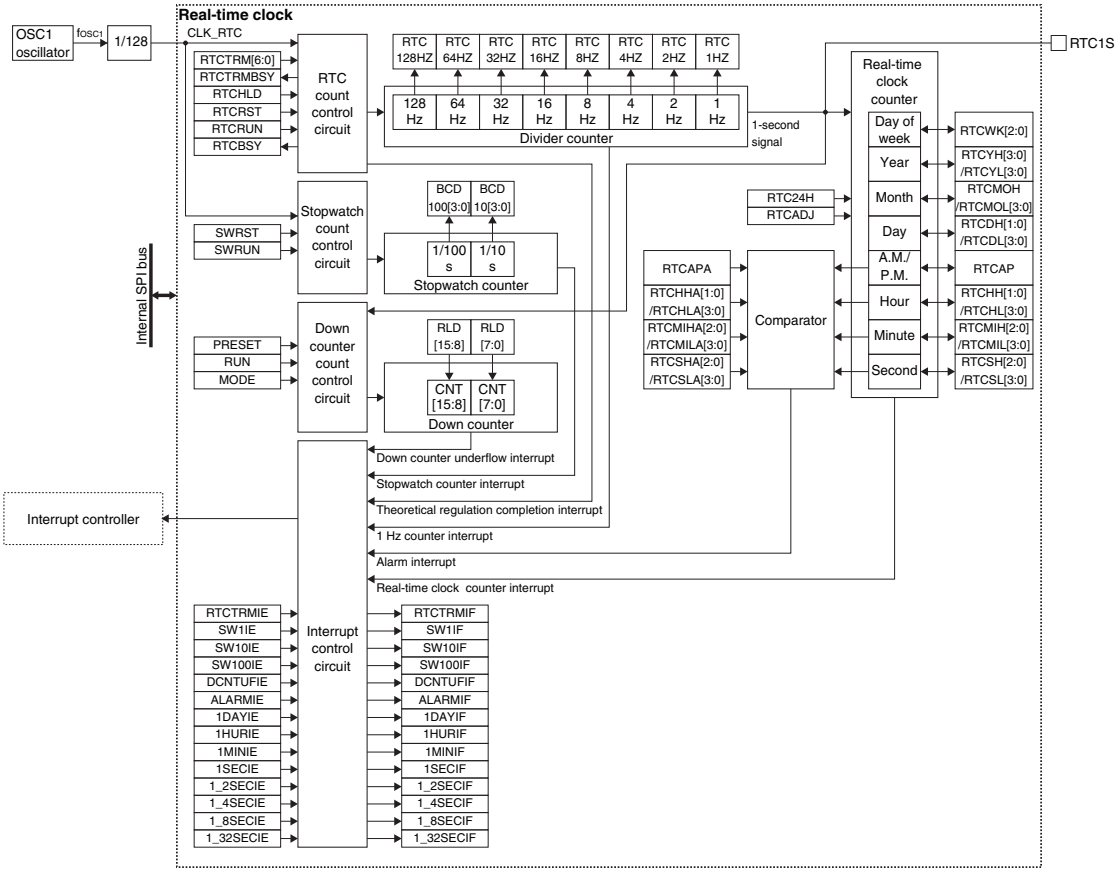


Figure 21.1.2 Real-Time Clock Configuration

21.2 Input/Output Pins

Table 21.2.1 lists the RTCLP pins.

Table 21.2.1 List of RTCLP Pins

Pin name	I/O	Initial status	Function
RTC1S	O*	O (L)*	1-second signal monitor output pin
P2[1:0]	I/O	Hi-Z	I/O port
OSC1	A	–	OSC1 oscillator circuit input
OSC2	A	–	OSC1 oscillator circuit output
V_{OSC}	P	–	V_{OSC} regulator output (OSC1 oscillator power supply)
T_{RTC}	A	–	Test output pin (Leave the pin open during normal operation.)
V_{D2}	A	–	MCU core block operating power supply
FOUT32K	O*	O (L)*	Clock external output (32 kHz clock output)

* Indicates the status when the pin function is switched.

If the port is shared with the RTCLP input/output function and other functions, the RTCLP function must be assigned to the port. For more information, refer to the "I/O Ports" chapter.

21.3 RTCLP Operating Clock

The RTCLP includes a 32.768 kHz crystal oscillator circuit (OSC1 oscillator) that generates the clock to operate the RTCLP functions. This oscillator is initially set into active state.

21.4 Operations

21.4.1 Accessing the RTCLP Registers

The RTCLP works as two SPI slave devices (SPI slaves 0 and 1) connected to the synchronous serial interface (SPIA Ch.0) of this MCU. SPIA and the SPI slave selector (SPISLV_SEL) are used to access to the RTCLP.
Table 21.4.1.1 shows the memory map of the RTCLP.

Note: The RTCLP exists independently from the S1C17 memory space, therefore, it cannot be accessed directly using a CPU instruction.

Table 21.4.1.1 RTCLP Memory Map

SPI slave No.	RTCLP address	Function assigned
0	0x00–0x0f	Real-time clock
	0x10–0x1f	
	0x20–0x2f	RTC power controller
	0x30–0x3f	I/O ports
	0x40–0x4f	OSC1 oscillator
	0x50–0x5f	–
	0x60–0x6f	
	0x70–0x7f	
1	0x00–0x0f	Backup RAM
	0x10–0x1f	
	0x20–0x2f	
	0x30–0x3f	
	0x40–0x4f	
	0x50–0x5f	
	0x60–0x6f	
	0x70–0x7f	

SPI slave selector (SPISLV_SEL)

The SPI slave selector (SPISLV_SEL) exists in the peripheral circuit area of the MCU core to select an SPI slave device (0 or 1). The SPISLV_SEL provides the SPISLVSEL.SLV[2:0] bits to control the internal SPI slave select signals.

Accessing method via SPIA

This section describes the communication protocol between SPIA and the RTCLP. For the SPIA control method, refer to the "Synchronous Serial Interface (SPIA)" chapter.

SPIA configuration

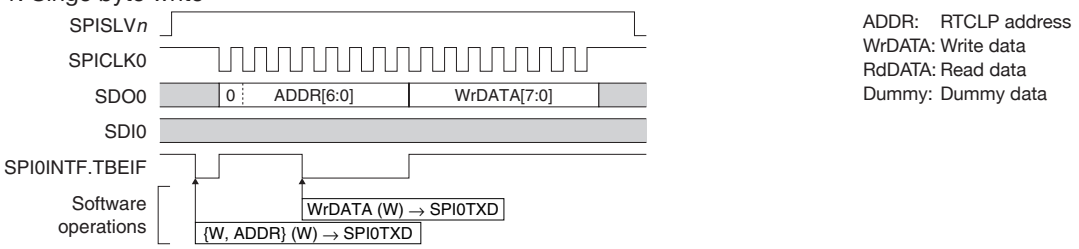
To access the RTCLP, configure SPIA Ch.0 as follows:

- Master/slave mode: Master mode
- Data length: 8 bits
- Data format: MSB first
- Clock phase/polarity: CPHA = 1, CPOL = 1
- Baud rate: 150 kbps

Write access

Figure 21.4.1.1 shows data write operations to the RTCLP.

1. Singe byte write



2. Continuous multiple bytes write

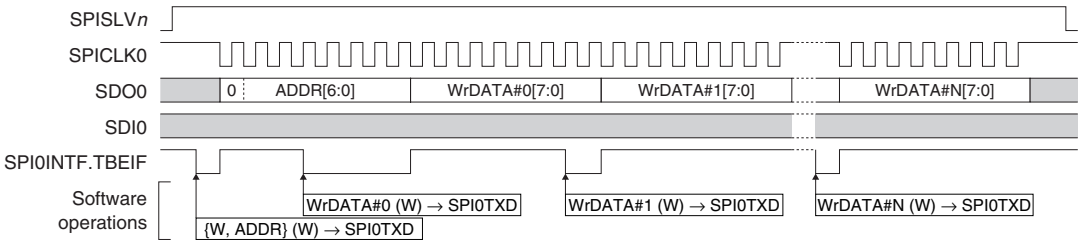
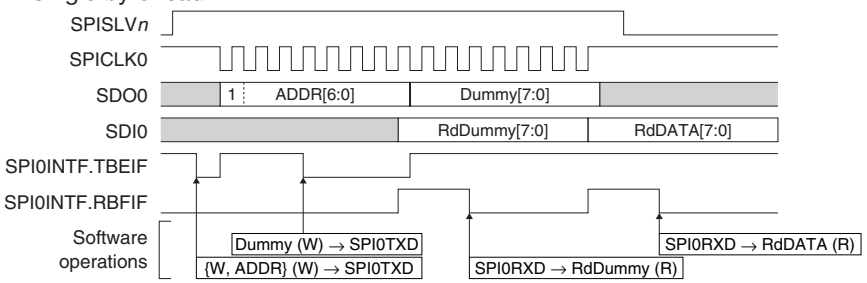


Figure 21.4.1.1 Data Write Operations

Read access

Figure 21.4.1.2 shows data read operations from the RTCLP.

1. Single byte read



2. Continuous multiple bytes read

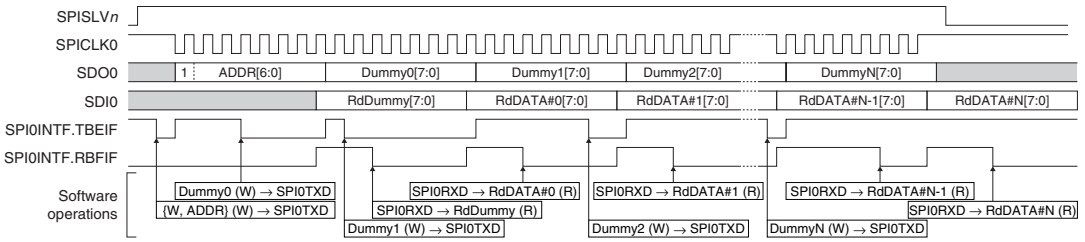


Figure 21.4.1.2 Data Read Operations

Automatic address increment

The address to be accessed is automatically incremented every 8-bit data writing/reading. However, continuous writing/reading does not increment the high-order three bits of the address even if the low-order four bits of the address are incremented from 0xf to 0x0. The write/read operation continues with the high-order three bits of the address left unchanged.

21.4.2 Real-Time Clock Function

The RTCLP includes a real-time clock with a perpetual calendar function. The real-time clock generates the RTC1S signal (1-second signal) from the clock output by the OSC1 oscillator using the divider counter, and counts it using the real-time clock counter. The real-time clock counter consists of second, minute, hour, AM/PM, day, month, year, and day of the week counters that allow software to read/write date and time in BCD codes.
The following shows procedures to set and read date and time, and other functions:

Date and time setting

1. Set the RTCCTL.RTC24H bit. (Set 12H or 24H mode)
2. Write 1 to the RTCCTL.RTCRUN bit. (Start real-time clock counter)
3. Check to see if the RTCCTL.RTCBSY bit = 0 (counter can be rewritten).
   If the RTCCTL.RTCBSY bit = 1, wait until it is set to 0.
4. Write the current date and time in BCD code to the control bits listed below.
   RTCSEC.RTCSH[2:0]/RTCSL[3:0] bits (second)
   RTCMIN.RTCMIH[2:0]/RTCMIL[3:0] bits (minute)
   RTCHUR.RTCHH[1:0]/RTCHL[3:0] bits (hour)
   RTCHUR.RTCAP bit (AM/PM) (effective when RTCCTL.RTC24H bit = 0)
   RTCDAY.RTCDH[1:0]/RTCDL[3:0] bits (day)
   RTCMON.RTCMOH/RTCMOL[3:0] bits (month)
   RTCYAR.RTCYH[3:0]/RTCYL[3:0] bits (year)
   RTCWK.RTCWK[2:0] bits (day of the week)
5 Write 1 to the RTCCTL.RTCADJ bit (execute 30-second correction) using a time signal to adjust the time. (For more information on the 30-second correction, refer to “30-second correction.”)
6. Write 1 to the interrupt flags in the RTCINTF1 register. (Clear interrupt flags)
7. Set the interrupt enable bits in the RTCINTE1 register. (Enable interrupts)

Date and time read

1. Check to see if the RTCCTL.RTCBSY bit = 0.
   If the RTCCTL.RTCBSY bit = 1, wait until it is set to 0.
2. Write 1 to the RTCCTL.RTCHLD bit. (Suspend real-time clock counter operation)
3. Read the date and time from the control bits listed in “Time setting, Step 4” above.
4. Write 0 to the RTCCTL.RTCHLD bit. (Resume real-time clock counter operation)

   If a second count-up timing has occurred in the count hold state, the hardware corrects the second counter for +1 second (for more information on the +1 second correction, refer to “+1 second correction”).

Recognizing leap years

The leap year recognizing algorithm used in the real-time clock is effective only for Christian Era years. Years within 0 to 99 that can be divided by four without a remainder are recognized as leap years. If the year counter = 0x00, the real-time clock assumes it as a common year. If a leap year is recognized, the count range of the day counter changes when the month counter is set to February.

30-second correction

This function is provided to set the time-of-day clock by the time signal. Writing 1 to the RTCCTL.RTCADJ bit clears the second counter and adds 1 to the minute counter if the second counter represents 30 to 59 seconds, or clears the second counter with the minute counter left unchanged if the second counter represents 0 to 29 seconds.

+1 second correction

If a second count-up timing occurred while the RTCCTL.RTCHLD bit = 1 (count hold state), the real-time clock counter counts up by +1 second (performs +1 second correction) after the counting has resumed by writing 0 to the RTCCTL.RTCHLD bit.

Note: If two or more second count-up timings occurred while the RTCCTL.RTCHLD bit = 1, the counter is always corrected for +1 second only.

Corrective operation when a value out of the effective range is set

When a value out of the effective range is set to the year, day of the week, or hour (in 24H mode) counter, the counter will be cleared to 0 at the next count-up timing. When a such value is set to the month, day, or hour (in 12H mode) counter, the counter will be set to 1 at the next count-up timing.

Note: Do not set the RTCMON.RTCMOL[3:0] bits to 0x0 if the RTCMON.RTCMOH bit = 0.

21.4.3 Alarm Function

The real-time clock has an alarm function to generate an interrupt at the designated time. Follow the procedure shown below to set alarm.

1. Set the RTCINTE2.ALARMIE bit to 0. (Disable alarm interrupts)
2. Write the alarm time in BCD code to the control bits listed below (a time within 24 hours from the current time can be specified).
   RTCALM1.RTCSHA[2:0]/RTCSLA[3:0] bits (second)
   RTCALM2.RTCMIHA[2:0]/RTCMILA[3:0] bits (minute)
   RTCALM3.RTCHHA[1:0]/RTCHLA[3:0] bits (hour)
   RTCALM3.RTCAPA bit (AM/PM) (effective when RTCCTL.RTC24H bit = 0)
3. Write 1 to the RTCINTF2.ALARMIF bit. (Clear alarm interrupt flag)
4. Set the RTCINTE2.ALARMIE bit to 1. (Enable alarm interrupts)
   When the real-time clock counter reaches the alarm time set in Step 2, an alarm interrupt occurs.

21.4.4 Stopwatch Function

The real-time clock includes a BCD stopwatch counter with 1/100-second counting supported.
Follow the procedure shown below to start counting of the stopwatch and to read the counter.

Count start

1. Write 1 to the RTCSWCTL.SWRST bit. (Reset stopwatch counter)
2. Write 1 to the interrupt flags in the RTCINTF2 register. (Clear stopwatch interrupt flags)
3. Set the interrupt enable bits in the RTCINTE2 register to 1. (Enable stopwatch interrupts)
4. Write 1 to the RTCSWCTL.SWRUN bit. (Start stopwatch counter)

Counter read

1. Read the count value from the RTCSWCNT.BCD10[3:0] and BCD100[3:0] bits.
2. Read again.
   i. If the two read values are the same, assume that the count values are read correctly.
   ii. If different values are read, perform reading once more and compare the read value with the previous one.

Stopwatch count-up pattern

The stopwatch consists of 1/100-second and 1/10-second counters and these counters perform counting up in increments of approximate 1/100 and 1/10 seconds with the count-up patterns shown in Figure 21.4.4.1.

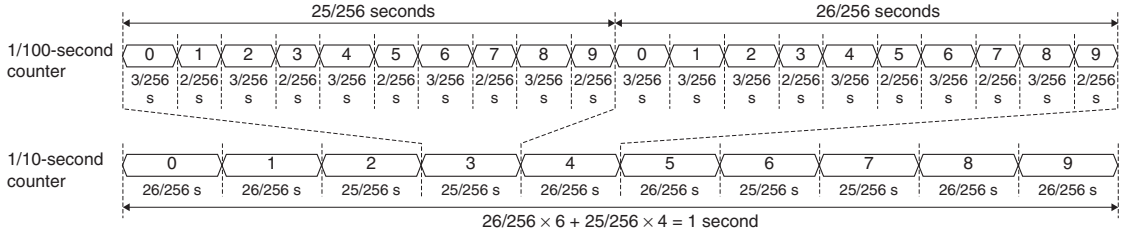


Figure 21.4.4.1 Stopwatch Count-Up Patterns

21.4.5 Down Counter Function

The real-time clock includes a 16-bit presettable down counter with a periodical interrupt generation function in second units (1 to 65,536 second intervals).
Follow the procedure shown below to start counting of the down counter and to read the counter.

Count start

1. Set the RTCDCNTMOD.MODE bit. (Select operation mode (Repeat mode or One-shot mode))
2. Set the RTCDCNTRLDL and RTCDCNTRLDH registers. (Set reload data (counter preset data))
3. Write 1 to the RTCINTF2.DCNTUFIF bit. (Clear down counter interrupt flag)
4. Set the RTCINTE2.DCNTUFIE bit. (Enable down counter interrupts)
5. Set the following RTCDCNTCTL register bits:
   - Set the RTCDCNTCTL.PRESET bit to 1. (Preset reload data to counter)
   - Set the RTCDCNTCTL.RUN bit to 1. (Start counting)

When the RTCDCNTCTL.RUN bit is set to 1, the down counter starts counting down from the preset reload data value using the 1-second signal. When an underflow occurs in the counter, the down counter sets the interrupt flag and presets the reload data to the counter again.

Counter read

1. Read the count value from the RTCDCNTH.CNT[15:8] and RTCDCNTL.CNT[7:0] bits.
2. Read again.
   i. If the two read values are the same, assume that the count values are read correctly.
   ii. If different values are read, perform reading once more and compare the read value with the previous one.

Down counter operation mode

The down counter has two operating modes, repeat mode and one-shot mode.

Repeat mode

The down counter enters repeat mode by setting the RTCDCNTMOD.MODE bit to 0. In repeat mode, the count operation starts by writing 1 to the RTCDCNTCTL.RUN bit and continues until 0 is written. A counter underflow presets the reload data to the counter, so an interrupt can be generated periodically. The underflow period is reload data + 1 [seconds].

One-shot mode

The down counter enters one-shot mode by setting the RTCDCNTMOD.MODE bit to 1. In one-shot mode, the count operation starts by writing 1 to the RTCDCNTCTL.RUN bit and stops after the reload data is preset to the counter when a counter underflow has occurred. At the same time the counter stops, and the RTCDCNTCTL.RUN bit is cleared automatically.

21.4.6 Theoretical Regulation Function

The time-of-day clock loses accuracy if the OSC1 frequency f_{OSC1} has a frequency tolerance from 32.768 kHz. To correct this error without changing any external part, the RTC provides a theoretical regulation function. Follow the procedure below to perform theoretical regulation.

1. Measure f_{OSC1} and calculate the frequency tolerance correction value "m [ppm] = -{(f_{OSC1} - 32,768 [Hz]) / 32,768 [Hz]} × 10^6."
2. Determine the theoretical regulation execution cycle time "n seconds."
3. Determine the value to be written to the RTCTRMCTL.RTCTRM[6:0] bits from the results in Steps 1 and 2.
4. Write the value determined in Step 3 to the RTCTRMCTL.RTCTRM[6:0] bits periodically in n-second cycles using an RTC alarm or second interrupt.
5. Monitor the RTC1S signal to check that every n-second cycle has no error included.

The correction value for theoretical regulation can be specified within the range from -64 to +63 and it should be written to the RTCTRMCTL.RTCTRM[6:0] bits as a two's-complement number. Use Eq. 21.1 to calculate the correction value.

$$\text{RTCTRM}[6:0] = \frac{m}{10^6} \times 256 \times n \qquad \text{(Eq. 21.1)}$$

(However, RTCTRM[6:0] is an integer after rounding off to -64 to +63.)

Where

n: Theoretical regulation execution cycle time [second] (time interval to write the correct value to the RTCTRMCTL.RTCTRM[6:0] bits periodically via software)

m: OSC1 frequency tolerance correction value [ppm]

Figure 21.4.6.1 shows the RTC1S signal waveform.

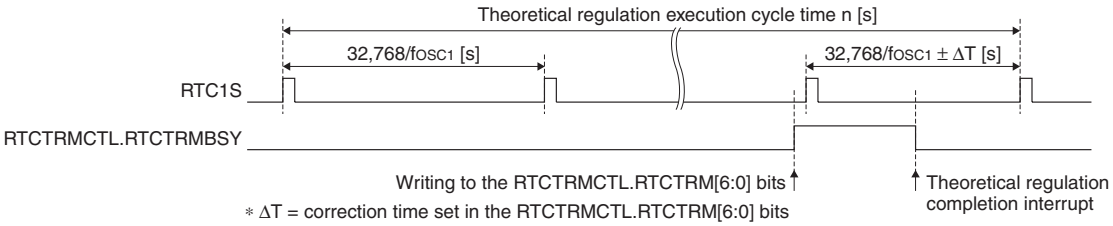


Figure 21.4.6.1 RTC1S Signal Waveform

Table 21.4.6.1 lists the frequency tolerance correction rates when the theoretical regulation execution cycle time n is 4,096 seconds as an example.

Table 21.4.6.1 Correction Rates when Theoretical Regulation Execution Cycle Time n = 4,096 Seconds

RTCTRMCTL.RTCTRM[6:0]bits (two's-complement)	Correction value (decimal)	Correction rate [ppm]	RTCTRMCTL.RTCTRM[6:0]bits (two's-complement)	Correction value (decimal)	Correction rate [ppm]
0x00	0	0.0	0x40	-64	-61.0
0x01	1	1.0	0x41	-63	-60.1
0x02	2	1.9	0x42	-62	-59.1
0x03	3	2.9	0x43	-61	-58.2
. . .	. . .	. . .	. . .	. . .	. . .
0x3e	62	59.1	0x7e	-2	-1.9
0x3f	63	60.1	0x7f	-1	-1.0

Minimum resolution: 1 ppm, Correction rate range: -61.0 to 60.1 ppm

Notes: • The theoretical regulation affects the real-time clock counter, divider counter, and down counter. It does not affect the stopwatch counter.

• After a value is written to the RTCTRMCTL.RTCTRM[6:0] bits, the theoretical regulation correction takes effect on the divider counter value at the same timing as when the divider counter changes to 0x7f. Also an interrupt occurs depending on the counter value at this time.

21.4.7 Power Control Function

The RTCLP has a power control function that turns the MCU core power supply on and off.

- The MCU core power supply voltage V_{D2} can be turned off.
- An RTCLP interrupt can turn V_{D2} on to restart the MCU core.

Turning the MCU core power supply off

Follow the procedure listed below to stop power supply to the MCU core.

1. Halt the peripheral circuits in the MCU core.
2. Enable RTCLP interrupts for restarting the MCU core.
3. Write 1 to the PWRCTL.MCUPD bit via SPIA. (Turn MCU core power supply off)

Writing 1 to the PWRCTL.MCUPD bit first puts the MCU core into reset state. About 1 ms later, V_{D2} turns off to stop the CPU core and peripheral circuits except for the RTCLP. The RTCLP operating voltage V_{OSC} is supplied continuously even while the MCU core is powered down.

Restoring the MCU core power

When an RTCLP interrupt occurs, the V_{D2} regulator starts the startup sequence. About 15 ms later, the reset state of the MCU core is canceled. This restarts the CPU core and peripheral circuits except for the RTCLP.

21.4.8 I/O Port Function

The I/O ports included in the RTCLP consist of two ports, P20 and P21. These ports have the GPIO and interrupt functions.
The port functions are the same as the I/O ports in the MCU core except for the control register configuration and the access method. For the I/O port functions, refer to the "I/O Ports" chapter.

Note: '*y*' of the port and control bit names (e.g. P2*y*), which is described in this chapter, refers to a port number (*y* = 0, 1).

21.4.9 OSC1 Oscillator Control Function

The RTCLP includes a low-power oscillator circuit, called OSC1, that uses a 32.768 kHz crystal resonator. It has the following functions:

- Oscillator power supply
  This is the dedicated power supply circuit for the OSC1 oscillator, and it consists of a regulator and a reference current source. The reference current value, driving capability of the regulator, and load current can be set up using control registers.
- Oscillation inverter
  This oscillator circuit includes a gain-controlled oscillation inverter, a feedback resistor, and a drain resistor, so no external parts are required except for a crystal resonator. It also includes variable gate and drain capacitors allowing adjustment of load capacitance according to the resonator to be used.
- Oscillation stop detector
  This circuit monitors the oscillation status of the crystal resonator and automatically controls the oscillation inverter gain. Also it issues a reset request to the reset circuit if it detects an oscillation stop. This prevents a malfunction of the MCU due to unstable oscillation.

Figure 21.4.9.1 shows the configuration of the OSC1 oscillator circuit.

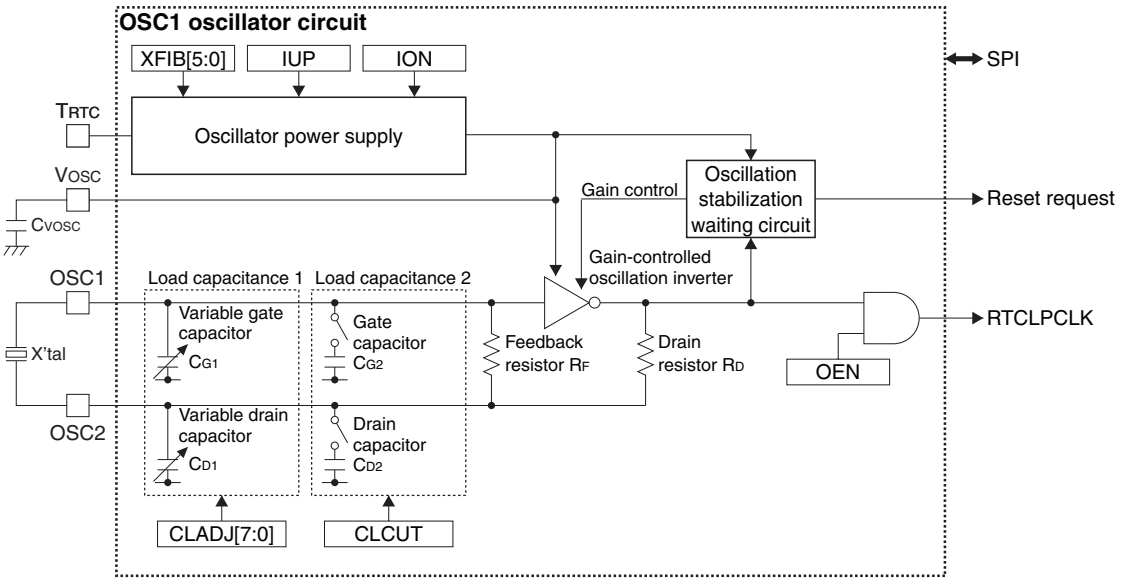


Figure 21.4.9.1 OSC1 Oscillator Circuit Configuration

For the recommended parts and the oscillation characteristics, refer to the "Basic External Connection Diagram" chapter and "OSC1 oscillator circuit characteristics" in the "Electrical Characteristics" chapter, respectively.

Initial settings

Perform the settings below according to the crystal resonator used.

1. Control the OSC1 oscillator power supply using the following bits:
   - Set the VOSCCTL.ION bit to 1. (Control VOSC regulator load current)
   - Set the VOSCCTL.IUP bit to 0. (Control VOSC regulator driving capability)
   - Write the value read from the CLGOSC1TRIM.XFIB[5:0] bits of the clock generator to the VOSCTRIM. XFIB[5:0] bits. (Adjust VOSC regulator reference current)
2. Control the oscillation inverter using the following bits:
   - Set the OSC1CL2.CLCUT bit to 1. (Connect load capacitance 2)
   - Set the OSC1CL1.CLADJ[7:0] bits according to the result of evaluation using the populated circuit board. (Adjust load capacitance 1 frequency)

Note: Do not configure the real-time clock before initializing the OSC1 oscillator circuit.

Stopping/resuming RTCLPCLK supply to MCU core

The OSC1 oscillator circuit always operates and it is initially set so that RTCLPCLK is supplied to the MCU core. When operating the RTCLP only, the RTCLPCLK supply to the MCU core can be stopped as in the procedure below.

1. Stop use of OSC1CLK in the peripheral circuits of the MCU core and the clock generator.
2. Set the CLGOSC.OSC1EN bit to 0. (Disable RTCLPCLK input to MCU core)
3. Set the F32KCTL.OEN bit to 0. (Disable RTCLPCLK output from RTCLP)

Follow the procedure below to resume supplying RTCLPCLK to the MCU core.

1. Set the F32KCTL.OEN bit to 1. (Enable RTCLPCLK output from RTCLP)
2. Set the CLGOSC.OSC1EN bit to 1. (Enable RTCLPCLK input to MCU core)

Note that the OSC1 oscillator circuit does not stop even when the MCU core enters SLEEP mode.
The operating clock of the real-time clock is always supplied regardless of how the F32KCTL.OEN bit is set.

FOUT32K output

The FOUT32K pin outputs RTCLPCLK externally while the F32KCTL.OEN bit = 1. To use this frequency monitor function, the pin function of the I/O port to which the FOUT32K output is assigned should be switched to FOUT32K.

21.4.10 Backup RAM Function

The RTCLP includes a backup RAM for storing various information, such as display data, while the MCU core is powered down.

- Capacity: 128 bytes
- Address: SPI slave 1 0x0 to 0x7f (RAM physical addresses 0x0 to 0x7f)

A reset request does not initialize the backup RAM. Writing a specific value to the backup RAM can determine what the current state is after turning power on or after resetting.

Precaution on access

The data size to be read/written continuously is limited up to 16 bytes at a time due to the restriction on the automatic address increment function (the high-order three bits of the RTCLP address are fixed without incrementing).

21.5 Interrupts

The RTCLP has a function to generate the interrupts shown in Table 21.5.1.

Table 21.5.1 RTCLP Interrupt Function

Interrupt	Interrupt flag	Set condition	Clear condition
Alarm	RTCINTF2.ALARMIF	Matching between the RTCALM1–3 register contents and the real-time clock counter contents	Writing 1
1-day	RTCINTF1.1DAYIF	Day counter count up	Writing 1
1-hour	RTCINTF1.1HURIF	Hour counter count up	Writing 1
1-minute	RTCINTF1.1MINIF	Minute counter count up	Writing 1
1-second	RTCINTF1.1SECIF	Second counter count up	Writing 1
1/2-second	RTCINTF1.1_2SECIF	See Figure 21.5.1.	Writing 1
1/4-second	RTCINTF1.1_4SECIF	See Figure 21.5.1.	Writing 1
1/8-second	RTCINTF1.1_8SECIF	See Figure 21.5.1.	Writing 1
1/32-second	RTCINTF1.1_32SECIF	See Figure 21.5.1.	Writing 1
Stopwatch 1 Hz	RTCINTF2.SW1IF	1/10-second counter overflow	Writing 1
Stopwatch 10 Hz	RTCINTF2.SW10IF	1/10-second counter count up	Writing 1
Stopwatch 100 Hz	RTCINTF2.SW100IF	1/100-second counter count up	Writing 1
Down counter underflow	RTCINTF2.RTCDCNTUFIF	When the down counter underflows	Writing 1
Theoretical regulation completion	RTCINTF2.RTCTRMIF	At the end of theoretical regulation operation	Writing 1
P2 port input interrupt	P2INTF.P2IF*y*	Rising or falling edge of the input signal	Writing 1
	(PINTFGRP.P2INT) *	Setting an interrupt flag in the port group	Clearing P2INTF.P2IF*y*

* This bit is assigned in an MCU core control register.

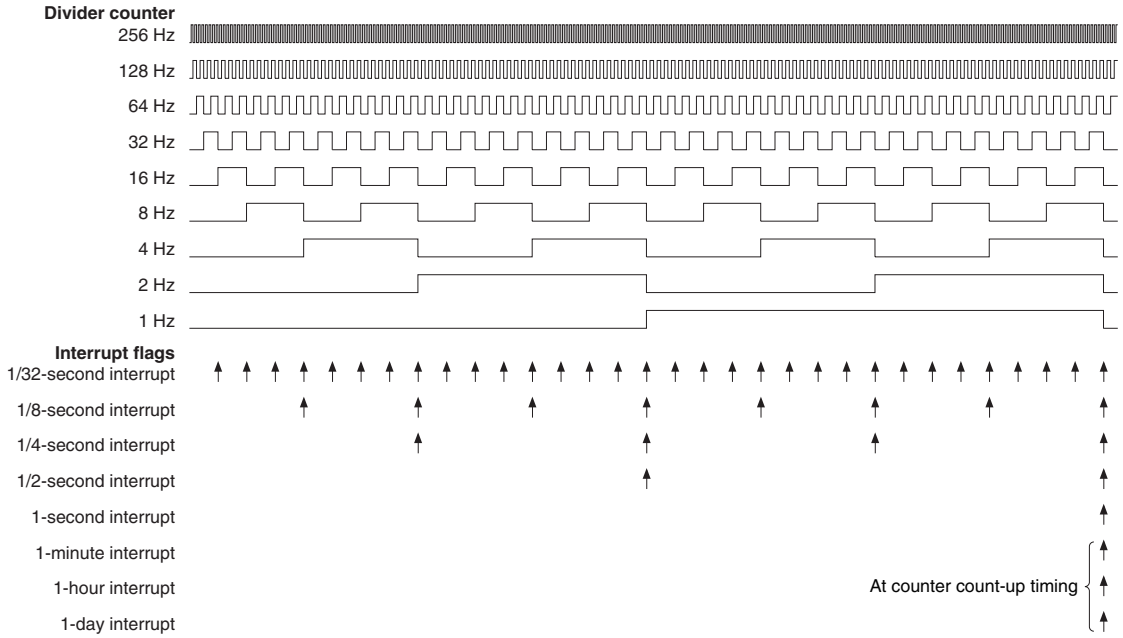


Figure 21.5.1 Real-Time Clock Interrupt Timings

Notes: • 1-second to 1/32-second interrupts occur after a lapse of 1/256 second from change of the divider counter value.

• An alarm interrupt occurs after a lapse of 1/256 second from matching between the AM/PM (in 12H mode), hour, minute, and second counter value and the alarm setting value.

The RTCLP provides interrupt enable bits corresponding to each interrupt flag. An interrupt request is sent to the interrupt controller only when the interrupt flag, of which interrupt has been enabled by the interrupt enable bit, is set. For more information on interrupt control, refer to the "Interrupt Controller" chapter.

For more information on the P2 port input interrupt, refer to the "I/O Ports" chapter.

Interrupt when the MCU core is operating (WRCTL.MCUPD bit = 0)

The interrupt request that has occurred is sent to the interrupt controller immediately and processed similar to other interrupts.

Interrupt when the MCU core is powered down (WRCTL.MCUPD bit = 1)

When an RTCLP interrupt occurs while the MCU core is powered down, the PWRCTL.MCUPD bit in the power controller is cleared to 0 to restart the MCU core. To clear the PWRCTL.MCUPD bit with an RTCLP interrupt, the corresponding interrupt enable bit must be set to 1.

The interrupt request that has occurred while the MCU core is powered down will be accepted by the interrupt controller after the MCU core is restarted (however, the CPU core and interrupt controller must be configured to enable interrupts).

21.6 Control Register

SPI Slave Select Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SPISLVSEL	15–8	–	0x00	–	R	–
	7–3	–	0x00	–	R	
	2–0	SLV[2:0]	0x0	H0	R/W	

Bits 15–3 Reserved

Bits 2–0 SLV[2:0]

These bits select the SPI slave device in the RTCLP to be accessed.

Table 21.4.1.2 SPI Slave Device Selection

SPISLVSEL.SLV[2:0] bits	Slave device
0b100	Setting prohibited
0b∗10	SPI slave 1
0b∗∗1	SPI slave 0
0b000	Not selected

Use this register to select the SPI slave to be accessed before starting RTCLP access via SPIA.
Selecting an SPI slave using the SPISLVSEL.SLV[2:0] bits asserts the internal SPI slave select signal (SPISLV*n*). To negate the slave select signal, select another SPI slave using the SPISLVSEL.SLV[2:0] bits or set the SPISLVSEL.SLV[2:0] bits to 0b000.

21.7 RTCLP Internal Control Registers

The RTCLP internal registers have an address independent of the S1C17 memory space. For how to access the registers, refer to Section 21.4.1, "Accessing the RTCLP Registers."
Table 21.7.1 shows the RTCLP register map.

Table 21.7.1 RTCLP Register Map

Peripheral circuit	Address	Register name	
Real-time clock	0x00	RTCCTL	RTC Control Register
	0x01	RTCTRMCTL	RTC Trimming Control Register
	0x03	RTCALM1	RTC Second Alarm Register
	0x04	RTCALM2	RTC Minute Alarm Register
	0x05	RTCALM3	RTC Hour Alarm Register
	0x06	RTCSWCTL	RTC Stopwatch Control Register
	0x07	RTCSWCNT	RTC Stopwatch Counter Register
	0x08	RTCDIV	RTC Divider Register
	0x09	RTCSEC	RTC Second Register
	0x0a	RTCMIN	RTC Minute Register
	0x0b	RTCHUR	RTC Hour Register
	0x0c	RTCDAY	RTC Day Register
	0x0d	RTCMON	RTC Month Register
	0x0e	RTCYAR	RTC Year Register
	0x0f	RTCWK	RTC Week Register
	0x10	RTCINTF1	RTC Interrupt Flag Register 1
	0x11	RTCINTF2	RTC Interrupt Flag Register 2
	0x12	RTCINTE1	RTC Interrupt Enable Register 1
	0x13	RTCINTE2	RTC Interrupt Enable Register 2
	0x18	RTCDCNTCTL	RTC Down Counter Control Register
	0x19	RTCDCNTMOD	RTC Down Counter Mode Register
	0x1a	RTCDCNTRLDL	RTC Down Counter Lower Reload Data Register
	0x1b	RTCDCNTRLDH	RTC Down Counter Upper Reload Data Register
	0x1c	RTCDCNTL	RTC Down Counter Lower Data Register
	0x1d	RTCDCNTH	RTC Down Counter Upper Data Register
Power controller	0x20	PWRCTL	Power Control Register

Peripheral circuit	Address	Register name	
P2 I/O port	0x30	P2IN	P2 Port Input Data Register
	0x31	P2OUT	P2 Port Output Data Register
	0x32	P2OEN	P2 Port Output Enable Register
	0x33	P2IEN	P2 Port Input Enable Register
	0x34	P2REN	P2 Port Pull-up/down Enable Register
	0x35	P2PDPU	P2 Port Pull-up/down Select Register
	0x36	P2INTF	P2 Port Interrupt Flag Register
	0x38	P2INTE	P2 Port Interrupt Enable Register
	0x39	P2IEDGE	P2 Port Interrupt Edge Select Register
	0x3a	P2CHATEN	P2 Port Chattering Filter Enable Register
	0x3c	P2MODSEL	P2 Port Mode Select Register
	0x3e	P2FNCSEL0	P2 Port Function Select Register 0
OSC1 oscillator	0x40	OSC1CL1	OSC1 Load Capacitance 1 Control Register
	0x41	OSC1CL2	OSC1 Load Capacitance 2 Control Register
	0x42	VOSCCTL	Vosc Regulator Control Register
	0x43	VOSCTRIM	Vosc Reference Current Adjustment Register
	0x44	F32KCTL	RTCLPCLK Control Register

RTC Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCCTL	7	–	0	–	R	–
	6	RTCBSY	0	H0	R	
	5	RTCHLD	0	H0	R/W	Cleared by setting the RTCCTL.RTCRST bit to 1.
	4	RTC24H	0	H0	R/W	–
	3	–	0	–	R	
	2	RTCADJ	0	H0	R/W	Cleared by setting the RTCCTL.RTCRST bit to 1.
	1	RTCRST	0	H0	R/W	–
	0	RTCRUN	0	H0	R/W	

Bit 7 Reserved

Bit 6 RTCBSY

This bit indicates whether the counter is performing count-up operation or not.

1 (R): In count-up operation

0 (R): Idle (ready to rewrite real-time clock counter)

This bit goes 1 when performing 1-second count-up, +1 second correction, or 30-second correction. It retains 1 for 1/256 second and then reverts to 0.

Bit 5 RTCHLD

This bit halts the count-up operation of the real-time clock counter.

1 (R/W): Halt real-time clock counter count-up operation

0 (R/W): Normal operation

Writing 1 to this bit halts the count-up operation of the real-time clock counter, this makes it possible to read the counter value correctly without changing the counter. Write 0 to this bit to resume count-up operation immediately after the counter has been read. Depending on these operation timings, the +1 second correction may be executed after the count-up operation resumes. For more information on the +1 second correction, refer to "Real-time clock counter operations."

Note: When the RTCTRMCTL.RTCTRMBSY bit = 1, the RTCCTL.RTCHLD bit cannot be rewritten to 1 (as fixed at 0).

Bit 4 RTC24H

This bit sets the hour counter to 24H mode or 12H mode.

1 (R/W): 24H mode

0 (R/W): 12H mode

This selection changes the count range of the hour counter. Note, however, that the counter value is not updated automatically, therefore, it must be programmed again.

Note: Be sure to avoid writing to this bit when the RTCCTL.RTCRUN bit = 1.

Bit 3 Reserved

Bit 2 RTCADJ

This bit executes the 30-second correction time adjustment function.

1 (W): Execute 30-second correction
0 (W): Ineffective
1 (R): 30-second correction is executing.
0 (R): 30-second correction has finished. (Normal operation)

Writing 1 to this bit executes 30-second correction and an enabled interrupt occurs even if the RTCCTL.RTCRUN bit = 0. The correction takes up to 2/256 seconds. The RTCCTL.RTCADJ bit is automatically cleared to 0 when the correction has finished. For more information on the 30-second correction, refer to "Real-time clock counter operations."

Notes:
- Be sure to avoid writing to this bit when the RTCCTL.RTCBSY bit = 1.
- Do not write 1 to this bit again while the RTCCTL.RTCADJ bit = 1.

Bit 1 RTCRST

This bit resets the divider counter, the RTCCTL.RTCADJ bit, and the RTCCTL.RTCHLD bit.

1 (W): Reset
0 (W): Ineffective
1 (R): Reset is being executed.
0 (R): Reset has finished. (Normal operation)

This bit is automatically cleared to 0 after reset has finished.

Bit 0 RTCRUN

This bit starts/stops the real-time clock counter.

1 (R/W): Running/start control
0 (R/W): Idle/stop control

When the real-time clock counter stops counting by writing 0 to this bit, the counter retains the value when it stopped. Writing 1 to this bit again resumes counting from the value retained.

RTC Trimming Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCTRMCTL	7	RTCTRMBSY	0	H0	R	–
	6–0	RTCTRM[6:0]	0x00	H0	W	Read as 0x00.

Bit 7 RTCTRMBSY

This bit indicates whether the theoretical regulation is currently executed or not.

1 (R): Theoretical regulation is executing.
0 (R): Theoretical regulation has finished (or not executed).

This bit goes 1 when a value is written to the RTCTRMCTL.RTCTRM[6:0] bits. The theoretical regulation takes up to 1 second for execution. This bit reverts to 0 automatically after the theoretical regulation has finished execution.

Bits 6–0 RTCTRM[6:0]

Write the correction value for adjusting the 1 Hz frequency to these bits to execute theoretical regulation. For a calculation method of correction value, refer to "Theoretical Regulation Function."

Notes:
- When the RTCTRMCTL.RTCTRMBSY bit = 1, the RTCTRMCTL.RTCTRM[6:0] bits cannot be rewritten.
- Writing 0x00 to the RTCTRMCTL.RTCTRM[6:0] bits sets the RTCTRMCTL.RTCTRMBSY bit to 1 as well. However, no correcting operation is performed.

RTC Second Alarm Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCALM1	7	–	0	–	R	–
	6–4	RTCSHA[2:0]	0x0	H0	R/W	
	3–0	RTCSLA[3:0]	0x0	H0	R/W	

Bit 7 Reserved

Bits 6–4 RTCSHA[2:0]

Bits 3–0 RTCSLA[3:0]

The RTCALM1.RTCSHA[2:0] bits and the RTCALM1.RTCSLA[3:0] bits set the 10-second digit and 1-second digit of the alarm time, respectively. A value within 0 to 59 seconds can be set in BCD code as shown in Table 21.7.2.

Table 21.7.2 Setting Examples in BCD Code

Setting value in BCD code		Alarm (second) setting
RTCALM1.RTCSHA[2:0] bits	RTCALM1.RTCSLA[3:0] bits	
0x0	0x0	00 seconds
0x0	0x1	01 second
. . .	. . .	. . .
0x0	0x9	09 seconds
0x1	0x0	10 seconds
. . .	. . .	. . .
0x5	0x9	59 seconds

RTC Minute Alarm Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCALM2	7	–	0	–	R	–
	6–4	RTCMIHA[2:0]	0x0	H0	R/W	
	3–0	RTCMILA[3:0]	0x0	H0	R/W	

Bit 7 Reserved

Bits 6–4 RTCMIHA[2:0]

Bits 3–0 RTCMILA[3:0]

The RTCALM2.RTCMIHA[2:0] bits and the RTCALM2.RTCMILA[3:0] bits set the 10-minute digit and 1-minute digit of the alarm time, respectively. A value within 0 to 59 minutes can be set in BCD code.

RTC Hour Alarm Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCALM3	7	–	0	–	R	–
	6	RTCAPA	0	H0	R/W	
	5–4	RTCHHA[1:0]	0x0	H0	R/W	
	3–0	RTCHLA[3:0]	0x0	H0	R/W	

Bit 7 Reserved

Bit 6 RTCAPA

This bit sets A.M. or P.M. of the alarm time in 12H mode (RTCCTL.RTC24H bit = 0).
1 (R/W): P.M.
0 (R/W): A.M.

This setting is ineffective in 24H mode (RTCCTL.RTC24H bit = 1).

Bits 5–4 RTCHHA[1:0]

Bits 3–0 RTCHLA[3:0]

The RTCALM3.RTCHHA[1:0] bits and the RTCALM3.RTCHLA[3:0] bits set the 10-hour digit and 1-hour digit of the alarm time, respectively. A value within 1 to 12 o'clock in 12H mode or 0 to 23 in 24H mode can be set in BCD code.

RTC Stopwatch Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCSWCTL	7–5	–	0x0	–	R	–
	4	SWRST	0	H0	W	Read as 0.
	3–1	–	0x0	–	R	–
	0	SWRUN	0	H0	R/W	

Bits 7–5 Reserved

Bit 4 SWRST

This bit resets the stopwatch counter to 0x00.

1 (W): Reset
0 (W): Ineffective
0 (R): Always 0 when being read

When the stopwatch counter in running status is reset, it continues counting from count 0x00. The stopwatch counter retains 0x00 if it is reset in idle status.

Bits 3–1 Reserved

Bit 0 SWRUN

This bit starts/stops the stopwatch counter.

1 (R/W): Running/start control
0 (R/W): Idle/stop control

When the stopwatch counter stops counting by writing 0 to this bit, the counter retains the value when it stopped. Writing 1 to this bit again resumes counting from the value retained.

Note: The stopwatch counter stops in sync with the stopwatch clock after 0 is written to the RTCSWCTL.SWRUN bit. Therefore, the counter value may be incremented (+1) from the value at writing 0.

RTC Stopwatch Counter Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCSWCNT	7–4	BCD10[3:0]	0x0	H0	R	–
	3–0	BCD100[3:0]	0x0	H0	R	

Bits 7–4 BCD10[3:0]
Bits 3–0 BCD100[3:0]

The 1/10-second and 1/100-second digits of the stopwatch counter can be read as a BCD code from the RTCSWCNT.BCD10[3:0] bits and the RTCSWCNT.BCD100[3:0] bits, respectively.

Note: The counter value may not be read correctly while the stopwatch counter is running. The RTCSWCNT.BCD10[3:0]/BCD100[3:0] bits must be read twice and assume the counter value was read successfully if the two read results are the same.

RTC Divider Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCDIV	7	RTC1HZ	0	H0	R	Cleared by setting the RTCCTL.RTCRST bit to 1.
	6	RTC2HZ	0	H0	R	
	5	RTC4HZ	0	H0	R	
	4	RTC8HZ	0	H0	R	
	3	RTC16HZ	0	H0	R	
	2	RTC32HZ	0	H0	R	
	1	RTC64HZ	0	H0	R	
	0	RTC128HZ	0	H0	R	

Bit 7 RTC1HZ
Bit 6 RTC2HZ
Bit 5 RTC4HZ
Bit 4 RTC8HZ
Bit 3 RTC16HZ
Bit 2 RTC32HZ
Bit 1 RTC64HZ
Bit 0 RTC128HZ

The divider counter data can be read from these bits.
The following shows the correspondence between the bit and frequency:
RTCDIV.RTC1HZ bit: 1 Hz
RTCDIV.RTC2HZ bit: 2 Hz
RTCDIV.RTC4HZ bit: 4 Hz
RTCDIV.RTC8HZ bit: 8 Hz
RTCDIV.RTC16HZ bit: 16 Hz
RTCDIV.RTC32HZ bit: 32 Hz
RTCDIV.RTC64HZ bit: 64 Hz
RTCDIV.RTC128HZ bit: 128 Hz

Note: The counter value may not be read correctly while the divider counter is running. These bits must be read twice and assume the counter value was read successfully if the two read results are the same.

RTC Second Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCSEC	7	–	0	–	R	–
	6–4	RTCSH[2:0]	0x0	H0	R/W	
	3–0	RTCSL[3:0]	0x0	H0	R/W	

Bit 7 Reserved

Bits 6–4 RTCSH[2:0]
Bits 3–0 RTCSL[3:0]

The RTCSEC.RTCSH[2:0] bits and the RTCSEC.RTCSL[3:0] bits are used to set and read the 10-second digit and the 1-second digit of the second counter, respectively. The setting/read values are a BCD code within the range from 0 to 59.

Note: Be sure to avoid writing to the RTCSEC.RTCSH[2:0]/RTCSL[3:0] bits while the RTCCTL.RTCBSY bit = 1.

RTC Minute Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCMIN	7	–	0	–	R	–
	6–4	RTCMIH[2:0]	0x0	H0	R/W	
	3–0	RTCMIL[3:0]	0x0	H0	R/W	

Bit 7 Reserved

Bits 6–4 RTCMIH[2:0]
Bits 3–0 RTCMIL[3:0]

The RTCMIN.RTCMIH[2:0] bits and the RTCMIN.RTCMIL[3:0] bits are used to set and read the 10-minute digit and the 1-minute digit of the minute counter, respectively. The setting/read values are a BCD code within the range from 0 to 59.

Note: Be sure to avoid writing to the RTCMIN.RTCMIH[2:0]/RTCMIL[3:0] bits while the RTCCTL.RTCBSY bit = 1.

RTC Hour Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCHUR	7	–	0	–	R	–
	6	RTCAP	0	H0	R/W	
	5–4	RTCHH[1:0]	0x1	H0	R/W	
	3–0	RTCHL[3:0]	0x2	H0	R/W	

Bit 7 Reserved

Bit 6 RTCAP

This bit is used to set and read A.M. or P.M. data in 12H mode (RTCCTL.RTC24H bit = 0).
1 (R/W): P.M.
0 (R/W): A.M.

In 24H mode (RTCCTL.RTC24H bit = 1), this bit is fixed at 0 and writing 1 is ignored. However, if the RTCHUR.RTCAP bit = 1 when changed to 24H mode, it goes 0 at the next count-up timing of the hour counter.

Bits 5–4 RTCHH[1:0]
Bits 3–0 RTCHL[3:0]

The RTCHUR.RTCHH[1:0] bits and the RTCHUR.RTCHL[3:0] bits are used to set and read the 10-hour digit and the 1-hour digit of the hour counter, respectively. The setting/read values are a BCD code within the range from 1 to 12 in 12H mode or 0 to 23 in 24H mode.

Note: Be sure to avoid writing to the RTCHUR.RTCHH[1:0]/RTCHL[3:0] bits while the RTCCTL.RTCBSY bit = 1.

RTC Day Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCDAY	7–6	–	0x0	–	R	–
	5–4	RTCDH[1:0]	0x0	H0	R/W	
	3–0	RTCDL[3:0]	0x1	H0	R/W	

Bits 7–6 Reserved

Bits 5–4 RTCDH[1:0]
Bits 3–0 RTCDL[3:0]

The RTCDAY.RTCDH[1:0] bits and the RTCDAY.RTCDL[3:0] bits are used to set and read the 10-day digit and the 1-day digit of the day counter, respectively. The setting/read values are a BCD code within the range from 1 to 31 (to 28 for February in a common year, to 29 for February in a leap year, or to 30 for April/June/September/November).

Note: Be sure to avoid writing to the RTCDAY.RTCDH[1:0]/RTCDL[3:0] bits while the RTCCTL.RTCBSY bit = 1.

RTC Month Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCMON	7–5	–	0x0	–	R	–
	4	RTCMOH	0	H0	R/W	
	3–0	RTCMOL[3:0]	0x1	H0	R/W	

Bits 7–5 Reserved

Bit 4 RTCMOH
Bits 3–0 RTCMOL[3:0]

The RTCMON.RTCMOH bit and the RTCMON.RTCMOL[3:0] bits are used to set and read the 10-month digit and the 1-month digit of the month counter, respectively. The setting/read values are a BCD code within the range from 1 to 12.

Notes: • Be sure to avoid writing to the RTCMON.RTCMOH/RTCMOL[3:0] bits while the RTCCTL.RTCBSY bit = 1.

• Be sure to avoid setting the RTCMON.RTCMOH/RTCMOL[3:0] bits to 0x00.

RTC Year Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCYAR	7–4	RTCYH[3:0]	0x0	H0	R/W	–
	3–0	RTCYL[3:0]	0x0	H0	R/W	

Bits 7–4 RTCYH[3:0]

Bits 3–0 RTCYL[3:0]

The RTCYAR.RTCYH[3:0] bits and the RTCYAR.RTCYL[3:0] bits are used to set and read the 10-year digit and the 1-year digit of the year counter, respectively. The setting/read values are a BCD code within the range from 0 to 99.

Note: Be sure to avoid writing to the RTCYAR.RTCYH[3:0]/RTCYL[3:0] bits while the RTCCTL.RTCBSY bit = 1.

RTC Week Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCWK	7–3	–	0x00	–	R	–
	2–0	RTCWK[2:0]	0x0	H0	R/W	

Bits 7–3 Reserved

Bits 2–0 RTCWK[2:0]

These bits are used to set and read day of the week.

The day of the week counter is a base-7 counter and the setting/read values are 0x0 to 0x6. Table 21.7.3 lists the correspondence between the count value and day of the week.

Table 21.7.3 Correspondence between the count value and day of the week

RTCWK.RTCWK[2:0] bits	Day of the week
0x6	Saturday
0x5	Friday
0x4	Thursday
0x3	Wednesday
0x2	Tuesday
0x1	Monday
0x0	Sunday

Note: Be sure to avoid writing to the RTCWK.RTCWK[2:0] bits while the RTCCTL.RTCBSY bit = 1.

RTC Interrupt Flag Register 1

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCINTF1	7	1DAYIF	0	H0	R/W	Cleared by writing 1.
	6	1HURIF	0	H0	R/W	
	5	1MINIF	0	H0	R/W	
	4	1SECIF	0	H0	R/W	
	3	1_2SECIF	0	H0	R/W	
	2	1_4SECIF	0	H0	R/W	
	1	1_8SECIF	0	H0	R/W	
	0	1_32SECIF	0	H0	R/W	

Bit 7 1DAYIF
Bit 6 1HURIF
Bit 5 1MINIF
Bit 4 1SECIF
Bit 3 1_2SECIF
Bit 2 1_4SECIF
Bit 1 1_8SECIF
Bit 0 1_32SECIF

These bits indicate the real-time clock interrupt cause occurrence status.
1 (R): Cause of interrupt occurred
0 (R): No cause of interrupt occurred
1 (W): Clear flag
0 (W): Ineffective

The following shows the correspondence between the bit and interrupt:
RTCINTF1.1DAYIF bit: 1-day interrupt
RTCINTF1.1HURIF bit: 1-hour interrupt
RTCINTF1.1MINIF bit: 1-minute interrupt
RTCINTF1.1SECIF bit: 1-second interrupt
RTCINTF1.1_2SECIF bit: 1/2-second interrupt
RTCINTF1.1_4SECIF bit: 1/4-second interrupt
RTCINTF1.1_8SECIF bit: 1/8-second interrupt
RTCINTF1.1_32SECIF bit: 1/32-second interrupt

RTC Interrupt Flag Register 2

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCINTF2	7	RTCTRMIF	0	H0	R/W	Cleared by writing 1.
	6	SW1IF	0	H0	R/W	
	5	SW10IF	0	H0	R/W	
	4	SW100IF	0	H0	R/W	
	3–2	–	0x0	–	R	–
	1	DCNTUFIF	0	H0	R/W	Cleared by writing 1.
	0	ALARMIF	0	H0	R/W	

Bit 7 RTCTRMIF
Bit 6 SW1IF
Bit 5 SW10IF
Bit 4 SW100IF
Bit 1 DCNTUFIF
Bit 0 ALARMIF

These bits indicate the real-time clock interrupt cause occurrence status.
1 (R): Cause of interrupt occurred
0 (R): No cause of interrupt occurred
1 (W): Clear flag
0 (W): Ineffective

The following shows the correspondence between the bit and interrupt:
RTCINTF2.RTCTRMIF bit: Theoretical regulation completion interrupt
RTCINTF2.SW1IF bit: Stopwatch 1 Hz interrupt
RTCINTF2.SW10IF bit: Stopwatch 10 Hz interrupt
RTCINTF2.SW100IF bit: Stopwatch 100 Hz interrupt
RTCINTF2. DCNTUFIF bit: Down counter underflow interrupt
RTCINTF2. ALARMIF bit: Alarm interrupt

Bits 3–2 Reserved

RTC Interrupt Enable Register 1

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCINTE1	7	1DAYIE	0	H0	R/W	–
	6	1HURIE	0	H0	R/W	
	5	1MINIE	0	H0	R/W	
	4	1SECIE	0	H0	R/W	
	3	1_2SECIE	0	H0	R/W	
	2	1_4SECIE	0	H0	R/W	
	1	1_8SECIE	0	H0	R/W	
	0	1_32SECIE	0	H0	R/W	

Bit 7 1DAYIE
Bit 6 1HURIE
Bit 5 1MINIE
Bit 4 1SECIE
Bit 3 1_2SECIE
Bit 2 1_4SECIE
Bit 1 1_8SECIE
Bit 0 1_32SECIE

These bits enable real-time clock interrupts.
1 (R/W): Enable interrupts
0 (R/W): Disable interrupts

The following shows the correspondence between the bit and interrupt:
RTCINTE1.1DAYIE bit: 1-day interrupt
RTCINTE1.1HURIE bit: 1-hour interrupt
RTCINTE1.1MINIE bit: 1-minute interrupt
RTCINTE1.1SECIE bit: 1-second interrupt
RTCINTE1.1_2SECIE bit: 1/2-second interrupt
RTCINTE1.1_4SECIE bit: 1/4-second interrupt
RTCINTE1.1_8SECIE bit: 1/8-second interrupt
RTCINTE1.1_32SECIE bit: 1/32-second interrupt

RTC Interrupt Enable Register 2

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCINTE2	7	RTCTRMIE	0	H0	R/W	–
	6	SW1IE	0	H0	R/W	
	5	SW10IE	0	H0	R/W	
	4	SW100IE	0	H0	R/W	
	3–2	–	0x0	–	R	
	1	DCNTUFIE	0	H0	R/W	
	0	ALARMIE	0	H0	R/W	

Bit 7 RTCTRMIE
Bit 6 SW1IE
Bit 5 SW10IE
Bit 4 SW100IE
Bit 1 DCNTUFIE
Bit 0 ALARMIE

These bits enable real-time clock interrupts.
1 (R/W): Enable interrupts
0 (R/W): Disable interrupts

The following shows the correspondence between the bit and interrupt:
RTCINTE2.RTCTRMIE bit: Theoretical regulation completion interrupt
RTCINTE2.SW1IE bit: Stopwatch 1 Hz interrupt
RTCINTE2.SW10IE bit: Stopwatch 10 Hz interrupt
RTCINTE2.SW100IE bit: Stopwatch 100 Hz interrupt
RTCINTE2. DCNTUFIE bit: Down counter underflow interrupt
RTCINTE2.ALARMIE bit: Alarm interrupt

Bits 3–2 Reserved

RTC Down Counter Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCDCNTCTL	7–5	–	0x0	–	R	–
	4	PRESET	0	H0	R/W	
	3–1	–	0x0	–	R	
	0	RUN	0	H0	R/W	

Bits 7–5 Reserved

Bit 4 PRESET

This bit presets the reload data stored in the RTCDCNTRLDL and RTCDCNTRLDH registers to the down counter.
1 (W): Preset
0 (W): Ineffective
1 (R): Presetting in progress
0 (R): Presetting finished or normal operation

By writing 1 to this bit, the RTCDCNTRLDL and RTCDCNTRLDH register values are preset to the down counter. This bit retains 1 during presetting and is automatically cleared to 0 after presetting has finished.

Bits 3–1 Reserved

Bit 0 RUN

This bit starts/stops the down counter.
1 (W): Start down counter
0 (W): Stop down counter
1 (R): Down counter is running
0 (R): Down counter is idle

By writing 1 to this bit, the down counter starts operating. While the down counter is running, writing 0 to this bit stops count operations. When the down counter stops due to a counter underflow in one-shot mode, this bit is automatically cleared to 0.

RTC Down Counter Mode Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCDCNTMOD	7–1	–	0x00	–	R	–
	0	MODE	0	H0	R/W	

Bits 7–1 Reserved

Bit 0 MODE

This bit selects the down counter operation mode.
1 (R/W): One-shot mode
0 (R/W): Repeat mode

For detailed information on the operation mode, refer to “Down Counter Function.”

RTC Down Counter Lower Reload Data Register
RTC Down Counter Upper Reload Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCDCNTRLDL	7–0	RLD[7:0]	0xff	H0	R/W	–
RTCDCNTRLDH	7–0	RLD[15:8]	0xff	H0	R/W	–

Bits 7–0 RLD[15:8], RLD[7:0]

These bits are used to set the initial value to be preset to the down counter.
The value set to this register will be preset to the down counter when 1 is written to the RTCDCNTCTL.PRESET bit or when the down counter underflows.

Notes: • The RTCDCNTRLDL/H registers cannot be altered while the down counter is running (RTCDCNTCTL.RUN bit = 1), as an incorrect initial value may be preset to the down counter.

• When one-shot mode is set, the RTCDCNTRLDL/H.RLD[15:0] bits should be set to a value equal to or greater than 0x0001.

RTC Down Counter Lower Data Register
RTC Down Counter Upper Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCDCNTL	7–0	CNT[7:0]	0xff	H0	R	–
RTCDCNTH	7–0	CNT[15:8]	0xff	H0	R	–

Bits 7–0 CNT[15:8], CNT[7:0]

The current down counter value can be read out from these bits.

Power Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
PWRCTL	7–1	–	0x00	–	R	–
	0	MCUPD	0	H0	R/W	

Bits 7–1 Reserved

Bit 0 MCUPD

This bit controls the MCU core operating voltage supply.
1 (W): Start MCU core operating voltage off sequence
1 (R): MCU core operating voltage off sequence start waiting status
0 (R/W): Ineffective

P2 Port Input Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P2IN	7–2	–	0x00	–	R	–
	1–0	P2IN[1:0]	0x0	H0	R	

∗1: This register is effective when the GPIO function is selected.

Bits 7–2 Reserved

Bits 1–0 P2IN[1:0]

The GPIO port pin status can be read out from these bits.
1 (R): Port pin = High level
0 (R): Port pin = Low level

The port pin status can be read out when input is enabled (P2IEN.P2IEN*y* bit = 1). When input is disabled (P2IEN.P2IEN*y* bit = 0), these bits are always read as 0. When the port is used for a peripheral I/O function, the input value cannot be read out from these bits.

P2 Port Output Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P2OUT	7–2	–	0x00	–	R	–
	1–0	P2OUT[1:0]	0x0	H0	R/W	

*1: This register is effective when the GPIO function is selected.

Bits 7–2 Reserved

Bits 1–0 P2OUT[1:0]

These bits are used to set data to be output from the GPIO port pins.
1 (R/W): Output high level from the port pin
0 (R/W): Output low level from the port pin

When output is enabled (P2OEN.P2OEN*y* bit = 1), the port pin outputs the data set here. Although data can be written when output is disabled (P2OEN.P2OEN*y* bit = 0), it does not affect the pin status.
These bits do not affect the outputs when the port is used as a peripheral I/O function.

P2 Port Output Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P2OEN	7–2	–	0x00	–	R	–
	1–0	P2OEN[1:0]	0x0	H0	R/W	

*1: This register is effective when the GPIO function is selected.

Bits 7–2 Reserved

Bits 1–0 P2OEN[1:0]

These bits enable/disable the GPIO port output.
1 (R/W): Enable (Data is output from the port pin.)
0 (R/W): Disable (The port is placed into Hi-Z.)

These bits do not affect the output control when the port is used as a peripheral I/O function.

P2 Port Input Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P2IEN	7–2	–	0x00	–	R	–
	1–0	P2IEN[1:0]	0x0	H0	R/W	

*1: This register is effective when the GPIO function is selected.

Bits 7–2 Reserved

Bits 1–0 P2IEN[1:0]

These bits enable/disable the GPIO port input.
1 (R/W): Enable (The port pin status is input.)
0 (R/W): Disable (Input data is fixed at 0.)

When both data output and data input are enabled, the pin output status controlled by this IC can be read.
These bits do not affect the input control when the port is used as a peripheral I/O function.

P2 Port Pull-up/down Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P2REN	7–2	–	0x00	–	R	–
	1–0	P2REN[1:0]	0x0	H0	R/W	

*1: This register is effective when the GPIO function is selected.

Bits 7–2 Reserved

Bits 1–0 P2REN[1:0]

These bits enable/disable the port pull-up/down control.
1 (R/W): Enable (The built-in pull-up/down resistor is used.)
0 (R/W): Disable (No pull-up/down control is performed.)

Enabling this function pulls up or down the port when output is disabled (P2OEN.P2OEN*y* bit = 0). When output is enabled (P2OEN.P2OEN*y* bit = 1), the P2REN.P2REN*y* bit setting is ineffective regardless of how the P2IEN.P2IEN*y* bit is set and the port is not pulled up/down.
These bits do not affect the pull-up/down control when the port is used as a peripheral I/O function.

P2 Port Pull-up/down Select Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P2PDPU	7–2	–	0x00	–	R	–
	1–0	P2PDPU[1:0]	0x0	H0	R/W	

∗1: This register is effective when the GPIO function is selected.

Bits 7–2 Reserved

Bits 1–0 P2PDPU[1:0]

These bits select either the pull-up resistor or the pull-down resistor when using a resistor built into the port.
1 (R/W): Pull-up resistor
0 (R/W): Pull-down resistor

The selected pull-up/down resistor is enabled when the P2REN.P2REN*y* bit = 1.

P2 Port Interrupt Flag Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P2INTF	7–2	–	0x00	–	R	–
	1–0	P2IF[1:0]	0x0	H0	R/W	Cleared by writing 1.

∗1: This register is effective when the GPIO function is selected.

Bits 7–2 Reserved

Bits 1–0 P2IF[1:0]

These bits indicate the port input interrupt cause occurrence status.
1 (R): Cause of interrupt occurred
0 (R): No cause of interrupt occurred
1 (W): Clear flag
0 (W): Ineffective

P2 Port Interrupt Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P2INTE	7–2	–	0x00	–	R	–
	1–0	P2IE[1:0]	0x0	H0	R/W	

∗1: This register is effective when the GPIO function is selected.

Bits 7–2 Reserved

Bits 1–0 P2IE[1:0]

These bits enable port input interrupts.
1 (R/W): Enable interrupts
0 (R/W): Disable interrupts

Note: To prevent generating unnecessary interrupts, the corresponding interrupt flag should be cleared before enabling interrupts.

P2 Port Interrupt Edge Select Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P2IEDGE	7–2	–	0x00	–	R	–
	1–0	P2EDGE[1:0]	0x0	H0	R/W	

∗1: This register is effective when the GPIO function is selected.

Bits 7–2 Reserved

Bits 1–0 P2EDGE[1:0]

These bits select the input signal edge to generate a port input interrupt.

1 (R/W): An interrupt will occur at a falling edge.

0 (R/W): An interrupt will occur at a rising edge.

P2 Port Chattering Filter Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P2CHATEN	7–2	–	0x00	–	R	–
	1–0	P2CHATEN[1:0]	0x0	H0	R/W	

Bits 7–2 Reserved

Bits 7–0 P2CHATEN[1:0]

These bits enable/disable the chattering filter function.

1 (R/W): Enable (The chattering filter is used.)

0 (R/W): Disable (The chattering filter is bypassed.)

P2 Port Mode Select Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P2MODSEL	7–2	–	0x00	–	R	–
	7–0	P2SEL[1:0]	0x00	H0	R/W	

Bits 7–2 Reserved

Bits 1–0 P2SEL[1:0]

These bits select whether each port is used for the GPIO function or a peripheral I/O function.

1 (R/W): Use peripheral I/O function

0 (R/W): Use GPIO function

P2 Port Function Select Register 0

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P2FNCSEL0	7–4	–	0x0	–	R	–
	3–2	P21MUX[1:0]	0x0	H0	R/W	
	1–0	P20MUX[1:0]	0x0	H0	R/W	

Bits 7–4 Reserved

Bits 3–2 P21MUX[1:0]

Bits 1–0 P20MUX[1:0]

These bits select the peripheral I/O function to be assigned to each port pin.

This selection takes effect when the P2MODSEL.P2SEL*y* bit = 1.

Table 21.7.4 P2 Port Group Function Assignment

Port name	P2SEL*y* = 0	P2SEL*y* = 1							
	GPIO	P2*y*MUX = 0x0 (Function 0)		P2*y*MUX = 0x1 (Function 1)		P2*y*MUX = 0x2 (Function 2)		P2*y*MUX = 0x3 (Function 3)	
		Peripheral	Pin	Peripheral	Pin	Peripheral	Pin	Peripheral	Pin
P20	P20	RTCLP	RTC1S	–	–	–	–	–	–
P21	P21	RTCLP	FOUT32K	–	–	–	–	–	–

OSC1 Load Capacitance 1 Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
OSC1CL1	7–0	CLADJ[7:0]	0x80	H0	R/W	–

Bits 7–0 CLADJ[7:0]

These bits adjust the load capacitance 1 (C_{G1}, C_{D1}) built into the OSC1 oscillator circuit.

Table 21.7.4 Load Capacitance 1 Setting

OSC1CL1.CLADJ[7:0] bits	Capacitance
0x7f (127)	Max.
0x7e (126)	↑
...	
0x00 (1)	
0xff (-1)	
...	
0x81 (-127)	↓
0x80 (-128)	Min.

OSC1 Load Capacitance 2 Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
OSC1CL2	7–1	–	0x00	–	R	–
	0	CLCUT	1	H0	R/W	

Bits 7–1 Reserved

Bit 0 CLCUT

This bit disconnects the load capacitance 2 (C_{G2}, C_{D2}) built into the OSC1 oscillator circuit.

1 (R/W): Normal

0 (R/W): Disconnect

VOSC Regulator Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
VOSCCTL	7–1	–	0x00	–	R	–
	1	ION	0	H0	R/W	
	0	IUP	0	H0	R/W	

Bits 7–2 Reserved

Bit 1 ION

This bit controls the load current of the VOSC regulator.

1 (R/W): Normal

0 (R/W): Load current On

Bit 0 IUP

This bit controls the driving capability of the VOSC regulator.

1 (R/W): Improve driving capability

0 (R/W): Normal

VOSC Reference Current Adjustment Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
VOSCTRIM	7–6	–	0x0	–	R	–
	5–0	XFIB[5:0]	0x00	H0	R/W	

Bits 7–6 Reserved

Bits 5–0 XFIB[5:0]

These bits adjust the reference current amount of the VOSC regulator.

Set the value read from the CLGOSC1TRIM.XFIB[5:0] bits of the clock generator to these bits.

RTCLPCLK Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
F32KCTL	7–1	–	0x00	–	R	–
	0	OEN	1	H0	R/W	

Bits 7–1 Reserved

Bit 0 OEN

This bit controls the RTCLPCLK output to the MCU core and FOUT32K pin.

1 (R/W): Output enable

0 (R/W): Output disable

22 Electrical Characteristics

22.1 Absolute Maximum Ratings

(V_{SS} = 0 V)

Item	Symbol	Condition		Rated value	Unit
Power supply voltage	V_{DD}			-0.3 to 7.0	V
Flash programming voltage	V_{PP}			-0.3 to 8.0	V
EPD power supply voltage	V_{EPD}			23	V
	V_{E2}			3.8	V
Input voltage	V_I	P10–13, P15, P20-21, PD1–D2		-0.3 to 7.0	V
		P00–07, P14, PD0, #RESET		-0.3 to V_{DD} + 0.5	V
Output voltage	V_O	P00–07, P10–15, P20-21, PD0–D2		-0.3 to V_{DD} + 0.5	V
High level output current	I_{OH}	1 pin	P00–07, P10–15, P20-21, PD0–D2	-10	mA
		Total of all pins		-20	mA
Low level output current	I_{OL}	1 pin	P00–07, P10–15, P20-21, PD0–D2	10	mA
		Total of all pins		20	mA
Operating temperature	Ta			-40 to 85	°C
Storage temperature	Tstg			-65 to 125	°C

22.2 Recommended Operating Conditions

(V_{SS} = 0 V) ∗1

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	For normal operation		1.8	–	5.5	V
		For Flash programming	When V_{PP} is supplied externally	2.2	–	5.5	V
			When V_{PP} is generated internally	2.2	–	5.5	V
		For EEPROM programming	When V_{PP} is generated internally	2.2	–	5.5	V
Flash programming voltage	V_{PP}			7.3	7.5	7.7	V
OSC1 oscillator oscillation frequency	f_{OSC1}			–	32.768	–	kHz
EXOSC external clock frequency	f_{EXOSC}	When supplied from an external oscillator		0.016	–	16.8	MHz
Bypass capacitor between V_{SS} and V_{DD}	C_{PW1}			–	3.3	–	µF
Capacitor between V_{SS} and V_{D2}	C_{PW2}			–	0.1	–	µF
Capacitor between V_{SS} and V_{D1}	C_{PW3}			–	1	–	µF
Capacitor between V_{SS} and V_{OSC}	C_{VOSC}	V_{DD} = 3.6 to 5.5 V		–	1	–	µF
		V_{DD} = 1.8 to 3.6 V		–	0.1	–	µF
Capacitor between V_{SS} and V_{E1}	C_{EPD1}	∗2		–	0.1	–	µF
Capacitor between V_{SS} and V_{E2}	C_{EPD2}	∗2		–	0.1	–	µF
Capacitor between V_{SS} and V_{E3}	C_{EPD3}	∗2		–	0.1	–	µF
Capacitor between V_{SS} and V_{E4}	C_{EPD4}	∗2		–	0.1	–	µF
Capacitor between V_{SS} and V_{E5}	C_{EPD5}	∗2		–	0.1	–	µF
Capacitor between C_{D1} and C_{D2}	C_{EPD6}	∗2		–	0.1	–	µF
Capacitor between C_{B1} and C_{B2}	C_{EPD7}	∗2		–	0.1	–	µF
Capacitor between C_{B3} and C_{B4}	C_{EPD8}	∗2		–	0.1	–	µF
Gate capacitor for OSC1 oscillator	C_{G1}	∗3		–	0	–	pF
Drain capacitor for OSC1 oscillator	C_{D1}	∗3		–	0	–	pF
DSIO pull-up resistor	R_{DBG}	∗4		–	10	–	kΩ
Capacitor between V_{SS} and V_{PP}	C_{VPP}			–	0.1	–	µF
Capacitor between V_{SS} and V_{REFA}	C_{VREFA}	∗5		–	0.1	–	µF

∗1 The potential variation of the V_{SS} voltage should be suppressed to within ±0.3 V on the basis of the ground potential of the MCU mounting board while the Flash is being programmed, as it affects the Flash memory characteristics (programming count).

∗2 The capacitors are not required when EPD controller/driver is not used. In this case, leave the V_{E1} to V_{E5}, C_{D1} to C_{D2}, and C_{B1} to C_{B4} pins open.

∗3 The component values should be determined after performing matching evaluation of the resonator mounted on the printed circuit board actually used.

∗4 R_{DBG} is not required when using the DSIO pin as a general-purpose I/O port.

∗5 Normally, C_{VREFA} is not required, as V_{REFA} is supplied externally.

∗6 The component values should be determined after evaluating operations using an actual mounting board.

22.3 Current Consumption

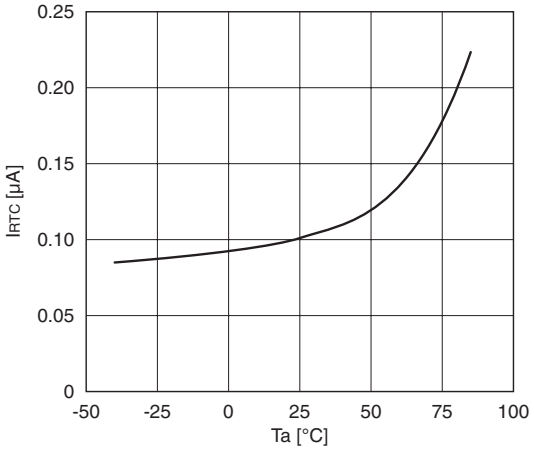
Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = 25°C, EXOSC = OFF, OSC1 = 32.768 kHz*1, MCU = ON, PWGCTL.PWGMOD[1:0] bits = 0x0 (automatic mode), FLASHCWAIT.RDWAIT[1:0] bits = 0x1 (2 cycles)

Item	Symbol	Condition	Ta	Min.	Typ.	Max.	Unit
Current consumption in RTC mode	I_{RTC}	MCU = OFF	25°C	–	0.11	0.18	µA
			50°C	–	0.13	0.30	µA
			85°C	–	0.23	0.65	µA
Current consumption in SLEEP mode	I_{SLP}	IOSC = OFF, OSC3 = OFF	25°C	–	0.45	2	µA
			85°C	–	1.1	10	µA
Current consumption in HALT mode	I_{HALT1}	IOSC = ON, OSC3 = OFF		–	42	60	µA
	I_{HALT2}	IOSC = OFF, OSC3 = OFF		–	0.7	3.5	µA
	I_{HALT3}	IOSC = OFF, OSC3 = 1 MHz*2		–	180	270	µA
		IOSC = OFF, OSC3 = 16 MHz*3		–	360	550	µA
Current consumption in RUN mode	I_{RUN1}*4	IOSC = ON, OSC3 = OFF, SYSCLK = IOSC		–	125	200	µA
		IOSC = ON, OSC3 = OFF, SYSCLK = IOSC FLASHCWAIT.RDWAIT[1:0] bits = 0x0 (1 cycle)		–	150	300	µA
	I_{RUN2}*4	IOSC = OFF, OSC3 = OFF, SYSCLK = OSC1		–	5	9	µA
	I_{RUN3}*4	IOSC = OFF, OSC3 = 1 MHz*2, SYSCLK = OSC3		–	305	450	µA
		IOSC = OFF, OSC3 = 16 MHz*3, SYSCLK = OSC3 FLASHCWAIT.RDWAIT[1:0] bits = 0x2 (3 cycles)		–	1,950	3,000	µA

*1 OSC1 oscillator: Crystal resonator = FC-12D (manufactured by Seiko Epson Corporation, R_1 = 75 kΩ (Max.), C_L = 7 pF), C_{G1} = C_{D1} = 0 pF
*2 OSC3 oscillator: CLGOSC3.OSC3FQ[2:0] bits = 0x1
*3 OSC3 oscillator: CLGOSC3.OSC3FQ[2:0] bits = 0x6
*4 The current consumption values were measured when a test program consisting of 60.5% ALU instructions, 17% branch instructions, 12% RAM read instructions, and 10.5% RAM write instructions was executed continuously in the Flash memory.

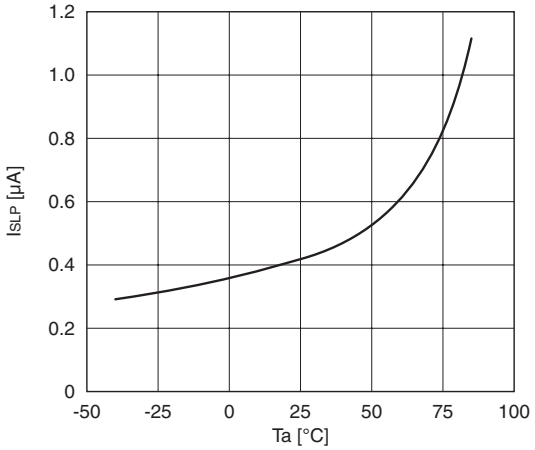
Current consumption-temperature characteristic in RTC mode

MCU = OFF, OSC1 = 32.768 kHz, V_{DD} = 5.5 V, Typ. value



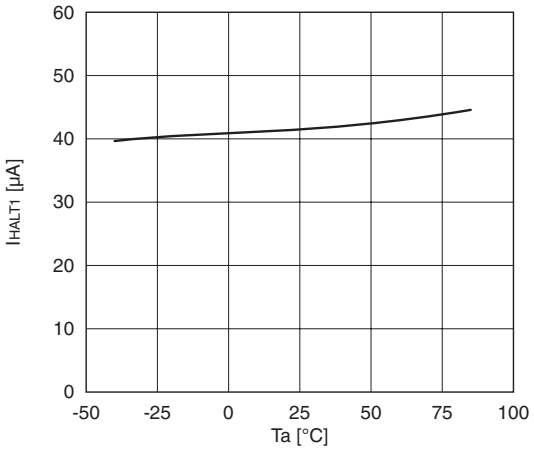
Current consumption-temperature characteristic in SLEEP mode

IOSC = ON, OSC1 = 32.768 kHz, OSC3 = OFF, V_{DD} = 5.5 V, Typ. value



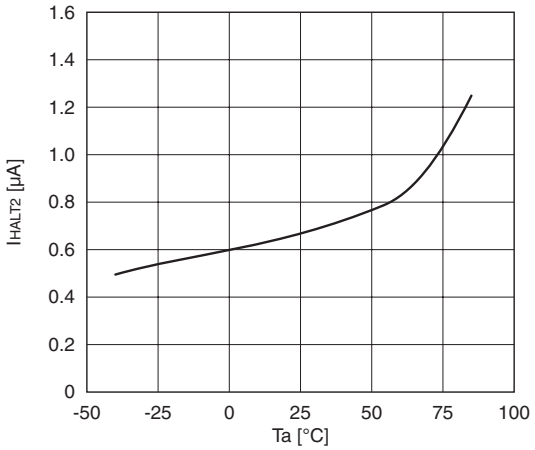
Current consumption-temperature characteristic in HALT mode (IOSC operation)

IOSC = ON, OSC1 = 32.768 kHz, OSC3 = OFF, Typ. value



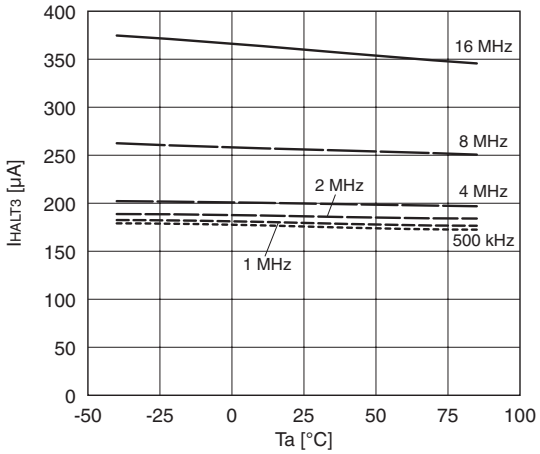
Current consumption-temperature characteristic in HALT mode (OSC1 operation)

IOSC = OFF, OSC1 = 32.768 kHz, OSC3 = OFF, Typ. value



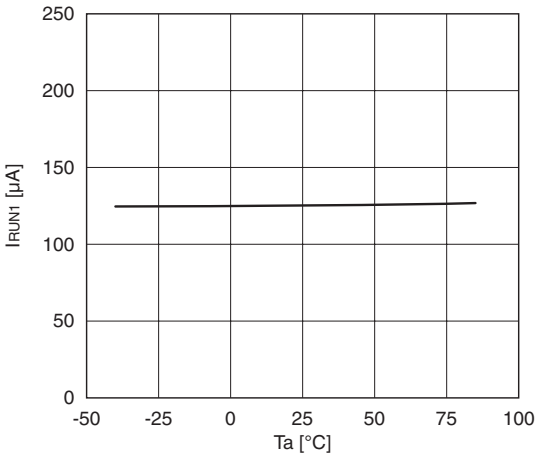
Current consumption-temperature characteristic in HALT mode (OSC3 operation)

IOSC = OFF, OSC1 = 32.768 kHz, OSC3 = ON, Typ. value



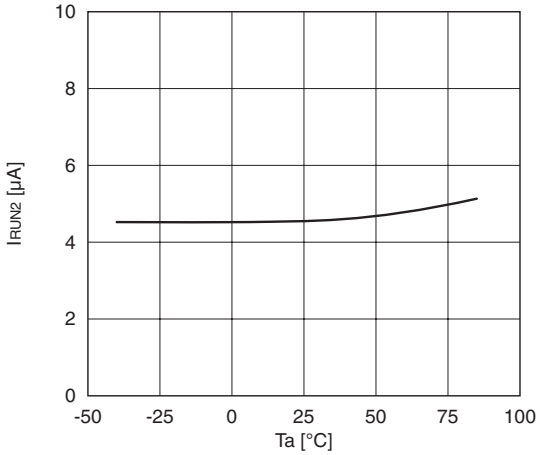
Current consumption-temperature characteristic in RUN mode (IOSC operation)

IOSC = ON, OSC1 = 32.768 kHz, OSC3 = OFF, Typ. value



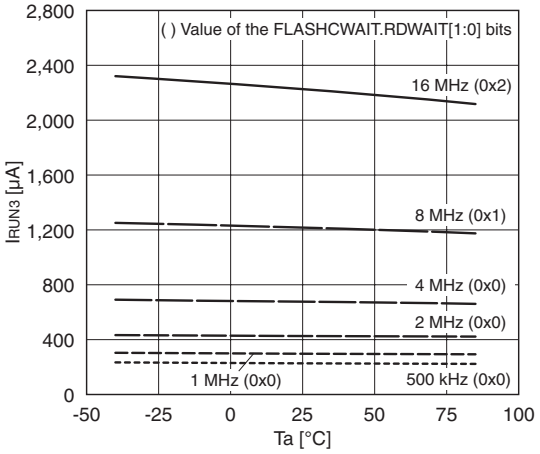
Current consumption-temperature characteristic in RUN mode (OSC1 operation)

IOSC = OFF, OSC1 = 32.768 kHz, OSC3 = OFF, Typ. value



Current consumption-temperature characteristic in RUN mode (OSC3 operation)

IOSC = OFF, OSC1 = 32.768 kHz, OSC3 = ON, Typ. value

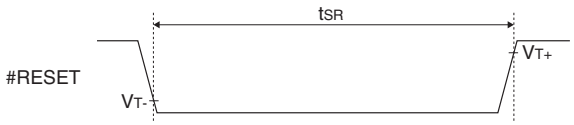


22.4 System Reset Controller (SRC) Characteristics

#RESET pin characteristics

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C

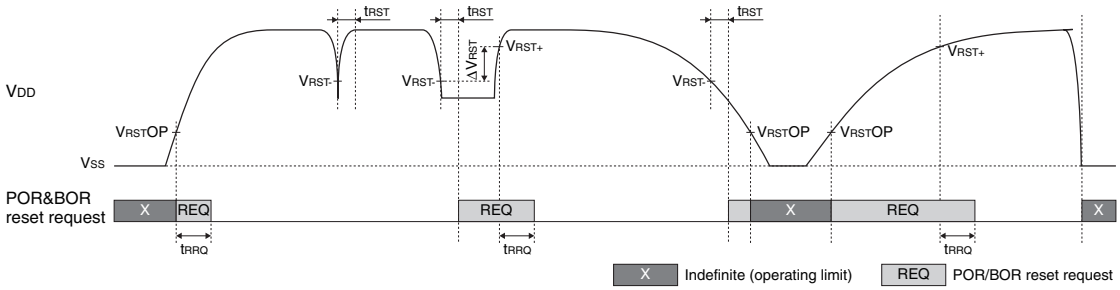
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
High level Schmitt input threshold voltage	V_{T+}		0.5 × V_{DD}	–	0.8 × V_{DD}	V
Low level Schmitt input threshold voltage	V_{T-}		0.2 × V_{DD}	–	0.5 × V_{DD}	V
Schmitt input hysteresis voltage	ΔV_T		180	–	–	mV
Input pull-up resistance	R_{IN}		100	230	500	kΩ
Pin capacitance	C_{IN}		–	–	15	pF
Reset Low pulse width	t_{SR}		40	–	–	µs



POR/BOR characteristics

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
POR/BOR canceling voltage	V_{RST+}		1.41	–	1.75	V
POR/BOR detection voltage	V_{RST-}		1.25	–	1.55	V
POR/BOR hysteresis voltage	ΔV_{RST}		40	60	–	mV
POR/BOR detection response time	t_{RST}		–	–	40	µs
POR/BOR operating limit voltage	V_{RSTOP}		–	0.5	0.95	V
POR/BOR reset request hold time	t_{RRQ}		0.01	–	4	ms



Note: When performing a power-on-reset again after the power is turned off, decrease the V_{DD} voltage to V_{RSTOP} or less.

Reset hold circuit characteristics

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset hold time*1	t_{RSTR}		0.5	–	16	ms

*1 Time until the internal reset signal is negated after the reset request is canceled.

22.5 Clock Generator (CLG) Characteristics

Oscillator circuit characteristics including resonators change depending on conditions (board pattern, components used, etc.). Use these characteristic values as a reference and perform matching evaluation using the actual printed circuit board.

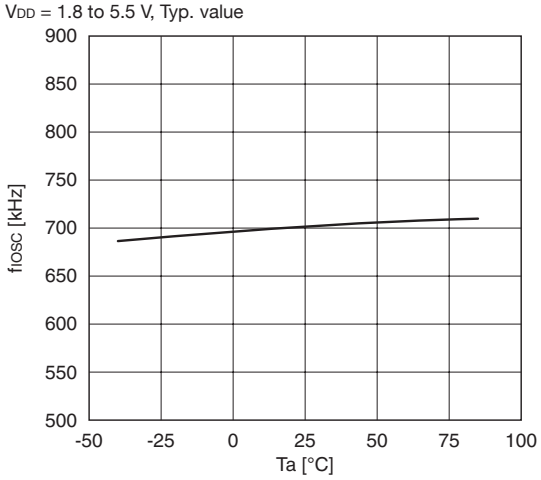
IOSC oscillator circuit characteristics

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C

Item	Symbol	Condition	Ta	Min.	Typ.	Max.	Unit
Oscillation start time	t_{stal}			–	–	3	µs
Oscillation frequency	f_{IOSC}		25°C	679	700	721	kHz
			-40 to 85°C	651	700	749	kHz

IOSC oscillation frequency-temperature characteristic

V_{DD} = 1.8 to 5.5 V, Typ. value



OSC1 oscillator circuit characteristics

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	t_{sta1}		–	–	4	s
Oscillation frequency	f_{OSC1}		–	32,768	–	Hz
Frequency-voltage characteristic	fv		-1	-0.2	1	ppm/V
Frequency-temperature characteristic	f_{TH}	Ta = -40 to 85°C, 25°C reference	-140	–	10	ppm

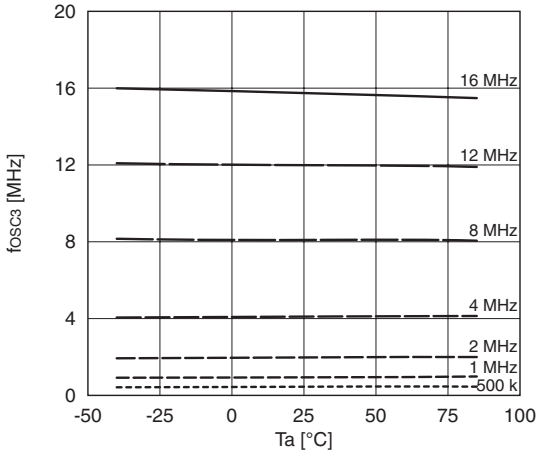
OSC3 oscillator circuit characteristics

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = 25°C

Item	Symbol	Condition	Ta	Min.	Typ.	Max.	Unit
Oscillation start time	t_{sta3}			–	–	3	µs
Oscillation frequency	f_{OSC3}	CLGOSC3.OSC3FQ[2:0] bits = 0x6	25°C	15.2	16.0	16.8	MHz
			-40 to 85°C	14.9	16.0	17.1	MHz
		CLGOSC3.OSC3FQ[2:0] bits = 0x5	25°C	11.4	12.0	12.6	MHz
			-40 to 85°C	11.2	12.0	12.8	MHz
		CLGOSC3.OSC3FQ[2:0] bits = 0x4	25°C	7.8	8.0	8.2	MHz
			-40 to 85°C	7.6	8.0	8.4	MHz
		CLGOSC3.OSC3FQ[2:0] bits = 0x3	25°C	3.8	4.0	4.2	MHz
			-40 to 85°C	3.7	4.0	4.3	MHz
		CLGOSC3.OSC3FQ[2:0] bits = 0x2	25°C	1.90	2.00	2.10	MHz
			-40 to 85°C	1.86	2.00	2.14	MHz
		CLGOSC3.OSC3FQ[2:0] bits = 0x1	25°C	0.95	1.00	1.05	MHz
			-40 to 85°C	0.93	1.00	1.07	MHz
		CLGOSC3.OSC3FQ[2:0] bits = 0x0	25°C	0.48	0.50	0.53	MHz
			-40 to 85°C	0.47	0.50	0.54	MHz

OSC3 internal oscillation frequency-temperature characteristic

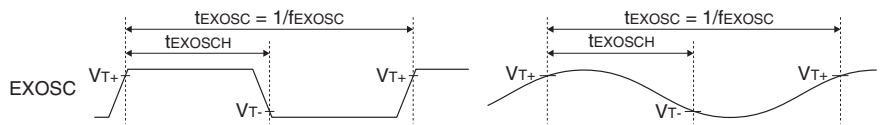
Typ. value



EXOSC external clock input characteristics

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
EXOSC external clock duty ratio	t_{EXOSCD}	$t_{EXOSCD} = t_{EXOSCH}/t_{EXOSC}$	46	–	54	%
High level Schmitt input threshold voltage	V_{T+}		0.5 × V_{DD}	–	0.8 × V_{DD}	V
Low level Schmitt input threshold voltage	V_{T-}		0.2 × V_{DD}	–	0.5 × V_{DD}	V
Schmitt input hysteresis voltage	ΔV_T		180	–	–	mV



22.6 Flash Memory Characteristics

Unless otherwise specified: V_{DD} = 2.2 to 5.5 V, V_{SS} = 0 V *1, Ta = -40 to 85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Programming count *2	C_{FEP}	Programmed data is guaranteed to be retained for 10 years.	1,000	–	–	times

*1 The potential variation of the V_{SS} voltage should be suppressed to within ±0.3 V on the basis of the ground potential of the MCU mounting board while the Flash is being programmed, as it affects the Flash memory characteristics (programming count).

*2 Assumed that Erasing + Programming as count of 1. The count includes programming in the factory for shipment with ROM data programmed.

22.7 EEPROM Characteristics

Unless otherwise specified: V_{DD} = 2.2 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C

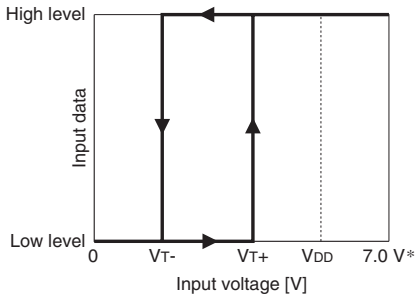
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Programming count	C_{EEP}	Programmed data is guaranteed to be retained for 10 years.	100,000	–	–	times
Programming time	t_{PRG}		–	0.2	15	ms
Programming power supply start-up time	t_{CPST}		*1			ms
Effective EEPROM reset pulse width	t_{XPOR}		500			ns

*1 Determine the value referencing the equation below.
$t_{CPST} = 37{,}500 \times C_{VPP} + 15$
t_{CPST}: Programming power supply start-up time [µs]、C_{VPP}: External smoothing capacitance [µF]

22.8 Input/Output Port (PPORT) Characteristics

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C

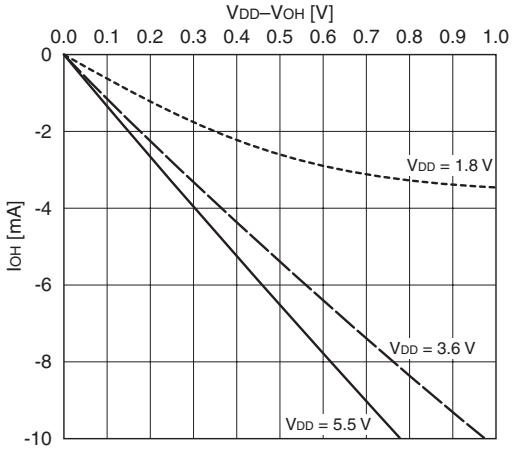
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
High level Schmitt input threshold voltage	V_{T+}	P00–07, P10–15, P20–21, PD0–D2	0.5 × V_{DD}	–	0.8 × V_{DD}	V
Low level Schmitt input threshold voltage	V_{T-}	P00–07, P10–15, P20–21, PD0–D2	0.2 × V_{DD}	–	0.5 × V_{DD}	V
Schmitt input hysteresis voltage	ΔV_T	P00–07, P10–15, P20–21, PD0–D2	180	–	–	mV
High level output current	I_{OH}	P00–07, P10–15, P20–21, PD0–D2, V_{OH} = 0.9 × V_{DD}	–	–	-0.5	mA
Low level output current	I_{OL}	P00–07, P10–15, P20–21, PD0–D2, V_{OL} = 0.1 × V_{DD}	0.5	–	–	mA
Leakage current	I_{LEAK}	P00–07, P10–15, P20–21, PD0–D2	-150	–	150	nA
Input pull-up resistance	R_{INU}	P00–07, P10–15, P20–21, PD0–D2	100	200	500	kΩ
Input pull-down resistance	R_{IND}	P00–07, P10–15, P20–21, PD0–D2	100	200	500	kΩ
Pin capacitance	C_{IN}	P00–07, P10–15, P20–21, PD0–D2	–	–	15	pF



(* For over voltage tolerant fail-safe type port)

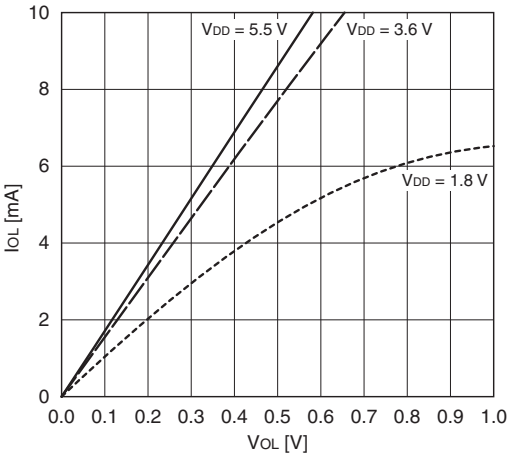
High-level output current characteristic

Ta = 85°C, Max. value



Low-level output current characteristic

Ta = 85°C, Min. value



22.9 Supply Voltage Detector (SVD3) Characteristics

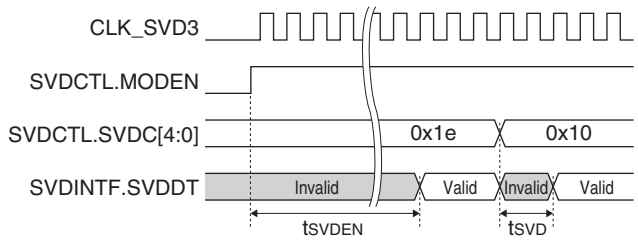
Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
EXSVD pin input voltage range	V_{EXSVD}		0	–	5.5	V
EXSVD input impedance	R_{EXSVD}	SVDCTL.SVDC[4:0] bits = 0x00	253	279	305	kΩ
		SVDCTL.SVDC[4:0] bits = 0x01	274	302	330	kΩ
		SVDCTL.SVDC[4:0] bits = 0x02	317	348	380	kΩ
		SVDCTL.SVDC[4:0] bits = 0x03	338	371	405	kΩ
		SVDCTL.SVDC[4:0] bits = 0x04	380	418	456	kΩ
		SVDCTL.SVDC[4:0] bits = 0x05	421	464	507	kΩ
		SVDCTL.SVDC[4:0] bits = 0x06	443	487	531	kΩ
		SVDCTL.SVDC[4:0] bits = 0x07	464	511	557	kΩ
		SVDCTL.SVDC[4:0] bits = 0x08	486	534	581	kΩ
		SVDCTL.SVDC[4:0] bits = 0x09	507	557	607	kΩ
		SVDCTL.SVDC[4:0] bits = 0x0a	528	580	631	kΩ
		SVDCTL.SVDC[4:0] bits = 0x0b	551	603	655	kΩ
		SVDCTL.SVDC[4:0] bits = 0x0c	571	626	682	kΩ
		SVDCTL.SVDC[4:0] bits = 0x0d	593	649	705	kΩ
		SVDCTL.SVDC[4:0] bits = 0x0e	616	672	727	kΩ
		SVDCTL.SVDC[4:0] bits = 0x0f	635	695	754	kΩ
		SVDCTL.SVDC[4:0] bits = 0x10	658	718	777	kΩ
		SVDCTL.SVDC[4:0] bits = 0x11	679	741	804	kΩ
		SVDCTL.SVDC[4:0] bits = 0x12	698	765	833	kΩ
		SVDCTL.SVDC[4:0] bits = 0x13	739	812	885	kΩ
		SVDCTL.SVDC[4:0] bits = 0x14	761	834	908	kΩ
		SVDCTL.SVDC[4:0] bits = 0x15	804	880	955	kΩ
		SVDCTL.SVDC[4:0] bits = 0x16	842	929	1,016	kΩ
		SVDCTL.SVDC[4:0] bits = 0x17	878	948	1,019	kΩ
		SVDCTL.SVDC[4:0] bits = 0x18	893	972	1,052	kΩ
		SVDCTL.SVDC[4:0] bits = 0x19	922	993	1,064	kΩ
		SVDCTL.SVDC[4:0] bits = 0x1a	963	1,041	1,119	kΩ
		SVDCTL.SVDC[4:0] bits = 0x1b	982	1,063	1,145	kΩ
		SVDCTL.SVDC[4:0] bits = 0x1c	1,001	1,086	1,171	kΩ
		SVDCTL.SVDC[4:0] bits = 0x1d	1,022	1,110	1,198	kΩ
		SVDCTL.SVDC[4:0] bits = 0x1e	1,054	1,129	1,204	kΩ
		SVDCTL.SVDC[4:0] bits = 0x1f	1,072	1,154	1,237	kΩ

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
EXSVD detection voltage	V_{SVD_EXT}	SVDCTL.SVDC[4:0] bits = 0x0	1.17	1.2	1.23	V
		SVDCTL.SVDC[4:0] bits = 0x1	1.27	1.3	1.33	V
		SVDCTL.SVDC[4:0] bits = 0x2	1.46	1.5	1.54	V
		SVDCTL.SVDC[4:0] bits = 0x3	1.56	1.6	1.64	V
		SVDCTL.SVDC[4:0] bits = 0x04	1.76	1.8	1.85	V
		SVDCTL.SVDC[4:0] bits = 0x05	1.95	2.0	2.05	V
		SVDCTL.SVDC[4:0] bits = 0x06	2.05	2.1	2.15	V
		SVDCTL.SVDC[4:0] bits = 0x07	2.15	2.2	2.26	V
		SVDCTL.SVDC[4:0] bits = 0x08	2.24	2.3	2.36	V
		SVDCTL.SVDC[4:0] bits = 0x09	2.34	2.4	2.46	V
		SVDCTL.SVDC[4:0] bits = 0x0a	2.44	2.5	2.56	V
		SVDCTL.SVDC[4:0] bits = 0x0b	2.54	2.6	2.67	V
		SVDCTL.SVDC[4:0] bits = 0x0c	2.63	2.7	2.77	V
		SVDCTL.SVDC[4:0] bits = 0x0d	2.73	2.8	2.87	V
		SVDCTL.SVDC[4:0] bits = 0x0e	2.83	2.9	2.97	V
		SVDCTL.SVDC[4:0] bits = 0x0f	2.93	3.0	3.08	V
		SVDCTL.SVDC[4:0] bits = 0x10	3.02	3.1	3.18	V
		SVDCTL.SVDC[4:0] bits = 0x11	3.12	3.2	3.28	V
		SVDCTL.SVDC[4:0] bits = 0x12	3.22	3.3	3.38	V
		SVDCTL.SVDC[4:0] bits = 0x13	3.41	3.5	3.59	V
		SVDCTL.SVDC[4:0] bits = 0x14	3.51	3.6	3.69	V
		SVDCTL.SVDC[4:0] bits = 0x15	3.71	3.8	3.90	V
		SVDCTL.SVDC[4:0] bits = 0x16	3.90	4.0	4.10	V
		SVDCTL.SVDC[4:0] bits = 0x17	4.00	4.1	4.20	V
		SVDCTL.SVDC[4:0] bits = 0x18	4.10	4.2	4.31	V
		SVDCTL.SVDC[4:0] bits = 0x19	4.19	4.3	4.41	V
		SVDCTL.SVDC[4:0] bits = 0x1a	4.39	4.5	4.61	V
		SVDCTL.SVDC[4:0] bits = 0x1b	4.49	4.6	4.72	V
		SVDCTL.SVDC[4:0] bits = 0x1c	4.58	4.7	4.82	V
		SVDCTL.SVDC[4:0] bits = 0x1d	4.68	4.8	4.92	V
		SVDCTL.SVDC[4:0] bits = 0x1e	4.78	4.9	5.02	V
		SVDCTL.SVDC[4:0] bits = 0x1f	4.88	5.0	5.13	V
SVD detection voltage	V_{SVD}	SVDCTL.SVDC[4:0] bits = 0x04	1.76	1.8	1.85	V
		SVDCTL.SVDC[4:0] bits = 0x05	1.95	2.0	2.05	V
		SVDCTL.SVDC[4:0] bits = 0x06	2.05	2.1	2.15	V
		SVDCTL.SVDC[4:0] bits = 0x07	2.15	2.2	2.26	V
		SVDCTL.SVDC[4:0] bits = 0x08	2.24	2.3	2.36	V
		SVDCTL.SVDC[4:0] bits = 0x09	2.34	2.4	2.46	V
		SVDCTL.SVDC[4:0] bits = 0x0a	2.44	2.5	2.56	V
		SVDCTL.SVDC[4:0] bits = 0x0b	2.54	2.6	2.67	V
		SVDCTL.SVDC[4:0] bits = 0x0c	2.63	2.7	2.77	V
		SVDCTL.SVDC[4:0] bits = 0x0d	2.73	2.8	2.87	V
		SVDCTL.SVDC[4:0] bits = 0x0e	2.83	2.9	2.97	V
		SVDCTL.SVDC[4:0] bits = 0x0f	2.93	3.0	3.08	V
		SVDCTL.SVDC[4:0] bits = 0x10	3.02	3.1	3.18	V
		SVDCTL.SVDC[4:0] bits = 0x11	3.12	3.2	3.28	V
		SVDCTL.SVDC[4:0] bits = 0x12	3.22	3.3	3.38	V
		SVDCTL.SVDC[4:0] bits = 0x13	3.41	3.5	3.59	V
		SVDCTL.SVDC[4:0] bits = 0x14	3.51	3.6	3.69	V
		SVDCTL.SVDC[4:0] bits = 0x15	3.71	3.8	3.90	V
		SVDCTL.SVDC[4:0] bits = 0x16	3.90	4.0	4.10	V
		SVDCTL.SVDC[4:0] bits = 0x17	4.00	4.1	4.20	V
		SVDCTL.SVDC[4:0] bits = 0x18	4.10	4.2	4.31	V
		SVDCTL.SVDC[4:0] bits = 0x19	4.19	4.3	4.41	V
		SVDCTL.SVDC[4:0] bits = 0x1a	4.39	4.5	4.61	V
		SVDCTL.SVDC[4:0] bits = 0x1b	4.49	4.6	4.72	V
		SVDCTL.SVDC[4:0] bits = 0x1c	4.58	4.7	4.82	V
		SVDCTL.SVDC[4:0] bits = 0x1d	4.68	4.8	4.92	V
		SVDCTL.SVDC[4:0] bits = 0x1e	4.78	4.9	5.02	V
		SVDCTL.SVDC[4:0] bits = 0x1f	4.88	5.0	5.13	V
SVD circuit enable response time	t_{SVDEN}	*1	–	–	500	µs
SVD circuit response time	t_{SVD}		–	–	60	µs

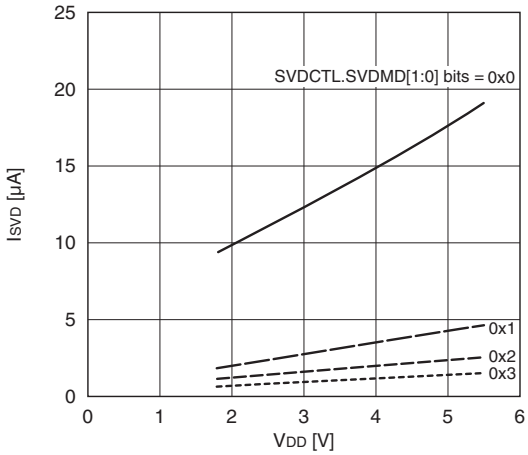
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SVD circuit current	I_{SVD}	SVDCTL.SVDMD[1:0] bits = 0x0, SVDCTL.SVDC[4:0] bits = 0x04, CLK_SVD3 = 32 kHz, Ta = 25°C	–	19	35	µA
		SVDCTL.SVDMD[1:0] bits = 0x1, SVDCTL.SVDC[4:0] bits = 0x04, CLK_SVD3 = 32 kHz, Ta = 25°C	–	4.7	7.7	µA
		SVDCTL.SVDMD[1:0] bits = 0x2, SVDCTL.SVDC[4:0] bits = 0x04, CLK_SVD3 = 32 kHz, Ta = 25°C	–	2.5	4.1	µA
		SVDCTL.SVDMD[1:0] bits = 0x3, SVDCTL.SVDC[4:0] bits = 0x04, CLK_SVD3 = 32 kHz, Ta = 25°C	–	1.5	2.4	µA

*1 If CLK_SVD3 is configured in the neighborhood of 32 kHz, the SVDINTF.SVDDT bit is masked during the t_{SVDEN} period and it retains the previous value.



SVD circuit current - power supply voltage characteristic

Ta = 25°C, SVDCTL.SVDC[4:0] bits = 0x04, CLK_SVD3 = 32 kHz, Typ. value



22.10 UART (UART3) Characteristics

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Transfer baud rate	U_{BRT1}	Normal mode	150	–	921,600	bps
	U_{BRT2}	IrDA mode	150	–	115,200	bps

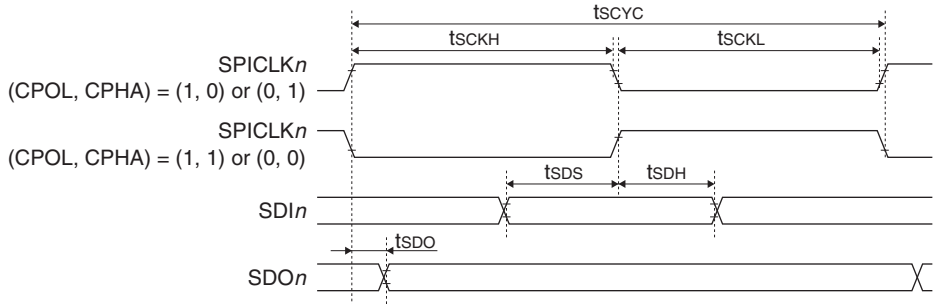
22.11 Synchronous Serial Interface (SPIA) Characteristics

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C

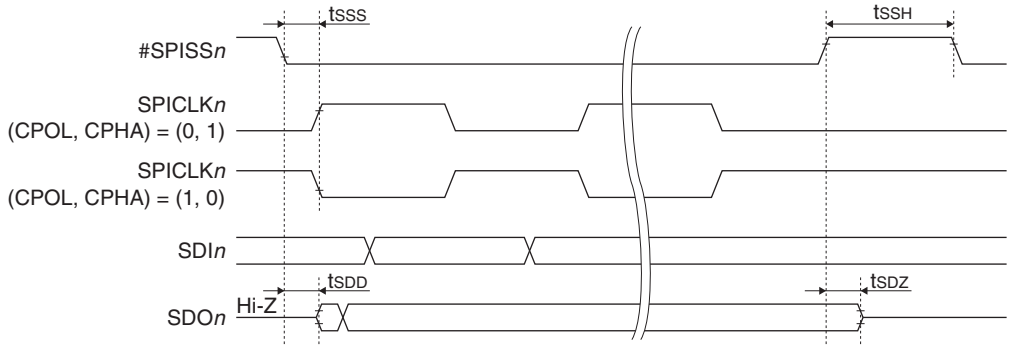
Item	Symbol	Condition	V_{DD}	Min.	Typ.	Max.	Unit
SPICLK*n* cycle time	t_{SCYC}		4.5 to 5.5 V	250	–	–	ns
			1.8 to 4.5 V	500	–	–	ns
SPICLK*n* High pulse width	t_{SCKH}		4.5 to 5.5 V	100	–	–	ns
			1.8 to 4.5 V	200	–	–	ns
SPICLK*n* Low pulse width	t_{SCKL}		4.5 to 5.5 V	100	–	–	ns
			1.8 to 4.5 V	200	–	–	ns
SDI*n* setup time	t_{SDS}		4.5 to 5.5 V	50	–	–	ns
			1.8 to 4.5 V	80	–	–	ns
SDI*n* hold time	t_{SDH}		4.5 to 5.5 V	20	–	–	ns
			1.8 to 4.5 V	30	–	–	ns
SDO*n* output delay time	t_{SDO}	C_L = 30 pF *1	4.5 to 5.5 V	–	–	60	ns
			1.8 to 4.5 V	–	–	90	ns
#SPISS*n* setup time	t_{SSS}			80	–	–	ns
#SPISS*n* High pulse width	t_{SSH}			100	–	–	ns
SDO*n* output start time	t_{SDD}	C_L = 30 pF *1		–	–	90	ns
SDO*n* output stop time	t_{SDZ}	C_L = 30 pF *1		–	–	80	ns

*1 C_L = Pin load

Master and slave modes



Slave mode

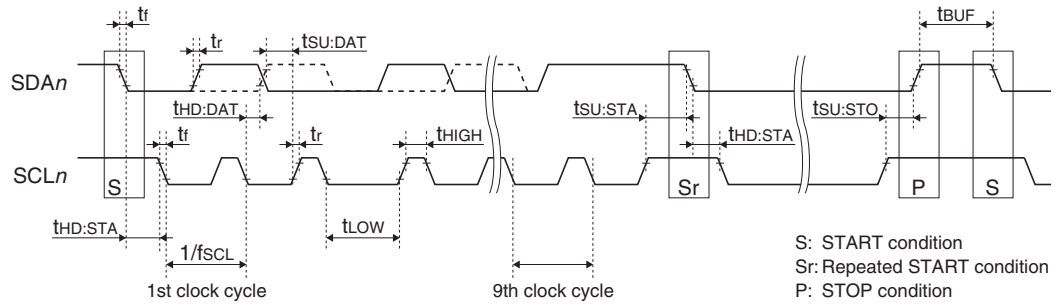


22.12 I²C (I2C) Characteristics

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C

Item	Symbol	Condition	Standard mode			Fast mode			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL*n* frequency	f_{SCL}		0	–	100	0	–	400	kHz
Hold time (repeated) START condition *	$t_{HD:STA}$		4.0	–	–	0.6	–	–	µs
SCL*n* Low pulse width	t_{LOW}		4.7	–	–	1.3	–	–	µs
SCL*n* High pulse width	t_{HIGH}		4.0	–	–	0.6	–	–	µs
Repeated START condition setup time	$t_{SU:STA}$		4.7	–	–	0.6	–	–	µs
Data hold time	$t_{HD:DAT}$		0	–	–	0	–	–	µs
Data setup time	$t_{SU:DAT}$		250	–	–	100	–	–	ns
SDA*n*, SCL*n* rise time	t_r		–	–	1,000	–	–	300	ns
SDA*n*, SCL*n* fall time	t_f		–	–	300	–	–	300	ns
STOP condition setup time	$t_{SU:STO}$		4.0	–	–	0.6	–	–	µs
Bus free time	t_{BUF}		4.7	–	–	1.3	–	–	µs

* After this period, the first clock pulse is generated.



22.13 EPD Driver Characteristics

The typical values in the following EPD driver characteristics varies depending on the panel load (panel size, drive waveform, number of display pixels and display contents), so evaluate them by connecting to the actually used EPD panel.

V_E regulator output voltage

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = 25°C, C_{EPD1} to C_{EPD8} = 0.1 µF, No panel load

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
V_E regulator output voltage (V_{E1} reference, EPDPWR0.VESEL bit = 0)	V_{E1}	EPDPWR0.VECONT[3:0] bits = 0x0	Typ. - 0.075	1.005	Typ. + 0.075	V
		EPDPWR0.VECONT[3:0] bits = 0x1		1.055		V
		EPDPWR0.VECONT[3:0] bits = 0x2		1.106		V
		EPDPWR0.VECONT[3:0] bits = 0x3		1.156		V
		EPDPWR0.VECONT[3:0] bits = 0x4		1.206		V
		EPDPWR0.VECONT[3:0] bits = 0x5		1.256		V
		EPDPWR0.VECONT[3:0] bits = 0x6		1.307		V
		EPDPWR0.VECONT[3:0] bits = 0x7		1.357		V
		EPDPWR0.VECONT[3:0] bits = 0x8		1.407		V
		EPDPWR0.VECONT[3:0] bits = 0x9		1.457		V
		EPDPWR0.VECONT[3:0] bits = 0xa		1.508		V
		EPDPWR0.VECONT[3:0] bits = 0xb		1.558		V
		EPDPWR0.VECONT[3:0] bits = 0xc		1.608		V
		EPDPWR0.VECONT[3:0] bits = 0xd		1.658		V
		EPDPWR0.VECONT[3:0] bits = 0xe		1.709		V
		EPDPWR0.VECONT[3:0] bits = 0xf		1.759		V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
V_E regulator output voltage (V_{E2} reference, EPDPWR0.VESEL bit = 1)	V_{E2}	EPDPWR0.VECONT[3:0] bits = 0x0		2.010		V
		EPDPWR0.VECONT[3:0] bits = 0x1		2.111		V
		EPDPWR0.VECONT[3:0] bits = 0x2		2.211		V
		EPDPWR0.VECONT[3:0] bits = 0x3		2.312		V
		EPDPWR0.VECONT[3:0] bits = 0x4		2.412		V
		EPDPWR0.VECONT[3:0] bits = 0x5		2.513		V
		EPDPWR0.VECONT[3:0] bits = 0x6		2.613		V
		EPDPWR0.VECONT[3:0] bits = 0x7	Typ.	2.714	Typ.	V
		EPDPWR0.VECONT[3:0] bits = 0x8	- 0.150	2.814	+ 0.150	V
		EPDPWR0.VECONT[3:0] bits = 0x9		2.915		V
		EPDPWR0.VECONT[3:0] bits = 0xa		3.015		V
		EPDPWR0.VECONT[3:0] bits = 0xb		3.116		V
		EPDPWR0.VECONT[3:0] bits = 0xc		3.216		V
		EPDPWR0.VECONT[3:0] bits = 0xd		3.317		V
		EPDPWR0.VECONT[3:0] bits = 0xe		3.417		V
		EPDPWR0.VECONT[3:0] bits = 0xf		3.518		V

EPD drive voltage

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = 25°C, C_{EPD1} to C_{EPD8} = 0.1 µF, No panel load

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
9V type EPD drive voltage (EPDPWR1.HVDSEL[1:0] bits = 0x2)	V_{EPD}	EPDPWR1.HVDCONT[3:0] bits = 0x0		8.10		V
		EPDPWR1.HVDCONT[3:0] bits = 0x1		8.28		V
		EPDPWR1.HVDCONT[3:0] bits = 0x2		8.46		V
		EPDPWR1.HVDCONT[3:0] bits = 0x3		8.64		V
		EPDPWR1.HVDCONT[3:0] bits = 0x4		8.82		V
		EPDPWR1.HVDCONT[3:0] bits = 0x5		9.00		V
		EPDPWR1.HVDCONT[3:0] bits = 0x6		9.18		V
		EPDPWR1.HVDCONT[3:0] bits = 0x7	Typ.	9.36	Typ.	V
		EPDPWR1.HVDCONT[3:0] bits = 0x8	- 0.75	9.54	+ 0.75	V
		EPDPWR1.HVDCONT[3:0] bits = 0x9		9.72		V
		EPDPWR1.HVDCONT[3:0] bits = 0xa		9.90		V
		EPDPWR1.HVDCONT[3:0] bits = 0xb		10.08		V
		EPDPWR1.HVDCONT[3:0] bits = 0xc		10.26		V
		EPDPWR1.HVDCONT[3:0] bits = 0xd		10.44		V
		EPDPWR1.HVDCONT[3:0] bits = 0xe		10.62		V
		EPDPWR1.HVDCONT[3:0] bits = 0xf		10.80		V
12V type EPD drive voltage (EPDPWR1.HVDSEL[1:0] bits = 0x1)	V_{EPD}	EPDPWR1.HVDCONT[3:0] bits = 0x0		10.80		V
		EPDPWR1.HVDCONT[3:0] bits = 0x1		11.04		V
		EPDPWR1.HVDCONT[3:0] bits = 0x2		11.28		V
		EPDPWR1.HVDCONT[3:0] bits = 0x3		11.52		V
		EPDPWR1.HVDCONT[3:0] bits = 0x4		11.76		V
		EPDPWR1.HVDCONT[3:0] bits = 0x5		12.00		V
		EPDPWR1.HVDCONT[3:0] bits = 0x6		12.24		V
		EPDPWR1.HVDCONT[3:0] bits = 0x7	Typ.	12.48	Typ.	V
		EPDPWR1.HVDCONT[3:0] bits = 0x8	- 0.75	12.72	+ 0.75	V
		EPDPWR1.HVDCONT[3:0] bits = 0x9		12.96		V
		EPDPWR1.HVDCONT[3:0] bits = 0xa		13.20		V
		EPDPWR1.HVDCONT[3:0] bits = 0xb		13.44		V
		EPDPWR1.HVDCONT[3:0] bits = 0xc		13.68		V
		EPDPWR1.HVDCONT[3:0] bits = 0xd		13.92		V
		EPDPWR1.HVDCONT[3:0] bits = 0xe		14.16		V
		EPDPWR1.HVDCONT[3:0] bits = 0xf		14.40		V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
15V type EPD drive voltage (EPDPWR1.HVDSEL[1:0] bits = 0x0)	V_{EPD}	EPDPWR1.HVDCONT[3:0] bits = 0x0	Typ. - 0.75	13.50	Typ. + 0.75	V
		EPDPWR1.HVDCONT[3:0] bits = 0x1		13.80		V
		EPDPWR1.HVDCONT[3:0] bits = 0x2		14.10		V
		EPDPWR1.HVDCONT[3:0] bits = 0x3		14.40		V
		EPDPWR1.HVDCONT[3:0] bits = 0x4		14.70		V
		EPDPWR1.HVDCONT[3:0] bits = 0x5		15.00		V
		EPDPWR1.HVDCONT[3:0] bits = 0x6		15.30		V
		EPDPWR1.HVDCONT[3:0] bits = 0x7		15.60		V
		EPDPWR1.HVDCONT[3:0] bits = 0x8		15.90		V
		EPDPWR1.HVDCONT[3:0] bits = 0x9		16.20		V
		EPDPWR1.HVDCONT[3:0] bits = 0xa		16.50		V
		EPDPWR1.HVDCONT[3:0] bits = 0xb		16.80		V
		EPDPWR1.HVDCONT[3:0] bits = 0xc		17.10		V
		EPDPWR1.HVDCONT[3:0] bits = 0xd		17.40		V
		EPDPWR1.HVDCONT[3:0] bits = 0xe		17.70		V
		EPDPWR1.HVDCONT[3:0] bits = 0xf		18.00		V

ESEG/ETP/EBP output characteristics

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Segment/top plane/back plane output current	I_{SEGH}	ESEG*xx*, ETP0, EBP0, V_{SEGH} = V_{EPD}	–	–	-10	µA
	I_{SEGL}	ESEG*xx*, ETP0, EBP0, V_{SEGL} = V_{SS}	10	–	–	µA

EPD driver circuit current consumption

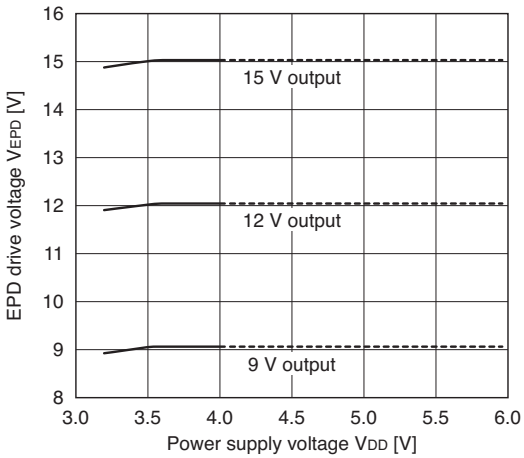
Unless otherwise specified: V_{DD} =1.8 to 5.5V, V_{SS} = 0 V, Ta = 25°C, C_{EPD1} to C_{EPD8} = 0.1 µF, No EPD panel load, OSC1 = 32.768 kHz, EPDTIMCLK.CLKSRC[1:0] bits = 0x1 (OSC1), EPDTIMCLK.CLKDIV[2:0] bits = 0x0 (CLK_EPDC = 32 kHz), EPDDBLCLK.CLKSRC[1:0] bits = 0x1 (OSC1), EPDDBLCLK.CLKDIV[2:0] bits = 0x0 (CLK_DBL = 32 kHz), EPDBSTCLK.CLKSRC[1:0] bits = 0x1 (OSC1), EPDBSTCLK.CLKDIV[2:0] bits = 0x1 (CLK_BST = 16 kHz)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
EPD circuit current *1	I_{EPD}	Reference voltage V_{E1} (= 1.759 V)	–	75	100	µA
EPD circuit current in heavy load protection mode *1	I_{EPDH}	Reference voltage V_{E1} (= 1.759 V), EPDPWR0.HVLDVE bit = 1	–	85	–	µA
		Reference voltage V_{E1} (= 1.759 V), EPDPWR1.HVLDHVD bit = 1	–	120	–	µA

*1 This value is added to the current consumption during HALT/execution when the EPD circuit is active. Current consumption increases according to the drive waveforms and panel load.

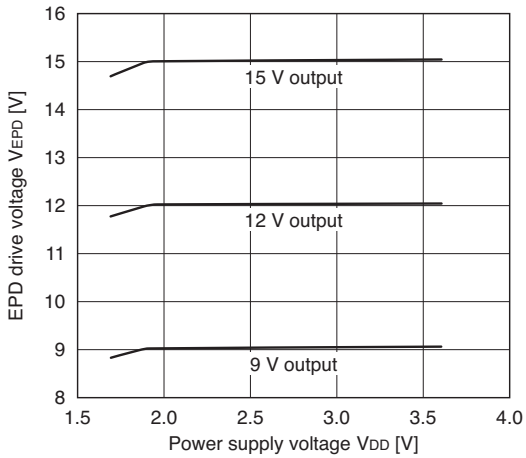
EPD drive voltage-power supply voltage characteristic (V_{E2} reference)

V_{E2} = 3.518 V, Ta = 25°C, 20 µA load, Typ. value



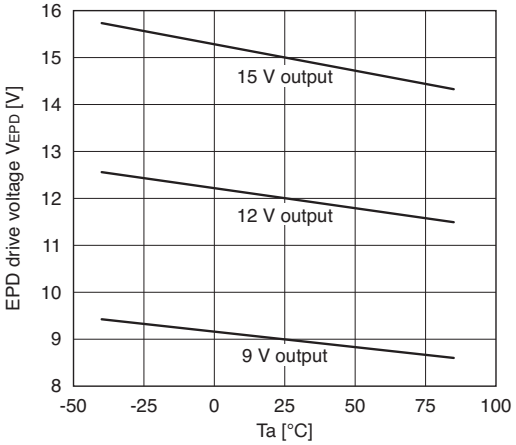
EPD drive voltage-power supply voltage characteristic (V_{E1} reference)

V_{E1} = 1.759 V, Ta = 25°C, 10 µA load, Typ. value



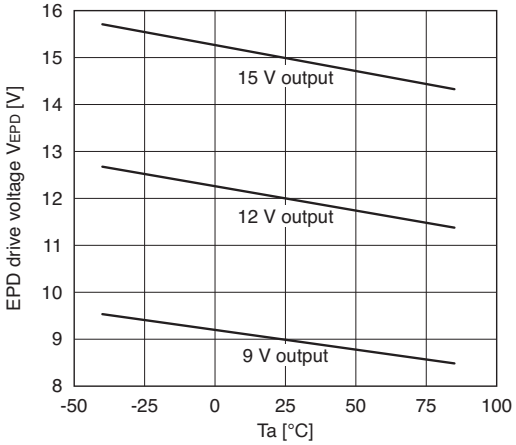
EPD drive voltage-temperature characteristic (V_{E2} reference)

V_{E2} = 3.518 V, V_{DD} = 3.6 V, 20 µA load, Typ. value



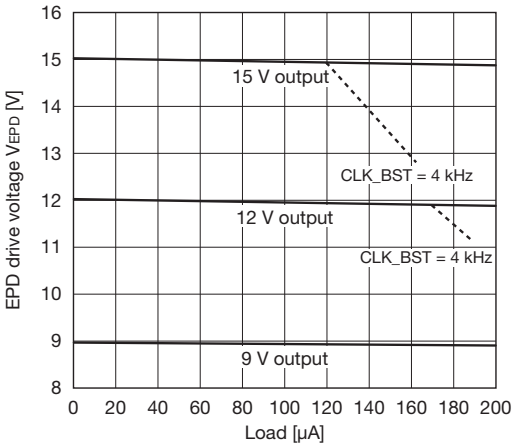
EPD drive voltage-temperature characteristic (V_{E1} reference)

V_{E1} = 1.759 V, V_{DD} = 2.0 V, 10 µA load, Typ. value



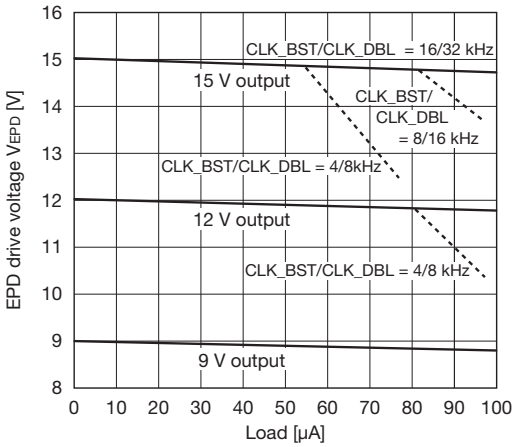
EPD drive voltage-load characteristic (V_{E2} reference)

V_{E2} = 3.518 V, Ta = 25°C, V_{DD} =3.6 V, Typ. value
CLK_BST = 4 kHz, 8 kHz, or 16 kHz



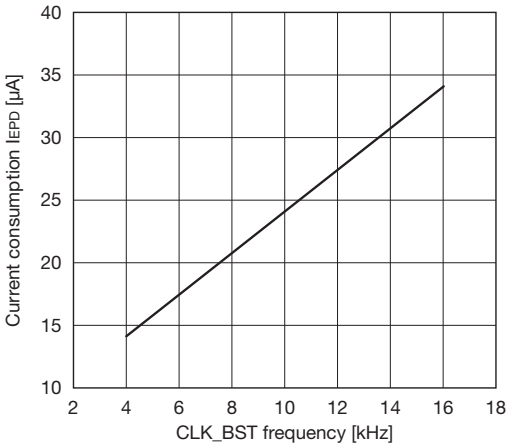
EPD drive voltage-load characteristic (V_{E1} reference)

V_{E1} = 1.759 V, Ta = 25°C, V_{DD} = 2.0 V, Typ. value
CLK_BST/CLK_DBL = 4/8 kHz, 8/16 kHz, or 16/32 kHz



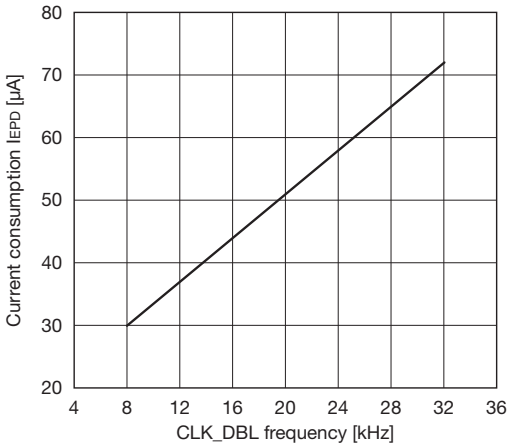
EPD driver circuit current consumption-booster clock frequency dependence (V_{E2} reference)

V_{E2} = 3.518 V, Ta = 25°C, V_{DD} = 3.6 V, No load, Typ. value



EPD driver circuit current consumption-doubler/booster clock frequency dependence (V_{E1} reference)

V_{E1} = 3.1.759 V, Ta = 25°C, V_{DD} = 2.0 V, No load, Typ. value
CLK_BST frequency = CLK_DBL frequency / 2



22.14 12-bit A/D Converter (ADC12A) Characteristics

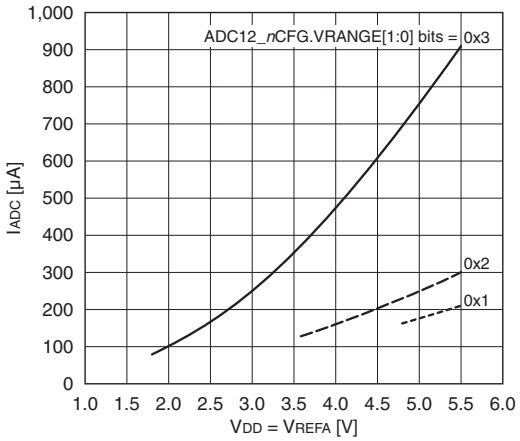
Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, VREFA*n* = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C,
ADC12_*n*TRG.SMPCLK[2:0] bits = 0x3 (7cycles)

Item	Symbol	Condition	V_{DD}	Min.	Typ.	Max.	Unit
VREFA*n* voltage range	V_{REFA}			1.8	–	V_{DD}	V
A/D conversion clock frequency	f_{CLK_ADC12A}			16	–	2,200	kHz
Sampling rate *1	f_{SMP}			–	–	100	ksps
Integral nonlinearity *2	INL	V_{DD} = VREFA*n* *3, ADC12_*n*CFG.VRANGE[1:0] bits = 0x3		–	–	±3	LSB
		V_{DD} = VREFA*n* *3, ADC12_*n*CFG.VRANGE[1:0] bits = 0x2		–	–	±6	LSB
		V_{DD} = VREFA*n* *3, ADC12_*n*CFG.VRANGE[1:0] bits = 0x1		–	–	±6	LSB
Differential nonlinearity	DNL	V_{DD} = VREFA*n* *3, ADC12_*n*CFG.VRANGE[1:0] bits = 0x3		–	–	±3	LSB
		V_{DD} = VREFA*n* *3, ADC12_*n*CFG.VRANGE[1:0] bits = 0x2		–	–	±6	LSB
		V_{DD} = VREFA*n* *3, ADC12_*n*CFG.VRANGE[1:0] bits = 0x1		–	–	±6	LSB
Zero-scale error	ZSE	V_{DD} = VREFA*n* *3		–	–	±5	LSB
Full-scale error	FSE	V_{DD} = VREFA*n* *3		–	–	±5	LSB
Analog input resistance	R_{ADIN}			–	–	4	kΩ
Analog input capacitance	C_{ADIN}			–	–	30	pF
A/D converter circuit current	I_{ADC}	ADC12_*n*CFG.VRANGE[1:0] bits = 0x3, V_{DD} = V_{REFA}, ADIN = V_{REFA}/2, f_{SMP} = 100 ksps, Ta = 25°C	3.6 V	–	380	670	µA
		ADC12_*n*CFG.VRANGE[1:0] bits = 0x2, V_{DD} = V_{REFA}, ADIN = V_{REFA}/2, f_{SMP} = 100 ksps, Ta = 25°C	4.8 V	–	230	390	µA
		ADC12_*n*CFG.VRANGE[1:0] bits = 0x1, V_{DD} = V_{REFA}, ADIN = V_{REFA}/2, f_{SMP} = 100 ksps, Ta = 25°C	5.5 V	–	210	350	µA

*1 The Max. value is the value when the A/D conversion clock frequency f_{CLK_ADC12A} = 2,000 kHz.
*2 Integral nonlinearity is measured at the end point line.
*3 The error will be increased according to the potential difference between V_{DD} and VREFA*n*.

A/D converter current consumption-power supply voltage characteristic

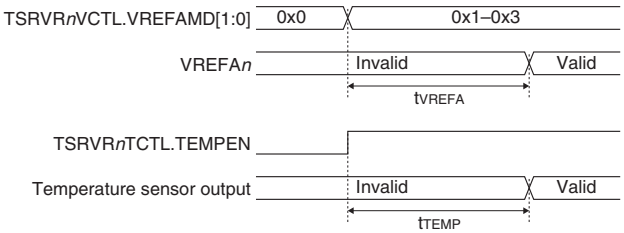
V_{DD} = V_{REFA}, ADIN = V_{REFA}/2, f_{SMP} = 100 ksps, Ta = 25°C, Typ. value



22.15 Temperature Sensor/Reference Voltage Generator (TSRVR) Characteristics

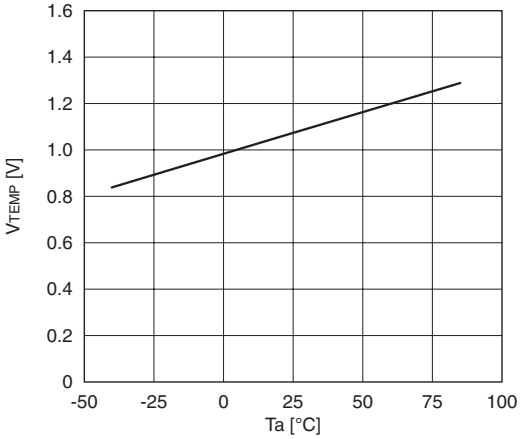
Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
V_{REFA} (2.5 V) output voltage	V_{VO25}	V_{DD} = 2.7 to 5.5 V	2.4	2.5	2.6	V
V_{REFA} (2.0 V) output voltage	V_{VO20}	V_{DD} = 2.2 to 5.5 V	1.9	2.0	2.1	V
V_{REFA} (V_{DD}) output voltage	V_{VODD}	V_{DD} = 1.8 to 5.5 V	V_{DD} - 0.1	V_{DD}	V_{DD} + 0.1	V
V_{REFA} (2.5/2.0 V) operating current	I_{VO1}	V_{DD} = 5.5 V, Ta = 25°C	25	40	60	µA
V_{REFA} (V_{DD}) operating current	I_{VO2}	V_{DD} = 5.5 V, Ta = 25°C	–	0.0	0.1	µA
V_{REFA} output voltage stabilization time	t_{VREFA}	C_{VREFA} = 0.1 µF	–	1.5	5	ms
Temperature sensor output voltage	V_{TEMP}	V_{DD} = 2.2 to 5.5 V, Ta = 25°C	1.04	1.07	1.1	V
Temperature sensor output voltage temperature coefficient	ΔV_{TEMP}	V_{DD} = 2.2to 5.5 V	–	3.6 ± 3%	3.7 ± 6%	mV/°C
Temperature sensor operating current	I_{VTEMP}	V_{DD} =5.5 V, Ta = 25°C	10	16	22	µA
Temperature sensor output stabilization time	t_{TEMP}		–	–	200	µs

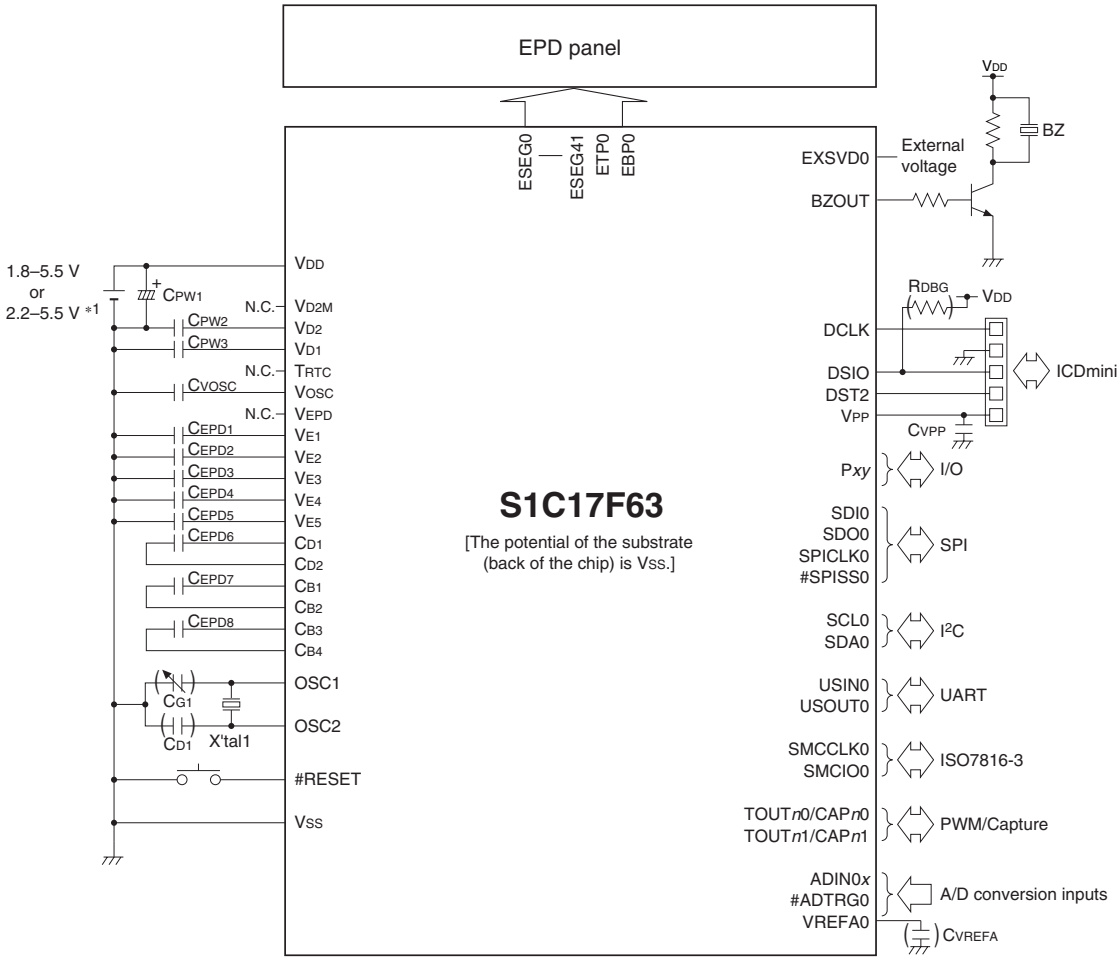


Temperature sensor output voltage-temperature characteristic

V_{DD} = 2.2 to 5.5 V, Typ. value



23 Basic External Connection Diagram



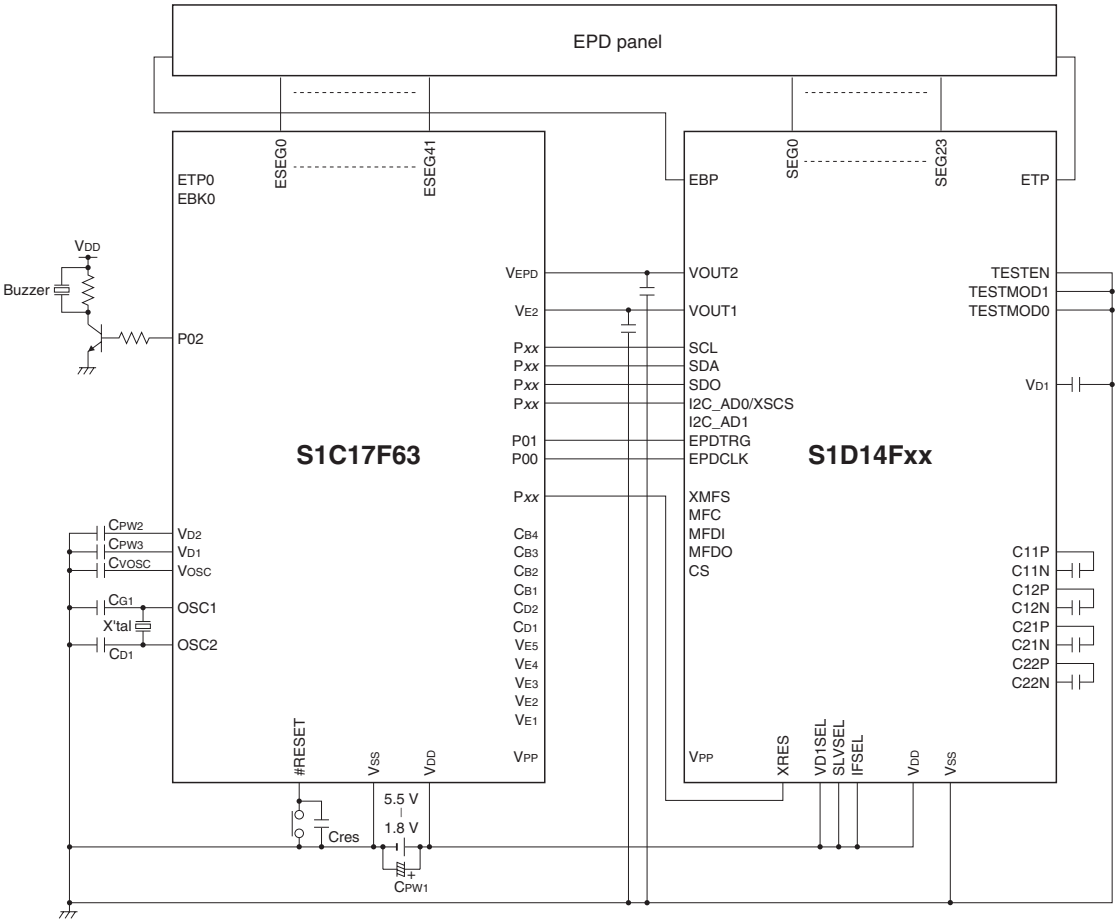
*1: For Flash/EEPROM programming
( ): Do not mount components if unnecessary.

Sample external components

Symbol	Name	Recommended components
X'tal1	32 kHz crystal resonator	C-002RX (R_1 = 50 kΩ (Max.), C_L = 7 pF) manufactured by Seiko Epson Corporation
C_{G1}	OSC1 gate capacitor	Trimmer capacitor or ceramic capacitor
C_{D1}	OSC1 drain capacitor	Ceramic capacitor
C_{PW1}	Bypass capacitor between V_{SS} and V_{DD}	Ceramic capacitor or electrolytic capacitor
C_{PW2}	Capacitor between V_{SS} and V_{D2}	Ceramic capacitor
C_{PW3}	Capacitor between V_{SS} and V_{D1}	Ceramic capacitor
C_{VOSC}	Capacitor between V_{SS} and V_{OSC}	Ceramic capacitor
C_{EPD1}	Capacitor between V_{SS} and V_{E1}	Ceramic capacitor
C_{EPD2}	Capacitor between V_{SS} and V_{E2}	Ceramic capacitor
C_{EPD3}	Capacitor between V_{SS} and V_{E3}	Ceramic capacitor
C_{EPD4}	Capacitor between V_{SS} and V_{E4}	Ceramic capacitor
C_{EPD5}	Capacitor between V_{SS} and V_{E5}	Ceramic capacitor
C_{EPD6}	Capacitor between C_{D1} and C_{D2}	Ceramic capacitor
C_{EPD7}	Capacitor between C_{B1} and C_{B2}	Ceramic capacitor
C_{EPD8}	Capacitor between C_{B3} and C_{B4}	Ceramic capacitor
BZ	Piezoelectric buzzer	PS1240P02 manufactured by TDK Corporation
C_{VREFA}	Capacitor between V_{SS} and VREFA	Ceramic capacitor
C_{VPP}	Capacitor between V_{SS} and V_{PP}	Ceramic capacitor

* For recommended component values, refer to “Recommended Operating Conditions” in the “Electrical Characteristics” chapter.

External EPD driver connection example
(when the EPD power supply in the external EPD driver is used)



24 Package

QFP15-100PIN (P-LQFP100-1414-0.50)

(Unit: mm)

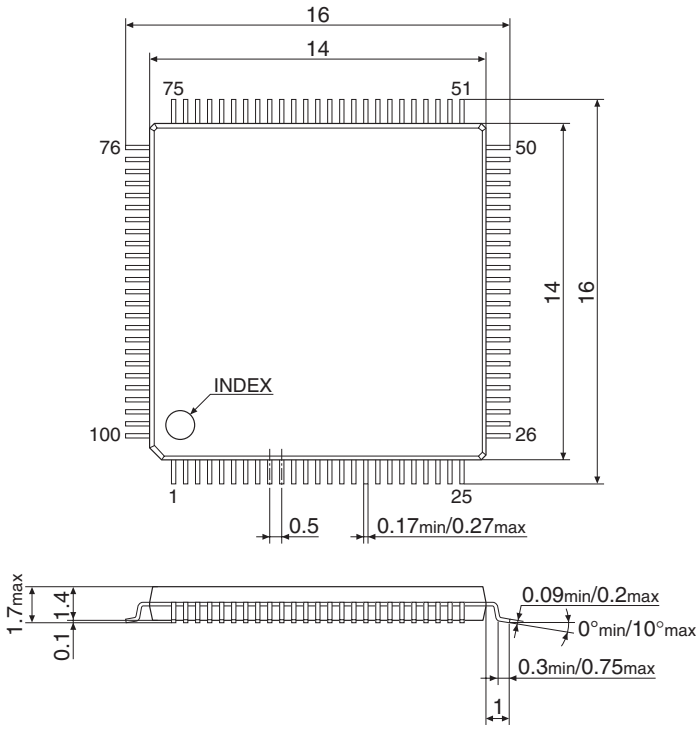


Figure 24.1 QFP15-100PIN Package Dimensions

Appendix A List of Peripheral Circuit Control Registers

0x4000–0x4008 Misc Registers (MISC)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x4000	MSCPROT (MISC System Protect Register)	15–0	PROT[15:0]	0x0000	H0	R/W	–
0x4002	MSCIRAMSZ (MISC IRAM Size Register)	15–9	–	0x00	–	R	–
		8	(reserved)	0	H0	R/WP	Always set to 0.
		7–3	–	0x04	–	R	–
		2–0	IRAMSZ[2:0]	0x2	H0	R/WP	
0x4004	MSCTTBRL (MISC Vector Table Address Low Register)	15–8	TTBR[15:8]	0x80	H0	R/WP	–
		7–0	TTBR[7:0]	0x00	H0	R	
0x4006	MSCTTBRH (MISC Vector Table Address High Register)	15–8	–	0x00	–	R	–
		7–0	TTBR[23:16]	0x00	H0	R/WP	
0x4008	MSCPSR (MISC PSR Register)	15–8	–	0x00	–	R	–
		7–5	PSRIL[2:0]	0x0	H0	R	
		4	PSRIE	0	H0	R	
		3	PSRC	0	H0	R	
		2	PSRV	0	H0	R	
		1	PSRZ	0	H0	R	
		0	PSRN	0	H0	R	

0x4020 Power Generator (PWG)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x4020	PWGVD1CTL (V_{D1} Control Register)	15–8	–	0x00	–	R	–
		7–2	–	0x00	–	R	
		1–0	REGMODE[1:0]	0x0	H0	R/WP	

0x4040–0x4054 Clock Generator (CLG)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x4040	CLGSCLK (CLG System Clock Control Register)	15	WUPMD	0	H0	R/WP	–
		14	–	0	–	R	
		13–12	WUPDIV[1:0]	0x0	H0	R/WP	
		11–10	–	0x0	–	R	
		9–8	WUPSRC[1:0]	0x0	H0	R/WP	
		7–6	–	0x0	–	R	
		5–4	CLKDIV[1:0]	0x0	H0	R/WP	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/WP	
0x4042	CLGOSC (CLG Oscillation Control Register)	15–12	–	0x0	–	R	–
		11	EXOSCSLPC	1	H0	R/W	
		10	OSC3SLPC	1	H0	R/W	
		9	OSC1SLPC	1	H0	R/W	
		8	IOSCSLPC	1	H0	R/W	
		7–4	–	0x0	–	R	
		3	EXOSCEN	0	H0	R/W	
		2	OSC3EN	0	H0	R/W	
		1	OSC1EN	0	H0	R/W	
		0	IOSCEN	1	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x4044	CLGIOSC (CLG IOSC Control Register)	15–8	–	0x00	–	R	–
		7–5	–	0x0	–	R	
		4	IOSCSTM	0	H0	R/WP	
		3–0	–	0x0	–	R	
0x4046	CLGOSC1TRIM (CLG OSC1 Trimming Register)	15–8	–	0x00	–	R	–
		7–6	–	0x0	–	R	
		5–0	XFIB[5:0]	*	H0	R	
0x4048	CLGOSC3 (CLG OSC3 Control Register)	15–13	–	0x0	–	R	–
		12–10	OSC3FQ[2:0]	0x3	H0	R/WP	
		9–8	–	0x0	–	R	
		7–3	–	0x00	–	R	
		2–0	OSC3WT[2:0]	0x6	H0	R/WP	
0x404c	CLGINTF (CLG Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7	–	0x0	–	R	
		6–5	(reserved)	0x0	H0	R	
		4	IOSCTEDIF	0	H0	R/W	Cleared by writing 1.
		3	–	0	–	R	–
		2	OSC3STAIF	0	H0	R/W	Cleared by writing 1.
		1	–	0	–	R	–
		0	IOSCSTAIF	0	H0	R/W	
0x404e	CLGINTE (CLG Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7	–	0	–	R	
		6–5	(reserved)	0x0	H0	R	
		4	IOSCTEDIE	0	H0	R/W	
		3	–	0	–	R	
		2	OSC3STAIE	0	H0	R/W	
		1	–	0	–	R	
		0	IOSCSTAIE	0	H0	R/W	
0x4050	CLGFOUT0 (CLG FOUT Control Register 0)	15–8	–	0x00	–	R	–
		7	–	0	–	R	
		6–4	FOUTDIV[2:0]	0x0	H0	R/W	
		3–2	FOUTSRC[1:0]	0x0	H0	R/W	
		1	–	0	–	R	
		0	FOUTEN	0	H0	R/W	
0x4054	CLGTRIM (CLG Oscillation Frequency Trimming Register)	15–14	–	0x0	–	R	–
		13–8	OSC3AJ[5:0]	*	H0	R/WP	* Determined by factory adjustment.
		7–6	–	0x0	–	R	–
		5–0	IOSCAJ[5:0]	*	H0	R/WP	* Determined by factory adjustment.

0x4080–0x4092 Interrupt Controller (ITC)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x4080	ITCLV0 (ITC Interrupt Level Setup Register 0)	15–11	–	0x00	–	R	–
		10–8	ILV1[2:0]	0x0	H0	R/W	Port interrupt (ILVPPORT)
		7–3	–	0x00	–	R	–
		2–0	ILV0[2:0]	0x0	H0	R/W	Supply voltage detector interrupt (ILVSVD3)
0x4082	ITCLV1 (ITC Interrupt Level Setup Register 1)	15–11	–	0x00	–	R	–
		10–8	ILV3[2:0]	0x0	H0	R/W	Clock generator interrupt (ILVCLG)
		7–0	–	0x00	–	R	–

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x4084	ITCLV2 (ITC Interrupt Level Setup Register 2)	15–11	–	0x00	–	R	–
		10–8	ILV5[2:0]	0x0	H0	R/W	16-bit timer Ch.0 interrupt (ILVT16_0)
		7–3	–	0x00	–	R	–
		2–0	ILV4[2:0]	0x0	H0	R/W	Real-time clock interrupt (ILVRTCB_0)
0x4086	ITCLV3 (ITC Interrupt Level Setup Register 3)	15–11	–	0x00	–	R	–
		10–8	ILV7[2:0]	0x0	H0	R/W	16-bit timer Ch.1 interrupt (ILVT16_1)
		7–3	–	0x00	–	R	–
		2–0	ILV6[2:0]	0x0	H0	R/W	UART Ch.0 interrupt (ILVUART3_0)
0x4088	ITCLV4 (ITC Interrupt Level Setup Register 4)	15–11	–	0x00	–	R	–
		10–8	ILV9[2:0]	0x0	H0	R/W	I²C interrupt (ILVI2C_0)
		7–3	–	0x00	–	R	–
		2–0	ILV8[2:0]	0x0	H0	R/W	Synchronous serial interface Ch.0 interrupt (ILVSPIA_0)
0x408a	ITCLV5 (ITC Interrupt Level Setup Register 5)	15–11	–	0x00	–	R	–
		10–8	ILV11[2:0]	0x0	H0	R/W	16-bit PWM timer Ch.1 interrupt (ILVT16B_1)
		7–3	–	0x00	–	R	–
		2–0	ILV10[2:0]	0x0	H0	R/W	16-bit PWM timer Ch.0 interrupt (ILVT16B_0)
0x408c	ITCLV6 (ITC Interrupt Level Setup Register 6)	15–11	–	0x00	–	R	–
		10–8	ILV13[2:0]	0x0	H0	R/W	Sound generator interrupt (ILVSNDA_0)
		7–3	–	0x00	–	R	–
		2–0	ILV12[2:0]	0x0	H0	R/W	Smart card interface interrupt (ILSMCIF_0)
0x408e	ITCLV7 (ITC Interrupt Level Setup Register 7)	15–11	–	0x00	–	R	–
		10–8	ILV15[2:0]	0x0	H0	R/W	12-bit A/D converter interrupt (ILVADC12A_0)
		7–3	–	0x00	–	R	–
		2–0	ILV14[2:0]	0x0	H0	R/W	16-bit timer Ch.2 interrupt (ILVT16_2)
0x4090	ITCLV8 (ITC Interrupt Level Setup Register 8)	15–11	–	0x00	–	R	–
		10–8	ILV17[2:0]	0x0	H0	R/W	EEPROM controller interrupt (ILVEPRC)
		7–3	–	0x00	–	R	–
		2–0	ILV16[2:0]	0x0	H0	R/W	EPD controller/driver interrupt (ILVEPDC)
0x4092	ITCLV9 (ITC Interrupt Level Setup Register 9)	15–11	–	0x00	–	R	–
		10–8	ILV19[2:0]	0x0	H0	R/W	Synchronous serial interface Ch.1 interrupt (ILVSPIA_1)
		7–3	–	0x00	–	R	–
		2–0	ILV18[2:0]	0x0	H0	R/W	16-bit timer Ch.3 interrupt (ILVT16_3)

0x40a0–0x40a4 Watchdog Timer (WDT2)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x40a0	WDTCLK (WDT2 Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/WP	
		7–6	–	0x0	–	R	
		5–4	CLKDIV[1:0]	0x0	H0	R/WP	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/WP	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x40a2	WDTCTL (WDT2 Control Register)	15–11	–	0x00	–	R	–
		10–9	MOD[1:0]	0x0	H0	R/WP	
		8	STATNMI	0	H0	R	
		7–5	–	0x0	–	R	
		4	WDTCNTRST	0	H0	WP	Always read as 0.
		3–0	WDTRUN[3:0]	0xa	H0	R/WP	–
0x40a4	WDTCMP (WDT2 Counter Compare Match Register)	15–10	–	0x00	–	R	–
		9–0	CMP[9:0]	0x3ff	H0	R/WP	

0x4100–0x4106 Supply Voltage Detector (SVD3)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x4100	SVDCLK (SVD3 Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	1	H0	R/WP	
		7	–	0	–	R	
		6–4	CLKDIV[2:0]	0x0	H0	R/WP	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/WP	
0x4102	SVDCTL (SVD3 Control Register)	15	VDSEL	0	H1	R/WP	–
		14–13	SVDSC[1:0]	0x0	H0	R/WP	Writing takes effect when the SVDCTL.SVDMD[1:0] bits are not 0x0.
		12–8	SVDC[4:0]	0x1e	H1	R/WP	–
		7–4	SVDRE[3:0]	0x0	H1	R/WP	
		3	–	0	–	R	
		2–1	SVDMD[1:0]	0x0	H0	R/WP	
		0	MODEN	0	H1	R/WP	
0x4104	SVDINTF (SVD3 Status and Interrupt Flag Register)	15–9	–	0x00	–	R	–
		8	SVDDT	x	–	R	
		7–1	–	0x00	–	R	
		0	SVDIF	0	H1	R/W	Cleared by writing 1.
0x4106	SVDINTE (SVD3 Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	SVDIE	0	H0	R/W	

0x4160–0x416c 16-bit Timer (T16) Ch.0

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x4160	T16_0CLK (T16 Ch.0 Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/W	
		7–4	CLKDIV[3:0]	0x0	H0	R/W	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/W	
0x4162	T16_0MOD (T16 Ch.0 Mode Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	TRMD	0	H0	R/W	
0x4164	T16_0CTL (T16 Ch.0 Control Register)	15–9	–	0x00	–	R	–
		8	PRUN	0	H0	R/W	
		7–2	–	0x00	–	R	
		1	PRESET	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x4166	T16_0TR (T16 Ch.0 Reload Data Register)	15–0	TR[15:0]	0xffff	H0	R/W	–
0x4168	T16_0TC (T16 Ch.0 Counter Data Register)	15–0	TC[15:0]	0xffff	H0	R	–

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x416a	T16_0INTF (T16 Ch.0 Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	UFIF	0	H0	R/W	Cleared by writing 1.
0x416c	T16_0INTE (T16 Ch.0 Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	UFIE	0	H0	R/W	

0x41b0 Flash Controller (FLASHC)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x41b0	FLASHCWAIT (FLASHC Flash Read Cycle Register)	15–8	–	0x00	–	R	–
		7–2	–	0x00	–	R	–
		1–0	RDWAIT[1:0]	0x1	H0	R/WP	

0x41c0–0x41ca EEPROM Controller (EEPROMC)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x41c0	EPRCCTL0 (EEPROMC Control Register 0)	15–9	–	0x00	–	R	–
		8	EP_XPOR	1	H0	R/WP	
		7–2	–	0x00	–	R	
		1	EP_PWRSET	0	H0	R/WP	
		0	EP_WMODE	0	H0	R/WP	
0x41c2	EPRCCTL1 (EEPROMC Control Register 1)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	EP_CK	0	H0	WP	
0x41c4	EPRCADR (EEPROMC Address Register)	15–8	–	0x00	–	R	–
		7–0	EP_ADDR[7:0]	0x00	H0	R/WP	
0x41c6	EPRCWDAT (EEPROMC Write Data Register)	15–8	–	0x00	–	R	–
		7–0	EP_WDAT[7:0]	0x00	H0	R/WP	
0x41c8	EPRCINTF (EEPROMC Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7–2	–	0x00	–	R	
		1	ECCERIF	0	H0	R/W	Cleared by writing 1.
		0	RXBIF	0	H0	R/W	
0x41ca	EPRCINTE (EEPROMC Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7–2	–	0x00	–	R	
		1	ECCERIE	0	H0	R/W	
		0	RXBIE	0	H0	R/W	

0x4200–0x42e2 I/O Ports (PPORT)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x4200	P0DAT (P0 Port Data Register)	15–8	P0OUT[7:0]	0x00	H0	R/W	–
		7–0	P0IN[7:0]	0x00	H0	R	
0x4202	P0IOEN (P0 Port Enable Register)	15–8	P0IEN[7:0]	0x00	H0	R/W	–
		7–0	P0OEN[7:0]	0x00	H0	R/W	
0x4204	P0RCTL (P0 Port Pull-up/down Control Register)	15–8	P0PDPU[7:0]	0x00	H0	R/W	–
		7–0	P0REN[7:0]	0x00	H0	R/W	
0x4206	P0INTF (P0 Port Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7–0	P0IF[7:0]	0x00	H0	R/W	Cleared by writing 1.
0x4208	P0INTCTL (P0 Port Interrupt Control Register)	15–8	P0EDGE[7:0]	0x00	H0	R/W	–
		7–0	P0IE[7:0]	0x00	H0	R/W	
0x420a	P0CHATEN (P0 Port Chattering Filter Enable Register)	15–8	–	0x00	–	R	–
		7–0	P0CHATEN[7:0]	0x00	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x420c	P0MODSEL (P0 Port Mode Select Register)	15–8	–	0x00	–	R	–
		7–0	P0SEL[7:0]	0x00	H0	R/W	
0x420e	P0FNCSEL (P0 Port Function Select Register)	15–14	P07MUX[1:0]	0x0	H0	R/W	–
		13–12	P06MUX[1:0]	0x0	H0	R/W	
		11–10	P05MUX[1:0]	0x0	H0	R/W	
		9–8	P04MUX[1:0]	0x0	H0	R/W	
		7–6	P03MUX[1:0]	0x0	H0	R/W	
		5–4	P02MUX[1:0]	0x0	H0	R/W	
		3–2	P01MUX[1:0]	0x0	H0	R/W	
		1–0	P00MUX[1:0]	0x0	H0	R/W	
0x4210	P1DAT (P1 Port Data Register)	15–14	–	0x0	–	R	–
		13–8	P1OUT[5:0]	0x00	H0	R/W	
		7–6	–	0x0	–	R	
		5–0	P1IN[5:0]	0x00	H0	R	
0x4212	P1IOEN (P1 Port Enable Register)	15–14	–	0x0	–	R	–
		13–8	P1IEN[5:0]	0x00	H0	R/W	
		7–6	–	0x0	–	R	
		5–0	P1OEN[5:0]	0x00	H0	R/W	
0x4214	P1RCTL (P1 Port Pull-up/down Control Register)	15–14	–	0x0	–	R	–
		13–8	P1PDPU[5:0]	0x00	H0	R/W	
		7–6	–	0x0	–	R	
		5–0	P1REN[5:0]	0x00	H0	R/W	
0x4216	P1INTF (P1 Port Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7–6	–	0x0	–	R	
		5–0	P1IF[5:0]	0x00	H0	R/W	Cleared by writing 1.
0x4218	P1INTCTL (P1 Port Interrupt Control Register)	15–14	–	0x0	–	R	–
		13–8	P1EDGE[5:0]	0x00	H0	R/W	
		7–6	–	0x0	–	R	
		5–0	P1IE[5:0]	0x00	H0	R/W	
0x421a	P1CHATEN (P1 Port Chattering Filter Enable Register)	15–8	–	0x00	–	R	–
		7–6	–	0x0	–	R	
		5–0	P1CHATEN[5:0]	0x00	H0	R/W	
0x421c	P1MODSEL (P1 Port Mode Select Register)	15–8	–	0x00	–	R	–
		7–6	–	0x0	–	R	
		5–0	P1SEL[5:0]	0x00	H0	R/W	
0x421e	P1FNCSEL (P1 Port Function Select Register)	15–12	–	0x0	–	R	–
		11–10	P15MUX[1:0]	0x0	H0	R/W	
		9–8	P14MUX[1:0]	0x0	H0	R/W	
		7–6	P13MUX[1:0]	0x0	H0	R/W	
		5–4	P12MUX[1:0]	0x0	H0	R/W	
		3–2	P11MUX[1:0]	0x0	H0	R/W	
		1–0	P10MUX[1:0]	0x0	H0	R/W	
0x42d0	PDDAT (Pd Port Data Register)	15–11	–	0x00	–	R	–
		10–8	PDOUT[2:0]	0x0	H0	R/W	
		7–3	–	0x00	–	R	
		2–0	PDIN[2:0]	x	H0	R	
0x42d2	PDIOEN (Pd Port Enable Register)	15–11	–	0x00	–	R	–
		10–8	PDIEN[2:0]	0x0	H0	R/W	
		7–3	–	0x00	–	R	
		2–0	PDOEN[2:0]	0x0	H0	R/W	
0x42d4	PDRCTL (Pd Port Pull-up/down Control Register)	15–11	–	0x00	–	R	–
		10–8	PDPDPU[2:0]	0x0	H0	R/W	
		7–3	–	0x00	–	R	
		2–0	PDREN[2:0]	0x0	H0	R/W	
0x42dc	PDMODSEL (Pd Port Mode Select Register)	15–8	–	0x00	–	R	–
		7–3	–	0x00	–	R	
		2–0	PDSEL[2:0]	0x7	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x42de	PDFNCSEL (Pd Port Function Select Register)	15–8	–	0x00	–	R	–
		7–6	–	0x0	–	R	
		5–4	PD2MUX[1:0]	0x0	H0	R/W	
		3–2	PD1MUX[1:0]	0x0	H0	R/W	
		1–0	PD0MUX[1:0]	0x0	H0	R/W	
0x42e0	PCLK (P Port Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/WP	
		7–4	CLKDIV[3:0]	0x0	H0	R/WP	
		3–2	KRSTCFG[1:0]	0x0	H0	R/WP	
		1–0	CLKSRC[1:0]	0x0	H0	R/WP	
0x42e2	PINTFGRP (P Port Interrupt Flag Group Register)	15–8	–	0x00	–	R	–
		7–3	–	0x00	–	R	
		2	P2INT	0	H0	R	
		1	P1INT	0	H0	R	
		0	P0INT	0	H0	R	

0x4300–0x430c Universal Port Multiplexer (UPMUX)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x4300	P0UPMUX0 (P00–01 Universal Port Multiplexer Setting Register)	15–13	P01PPFNC[2:0]	0x0	H0	R/W	–
		12–11	P01PERICH[1:0]	0x0	H0	R/W	
		10–8	P01PERISEL[2:0]	0x0	H0	R/W	
		7–5	P00PPFNC[2:0]	0x0	H0	R/W	
		4–3	P00PERICH[1:0]	0x0	H0	R/W	
		2–0	P00PERISEL[2:0]	0x0	H0	R/W	
0x4302	P0UPMUX1 (P02–03 Universal Port Multiplexer Setting Register)	15–13	P03PPFNC[2:0]	0x0	H0	R/W	–
		12–11	P03PERICH[1:0]	0x0	H0	R/W	
		10–8	P03PERISEL[2:0]	0x0	H0	R/W	
		7–5	P02PPFNC[2:0]	0x0	H0	R/W	
		4–3	P02PERICH[1:0]	0x0	H0	R/W	
		2–0	P02PERISEL[2:0]	0x0	H0	R/W	
0x4304	P0UPMUX2 (P04–05 Universal Port Multiplexer Setting Register)	15–13	P05PPFNC[2:0]	0x0	H0	R/W	–
		12–11	P05PERICH[1:0]	0x0	H0	R/W	
		10–8	P05PERISEL[2:0]	0x0	H0	R/W	
		7–5	P04PPFNC[2:0]	0x0	H0	R/W	
		4–3	P04PERICH[1:0]	0x0	H0	R/W	
		2–0	P04PERISEL[2:0]	0x0	H0	R/W	
0x4306	P0UPMUX3 (P06–07 Universal Port Multiplexer Setting Register)	15–13	P07PPFNC[2:0]	0x0	H0	R/W	–
		12–11	P07PERICH[1:0]	0x0	H0	R/W	
		10–8	P07PERISEL[2:0]	0x0	H0	R/W	
		7–5	P06PPFNC[2:0]	0x0	H0	R/W	
		4–3	P06PERICH[1:0]	0x0	H0	R/W	
		2–0	P06PERISEL[2:0]	0x0	H0	R/W	
0x4308	P1UPMUX0 (P10–11 Universal Port Multiplexer Setting Register)	15–13	P11PPFNC[2:0]	0x0	H0	R/W	–
		12–11	P11PERICH[1:0]	0x0	H0	R/W	
		10–8	P11PERISEL[2:0]	0x0	H0	R/W	
		7–5	P10PPFNC[2:0]	0x0	H0	R/W	
		4–3	P10PERICH[1:0]	0x0	H0	R/W	
		2–0	P10PERISEL[2:0]	0x0	H0	R/W	
0x430a	P1UPMUX1 (P12–13 Universal Port Multiplexer Setting Register)	15–13	P13PPFNC[2:0]	0x0	H0	R/W	–
		12–11	P13PERICH[1:0]	0x0	H0	R/W	
		10–8	P13PERISEL[2:0]	0x0	H0	R/W	
		7–5	P12PPFNC[2:0]	0x0	H0	R/W	
		4–3	P12PERICH[1:0]	0x0	H0	R/W	
		2–0	P12PERISEL[2:0]	0x0	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x430c	P1UPMUX2 (P14–15 Universal Port Multiplexer Setting Register)	15–13	P15PPFNC[2:0]	0x0	H0	R/W	–
		12–11	P15PERICH[1:0]	0x0	H0	R/W	
		10–8	P15PERISEL[2:0]	0x0	H0	R/W	
		7–5	P14PPFNC[2:0]	0x0	H0	R/W	
		4–3	P14PERICH[1:0]	0x0	H0	R/W	
		2–0	P14PERISEL[2:0]	0x0	H0	R/W	

0x4380–0x4390 UART (UART3) Ch.0

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x4380	UA0CLK (UART3 Ch.0 Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/W	
		7–6	–	0x0	–	R	
		5–4	CLKDIV[1:0]	0x0	H0	R/W	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/W	
0x4382	UA0MOD (UART3 Ch.0 Mode Register)	15–13	–	0x0	–	R	–
		12	PECAR	0	H0	R/W	
		11	CAREN	0	H0	R/W	
		10	BRDIV	0	H0	R/W	
		9	INVRX	0	H0	R/W	
		8	INVTX	0	H0	R/W	
		7	–	0	–	R	
		6	PUEN	0	H0	R/W	
		5	OUTMD	0	H0	R/W	
		4	IRMD	0	H0	R/W	
		3	CHLN	0	H0	R/W	
		2	PREN	0	H0	R/W	
		1	PRMD	0	H0	R/W	
		0	STPB	0	H0	R/W	
0x4384	UA0BR (UART3 Ch.0 Baud-Rate Register)	15–12	–	0x0	–	R	–
		11–8	FMD[3:0]	0x0	H0	R/W	
		7–0	BRT[7:0]	0x00	H0	R/W	
0x4386	UA0CTL (UART3 Ch.0 Control Register)	15–8	–	0x00	–	R	–
		7–2	–	0x00	–	R	
		1	SFTRST	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x4388	UA0TXD (UART3 Ch.0 Transmit Data Register)	15–8	–	0x00	–	R	–
		7–0	TXD[7:0]	0x00	H0	R/W	
0x438a	UA0RXD (UART3 Ch.0 Receive Data Register)	15–8	–	0x00	–	R	–
		7–0	RXD[7:0]	0x00	H0	R	
0x438c	UA0INTF (UART3 Ch.0 Status and Interrupt Flag Register)	15–10	–	0x00	–	R	–
		9	RBSY	0	H0/S0	R	
		8	TBSY	0	H0/S0	R	
		7	–	0	–	R	
		6	TENDIF	0	H0/S0	R/W	Cleared by writing 1.
		5	FEIF	0	H0/S0	R/W	Cleared by writing 1 or reading the UA0RXD register.
		4	PEIF	0	H0/S0	R/W	
		3	OEIF	0	H0/S0	R/W	Cleared by writing 1.
		2	RB2FIF	0	H0/S0	R	Cleared by reading the UA0RXD register.
		1	RB1FIF	0	H0/S0	R	
		0	TBEIF	1	H0/S0	R	Cleared by writing to the UA0TXD register.

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x438e	UA0INTE (UART3 Ch.0 Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7	–	0	–	R	
		6	TENDIE	0	H0	R/W	
		5	FEIE	0	H0	R/W	
		4	PEIE	0	H0	R/W	
		3	OEIE	0	H0	R/W	
		2	RB2FIE	0	H0	R/W	
		1	RB1FIE	0	H0	R/W	
		0	TBEIE	0	H0	R/W	
0x4390	UA0CAWF (UART3 Ch.0 Carrier Waveform Register)	15–8	–	0x00	–	R	–
		7–0	CRPER[7:0]	0x00	H0	R/W	

0x43a0–0x43ac 16-bit Timer (T16) Ch.1

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x43a0	T16_1CLK (T16 Ch.1 Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/W	
		7–4	CLKDIV[3:0]	0x0	H0	R/W	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/W	
0x43a2	T16_1MOD (T16 Ch.1 Mode Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	TRMD	0	H0	R/W	
0x43a4	T16_1CTL (T16 Ch.1 Control Register)	15–9	–	0x00	–	R	–
		8	PRUN	0	H0	R/W	
		7–2	–	0x00	–	R	
		1	PRESET	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x43a6	T16_1TR (T16 Ch.1 Reload Data Register)	15–0	TR[15:0]	0xffff	H0	R/W	–
0x43a8	T16_1TC (T16 Ch.1 Counter Data Register)	15–0	TC[15:0]	0xffff	H0	R	–
0x43aa	T16_1INTF (T16 Ch.1 Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	UFIF	0	H0	R/W	Cleared by writing 1.
0x43ac	T16_1INTE (T16 Ch.1 Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	UFIE	0	H0	R/W	

0x43b0–0x43ba Synchronous Serial Interface (SPIA) Ch.0

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x43b0	SPI0MOD (SPIA Ch.0 Mode Register)	15–12	–	0x0	–	R	–
		11–8	CHLN[3:0]	0x7	H0	R/W	
		7–6	–	0x0	–	R	
		5	PUEN	0	H0	R/W	
		4	NOCLKDIV	0	H0	R/W	
		3	LSBFST	0	H0	R/W	
		2	CPHA	0	H0	R/W	
		1	CPOL	0	H0	R/W	
		0	MST	0	H0	R/W	
0x43b2	SPI0CTL (SPIA Ch.0 Control Register)	15–8	–	0x00	–	R	–
		7–2	–	0x00	–	R	
		1	SFTRST	0	H0	R/W	
		0	MODEN	0	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x43b4	SPI0TXD (SPIA Ch.0 Transmit Data Register)	15–0	TXD[15:0]	0x0000	H0	R/W	–
0x43b6	SPI0RXD (SPIA Ch.0 Receive Data Register)	15–0	RXD[15:0]	0x0000	H0	R	–
0x43b8	SPI0INTF (SPIA Ch.0 Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7	BSY	0	H0	R	
		6–4	–	0x0	–	R	
		3	OEIF	0	H0/S0	R/W	Cleared by writing 1.
		2	TENDIF	0	H0/S0	R/W	
		1	RBFIF	0	H0/S0	R	Cleared by reading the SPI0RXD register.
		0	TBEIF	1	H0/S0	R	Cleared by writing to the SPI0TXD register.
0x43ba	SPI0INTE (SPIA Ch.0 Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7–4	–	0x0	–	R	
		3	OEIE	0	H0	R/W	
		2	TENDIE	0	H0	R/W	
		1	RBFIE	0	H0	R/W	
		0	TBEIE	0	H0	R/W	

0x43c0–0x43d2 I²C (I2C) Ch.0

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x43c0	I2C0CLK (I2C Ch.0 Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/W	
		7–6	–	0x0	–	R	
		5–4	CLKDIV[1:0]	0x0	H0	R/W	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/W	
0x43c2	I2C0MOD (I2C Ch.0 Mode Register)	15–8	–	0x00	–	R	–
		7–3	–	0x00	–	R	
		2	OADR10	0	H0	R/W	
		1	GCEN	0	H0	R/W	
		0	–	0	–	R	
0x43c4	I2C0BR (I2C Ch.0 Baud-Rate Register)	15–8	–	0x00	–	R	–
		7	–	0	–	R	
		6–0	BRT[6:0]	0x7f	H0	R/W	
0x43c8	I2C0OADR (I2C Ch.0 Own Address Register)	15–10	–	0x00	–	R	–
		9–0	OADR[9:0]	0x000	H0	R/W	
0x43ca	I2C0CTL (I2C Ch.0 Control Register)	15–8	–	0x00	–	R	–
		7–6	–	0x0	–	R	
		5	MST	0	H0	R/W	
		4	TXNACK	0	H0/S0	R/W	
		3	TXSTOP	0	H0/S0	R/W	
		2	TXSTART	0	H0/S0	R/W	
		1	SFTRST	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x43cc	I2C0TXD (I2C Ch.0 Transmit Data Register)	15–8	–	0x00	–	R	–
		7–0	TXD[7:0]	0x00	H0	R/W	
0x43ce	I2C0RXD (I2C Ch.0 Receive Data Register)	15–8	–	0x00	–	R	–
		7–0	RXD[7:0]	0x00	H0	R	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x43d0	I2C0INTF (I2C Ch.0 Status and Interrupt Flag Register)	15–13	–	0x0	–	R	–
		12	SDALOW	0	H0	R	
		11	SCLLOW	0	H0	R	
		10	BSY	0	H0/S0	R	
		9	TR	0	H0	R	
		8	–	0	–	R	
		7	BYTEENDIF	0	H0/S0	R/W	Cleared by writing 1.
		6	GCIF	0	H0/S0	R/W	
		5	NACKIF	0	H0/S0	R/W	
		4	STOPIF	0	H0/S0	R/W	
		3	STARTIF	0	H0/S0	R/W	
		2	ERRIF	0	H0/S0	R/W	
		1	RBFIF	0	H0/S0	R	Cleared by reading the I2C0RXD register.
		0	TBEIF	0	H0/S0	R	Cleared by writing to the I2C0TXD register.
0x43d2	I2C0INTE (I2C Ch.0 Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7	BYTEENDIE	0	H0	R/W	
		6	GCIE	0	H0	R/W	
		5	NACKIE	0	H0	R/W	
		4	STOPIE	0	H0	R/W	
		3	STARTIE	0	H0	R/W	
		2	ERRIE	0	H0	R/W	
		1	RBFIE	0	H0	R/W	
		0	TBEIE	0	H0	R/W	

0x43e0 SPI Slave Selector (SPISLV_SEL)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x43e0	SPISLVSEL (SPI Slave Select Register)	15–8	–	0x00	–	R	–
		7–3	–	0x00	–	R	
		2–0	SLV[2:0]	0x0	H0	R/W	

0x5000–0x501a 16-bit PWM Timer (T16B) Ch.0

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5000	T16B0CLK (T16B Ch.0 Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/W	
		7–4	CLKDIV[3:0]	0x0	H0	R/W	
		3	–	0	–	R	
		2–0	CLKSRC[2:0]	0x0	H0	R/W	
0x5002	T16B0CTL (T16B Ch.0 Counter Control Register)	15–9	–	0x00	–	R	–
		8	MAXBSY	0	H0	R	
		7–6	–	0x0	–	R	
		5–4	CNTMD[1:0]	0x0	H0	R/W	
		3	ONEST	0	H0	R/W	
		2	RUN	0	H0	R/W	
		1	PRESET	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x5004	T16B0MC (T16B Ch.0 Max Counter Data Register)	15–0	MC[15:0]	0xffff	H0	R/W	–
0x5006	T16B0TC (T16B Ch.0 Timer Counter Data Register)	15–0	TC[15:0]	0x0000	H0	R	–

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5008	T16B0CS (T16B Ch.0 Counter Status Register)	15–8	–	0x00	–	R	–
		7–4	–	0x0	–	R	
		3	CAPI1	0	H0	R	
		2	CAPI0	0	H0	R	
		1	UP_DOWN	1	H0	R	
		0	BSY	0	H0	R	
0x500a	T16B0INTF (T16B Ch.0 Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7–6	–	0x0	–	R	
		5	CAPOW1IF	0	H0	R/W	Cleared by writing 1.
		4	CMPCAP1IF	0	H0	R/W	
		3	CAPOW0IF	0	H0	R/W	
		2	CMPCAP0IF	0	H0	R/W	
		1	CNTMAXIF	0	H0	R/W	
		0	CNTZEROIF	0	H0	R/W	
0x500c	T16B0INTE (T16B Ch.0 Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7–6	–	0x0	–	R	
		5	CAPOW1IE	0	H0	R/W	
		4	CMPCAP1IE	0	H0	R/W	
		3	CAPOW0IE	0	H0	R/W	
		2	CMPCAP0IE	0	H0	R/W	
		1	CNTMAXIE	0	H0	R/W	
		0	CNTZEROIE	0	H0	R/W	
0x5010	T16B0CCCTL0 (T16B Ch.0 Compare/ Capture 0 Control Register)	15	SCS	0	H0	R/W	–
		14–12	CBUFMD[2:0]	0x0	H0	R/W	
		11–10	CAPIS[1:0]	0x0	H0	R/W	
		9–8	CAPTRG[1:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6	TOUTMT	0	H0	R/W	
		5	TOUTO	0	H0	R/W	
		4–2	TOUTMD[2:0]	0x0	H0	R/W	
		1	TOUTINV	0	H0	R/W	
		0	CCMD	0	H0	R/W	
0x5012	T16B0CCR0 (T16B Ch.0 Compare/ Capture 0 Data Register)	15–0	CC[15:0]	0x0000	H0	R/W	–
0x5018	T16B0CCCTL1 (T16B Ch.0 Compare/ Capture 1 Control Register)	15	SCS	0	H0	R/W	–
		14–12	CBUFMD[2:0]	0x0	H0	R/W	
		11–10	CAPIS[1:0]	0x0	H0	R/W	
		9–8	CAPTRG[1:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6	TOUTMT	0	H0	R/W	
		5	TOUTO	0	H0	R/W	
		4–2	TOUTMD[2:0]	0x0	H0	R/W	
		1	TOUTINV	0	H0	R/W	
		0	CCMD	0	H0	R/W	
0x501a	T16B0CCR1 (T16B Ch.0 Compare/ Capture 1 Data Register)	15–0	CC[15:0]	0x0000	H0	R/W	–

0x5040–0x505a 16-bit PWM Timer (T16B) Ch.1

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5040	T16B1CLK (T16B Ch.1 Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/W	
		7–4	CLKDIV[3:0]	0x0	H0	R/W	
		3	–	0	–	R	
		2–0	CLKSRC[2:0]	0x0	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5042	T16B1CTL (T16B Ch.1 Counter Control Register)	15–9	–	0x00	–	R	–
		8	MAXBSY	0	H0	R	
		7–6	–	0x0	–	R	
		5–4	CNTMD[1:0]	0x0	H0	R/W	
		3	ONEST	0	H0	R/W	
		2	RUN	0	H0	R/W	
		1	PRESET	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x5044	T16B1MC (T16B Ch.1 Max Counter Data Register)	15–0	MC[15:0]	0xffff	H0	R/W	–
0x5046	T16B1TC (T16B Ch.1 Timer Counter Data Register)	15–0	TC[15:0]	0x0000	H0	R	–
0x5048	T16B1CS (T16B Ch.1 Counter Status Register)	15–8	–	0x00	–	R	–
		7–4	–	0x0	–	R	
		3	CAPI1	0	H0	R	
		2	CAPI0	0	H0	R	
		1	UP_DOWN	1	H0	R	
		0	BSY	0	H0	R	
0x504a	T16B1INTF (T16B Ch.1 Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7–6	–	0x0	–	R	
		5	CAPOW1IF	0	H0	R/W	Cleared by writing 1.
		4	CMPCAP1IF	0	H0	R/W	
		3	CAPOW0IF	0	H0	R/W	
		2	CMPCAP0IF	0	H0	R/W	
		1	CNTMAXIF	0	H0	R/W	
		0	CNTZEROIF	0	H0	R/W	
0x504c	T16B1INTE (T16B Ch.1 Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7–6	–	0x0	–	R	
		5	CAPOW1IE	0	H0	R/W	
		4	CMPCAP1IE	0	H0	R/W	
		3	CAPOW0IE	0	H0	R/W	
		2	CMPCAP0IE	0	H0	R/W	
		1	CNTMAXIE	0	H0	R/W	
		0	CNTZEROIE	0	H0	R/W	
0x5050	T16B1CCCTL0 (T16B Ch.1 Compare/ Capture 0 Control Register)	15	SCS	0	H0	R/W	–
		14–12	CBUFMD[2:0]	0x0	H0	R/W	
		11–10	CAPIS[1:0]	0x0	H0	R/W	
		9–8	CAPTRG[1:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6	TOUTMT	0	H0	R/W	
		5	TOUTO	0	H0	R/W	
		4–2	TOUTMD[2:0]	0x0	H0	R/W	
		1	TOUTINV	0	H0	R/W	
		0	CCMD	0	H0	R/W	
0x5052	T16B1CCR0 (T16B Ch.1 Compare/ Capture 0 Data Register)	15–0	CC[15:0]	0x0000	H0	R/W	–

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5058	T16B1CCCTL1 (T16B Ch.1 Compare/ Capture 1 Control Register)	15	SCS	0	H0	R/W	–
		14–12	CBUFMD[2:0]	0x0	H0	R/W	
		11–10	CAPIS[1:0]	0x0	H0	R/W	
		9–8	CAPTRG[1:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6	TOUTMT	0	H0	R/W	
		5	TOUTO	0	H0	R/W	
		4–2	TOUTMD[2:0]	0x0	H0	R/W	
		1	TOUTINV	0	H0	R/W	
		0	CCMD	0	H0	R/W	
0x505a	T16B1CCR1 (T16B Ch.1 Compare/ Capture 1 Data Register)	15–0	CC[15:0]	0x0000	H0	R/W	–

0x5220–0x5238 Smart Card Interface (SMCIF) Ch.0

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5220	SMC0CLK (SMCIF Ch.0 Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/W	
		7–6	–	0x0	–	R	
		5–4	CLKDIV[1:0]	0x0	H0	R/W	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/W	
0x5222	SMC0MOD (SMCIF Ch.0 Mode Register)	15–8	–	0x00	–	R	–
		7	PRT	0	H0	R/W	
		6	PRY	0	H0	R/W	
		5	INV	0	H0	R/W	
		4	DIR	0	H0	R/W	
		3	–	0	–	R	
		2	OUTMD	1	H0	R/W	
		1	CLKPOL	0	H0	R/W	
		0	MST	1	H0	R/W	
0x5224	SMC0BR (SMCIF Ch.0 Baud Rate Register)	15–11	–	0x00	–	R	–
		10–0	FDR[10:0]	0x173	H0	R/W	
0x5226	SMC0CTL (SMCIF Ch.0 Control Register)	15–12	–	0x0	–	R	–
		11	ICNT	0	H0	R/W	
		10	CLKOUT	0	H0	R/W	
		9	RXEN	0	H0	R/W	
		8	TXEN	0	H0	R/W	
		7–5	–	0x0	–	R	
		4	CRP	0	H0	R/W	
		3–2	–	0x0	–	R	
		1	SFTRST	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x5228	SMC0TXD (SMCIF Ch.0 Transmit Data Register)	15–8	–	0x00	–	R	–
		7–0	TXD[7:0]	0x00	H0	R/W	
0x522a	SMC0RXD (SMCIF Ch.0 Receive Data Register)	15–9	–	0x00	–	R	–
		8	RXP	0	H0	R	
		7–0	RXD[7:0]	0x00	H0	R	
0x522c	SMC0WTC0 (SMCIF Ch.0 Wait Time Compare Data Register 0)	15–0	WTC[15:0]	0x0000	H0	R/W	–
0x522e	SMC0WTC1 (SMCIF Ch.0 Wait Time Compare Data Register 1)	15–8	–	0x00	–	R	–
		7–0	WTC[23:16]	0x00	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5230	SMC0GTC (SMCIF Ch.0 Guard Time Compare Data Register)	15–8	–	0x00	–	R	–
		7–0	GTC[7:0]	0x00	H0	R/W	
0x5232	SMC0INTF (SMCIF Ch.0 Status and Interrupt Flag Register)	15–12	–	0x0	–	R	–
		11	WTTM	0	H0/S0	R	
		10	GDTM	0	H0/S0	R	
		9	RBSY	0	H0/S0	R	
		8	TBSY	0	H0/S0	R	
		7	WTEIF	0	H0/S0	R/W	Cleared by writing 1.
		6	TENDIF	0	H0/S0	R/W	
		5	EDTIF	0	H0/S0	R/W	
		4	PEIF	0	H0/S0	R/W	
		3	OEIF	0	H0/S0	R/W	
		2	RB2FIF	0	H0/S0	R	Cleared by reading the SMC0RXD register.
		1	RB1FIF	0	H0/S0	R	
		0	TBEIF	1	H0/S0	R	Cleared by writing to the SMC0TXD register.
0x5234	SMC0INTE (SMCIF Ch.0 Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7	WTEIE	0	H0	R/W	
		6	TENDIE	0	H0	R/W	
		5	EDTIE	0	H0	R/W	
		4	PEIE	0	H0	R/W	
		3	OEIE	0	H0	R/W	
		2	RB2FIE	0	H0	R/W	
		1	RB1FIE	0	H0	R/W	
		0	TBEIE	0	H0	R/W	
0x5236	SMC0ETU0 (SMCIF Ch.0 Etu Counter Data Register 0)	15–0	ETUC[15:0]	0xffff	H0/S0	R	–
0x5238	SMC0ETU1 (SMCIF Ch.0 Etu Counter Data Register 1)	15–8	–	0x00	–	R	–
		7–0	ETUC[23:16]	0xff	H0/S0	R	

0x5260–0x526c 16-bit Timer (T16) Ch.3

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5260	T16_3CLK (T16 Ch.3 Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/W	
		7–4	CLKDIV[3:0]	0x0	H0	R/W	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/W	
0x5262	T16_3MOD (T16 Ch.3 Mode Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	TRMD	0	H0	R/W	
0x5264	T16_3CTL (T16 Ch.3 Control Register)	15–9	–	0x00	–	R	–
		8	PRUN	0	H0	R/W	
		7–2	–	0x00	–	R	
		1	PRESET	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x5266	T16_3TR (T16 Ch.3 Reload Data Register)	15–0	TR[15:0]	0xffff	H0	R/W	–
0x5268	T16_3TC (T16 Ch.3 Counter Data Register)	15–0	TC[15:0]	0xffff	H0	R	–

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x526a	T16_3INTF (T16 Ch.3 Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	UFIF	0	H0	R/W	Cleared by writing 1.
0x526c	T16_3INTE (T16 Ch.3 Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	UFIE	0	H0	R/W	

0x5270–0x527a Synchronous Serial Interface (SPIA) Ch.1

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5270	SPI1MOD (SPIA Ch.1 Mode Register)	15–12	–	0x0	–	R	–
		11–8	CHLN[3:0]	0x7	H0	R/W	
		7–6	–	0x0	–	R	
		5	PUEN	0	H0	R/W	
		4	NOCLKDIV	0	H0	R/W	
		3	LSBFST	0	H0	R/W	
		2	CPHA	0	H0	R/W	
		1	CPOL	0	H0	R/W	
		0	MST	0	H0	R/W	
0x5272	SPI1CTL (SPIA Ch.1 Control Register)	15–8	–	0x00	–	R	–
		7–2	–	0x00	–	R	
		1	SFTRST	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x5274	SPI1TXD (SPIA Ch.1 Transmit Data Register)	15–0	TXD[15:0]	0x0000	H0	R/W	–
0x5276	SPI1RXD (SPIA Ch.1 Receive Data Register)	15–0	RXD[15:0]	0x0000	H0	R	–
0x5278	SPI1INTF (SPIA Ch.1 Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7	BSY	0	H0	R	
		6–4	–	0x0	–	R	
		3	OEIF	0	H0/S0	R/W	Cleared by writing 1.
		2	TENDIF	0	H0/S0	R/W	
		1	RBFIF	0	H0/S0	R	Cleared by reading the SPI1RXD register.
		0	TBEIF	1	H0/S0	R	Cleared by writing to the SPI1TXD register.
0x527a	SPI1INTE (SPIA Ch.1 Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7–4	–	0x0	–	R	
		3	OEIE	0	H0	R/W	
		2	TENDIE	0	H0	R/W	
		1	RBFIE	0	H0	R/W	
		0	TBEIE	0	H0	R/W	

0x5300–0x530a Sound Generator (SNDA)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5300	SNDCLK (SNDA Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/W	
		7	–	0	–	R	
		6–4	CLKDIV[2:0]	0x0	H0	R/W	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/W	
0x5302	SNDSEL (SNDA Select Register)	15–12	–	0x0	–	R	–
		11–8	STIM[3:0]	0x0	H0	R/W	
		7–3	–	0x00	–	R	
		2	SINV	0	H0	R/W	
		1–0	MOSEL[1:0]	0x0	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5304	SNDCTL (SNDA Control Register)	15–9	–	0x00	–	R	–
		8	SSTP	0	H0	R/W	
		7–1	–	0x00	–	R	
		0	MODEN	0	H0	R/W	
0x5306	SNDDAT (SNDA Data Register)	15	MDTI	0	H0	R/W	–
		14	MDRS	0	H0	R/W	
		13–8	SLEN[5:0]	0x00	H0	R/W	
		7–0	SFRQ[7:0]	0xff	H0	R/W	
0x5308	SNDINTF (SNDA Interrupt Flag Register)	15–9	–	0x00	–	R	–
		8	SBSY	0	H0	R	
		7–2	–	0x00	–	R	
		1	EMIF	1	H0	R	Cleared by writing to the SNDDAT register.
		0	EDIF	0	H0	R/W	Cleared by writing 1 or writing to the SNDDAT register.
0x530a	SNDINTE (SNDA Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7–2	–	0x00	–	R	
		1	EMIE	0	H0	R/W	
		0	EDIE	0	H0	R/W	

0x5480–0x548c 16-bit Timer (T16) Ch.2

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5480	T16_2CLK (T16 Ch.2 Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/W	
		7–4	CLKDIV[3:0]	0x0	H0	R/W	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/W	
0x5482	T16_2MOD (T16 Ch.2 Mode Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	TRMD	0	H0	R/W	
0x5484	T16_2CTL (T16 Ch.2 Control Register)	15–9	–	0x00	–	R	–
		8	PRUN	0	H0	R/W	
		7–2	–	0x00	–	R	
		1	PRESET	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x5486	T16_2TR (T16 Ch.2 Reload Data Register)	15–0	TR[15:0]	0xffff	H0	R/W	–
0x5488	T16_2TC (T16 Ch.2 Counter Data Register)	15–0	TC[15:0]	0xffff	H0	R	–
0x548a	T16_2INTF (T16 Ch.2 Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	UFIF	0	H0	R/W	Cleared by writing 1.
0x548c	T16_2INTE (T16 Ch.2 Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	UFIE	0	H0	R/W	

0x54a0–0x54ba 12-bit A/D Converter (ADC12A)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x54a2	ADC12_0CTL (ADC12A Ch.0 Control Register)	15	–	0	–	R	–
		14–12	ADSTAT[2:0]	0x0	H0	R	
		11	–	0	–	R	
		10	BSYSTAT	0	H0	R	
		9–8	–	0x0	–	R	
		7–2	–	0x00	–	R	
		1	ADST	0	H0	R/W	
		0	MODEN	0	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x54a4	ADC12_0TRG (ADC12A Ch.0 Trigger/Analog Input Select Register)	15–14	–	0x0	–	R	–
		13–11	ENDAIN[2:0]	0x0	H0	R/W	
		10–8	STAAIN[2:0]	0x0	H0	R/W	
		7	STMD	0	H0	R/W	
		6	CNVMD	0	H0	R/W	
		5–4	CNVTRG[1:0]	0x0	H0	R/W	
		3	–	0	–	R	
		2–0	SMPCLK[2:0]	0x7	H0	R/W	
0x54a6	ADC12_0CFG (ADC12A Ch.0 Configuration Register)	15–8	–	0x00	–	R	–
		7–2	–	0x00	–	R	
		1–0	VRANGE[1:0]	0x0	H0	R/W	
0x54a8	ADC12_0INTF (ADC12A Ch.0 Interrupt Flag Register)	15	AD7OVIF	0	H0	R/W	Cleared by writing 1.
		14	AD6OVIF	0	H0	R/W	
		13	AD5OVIF	0	H0	R/W	
		12	AD4OVIF	0	H0	R/W	
		11	AD3OVIF	0	H0	R/W	
		10	AD2OVIF	0	H0	R/W	
		9	AD1OVIF	0	H0	R/W	
		8	AD0OVIF	0	H0	R/W	
		7	AD7CIF	0	H0	R/W	
		6	AD6CIF	0	H0	R/W	
		5	AD5CIF	0	H0	R/W	
		4	AD4CIF	0	H0	R/W	
		3	AD3CIF	0	H0	R/W	
		2	AD2CIF	0	H0	R/W	
		1	AD1CIF	0	H0	R/W	
		0	AD0CIF	0	H0	R/W	
0x54aa	ADC12_0INTE (ADC12A Ch.0 Interrupt Enable Register)	15	AD7OVIE	0	H0	R/W	–
		14	AD6OVIE	0	H0	R/W	
		13	AD5OVIE	0	H0	R/W	
		12	AD4OVIE	0	H0	R/W	
		11	AD3OVIE	0	H0	R/W	
		10	AD2OVIE	0	H0	R/W	
		9	AD1OVIE	0	H0	R/W	
		8	AD0OVIE	0	H0	R/W	
		7	AD7CIE	0	H0	R/W	
		6	AD6CIE	0	H0	R/W	
		5	AD5CIE	0	H0	R/W	
		4	AD4CIE	0	H0	R/W	
		3	AD3CIE	0	H0	R/W	
		2	AD2CIE	0	H0	R/W	
		1	AD1CIE	0	H0	R/W	
		0	AD0CIE	0	H0	R/W	
0x54ac	ADC12_0AD0D (ADC12A Ch.0 Result Register 0)	15–0	AD0D[15:0]	0x0000	H0	R	–
0x54ae	ADC12_0AD1D (ADC12A Ch.0 Result Register 1)	15–0	AD1D[15:0]	0x0000	H0	R	–
0x54b0	ADC12_0AD2D (ADC12A Ch.0 Result Register 2)	15–0	AD2D[15:0]	0x0000	H0	R	64-pin PKG only
0x54b2	ADC12_0AD3D (ADC12A Ch.0 Result Register 3)	15–0	AD3D[15:0]	0x0000	H0	R	–
0x54b4	ADC12_0AD4D (ADC12A Ch.0 Result Register 4)	15–0	AD4D[15:0]	0x0000	H0	R	–

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x54b6	ADC12_0AD5D (ADC12A Ch.0 Result Register 5)	15–0	AD5D[15:0]	0x0000	H0	R	–
0x54b8	ADC12_0AD6D (ADC12A Ch.0 Result Register 6)	15–0	AD6D[15:0]	0x0000	H0	R	–
0x54ba	ADC12_0AD7D (ADC12A Ch.0 Result Register 7)	15–0	AD7D[15:0]	0x0000	H0	R	–

0x54c0–0x54c2 Temperature Sensor/Reference Voltage Generator (TSRVR)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x54c0	TSRVR0TCTL (TSRVR Ch.0 Temperature Sensor Control Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	H0	R	
		0	TEMPEN	0	H0	R/W	
0x54c2	TSRVR0VCTL (TSRVR Ch.0 Reference Voltage Generator Control Register)	15–8	–	0x00	–	R	–
		7–2	–	0x00	H0	R	
		1–0	VREFAMD[1:0]	0x0	H0	R/W	

0x5500–0x557e EPD Controller/Driver (EPDC)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5500	EPDTIMCLK (EPDC Timing Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	1	H0	R/W	
		7	–	0	–	R	
		6–4	CLKDIV[2:0]	0x0	H0	R/W	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/W	
0x5502	EPDDBLCLK (EPDC Doubler Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	1	H0	R/W	
		7	–	0	–	R	
		6–4	CLKDIV[2:0]	0x0	H0	R/W	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/W	
0x5504	EPDBSTCLK (EPDC Booster Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	1	H0	R/W	
		7	–	0	–	R	
		6–4	CLKDIV[2:0]	0x0	H0	R/W	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/W	
0x5506	EPDCTL (EPDC Control Register)	15–8	–	0x00	–	R	–
		7–2	–	0x00	–	R	
		1	DIS	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x5508	EPDPWR0 (EPDC Power Supply Control Register 0)	15–10	–	0x00	–	R	–
		9	DBSRT	0	H0	R/W	
		8	DBON	0	H0	R/W	
		7–4	VECONT[3:0]	0x0	H0	R/W	
		3	–	0	–	R	
		2	HVLDVE	0	H0	R/W	
		1	VESEL	0	H0	R/W	
		0	VEON	0	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x550a	EPDPWR1 (EPDC Power Supply Control Register 1)	15–12	HVDCONT[3:0]	0x0	H0	R/W	–
		11–10	HVDSEL[1:0]	0x0	H0	R/W	
		9	HVLDHVD	0	H0	R/W	
		8	HVDON	0	H0	R/W	
		7–2	–	0x00	–	R	
		1	BSTPLD	0	H0	R/W	
		0	BSTON	0	H0	R/W	
0x550c	EPDDSP (EPDC Display Control Register)	15–8	–	0x00	–	R	–
		7–6	–	0x0	–	R	
		5	SELCUR	0	H0	R/W	
		4	DIRCTL	0	H0	R/W	
		3–2	DSPMD[1:0]	0x0	H0	R/W	
		1	–	0	–	R	
		0	UPDTRG	0	H0	W	
0x550e	EPDPOS (EPDC Pin Assignment Select Register)	15–8	–	0x00	–	R	–
		7–2	–	0x00	–	R	
		1–0	PINPOS[1:0]	0x0	H0	R/W	
0x5510	EPDINTF (EPDC Interrupt Flag/ Status Register)	15–9	–	0x00	–	R	–
		8	UPDST	0	H0	R	
		7–1	–	0x00	–	R	
		0	DUPDIF	0	H0	R/W	Cleared by writing 1.
0x5512	EPDINTE (EPDC Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	DUPDIE	0	H0	R/W	
0x5520	EPDTPBP (EPDC Top/Back Plane Data Register)	15–10	–	0x00	–	R	–
		9	SEGHZ	0	H0	R/W	Effective only in direct mode
		8	TPHZ	0	H0	R/W	–
		7–5	–	0x0	–	R	
		4	TP	0	H0	R/W	Effective only in direct mode
		3–1	–	0x0	–	R	–
		0	BP	0	H0	R/W	
0x5522	EPDSEG0 (EPDC Segment Data Register 0)	15–0	SEG[15:0]	0x0000	H0	R/W	–
0x5524	EPDSEG1 (EPDC Segment Data Register 1)	15–0	SEG[31:16]	0x0000	H0	R/W	–
0x5526	EPDSEG2 (EPDC Segment Data Register 2)	15–10	–	0x00	–	R	–
		9–0	SEG[41:32]	0x00	H0	R/W	
0x5530	EPDTPBPEN (EPDC Top/Back Plane Enable Register)	15–8	–	0x00	–	R	–
		7–5	–	0x0	–	R	
		4	TPEN	1	H0	R/W	
		3–1	–	0x0	–	R	
		0	BPEN	1	H0	R/W	
0x5532	EPDSEGEN0 (EPDC Segment Enable Register 0)	15–0	SEG[15:0]EN	0x0000	H0	R/W	–
0x5534	EPDSEGEN1 (EPDC Segment Enable Register 1)	15–0	SEG[31:16]EN	0x0000	H0	R/W	–
0x5536	EPDSEGEN2 (EPDC Segment Enable Register 2)	15–10	–	0x00	–	R	–
		9–0	SEG[41:32]EN	0x00	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5540	EPDWAVE0	15	EOW	0	H0	R/W	–
|	(EPDC Waveform	14	–	0	–	R	
0x557e	Timing Set Register 0)	13	HIZ	0	H0	R/W	
	|	12	TP	0	H0	R/W	
	EPDWAVE31	11	BB	0	H0	R/W	
	(EPDC Waveform	10	BW	0	H0	R/W	
	Timing Set Register 31)	9	WB	0	H0	R/W	
		8	WW	0	H0	R/W	
		7–0	INTV[7:0]	0x00	H0	R/W	

0xffff90 Debugger (DBG)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0xffff90	DBRAM	31–24	–	0x00	–	R	–
	(Debug RAM Base Register)	23–0	DBRAM[23:0]	0x00 07c0	H0	R	

Appendix B Power Saving

Current consumption will vary dramatically, depending on CPU operating mode, operation clock frequency, peripheral circuits being operated, and power generator operating mode. Listed below are the control methods for saving power.

B.1 Operating Status Configuration Examples for Power Saving

Table B.1.1 lists typical examples of operating status configuration with consideration given to power saving.

Table B.1.1 Typical Operating Status Configuration Examples

Operating status configuration	Current consumption	V_{D1}	OSC1	IOSC/ OSC3/ EXOSC	Real-time clock	CPU	Current consumption listed in electrical characteristics
Standby	↑		OFF		OFF	SLEEP	I_{SLP}
Clock counting	Low	Economy		OFF		SLEEP or HALT	I_{HALT2}
Low-speed processing						RTCLPCLK RUN	I_{RUN2}
Peripheral circuit operations			ON		ON	SLEEP or HALT	I_{HALT1}
High-speed processing	High	Normal		ON		IOSC/OSC3/EXOSC RUN	I_{RUN1}
	↓						

If the current consumption order by the operating status configuration shown in Table B.1.1 is different from one that is listed in "Electrical Characteristics," check the settings shown below.

PWGVD1CTL.REGMODE[1:0] bits of the power generator

If the PWGVD1CTL.REGMODE[1:0] bits of the power generator is 0x2 (normal mode) when the CPU enters SLEEP mode, current consumption in SLEEP mode will be larger than I_{SLP} that is listed in "Electrical Characteristics." Set the PWGVD1CTL.REGMODE[1:0] bits to 0x3 (economy mode) or 0x0 (automatic mode) before executing the slp instruction.

CLGOSC.IOSCSLPC/OSC1SLPC/OSC3SLPC/EXOSCSLPC bits of the clock generator

Setting the CLGOSC.IOSCSLPC, OSC1SLPC, OSC3SLPC, or EXOSCSLPC bit of the clock generator to 0 disables the oscillator circuit stop control when the slp instruction is executed. To stop the oscillator circuits during SLEEP mode, set these bits to 1.

MODEN bits of the peripheral circuits

Setting the MODEN bit of each peripheral circuit to 1 starts supplying the operating clock enabling the peripheral circuit to operate. To reduce current consumption, set the MODEN bits of unnecessary peripheral circuits to 0. Note that the real-time clock has no MODEN bit, therefore, current consumption does not vary if it is counting or idle.

B.2 Other Power Saving Methods

Supply voltage detector configuration

Continuous operation mode (SVDCTL.SVDMD[1:0] bits = 0x0) always detects the power supply voltage, therefore, it increases current consumption. Set the supply voltage detector to intermittent operation mode or turn it on only when required.

EPD power supply circuit

- When generating V_{E1} by the V_E regulator (EPDPWR0.VESEL bit = 0), current consumption will increase. If the power supply voltage V_{DD} is in the range that allows it to generate V_{E2}, generate V_{E2} (EPDPWR0.VESEL bit = 1) and turn the doubler off (EPDPWR0.DBON bit = 0).
- Turning on the EPD power supply heavy load protection will increase current consumption. The heavy load protection function should be turned on only when the display is unstable, otherwise it should be turned off.
- If no EPD driving is required, turn off the EPD power supply.

Appendix C Mounting Precautions

This section describes various precautions for circuit board design and IC mounting.

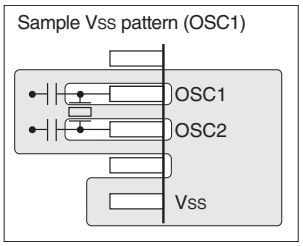
OSC1/OSC3 oscillator circuit

- Oscillation characteristics depend on factors such as components used (resonator, CG, CD) and circuit board patterns. In particular, with crystal resonators, select the appropriate capacitors (CG, CD) only after fully evaluating components actually mounted on the circuit board.
- Oscillator clock disturbances caused by noise may cause malfunctions. To prevent such disturbances, consider the following points.

(1) Components such as a resonator, resistors, and capacitors connected to the OSC1 and OSC2 pins should have the shortest connections possible.

(2) Wherever possible, avoid locating digital signal lines within 3 mm of the OSC1 and OSC2 pins or related circuit components and wiring. Rapidly-switching signals, in particular, should be kept at a distance from these components. Since the spacing between layers of multi-layer printed circuit boards is a mere 0.1 mm to 0.2 mm, the above precautions also apply when positioning digital signal lines on other layers.
Never place digital signal lines alongside such components or wiring, even if more than 3 mm distance or located on other layers. Avoid crossing wires.

(3) Use VSS to shield the OSC1 and OSC2 pins and related wiring (including wiring for adjacent circuit board layers). Layers wired should be adequately shielded as shown to the right. Fully ground adjacent layers, where possible. At minimum, shield the area at least 5 mm around the above pins and wiring.
Even after implementing these precautions, avoid configuring digital signal lines in parallel, as described in (2) above. Avoid crossing even on discrete layers, except for lines carrying signals with low switching frequencies.



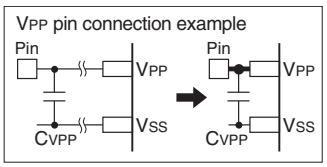
(4) After implementing these precautions, check the FOUT pin output clock waveform by running the actual application program within the product.
For the OSC1 waveform, enlarge the areas before and after the clock rising and falling edges and take special care to confirm that the regions approximately 100 ns to either side are free of clock or spiking noise.
Failure to observe precautions (1) to (3) adequately may lead to noise in RTCLPCLK and it may destabilize timers that use RTCLPCLK as well as CPU core operations.

#RESET pin

Components such as a switch and resistor connected to the #RESET pin should have the shortest connections possible to prevent noise-induced resets.

VPP pin

Connect a capacitor CVPP between the VSS and VPP pins to suppress fluctuations within VPP ± 1 V. The CVPP should be placed as close to the VPP pin as possible and use a sufficiently thick wiring pattern that allows current of several tens of mA to flow.

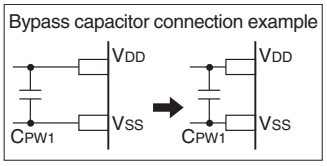


Power supply circuit

Sudden power supply fluctuations due to noise will cause malfunctions. Consider the following issues.

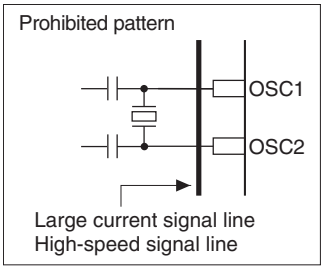
(1) Connections from the power supply to the VDD and VSS pins should be implemented via the shortest, thickest patterns possible.

(2) If a bypass capacitor is connected between VDD and VSS, connections between the VDD and VSS pins should be as short as possible.



Signal line location

- To prevent electromagnetically-induced noise arising from mutual induction, large-current signal lines should not be positioned close to pins susceptible to noise, such as oscillator and analog measurement pins.
- Locating signal lines in parallel over significant distances or crossing signal lines operating at high speed will cause malfunctions due to noise generated by mutual interference.



Handling of light (for bare chip mounting)

The characteristics of semiconductor components can vary when exposed to light. ICs may malfunction or nonvolatile memory data may be corrupted if ICs are exposed to light.
Consider the following precautions for circuit boards and products in which this IC is mounted to prevent IC malfunctions attributable to light exposure.

(1) Design and mount the product so that the IC is shielded from light during use.

(2) Shield the IC from light during inspection processes.

(3) Shield the IC on the upper, underside, and side faces of the IC chip.

(4) Mount the IC chip within one week of opening the package. If the IC chip must be stored before mounting, take measures to ensure light shielding.

(5) Adequate evaluations are required to assess nonvolatile memory data retention characteristics before product delivery if the product is subjected to heat stress exceeding regular reflow conditions during mounting processes.

Unused pins

(1) I/O port (P) pins
Unused pins should be left open. The control registers should be fixed at the initial status.

(2) EXOSC pin
If the EXOSC input circuit is not used, the pin should be configured as a general-purpose I/O port. The control registers should be fixed at the initial status (disabled).

(3) V_{E1-5}, V_{EPD}, C_{D1}, C_{D2}, C_{B1}–C_{B4}, ESEG*x*, ETP0, and EBP0 pins
If the EPD controller/driver is not used, these pins should be left open. The control registers should be fixed at the initial status (display off). The unused ESEG*x* pins that are not required to connect should be left open even if the EPD controller/driver is used.

Handling gold bump chip products (subjecting to high temperature stress)

If an IC is subjected to high temperature stress such as when a gold bump chip is mounted on COF, the internal Flash memory characteristics may vary. Confirm the heat conditions (temperature and time) for mounting using the table below. If any of the "Data reprogramming required" conditions apply, be sure to reprogram the Flash memory using the corresponding fls program or the standalone Flash programmer. For details of the fls program or the standalone Flash programmer, refer to the respective manual.

Time / Temperature	Not affected to Flash memory	Affected to Flash memory	
		Data reprogramming required	Allowable time
Lower than 250°C	≤ 5 hours	5 hours to 450 hours	Max. 450 hours
250°C to 300°C	≤ 400 seconds	400 seconds to 10 hours	Max. 10 hours
300°C to 350°C	≤ 20 seconds	20 seconds to 0.5 hour	Max. 0.5 hour
350°C to 400°C	≤ 1 second	1 second to 100 seconds	Max. 100 seconds
400°C to 450°C	≤ 0.1 second	0.1 second to 10 seconds	Max. 10 seconds
Higher than 450°C			Max. 0 seconds

Miscellaneous

Minor variations over time may result in electrical damage arising from disturbances in the form of voltages exceeding the absolute maximum rating when mounting the product in addition to physical damage. The following factors can give rise to these variations:

(1) Electromagnetically-induced noise from industrial power supplies used in mounting reflow, reworking after mounting, and individual characteristic evaluation (testing) processes
(2) Electromagnetically-induced noise from a solder iron when soldering

In particular, during soldering, take care to ensure that the soldering iron GND (tip potential) has the same potential as the IC GND.

Appendix D Measures Against Noise

To improve noise immunity, take measures against noise as follows:

Noise Measures for V_{DD} and V_{SS} Power Supply Pins

When noise falling below the rated voltage is input, an IC malfunction may occur. If desired operations cannot be achieved, take measures against noise on the circuit board, such as designing close patterns for circuit board power supply circuits, adding noise-filtering decoupling capacitors, and adding surge/noise prevention components on the power supply line.
For the recommended patterns on the circuit board, see "Mounting Precautions" in Appendix.

Noise Measures for #RESET Pin

If noise is input to the #RESET pin, the IC may be reset. Therefore, the circuit board must be designed properly taking noise measures into consideration.
For the recommended patterns on the circuit board, see "Mounting Precautions" in Appendix.

Noise Measures for Oscillator Pins

The oscillator input pins must pass a signal of small amplitude, so they are hypersensitive to noise. Therefore, the circuit board must be designed properly taking noise measures into consideration.
For the recommended patterns on the circuit board, see "Mounting Precautions" in Appendix.

Noise Measures for Debug Pins

This product provides the input/output pins (DCLK, DST2, and DSIO) to connect ICDmini (S5U1C17001H) for debugging. If noise is input to these pins with the debugging function enabled, the S1C17 Core may enter DEBUG mode. To prevent unexpected transitions to DEBUG mode caused by extraneous noise, switch the DCLK, DST2, and DSIO pins to general-purpose I/O port pins within the initialization routine when the debug functions are not used.
For details of the pin functions and the function switch control, see the "I/O Ports" chapter.

Note: Do not perform the function switching shown above when the application is under development, as the debug functions must be used. The debugging cannot be performed after the pin function is switched. The above processing must be added after the application development has completed and debugging is no longer necessary.

The DSIO pin should be pulled up with a 10 kΩ resistor when using the debug pin functions.

Noise Measures for Interrupt Input Pins

This product is able to generate a port input interrupt when the input signal changes. The interrupt is generated when an input signal edge is detected, therefore, an interrupt may occur if the signal changes due to extraneous noise. To prevent occurrence of unexpected interrupts due to extraneous noise, enable the chattering filter circuit when using the port input interrupt.
For details of the port input interrupt and chattering filter circuit, see the "I/O Ports" chapter.

Noise Measures for UART Pins

This product includes a UART for asynchronous communications. The UART starts receive operation when it detects a low level input from the SIN*n* pin. Therefore, a receive operation may be started if the SIN*n* pin is set to low due to extraneous noise. In this case, a receive error will occur or invalid data will be received.
To prevent the UART from malfunction caused by extraneous noise, take the following measures:

- Stop the UART operations while asynchronous communication is not performed.
- Execute the resending process via software after executing the receive error handler with a parity check.

For details of the pin functions and the function switch control, see the "I/O Ports" chapter. For the UART control and details of receive errors, see the "UART" chapter.

Noise Measures for Input Pins Connected to Signal with High Driving Capability Such As Power Supply

There is a possibility of a large current flow into the pins that are directly connected to a power supply or an output of a device with high driving capability if noise is input to those pins. To prevent this, connect a 30 Ω or more pin protection resistor to the pins in series. The resistance value should be determined by evaluating it on the mounting board.

When connecting a power supply directly to the VREFA pin, insert a 100 Ω resistor in series. This resistance does not affect the A/D converter characteristics.

Appendix E Initialization Routine

The following lists typical vector tables and initialization routines:

boot.s

```
.org    0x8000
.section .rodata                                                          ...(1)

; ======================================================================
;       Vector table
; ======================================================================
                                ; interrupt  vector  interrupt
                                ; number     offset  source

.long BOOT                      ; 0x00       0x00    reset                ...(2)
.long unalign_handler           ; 0x01       0x04    unalign
.long nmi_handler               ; 0x02       0x08    NMI
.long int03_handler             ; 0x03       0x0c    -
.long svd3_handler              ; 0x04       0x10    SVD3
.long pport_handler             ; 0x05       0x14    PPORT
.long int06_handler             ; 0x06       0x18    -
.long clg_handler               ; 0x07       0x1c    CLG
.long rtcb_handler              ; 0x08       0x20    RTCB
.long t16_0_handler             ; 0x09       0x24    T16 ch0
.long uart3_0_handler           ; 0x0a       0x28    UART3 ch0
.long t16_1_handler             ; 0x0b       0x2c    T16 ch1
.long spia_0_handler            ; 0x0c       0x30    SPIA ch0
.long i2c_handler               ; 0x0d       0x34    I2C
.long t16b_0_handler            ; 0x0e       0x38    T16B ch0
.long t16b_1_handler            ; 0x0f       0x3c    T16B ch1
.long smcif_0_handler           ; 0x10       0x40    SMCIF ch0
.long snda_handler              ; 0x11       0x44    SNDA
.long t16_2_handler             ; 0x12       0x48    T16 ch2
.long adc12a_handler            ; 0x13       0x4c    ADC12A
.long epdc_handler              ; 0x14       0x50    EPDC
.long eepromc_handler           ; 0x15       0x54    EEPROMC
.long int16_handler             ; 0x16       0x58    -
.long int17_handler             ; 0x17       0x5c    -
.long int18_handler             ; 0x18       0x60    -
.long int19_handler             ; 0x19       0x64    -
.long int1a_handler             ; 0x1a       0x68    -
.long int1b_handler             ; 0x1b       0x6c    -
.long int1c_handler             ; 0x1c       0x70    -
.long int1d_handler             ; 0x1d       0x74    -
.long int1e_handler             ; 0x1e       0x78    -
.long int1f_handler             ; 0x1f       0x7c    -
; ======================================================================
;       Program code
; ======================================================================

.text                                                                     ...(3)
.align 1

BOOT:
        ; ===== Initialize ============================================

        ; ----- Stack pointer --------------------
        Xld.a   %sp, 0x7c0                                                ...(4)

        ; ----- Memory controller ----------------
        Xld.a   %r1, 0x41b0     ; FLASHC register address

        ; Flash read wait cycle
        Xld.a   %r0, 0x00       ; 0x00 = No wait
        ld.b    [%r1], %r0      ; [0x41b0] <= 0x00                        ...(5)

        ; ===== Main routine ==========================================
         ...
```

```
; ========================================================================
;       Interrupt handler
; ========================================================================
; ----- Address unalign --------------------------
unalign_handler:
        ...

; ----- NMI --------------------------------------
nmi_handler:
        ...
```

(1) A ".rodata" section is declared to locate the vector table in the ".vector" section.

(2) Interrupt handler routine addresses are defined as vectors.
"int*XX*_handler" can be used for software interrupts.

(3) The program code is written in the ".text" section.

(4) Sets the stack pointer.

(5) Sets the number of Flash memory read cycles.
(See the "Memory and Bus" chapter.)

Revision History

Code No.	Page	Contents
413942900	All	New establishment
413942901	1-2 to 3	1.1 Features Added the following annotations to Table 1.1.1. I²C (I2C) *1 *1 The input filter in I2C (SDA and SCL inputs) does not comply with the standard for removing noise spikes less than 50 ns. SLEEP mode *2 *2 The RAM retains data even in SLEEP mode. Modified Table 1.1.1. RTCLP: An item (Backup RAM function) was added. Power supply voltage: VDD operating voltage for EEPROM programming 2.7 to 5.5 V → 2.2 to 5.5 V Shipping form: A JEITA name was added to the package name.
	1-4	1.2 Block Diagram Modified Figure 1.2.1. The backup RAM capacity was changed.
	2-11	2.4.2 Transition between Operating Modes SLEEP mode Added the following description: The RAM retains data even in SLEEP mode.
	4-3	4.4.1 EEPROM pin Added the following description: The notes described in Section 4.3.3 are also applied to EEPROM reprogramming. Deleted the notes. ~~Notes: • When programming the EEPROM, 2.7 V or more VDD voltage is required.~~ ~~• Be sure to avoid using the VPP pin output for driving external circuits when the VPP voltage is generated internally.~~
	13-1	13.1 Overview Added the following description: • The input filter for the SDA and SCL inputs does not comply with the standard for removing noise spikes less than 50 ns.
	21-1	21.1 Overview Corrected the description. • Includes a 128-byte backup RAM. Modified Figure 21.1.1. SPI slave 2 was deleted.
	21-3	21.4.1 Accessing the RTCLP Registers Corrected the description. The RTCLP works as two SPI slave devices (SPI slaves 0 and 1) connected to the synchronous serial interface (SPIA Ch.0) of this MCU. ... SPI slave selector (SPISLV_SEL) The SPI slave selector (SPISLV_SEL) exists in the peripheral circuit area of the MCU core to select an SPI slave device (0 or 1). Modified Table 21.4.1.1. SPI slave No. 2 (Backup RAM 1) was deleted.
	21-6	21.4.2 Real-Time Clock Function Corrective operation when a value out of the effective range is set Added a note. Note: Do not set the RTCMON.RTCMOL[3:0] bits to 0x0 if the RTCMON.RTCMOH bit = 0.
	21-11	21.4.10 Backup RAM Function • Capacity: 256 bytes → 128 bytes • Address: SPI slave 2 was deleted.
	21-13	21.6 Control Registers Modified Table 21.4.1.2. SPISLVSEL.SLV[2:0] bits = 0b100 → Setting prohibited
	21-20	21.6 Control Registers RTC Month Register Bit 4 RTCMOH Bits 3–0 RTCMOL[3:0] Added a note. Notes: ... • Be sure to avoid setting the RTCMON.RTCMOH/RTCMOL[3:0] bits to 0x00.

REVISION HISTORY

Code No.	Page	Contents
413942901	22-1	22.2 Recommended Operating Conditions Added "(V_{SS} = 0 V) ∗1" and the following annotations: ∗1 The potential variation of the V_{SS} voltage should be suppressed to within ±0.3 V on the basis of the ground potential of the MCU mounting board while the Flash is being programmed, as it affects the Flash memory characteristics (programming count). ∗6 The component values should be determined after evaluating operations using an actual mounting board. Modified the characteristics table. V_{DD}: Min. = 2.7 → 2.2 V, For EEPROM programming (When V_{PP} is generated internally)
	22-6	22.6 Flash Memory Characteristics Added an annotation. ∗1 The potential variation of the V_{SS} voltage should be suppressed to within ±0.3 V on the basis of the ground potential of the MCU mounting board while the Flash is being programmed, as it affects the Flash memory characteristics (programming count).
	23-1	23 Basic External Connection Diagram Modified the figure. V_{DD} = 2.7–5.5 V and ∗2 were delete. Annotation ∗1 was corrected. ∗1: For Flash/EEPROM programming
	24-1	24 Package A JEITA name was added to the package name.
	AP-D-2	Appendix D Measures Against Noise Added a description. Noise Measures for Input Pins Connected to Signal with High Driving Capability Such As Power Supply

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