CMOS 32-BIT SINGLE CHIP MICROCONTROLLER

S5U1C31001L1100
(Bridge Board)
Manual

Rev.1.1

Evaluation board/kit and Development tool important notice

1. This evaluation board/kit or development tool is designed for use for engineering evaluation, demonstration, or development purposes only. Do not use it for other purposes. It is not intended to meet the requirements of design for finished products.
2. This evaluation board/kit or development tool is intended for use by an electronics engineer and is not a consumer product. The user should use it properly and in a safe manner. Seiko Epson dose not assume any responsibility or liability of any kind of damage and/or fire coursed by the use of it. The user should cease to use it when any abnormal issue occurs even during proper and safe use.
3. The part used for this evaluation board/kit or development tool may be changed without any notice.

NOTICE

Table of Contents

1. Overview

The S5U1C31001L1100 (Bridge Board) is used by inserting between the user target board and a debug probe either I-jet manufactured by IAR or J-Link manufactured by SEGGER.

The embedded flash memory of Seiko Epson S1C31 Family MCUs requires a 7.5 V power supply exclusive use for high-speed programming that cannot be generated by general-purpose debug probes. The S5U1C31001L1100 (Bridge Board) generates a 7.5 V flash programming voltage from the 5 V power voltage supplied by a general-purpose debug probe and supplies it to the user target board.

If the target S1C32 Family MCU includes a voltage booster and is being used for flash programming, it is not necessary to use the S5U1C31001L1100 (Bridge Board).
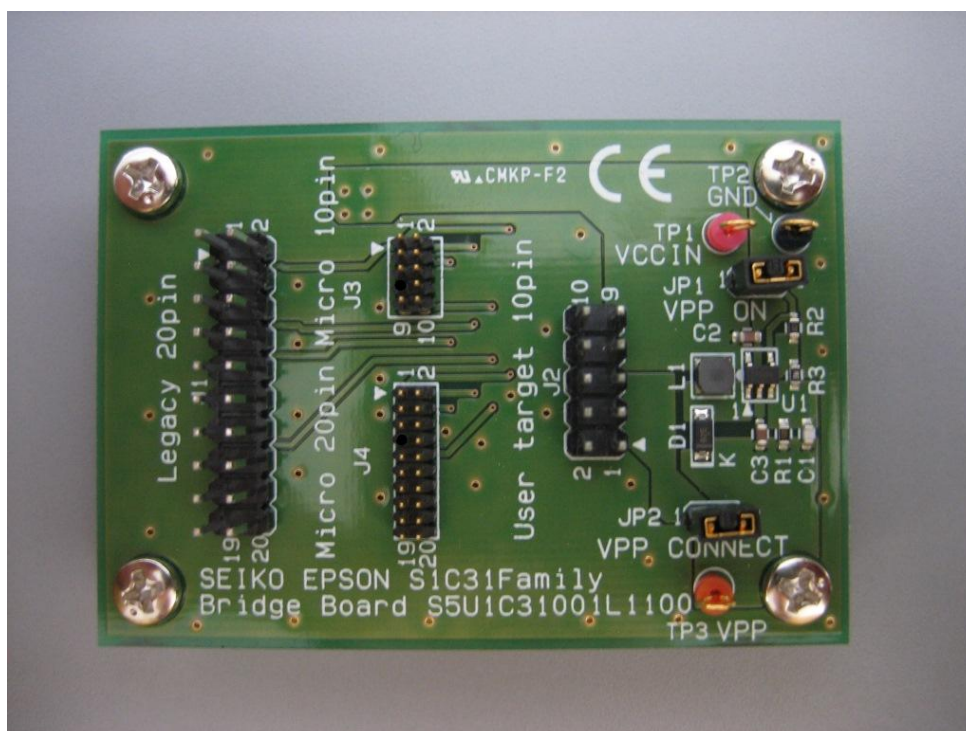
Figure 1.1   S5U1C31001L1100 (Bridge Board) External View

2. Connection Examples

When J-Link (20-pin legacy connector) is used
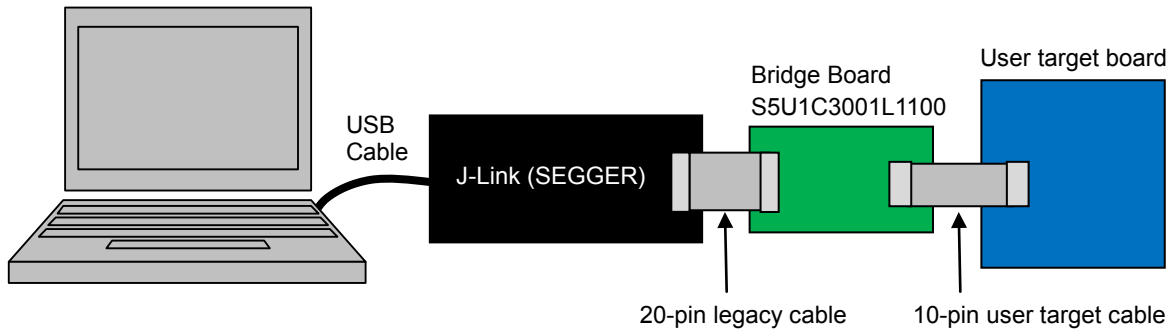
Figure 2.1   Connection Diagram when J-Link (20-pin Legacy Connector) is Used

When I-jet (20-pin micro pitch connector) is used
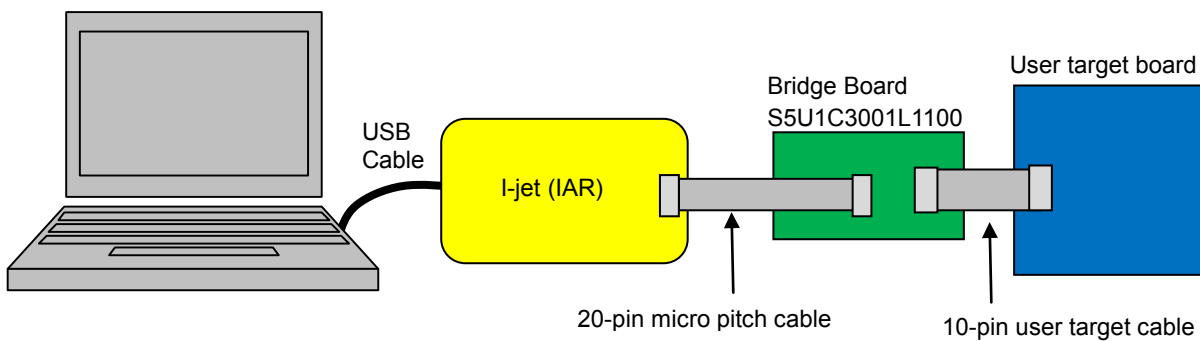
Figure 2.2   Connection Diagram when I-jet (20-pin Micro Pitch Connector) is Used

When I-jet (10-pin micro pitch connector) is used
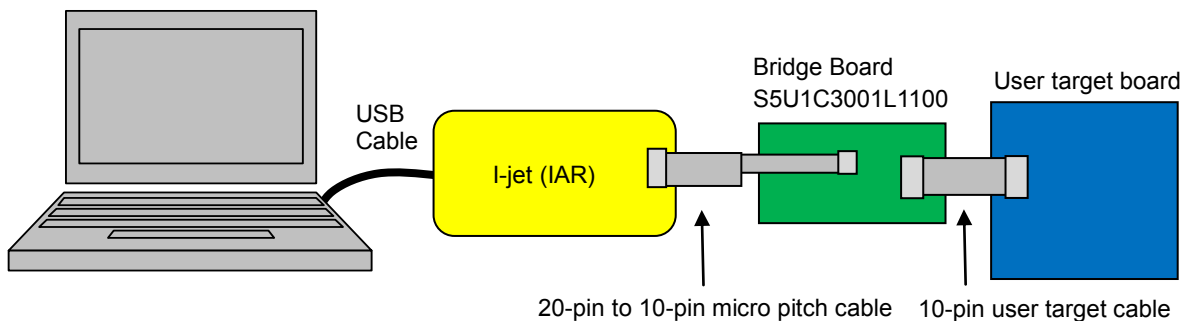
Figure 2.3   Connection Diagram when I-jet (10-pin Micro Pitch Connector) is Used

3. Name and Function of Each Part
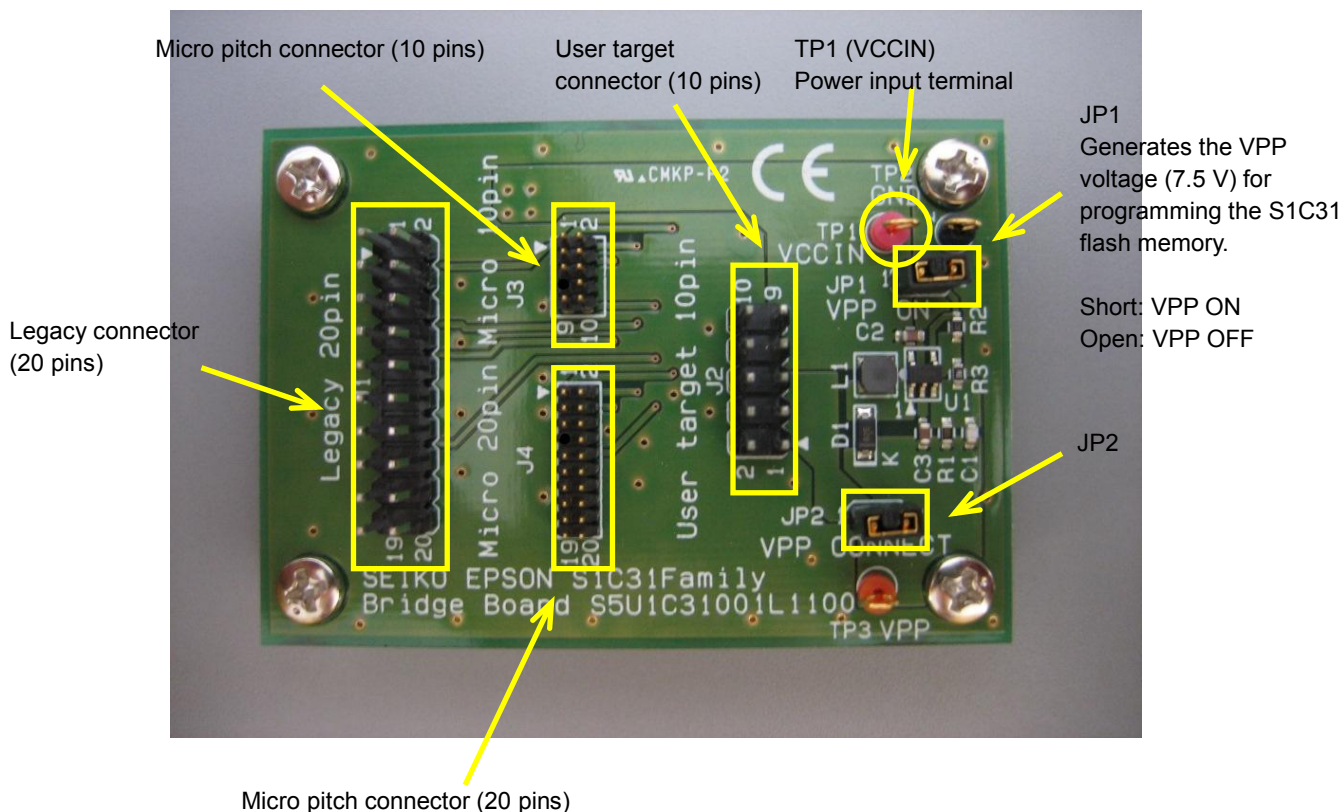
Figure 3.1   Name of Each Part

TP1 (VCCIN)

When the debug probe I-jet is connected to the 10-pin micro pitch connector, the programing power voltage (VPP) for the flash memory embedded in the S1C31 Family MCU cannot be supplied to the user target board, as this connector does not have a power supply pin used to input 5 V from the debug probe. In this case, the TP1 pin is used to supply power voltage from an external power supply (1.8 to 5.5 V, 500 mA or more). The S5U1C31001L1100 (Bridge Board) generates the VPP voltage by boosting the TP1 input voltage to supply to the user target board.

If the target S1C32 Family MCU includes a voltage booster and is being used for flash programming, it is not necessary to supply an external power voltage.
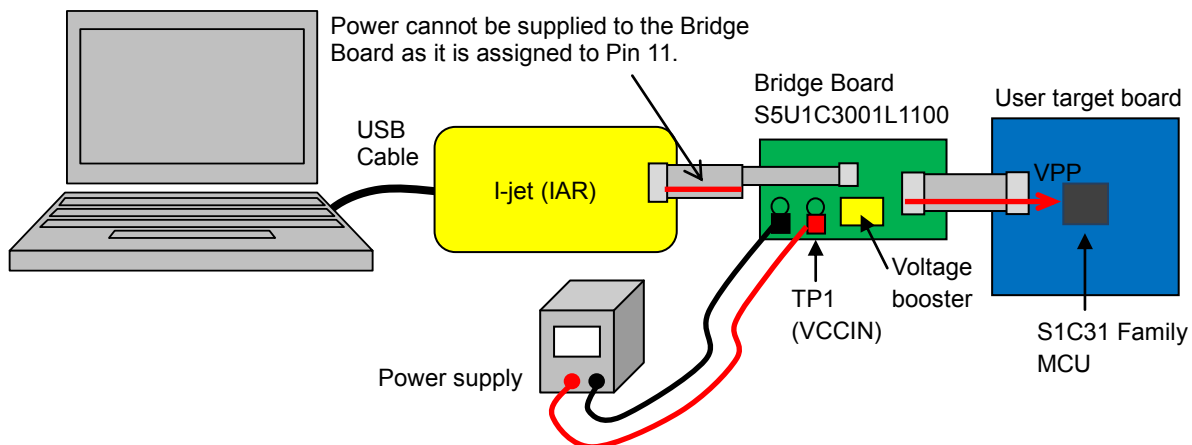
Figure 3.2   VPP Power Supply Example when I-jet is connected to 10-pin Micro Pitch Connector

3. Name and Function of Each Part

JP1, JP2

These switches select the power supply for programming the flash memory embedded in the S1C31 Family MCUs. Set both JP1 and JP2 as follows:

Table 3.1   JP1 and JP2 Settings

JP1 and JP2 settings	Flash programming power supply selected
Short (ON)	Power supply on the S5U1C31001L1100 (Bridge Board)
Open (OFF)	Power supply (voltage booster) built into the S1C31 Family MCU

4. Connectors

4.1 Legacy Connector (20 pins)

Table 4.1   20-pin Legacy Connector Pin Assignment

No	Name	No	Name
1	VTref	2	VCC (optional)
3	TRST	4	GND
5	NC/TDI	6	GND
7	SWDIO / TMS	8	GND
9	SWDCLK / TCK	10	GND
11	RTCK	12	GND
13	SWO / TDO	14	GND
15	nRESET	16	GND
17	NC/DBGRQ	18	GND
19	NC/DBACK	20	GND

4.2 Micro Pitch Connector (10 pins)

Table 4.2   10-pin Micro Pitch Connector Pin Assignment

No	Name	No	Name
1	VTref	2	SWDIO / TMS
3	GND	4	SWDCLK / TCK
5	GND	6	SWO / TDO
7	KEY	8	NC / TDI
9	GNDDetect	10	nRESET

4. Connectors

4.3 Micro Pitch Connector (20 pins)

Table 4.3   20-pin Micro Pitch Connector Pin Assignment

No	Name	No	Name
1	VTref	2	SWDIO / TMS
3	GND	4	SWDCLK / TCK
5	GND	6	SWO / TDO / EXTa / TRACECTL
7	KEY	8	NC/EXTb/TDI
9	GNDDetect	10	nRESET
11	GND/TgtPwr+Cap	12	TRACECLK
13	GND/TgtPwr+Cap	14	TRACEDATA[0]
15	GND	16	TRACEDATA[1]
17	GND	18	TRACEDATA[2]
19	GND	20	TRACEDATA[3]

4.4 User Target Connector (10 pins)

Table 4.4   10-pin User Target Connector Pin Assignment

No	Name	No	Name
1	SWDCLK	2	GND
3	SWDIO	4	NC
5	VPP	6	GND
7	nRESET	8	VTref
9	VCC	10	NC

5. Circuit Diagram

Notes:

There is no pin to prevent the wrong insertion about the terminal KEY of J3 and J4 connector.

Revision History

Rev. No.	Date	Page	Category	Contents
Rev 1.0	2016/03/11	All	New	New establishment
Rev. 1.1	2016/06/13	3	Correction	"FIXED ON" described in Figure 3.1 was changed to "JP2."
		4	Addition	"JP2" was added to the explanation of "JP1."

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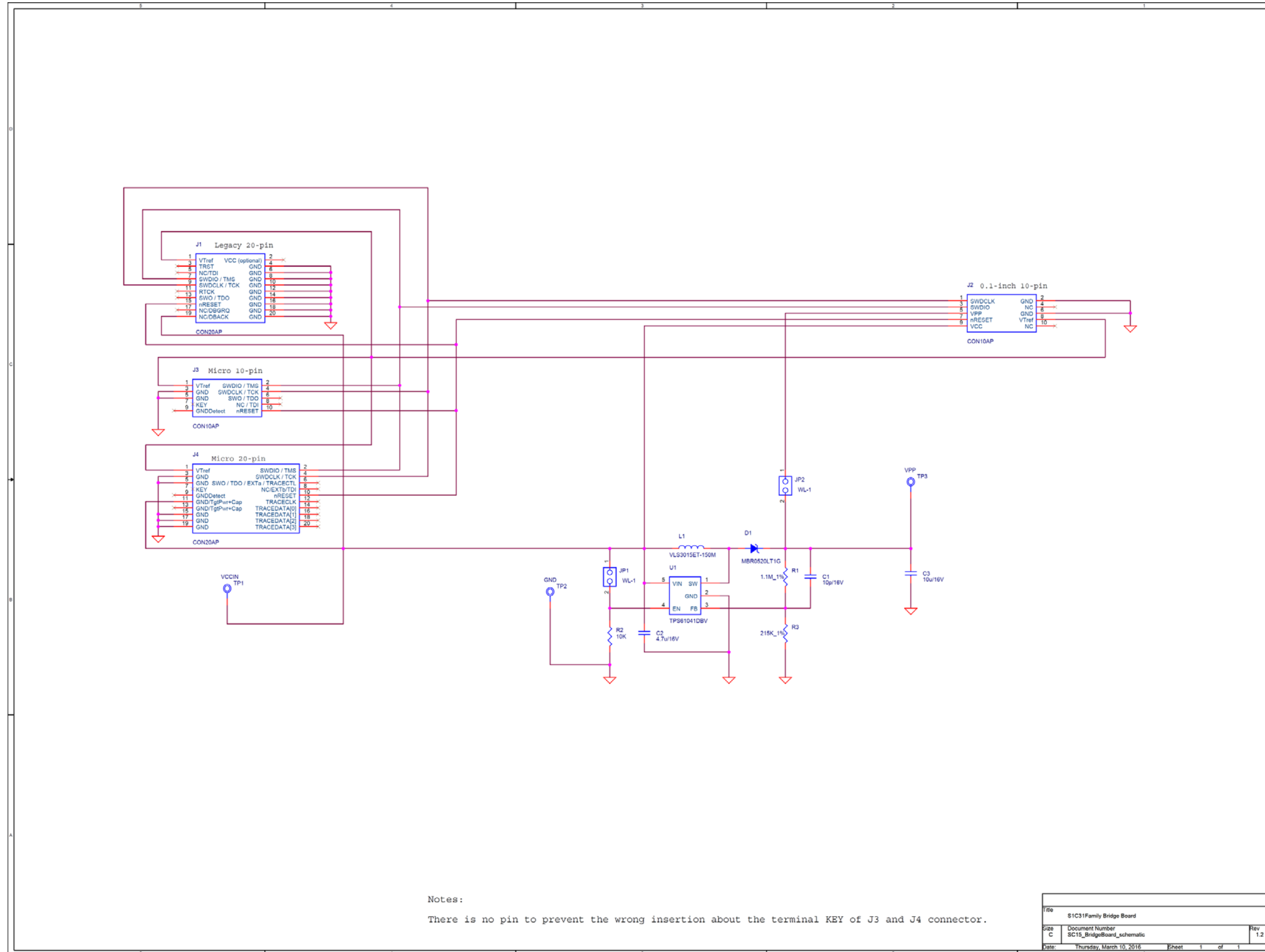
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