

S1V3G340
External SPI-Flash
Select Guide

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1. Description

This document describes how to select external SPI-Flash for S1V3G340.

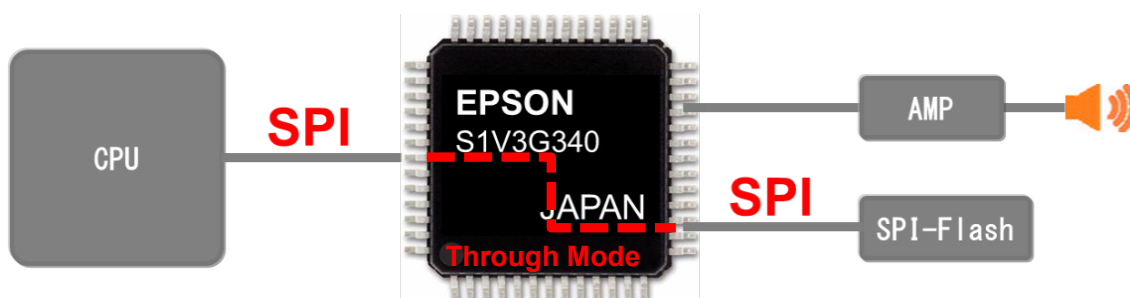
Note: Please evaluate selected SPI-Flash by a customer because of the difference about detail specification.

■ Read Mode

Regarding the read mode, SPI should be complaint with S1V3G340 specification, if not S1V3G340 cannot read the voice data from SPI-Flash.

■ Write Mode

To write the data from Host CPU to SPI-Flash via S1V3G340, Host CPU should be compliant with SPI-Flash write mode specification(note: SPI frequency should be up to 1MHz because of S1V3G340 max frequency), so typically no limitation, but S1V3G340 evaluation board tool has a limitation. Please check if a customer uses S1V3G340 evaluation board tool for evaluation.

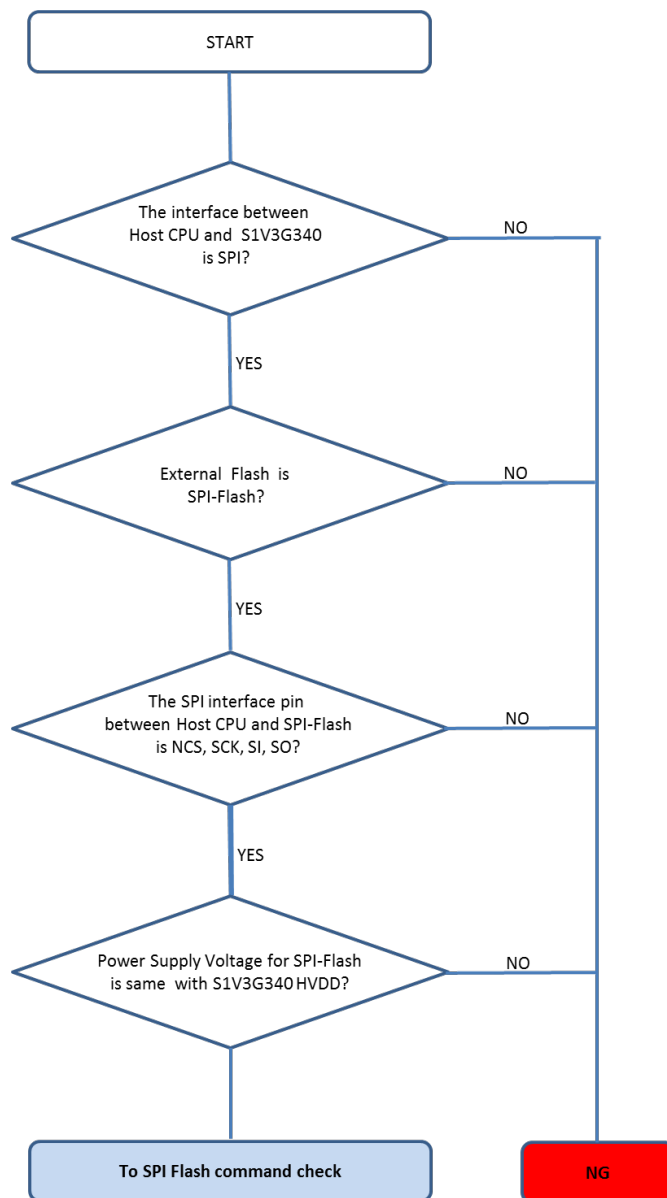


2. Checkpoint

2. Checkpoint

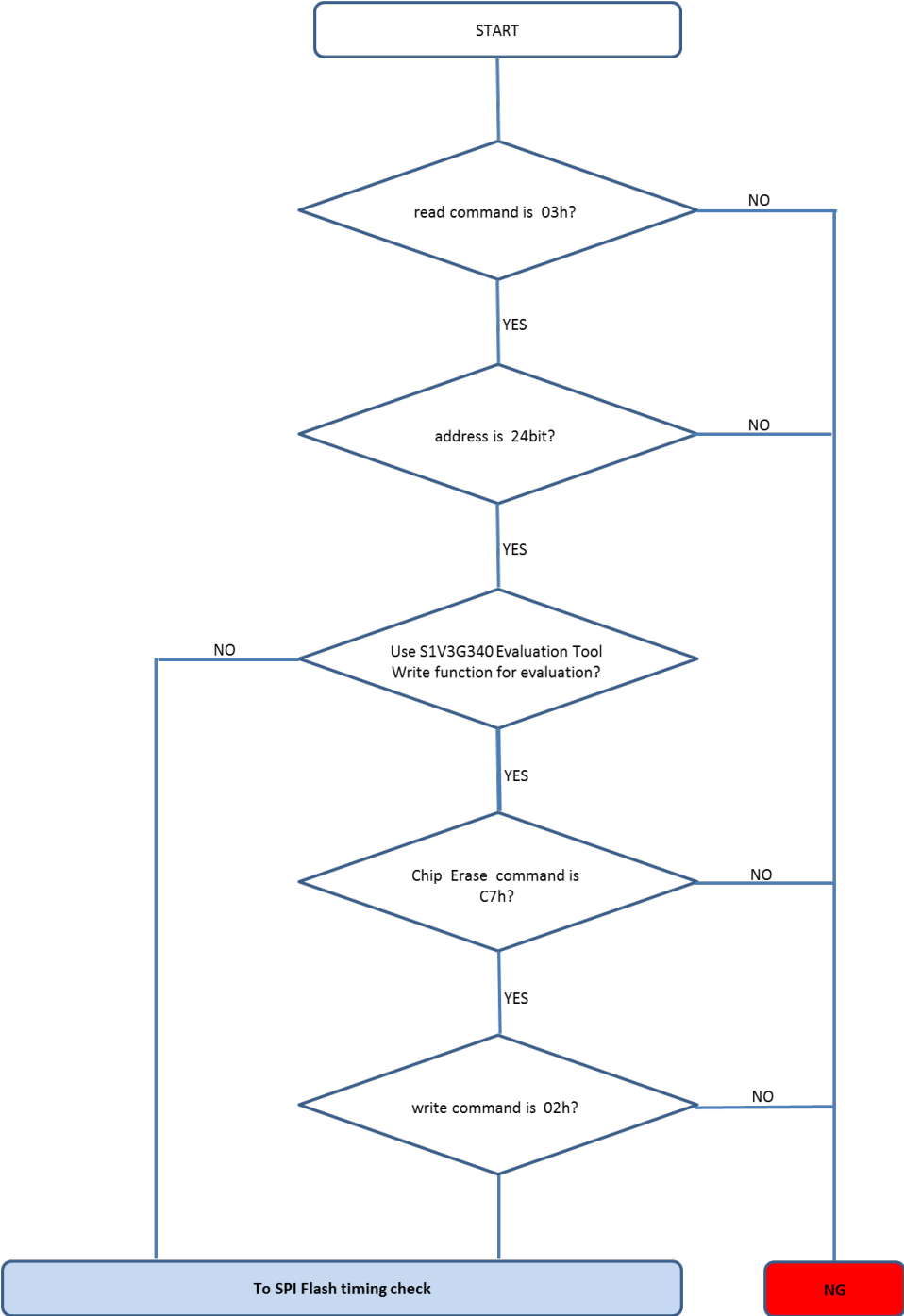
2.1 System specification CHECK

- Please check by following chart.



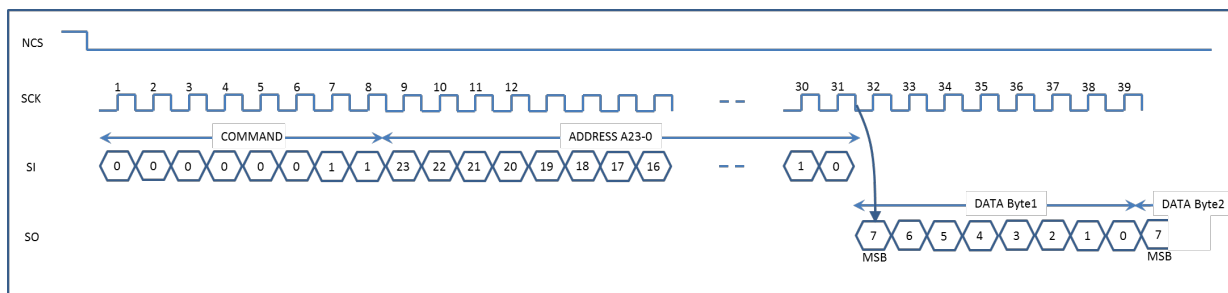
2.2 SPI-Flash comandnd specification CHECK

- Please check by following chart.



2. Checkpoint

2.3 READ timing specification CHECK

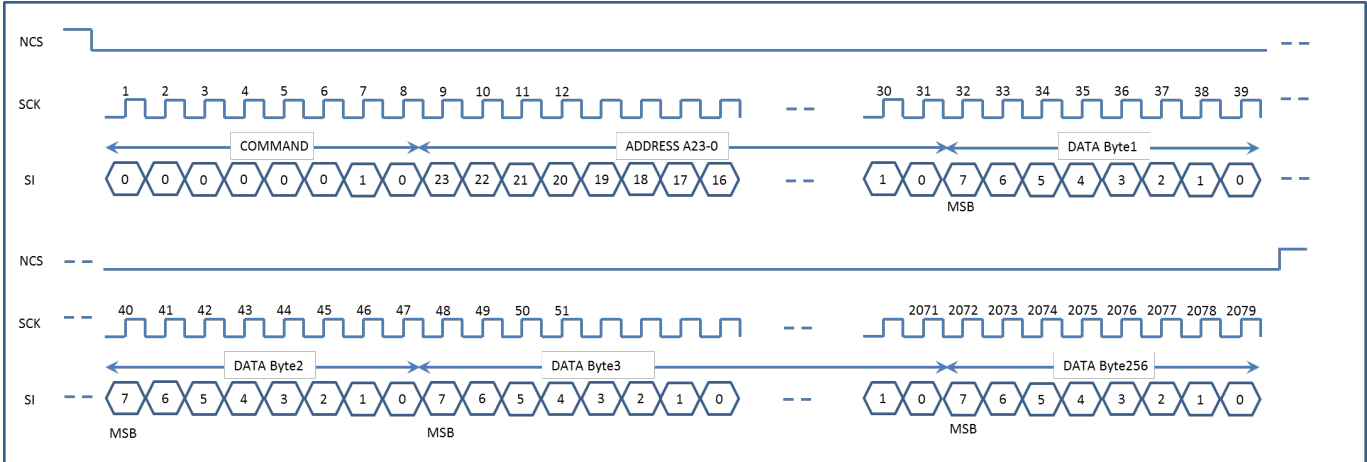


SPI-Flash Read Timing

Please check following point

- ① First 8 clock COMMAND : READ instruction :03h
- ② After COMMAND ADDRESS 24bit
- ③ After ADDRESS DATA: 8bit data is out

2.4 WRITE timing specification CHECK



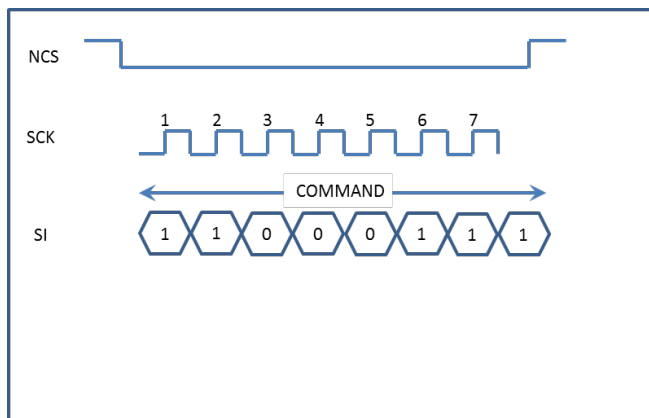
SPI-Flash Write Timing

Please check following point

- ① First 8 clock COMMAND : WRITE instruction :02h
- ② After COMMAND ADDRESS 24bit
- ③ After ADDRESS DATA: input 8bit data

2. Checkpoint

2.5 ERASE timing specification CHECK



SPI-Flash Erase Timing

Please check following point

- ① First 8 clock COMAMND : ERASE instruction :C7h

Revision History

Attachment-1

Rev. No.	Date	Page	Category	Contents
Rev 1.00	2016/1/12	All	new	New release.

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