

16-bit Single Chip Microcontroller

- 24KB FLASH ROM(50 times): Read/program protection function, 2KB RAM
 *A programming power supply (V_{PP}) is required.
- Generates the operating clocks with the built-in oscillators.
 - OSC3B oscillator circuit: 4 MHz/2 MHz/1 MHz/500 kHz (typ.) internal oscillator circuit
 - OSC1A oscillator circuit: 32.768 kHz (typ.) crystal oscillator circuit
- LCD driver Number of driver outputs: 32seg. x 4com.
- Shipping form: Die, TQFP14-80PIN
- RISC CPU core S1C17: the compact code optimized for C, and high throughput of an instruction/clock, supports serial ICE

DESCRIPTIONS

The S1C17656 is a 16-bit MCU featuring low-power operations and compact dimensions in die form. The S1C17656 is ideal for battery-driven electronic equipment, such as OTP cards, eTokens, and remote control units with a simple display.

■ FEATURES

The main features of the S1C17656 are listed below.

CPU core Seiko Epson original 16-bit RISC CPU core S1C17 Multiplier/Divider (COPRO) • 16-bit × 16-bit multiplier • 16-bit × 16-bit + 32-bit multiply and accumulation unit • 16-bit + 32-bit multiply and accumulation unit • 16-bit × 16-bit + 32-bit multiply and accumulation unit • 16-bit + 32-bit multiply and accumulation unit • 16-bit + 16-bit divider • 16-bit + 16-bit divider Capacity 24K bytes (for both instructions and data) Erase/program count 50 times(min.) Other • Security function to protect from reading/programming by the debugging tool ICDmini • A programming power supply (V _{PP}) is required. • Allows on-board programming using the debugging tool ICDmini. Embedded RAM Expective 2K bytes Clock generator (CLG) 2K bytes System clock source 2 sources (OSC3B/OSC1A) OSC3B oscillator circuit 32.768 kHz (typ.) crystal oscillator circuit OSC1A oscillator circuit 32.768 kHz (typ.) crystal oscillator circuit Other • Core clock frequency control • Pripheral module clock supply control • Pripheral module clock supply control	CF 0					
Multiplier/Divider (COPRO) 16-bit × 16-bit multiplier 16-bit × 16-bit + 32-bit multiply and accumulation unit 16-bit + 16-bit divider Embedded Flash memory 24K bytes (for both instructions and data) Erase/program count 50 times(min.) Other Security function to protect from reading/programming by the debugging tool ICDmini A programming power supply (V_{PP}) is required. Allows on-board programming using the debugging tool ICDmini. Embedded RAM Capacity 2K bytes Clock generator (CLG) System clock source 2 sources (OSC3B/OSC1A) OSC1A oscillator circuit 4M/2M/1M/500k Hz (typ.) internal oscillator circuit Other Core clock frequency control Peripheral module clock supply control 	CPU core	Seiko Epson original 16-bit RISC CPU core S1C17				
• 16-bit × 16-bit + 32-bit multiply and accumulation unit • 16-bit + 16-bit divider Embedded Flash memory Capacity 24K bytes (for both instructions and data) Erase/program count 50 times(min.) Other • Security function to protect from reading/programming by the debugging tool ICDmini • A programming power supply (V _{PP}) is required. • Allows on-board programming using the debugging tool ICDmini. Embedded RAM - Allows on-board programming using the debugging tool ICDmini. Clock generator (CLG) 2K bytes System clock source 2 sources (OSC3B/OSC1A) OSC3B oscillator circuit 32.768 kHz (typ.) internal oscillator circuit OSC1A oscillator circuit 32.768 kHz (typ.) crystal oscillator circuit Other • Core clock frequency control • Peripheral module clock supply control • Peripheral module clock supply control	Multiplier/Divider (COPRO)	16-bit × 16-bit multiplier				
• 16-bit ÷ 16-bit divider Embedded Flash memory Capacity 24K bytes (for both instructions and data) Erase/program count 50 times(min.) Other • Security function to protect from reading/programming by the debugging tool ICDmini • A programming power supply (V _{PP}) is required. • Allows on-board programming using the debugging tool ICDmini. Embedded RAM • Allows on-board programming using the debugging tool ICDmini. Capacity 2K bytes Clock generator (CLG) • Secures (OSC3B/OSC1A) OSC3B oscillator circuit 4M/2M/1M/500k Hz (typ.) internal oscillator circuit OSC1A oscillator circuit 32.768 kHz (typ.) crystal oscillator circuit Other • Core clock frequency control • Peripheral module clock supply control • Peripheral module clock supply control		 16-bit × 16-bit + 32-bit multiply and accumulation unit 				
Embedded Flash memory Capacity 24K bytes (for both instructions and data) Erase/program count 50 times(min.) Other • Security function to protect from reading/programming by the debugging tool ICDmini Other • Security function to protect from reading/programming by the debugging tool ICDmini Embedded RAM • Allows on-board programming using the debugging tool ICDmini. Capacity 2K bytes Clock generator (CLG) • Sources (OSC3B/OSC1A) System clock source 2 sources (OSC3B/OSC1A) OSC3B oscillator circuit 4M/2M/1M/500k Hz (typ.) internal oscillator circuit OSC1A oscillator circuit 32.768 kHz (typ.) crystal oscillator circuit Other • Core clock frequency control • Peripheral module clock supply control • Peripheral module clock supply control		• 16-bit ÷ 16-bit divider				
Capacity 24K bytes (for both instructions and data) Erase/program count 50 times(min.) Other • Security function to protect from reading/programming by the debugging tool ICDmini • A programming power supply (V _{PP}) is required. • Allows on-board programming using the debugging tool ICDmini. Embedded RAM • Allows on-board programming using the debugging tool ICDmini. Capacity 2K bytes Clock generator (CLG) • Sources (OSC3B/OSC1A) System clock source 2 sources (OSC3B/OSC1A) OSC3B oscillator circuit 4M/2M/1M/500k Hz (typ.) internal oscillator circuit OSC1A oscillator circuit 32.768 kHz (typ.) crystal oscillator circuit Other • Core clock frequency control • Peripheral module clock supply control • Peripheral module clock supply control	Embedded Flash memory					
Erase/program count 50 times(min.) Other • Security function to protect from reading/programming by the debugging tool ICDmini • A programming power supply (V _{PP}) is required. • Allows on-board programming using the debugging tool ICDmini. Embedded RAM • Allows on-board programming using the debugging tool ICDmini. Capacity 2K bytes Clock generator (CLG) • Sources (OSC3B/OSC1A) System clock source 2 sources (OSC3B/OSC1A) OSC3B oscillator circuit 4M/2M/1M/500k Hz (typ.) internal oscillator circuit OSC1A oscillator circuit 32.768 kHz (typ.) crystal oscillator circuit Other • Core clock frequency control • Peripheral module clock supply control • Peripheral module clock supply control	Capacity	24K bytes (for both instructions and data)				
Other • Security function to protect from reading/programming by the debugging tool ICDmini • A programming power supply (V _{PP}) is required. • Allows on-board programming using the debugging tool ICDmini. Embedded RAM 2K bytes Capacity 2K bytes Clock generator (CLG) 2 sources (OSC3B/OSC1A) OSC3B oscillator circuit 4M/2M/1M/500k Hz (typ.) internal oscillator circuit OSC1A oscillator circuit 32.768 kHz (typ.) crystal oscillator circuit Other • Core clock frequency control • Peripheral module clock supply control • Peripheral module clock supply control	Erase/program count	50 times(min.)				
A programming power supply (V _{PP}) is required. Allows on-board programming using the debugging tool ICDmini. Embedded RAM Capacity Capacity Clock generator (CLG) System clock source 2 sources (OSC3B/OSC1A) OSC3B oscillator circuit 4W/2M/1M/500k Hz (typ.) internal oscillator circuit OSC1A oscillator circuit 32.768 kHz (typ.) crystal oscillator circuit Other Core clock frequency control Peripheral module clock supply control	Other	 Security function to protect from reading/programming by the debugging tool ICDmini 				
Allows on-board programming using the debugging tool ICDmini. Embedded RAM Capacity 2K bytes Clock generator (CLG) System clock source 2 sources (OSC3B/OSC1A) OSC3B oscillator circuit 4W/2M/1M/500k Hz (typ.) internal oscillator circuit OSC1A oscillator circuit 32.768 kHz (typ.) crystal oscillator circuit Other - Core clock frequency control Peripheral module clock supply control		 A programming power supply (V_{PP}) is required. 				
Embedded RAM Capacity 2K bytes Clock generator (CLG) System clock source 2 sources (OSC3B/OSC1A) OSC3B oscillator circuit 4W/2M/1M/500k Hz (typ.) internal oscillator circuit OSC1A oscillator circuit 32.768 kHz (typ.) crystal oscillator circuit Other • Core clock frequency control • Peripheral module clock supply control		Allows on-board programming using the debugging tool ICDmini.				
Capacity 2K bytes Clock generator (CLG) System clock source 2 sources (OSC3B/OSC1A) OSC3B oscillator circuit 4M/2M/1M/500k Hz (typ.) internal oscillator circuit OSC1A oscillator circuit 32.768 kHz (typ.) crystal oscillator circuit Other • Core clock frequency control • Peripheral module clock supply control	Embedded RAM					
Clock generator (CLG) System clock source 2 sources (OSC3B/OSC1A) OSC3B oscillator circuit 4M/2M/1M/500k Hz (typ.) internal oscillator circuit OSC1A oscillator circuit 32.768 kHz (typ.) crystal oscillator circuit Other • Core clock frequency control • Peripheral module clock supply control	Capacity	2K bytes				
System clock source 2 sources (OSC3B/OSC1A) OSC3B oscillator circuit 4M/2M/1M/500k Hz (typ.) internal oscillator circuit OSC1A oscillator circuit 32.768 kHz (typ.) crystal oscillator circuit Other • Core clock frequency control • Peripheral module clock supply control	Clock generator (CLG)					
OSC3B oscillator circuit 4M/2M/1M/500k Hz (typ.) internal oscillator circuit OSC1A oscillator circuit 32.768 kHz (typ.) crystal oscillator circuit Other • Core clock frequency control • Peripheral module clock supply control	System clock source	2 sources (OSC3B/OSC1A)				
OSC1A oscillator circuit 32.768 kHz (typ.) crystal oscillator circuit Other Core clock frequency control Peripheral module clock supply control	OSC3B oscillator circuit	4M/2M/1M/500k Hz (typ.) internal oscillator circuit				
Other Core clock frequency control Peripheral module clock supply control CD driver (LCD)	OSC1A oscillator circuit	32.768 kHz (typ.) crystal oscillator circuit				
Peripheral module clock supply control	Other	Core clock frequency control				
LCD driver (LCD)		Peripheral module clock supply control				
	LCD driver (LCD)					
Number of driver outputs Segment output: 32 pins, Common output: 4 pins	Number of driver outputs	Segment output: 32 pins, Common output: 4 pins				
Other • Includes a power supply voltage booster/reducer.	Other	 Includes a power supply voltage booster/reducer. 				
Includes a display data memory.		Includes a display data memory.				
I/O ports (P)	I/O ports (P)					
Number of general-purpose I/O ports Max. 19 bits (The pins are shared with the peripheral I/O.)	Number of general-purpose I/O ports	Max. 19 bits (The pins are shared with the peripheral I/O.)				
Number of general-purpose Output ports Max. 1 bit (The pin is shared with the debug signal output.)	Number of general-purpose Output ports	Max. 1 bit (The pin is shared with the debug signal output.)				
Other • Schmitt input	Other	Schmitt input				
Pull-up control function		Pull-up control function				
Port input interrupt: 8 bits (P00–P07)		Port input interrupt: 8 bits (P00–P07)				
Serial interfaces	Serial interfaces					
SPI 1 channel	SPI	1 channel				
UART 1 channel (IrDA1.0 supported)	UART	1 channel (IrDA1.0 supported)				
Timers/Counters	Timers/Counters					
8-bit timer (T8) 1 channel (Generates the SPI clock.)	8-bit timer (T8)	1 channel (Generates the SPI clock.)				
16-bit PWM timer (T16A2) 1 channel (PWM output, event counter, and count capture functions)	16-bit PWM timer (T16A2)	1 channel (PWM output, event counter, and count capture functions)				
Watchdog timer (WDT) 1 channel (Generates NMI/reset.)	Watchdog timer (WDT)	1 channel (Generates NMI/reset.)				
Clock functions	Clock functions					
Real-time clock (RTC) 1 channel (Hour, minute, and second counters)	Real-time clock (RTC)	1 channel (Hour, minute, and second counters)				
Clock timer (CT) 1 channel (128 Hz to 1 Hz counters)	Clock timer (CT)	1 channel (128 Hz to 1 Hz counters)				
Sound generator (SND)	Sound generator (SND)					

Buzzer frequency	8 frequencies selectable					
Volume control	8 steps adjustable					
Other	One-shot buzzer					
	Auto envelope function					
Supply voltage detection circuit (SVD)						
Detection level	13 levels (2.0 V to 3.2 V)					
Other	Intermittent mode					
	Generates an interrupt or reset according to the detection level evaluation.					
	 V_{DD} or an external voltage (P02 pin input, up to V_{DD} level) can be detected. 					
R/F converter (RFC)						
Conversion method	CR oscillation type with 24-bit counter					
Number of conversion channels	1 channel (2 sensors can be connected.)					
Sensor supported	DC-bias resistive sensors					
Other	Supports external input for counting pulses.					
Interrupts	F					
Reset interrupt	#RESET pin/watchdog timer					
NMI	Watchdog timer					
Programmable interrupts	10 systems (8 levels)					
Power supply voltage						
Operating voltage (V _{DD})	1.8 V to 3.6 V					
Flash programming/erasing voltage (VPP)	7.5V					
Operating temperature						
Operating temperature range	-40°C to 85°C					
Current consumption (Typ value, V _{DD} = 1.8 V	to 3.6 V)					
SLEEP state	130 nA (OSC1A = Off, RTC = Off, OSC3B = Off)					
	400 nA (OSC1A = 32 kHz, RTC = On, OSC3B = Off)					
HALT state	0.5 μA (OSC1A = 32 kHz, RTC = Off, OSC3B = Off)					
	0.5 μA (OSC1A = 32 kHz, RTC = On, OSC3B = Off)					
Run state	7.3 μA (OSC1A = 32 kHz, RTC = Off, OSC3B = Off)					
	280 μA (OSC1A = Off, RTC = Off, OSC3B = 1 MHz)					
Shipping form						
1	Aluminum pad chip					
2	TQFP14-80pin (14 mm × 14 mm × 1 mm, lead pitch: 0.5 mm)					

BLOCK DIAGRAM



PIN CONFIGURATION DIAGRAM

CHIP



TQFP14-80pin



PIN DESCRIPTIONS

Note: The pin names described in boldface type are default settings.

	Pin no.	News	1/0	Initial	E-matter
Chip	TQFP14-80	Name	1/0	status	Function
67, 68,	78, 79, 1–10,	SEG31-SE0	0	O(Hi-Z)	LCD segment output pins
1–30	12–20, 23–29,				
	31–34				
31-34	35-38	COM3-COM0	0	O(Hi-Z)	LCD common output pins
35	42	V _{C3}	-	-	LCD system power supply circuit output pin
36	43	V _{C2}	-	-	LCD system power supply circuit output pin
37	44	V _{C1}	-	-	LCD system power supply circuit output pin
38	45	CB	-	-	Voltage boost capacitor connecting pin for LCD system power supply circuit
39	46	CA	-	-	Voltage boost capacitor connecting pin for LCD system power supply circuit
40	47	Vss	-	-	
41	48	V _{DD}	-	-	Power supply pin (1.8 to 3.6 V)
42	49	V _{D1}	-	-	
43	50	0501	1	1	
44	52	#DESET	- 0		
40	77	W	I	i(Full-up)	Flash programming/grasing power supply pin (7.5.)/)
00		¥ PP	-	-	(Leave the nin open during normal operation)
49	56	P00	1/0	I(Pull-up)	I/O port pin (with interrupt function)
10		SINO	1	i(i ai ap)	LIART Ch 0 data input pin
50	57	P01	I/O	I(Pull-up)	I/O port pin (with interrupt function)
		SOUTO	0	.(. a. ap)	UART Ch 0 data output pin
51	58	P02(EXSVD)	1/0	I(Pull-up)	I/O port pin (with interrupt function). SVD detection target voltage input pin
		SCLK0	1		UART Ch.0 external clock input pin
		FOUTA	0		Clock output pin
52	62	P03	I/O	I(Pull-up)	I/O port pin (with interrupt function)
		EXCL0	I	· · · /	T16A2 Ch.0 external clock input pin
		LFRO	0		LCD frame signal output pin
53	63	P04	I/O	I(Pull-up)	I/O port pin (with interrupt function)
		TOUTA0	0		T16A2 Ch.0 TOUT A signal output pin
		CAPA0	_		T16A2 Ch.0 capture A trigger signal input pin
54	64	P05	I/O	I(Pull-up)	I/O port pin (with interrupt function)
		TOUTB0	0		T16A2 Ch.0 TOUT B signal output pin
		CAPB0	Ι		T16A2 Ch.0 capture B trigger signal input pin
		#SPISS0	I		SPI Ch.0 slave select signal input pin
55	65	P06	I/O	I(Pull-up)	I/O port pin (with interrupt function)
		BZ	0	-	Buzzer output pin
		SDIO			SPI Ch.0 data input pin
56	66	P07	1/0	I(Pull-up)	I/O port pin (with interrupt function)
		#BZ	0		Buzzer inverted output pin
F7	07	SDOU	0		SPI Cn.0 data output pin
57	67		1/0	I(Pull-up)	I/O port pin
			1/0		SPI Ch 0 clock input/output pip
58	89		0	O(H) *	On-chin debugger clock output pin
50	00	D11	0		
		BZ	0	-	Buzzer output pin
59	69	DSIO		l(Pull-up)	On-chip debugger data input/output pin
		P12	I/O	·(· • • • • • • • • • • • • • • • • • •	I/O port pin
		#BZ	0		Buzzer inverted output pin
60	71	DST2	0	O(L)	On-chip debugger status output pin
		P13	I/O		I/O port pin
61	72	P14	I/O	I(Pull-up)	I/O port pin
		RFIN0	I/O	1	R/F converter Ch.0 RFCLK input and oscillation control pin
62	73	P15	I/O	I(Pull-up)	I/O port pin
		REF0	I/O		R/F converter Ch.0 reference oscillation control pin
63	74	P16	I/O	I(Pull-up)	I/O port pin
		SENA0	I/O		R/F converter Ch.0 sensor A oscillation control pin
64	75	P17	I/O	I(Pull-up)	I/O port pin
		SENB0	I/O		R/F converter Ch.0 sensor B oscillation control pin
65	76	P20	I/O	I(Pull-up)	I/O port pin
46	53	P21	I/O	I(Pull-up)	I/O port pin

47	54	P22	I/O	I(Pull-up)	I/O port pin
48	55	P23	I/O	I(Pull-up)	I/O port pin
		RFCLKO	0		R/F clock monitor output pin

NOTICE:

No part of this material may be reproduced or duplicated in any form or by any means without the written permission of Seiko Epson. Seiko Epson reserves the right to make changes to this material without notice. Seiko Epson does not assume any liability of any kind arising out of any inaccuracies contained in this material or due to its application or use in any product or circuit and, further, there is no representation that this material is applicable to products requiring high level reliability, such as, medical products. Moreover, no license to any intellectual property rights is granted by implication or otherwise, and there is no representation or warranty that anything made in accordance with this material will be free from any patent or copyright infringement of a third party. This material or portions thereof may contain technology or the subject relating to strategic products under the control of the Foreign Exchange and Foreign Trade Law of Japan and may require an export license from the Ministry of Economy, Trade and Industry or other approval from another government agency.

All brands or product names mentioned herein are trademarks and/or registered trademarks of their respective companies.

©Seiko Epson Corporation 2014, All rights reserve

SEIKO EPSON CORPORATION

MICRODEVICES OPERATIONS DIVISION

EPSON semiconductor website

http://global.epson.com/products/semicon/

Document code: 412746500 First issue April, 2014 in Japan