EPSON

S1C17W15 (rev 1.01)

16-bit Single Chip Microcontroller • Low power operation from 1.2V with a single alkaline or silver

- oxide button battery.

 Low power consumption standby driving at HALT 0.5 μA.
- Built-in LCD Driver: 30 SEG x 8 COM (max.)
- Internal 4ch R/F converters enable to realizé various sensing.

■ DESCRIPTIONS

The S1C17W15 is a 16-bit MCU that features low-voltage operation from 1.2 V even though the Flash memory is included. The embedded high-efficiency DC-DC converter generates the constant-voltage to drive the IC with lower power consumption than 4-bit MCUs. This IC includes a real-time clock, a stopwatch, an LCD driver, and a PWM timer capable of being used to generate drive waveforms for a motor driver as well as a high-performance 16-bit CPU. It is suitable for battery-driven applications that require an LCD display and timers.

■ FEATURES

Model	S1C17W15
CPU	
CPU Core	Seiko Epson original 16-bit RISC CPU Core S1C17
Other	On-chip debugger
Embedded Flash memory	
Capacity	64K bytes (for both instructions and data)
Erase/program count	50 times (min.) * Programming by the debugging tool ICDmini
Other	Security function to protect from reading/programming by ICDmini
	On-board programming function using ICDmini
Embedded RAM	
Capacity	4K bytes
Embedded display RAM	
Capacity	68 bytes
Clock generator (CLG)	
System clock source	4 sources (IOSC/OSC1/OSC3/EXOSC)
System clock frequency	1.1 MHz (max.) VDD = 1.2 to 1.6 V
(operating frequency)	4.2 MHz (max.) VDD = 1.6 to 3.6 V
IOSC oscillator circuit	700 kHz (typ.) embedded oscillator
(boot clock source)	23 µs (max.) starting time (time from cancelation of SLEEP state to vector table read by the CPU)
OSC1 oscillator circuit	32.768 kHz (typ.) crystal oscillator
	Oscillation stop detection circuit included
OSC3 oscillator circuit	4.2 MHz (max.) crystal/ceramic oscillator
	500 kHz, 1, 2, and 4 MHz-switchable embedded oscillator
	500 Hz to 2 MHz CR oscillator (an external R is required)
EXOSC clock input	4.2 MHz (max.) square or sine wave input
Other	Configurable system clock division ratio
	Configurable system clock used at wake up from SLEEP state
	Operating clock frequency for the CPU and all peripheral circuits is selectable.
I/O port (PPORT)	
Number of general-purpose I/O ports	Input/output port: 35 bits (max., 100-pin package or chip)
	32 bits (max., 80-pin package)
	27 bits (max., 64-pin package)
	Output port: 1 bit (max.)
Number of investing and a set	Pins are shared with the peripheral I/O.
Number of input interrupt ports	31 bits (max., 100-pin package or chip) 28 bits (max., 80-pin package)
	23 bits (max., 64-pin package)
Number of ports that support universal port	23 bits (max., 04-pin package)
multiplexer (UPMUX)	A peripheral circuit I/O function selected via software can be assigned to each port.
Timers	A periprieral direction selected via software earlier assigned to each port.
Watchdog timer (WDT)	Generates watchdog timer reset.
Real-time clock (RTCA)	128–1 Hz counter, second/minute/hour/day/day of the week/month/year counters
real time block (referr)	Theoretical regulation function for 1-second correction
	Alarm and stopwatch functions
16-bit timer (T16)	3 channels
10 2.3 (110)	Generates the SPIA master clock.
16-bit PWM timer (T16B)	2 channels
10 2.1. 1.111 (1110)	Event counter/capture function
	PWM waveform generation function
	Number of PWM output or capture input ports: 2 ports/channel
Supply voltage detector (SVD)	1
Detection level	30 levels (1.2 to 3.6 V)
Detection accuracy	±3%
Other	Intermittent operation mode
	Generates an interrupt or reset according to the detection level evaluation.
L	1

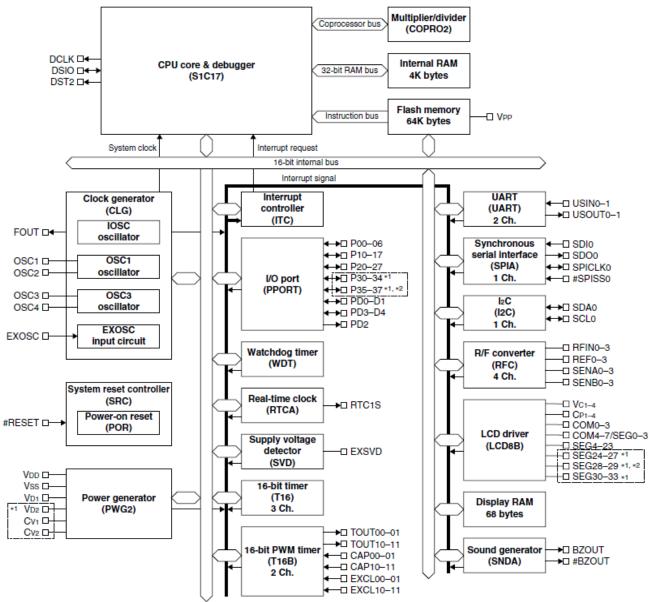
Serial interfaces	
UART (UART)	2 channel
UAIXI (UAIXI)	Baud-rate generator included, IrDA1.0 supported
Cymahanaya Carial Interfess (CDIA)	, 11
Synchronous Serial Interface (SPIA)	1 channel
	2 to 16-bit variable data length
120 (100) *1	The 16-bit timer (T16) can be used for the baud-rate generator in master mode.
I ² C (I2C) *1	1 channel
	Baud-rate generator included
Sound generator (SNDA)	
Buzzer output function	512 Hz to 16 kHz output frequencies
	One-shot output function
Melody generation function	Pitch: 128 Hz to 16 kHz ≈ C3 to C6
	Duration: 7 notes/rests (Half note/rest to thirty-second note/rest)
	Tempo: 16 tempos (30 to 480)
	Tie may be specified.
LCD driver (LCD24A)	
LCD output	30 SEG × 5–8 COM (max.), 34 SEG × 1–4 COM (max.) (100-pin package or chip) 28 SEG × 5–8 COM (max.), 32 SEG × 1–4 COM (max.) (80-pin package) 20 SEG × 5–8 COM (max.), 24 SEG × 1–4 COM (max.) (64-pin package)
LCD contrast	32 levels
Other	1/4 or 1/3 bias power supply included, external voltage can be applied.
R/F converter (RFC)	
Conversion method	CR oscillation type with 24-bit counters
Number of conversion channels	4 channels (Up to two sensors can be connected to each channel.)
Supported sensors	DC-bias resistive sensors, AC-bias resistive sensors (Ch.0 only)
Multiplier/divider (COPRO2)	
Arithmetic functions	16-bit × 16-bit multiplier
	16-bit × 16-bit + 32-bit multiply and accumulation unit
	32-bit ÷ 32-bit divider
Reset	
#RESET pin	Reset when the reset pin is set to low.
Power-on reset	Reset at power on.
Key entry reset	Reset when the P00 to P01/P02/P03 keys are pressed simultaneously (can be enabled/disabled
, ,	using a register).
Watchdog timer reset	Reset when the watchdog timer overflows (can be enabled/disabled using a register).
Supply voltage detector reset	Reset when the supply voltage detector detects the set voltage level (can be enabled/disabled using
11,7	a register).
Non-maskable interrupt	4 systems (Reset, address misaligned interrupt, debug, NMI)
Programmable interrupt	External interrupt: 1 system (8 levels)
,	Internal interrupt: 20 systems (8 levels)
Power supply voltage	
VDD operating voltage	1.2 to 3.6 V
VDD operating voltage for Flash programming	1.8 to 3.6 V (V _{PP} = 7.5 V external power supply is required.)
VDD operating voltage for super economy mode	2.5 to 3.6 V (100-pin/80-pin package or chip)
Operating temperature	
Operating temperature range	-40 to 85 °C
Current consumption	
SLEEP mode *2	0.15 μΑ
	IOSC=OFF, OSC1=OFF, OSC3=OFF
HALT mode	0.5 μA OSC1=32 kHz, RTC=ON
	0.3 μA OSC1=32 kHz, RTC=ON, Super economy mode (100-pin/80-pin package or chip)
	, , , , , , , , , , , , , , , , , , , ,
	1.2 µA
	7 1 7 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
	1.2 µA
RUN mode	1.2 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, LCD=ON (no panel load, Vc2 reference, 1/3bias),
RUN mode	1.2 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, LCD=ON (no panel load, Vc2 reference, 1/3bias), Super economy mode (100-pin/80-pin package or chip)
RUN mode	1.2 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, LCD=ON (no panel load, Vc2 reference, 1/3bias), Super economy mode (100-pin/80-pin package or chip) 8 μA OSC1=32 kHz, RTC=ON, CPU=OSC1 4 μA
RUN mode	1.2 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, LCD=ON (no panel load, Vc2 reference, 1/3bias), Super economy mode (100-pin/80-pin package or chip) 8 μA OSC1=32 kHz, RTC=ON, CPU=OSC1
RUN mode	1.2 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, LCD=ON (no panel load, Vc2 reference, 1/3bias), Super economy mode (100-pin/80-pin package or chip) 8 μA OSC1=32 kHz, RTC=ON, CPU=OSC1 4 μA
RUN mode	1.2 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, LCD=ON (no panel load, Vc2 reference, 1/3bias), Super economy mode (100-pin/80-pin package or chip) 8 μA OSC1=32 kHz, RTC=ON, CPU=OSC1 4 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, Super economy mode (100-pin/80-pin package or chip)
	1.2 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, LCD=ON (no panel load, Vc2 reference, 1/3bias), Super economy mode (100-pin/80-pin package or chip) 8 μA OSC1=32 kHz, RTC=ON, CPU=OSC1 4 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, Super economy mode (100-pin/80-pin package or chip) 250 μA
RUN mode Shipping form 1*3	1.2 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, LCD=ON (no panel load, Vc2 reference, 1/3bias), Super economy mode (100-pin/80-pin package or chip) 8 μA OSC1=32 kHz, RTC=ON, CPU=OSC1 4 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, Super economy mode (100-pin/80-pin package or chip) 250 μA OSC3=1MHz (ceramic oscillator), OSC1=32kHz, RTC=ON, CPU=OSC3
Shipping form	1.2 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, LCD=ON (no panel load, Vc2 reference, 1/3bias), Super economy mode (100-pin/80-pin package or chip) 8 μA OSC1=32 kHz, RTC=ON, CPU=OSC1 4 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, Super economy mode (100-pin/80-pin package or chip) 250 μA OSC3=1MHz (ceramic oscillator), OSC1=32kHz, RTC=ON, CPU=OSC3
Shipping form	1.2 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, LCD=ON (no panel load, Vc2 reference, 1/3bias), Super economy mode (100-pin/80-pin package or chip) 8 μA OSC1=32 kHz, RTC=ON, CPU=OSC1 4 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, Super economy mode (100-pin/80-pin package or chip) 250 μA OSC3=1MHz (ceramic oscillator), OSC1=32kHz, RTC=ON, CPU=OSC3 SQFN9-64pin(P-VQFN064-0909-0.50, 9 × 9 mm, t = 1 mm, 0.5 mm pitch) TQFP13-64pin(P-TQFP064-1010-0.50, 10 × 10 mm, t = 1.2 mm, 0.5 mm pitch)
Shipping form 1'3 2 '3	1.2 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, LCD=ON (no panel load, Vc2 reference, 1/3bias), Super economy mode (100-pin/80-pin package or chip) 8 μA OSC1=32 kHz, RTC=ON, CPU=OSC1 4 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, Super economy mode (100-pin/80-pin package or chip) 250 μA OSC3=1MHz (ceramic oscillator), OSC1=32kHz, RTC=ON, CPU=OSC3 SQFN9-64pin(P-VQFN064-0909-0.50, 9 × 9 mm, t = 1 mm, 0.5 mm pitch) TQFP13-64pin(P-TQFP064-1010-0.50, 10 × 10 mm, t = 1.2 mm, 0.5 mm pitch) QFP14-80pin(P-LQFP080-1212-0.50, 12 × 12 mm, t = 1.7 mm, 0.5 mm pitch)
Shipping form 1 '3 2 '3 3 *3	1.2 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, LCD=ON (no panel load, Vc2 reference, 1/3bias), Super economy mode (100-pin/80-pin package or chip) 8 μA OSC1=32 kHz, RTC=ON, CPU=OSC1 4 μA OSC1=32 kHz, RTC=ON, CPU=OSC1, Super economy mode (100-pin/80-pin package or chip) 250 μA OSC3=1MHz (ceramic oscillator), OSC1=32kHz, RTC=ON, CPU=OSC3 SQFN9-64pin(P-VQFN064-0909-0.50, 9 × 9 mm, t = 1 mm, 0.5 mm pitch) TQFP13-64pin(P-TQFP064-1010-0.50, 10 × 10 mm, t = 1.2 mm, 0.5 mm pitch)

^{*1} The input filter in I2C (SDA and SCL inputs) does not comply with the standard for removing noise spikes less than 50 ns.

^{*2} The RAM retains data even in SLEEP mode.

^{*3} Shown in parentheses are JEITA package names.

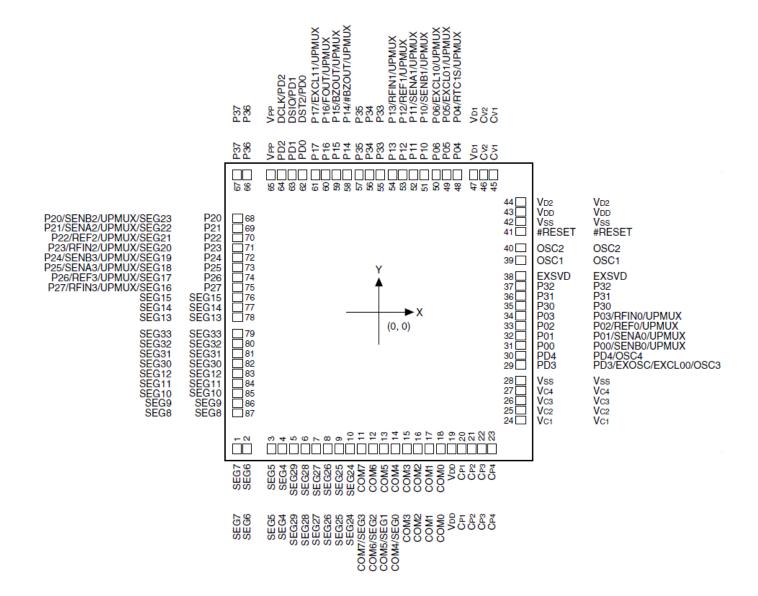
■ BLOCK DIAGRAM



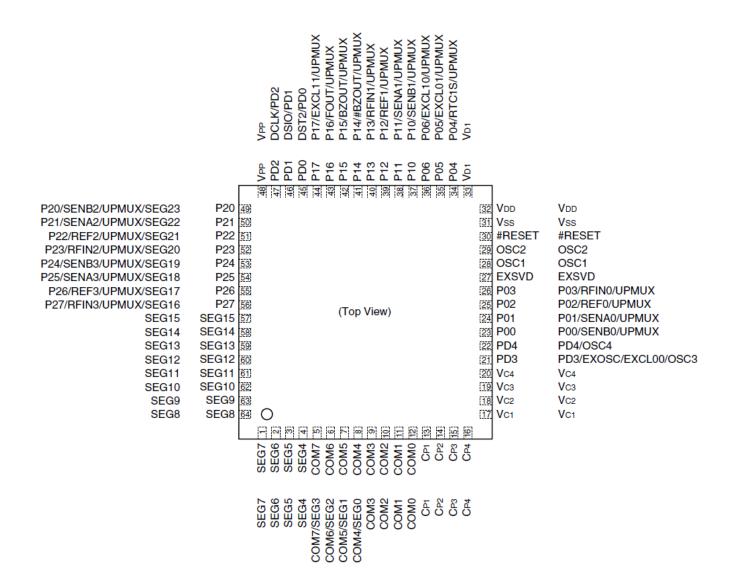
- *1 These pins do not exist in the 64-pin package.
- *2 These pins do not exist in the 80-pin package.

PIN CONFIGURATION DIAGRAM

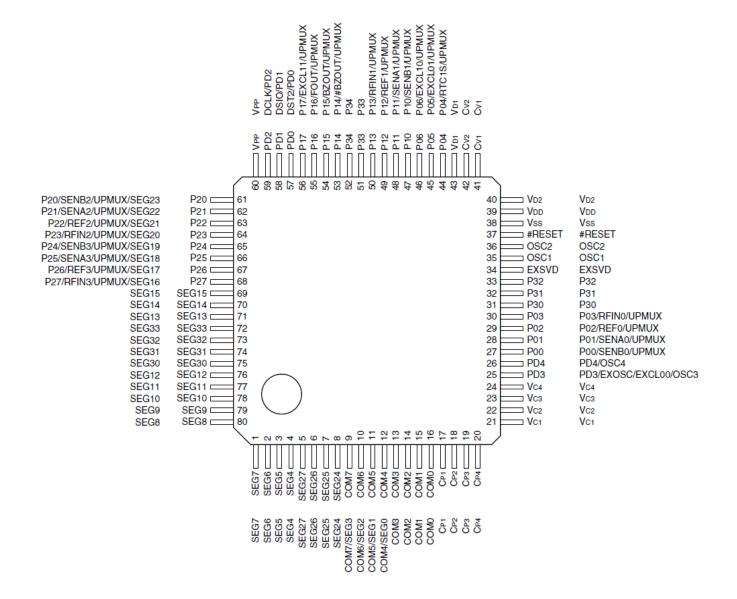
Die form



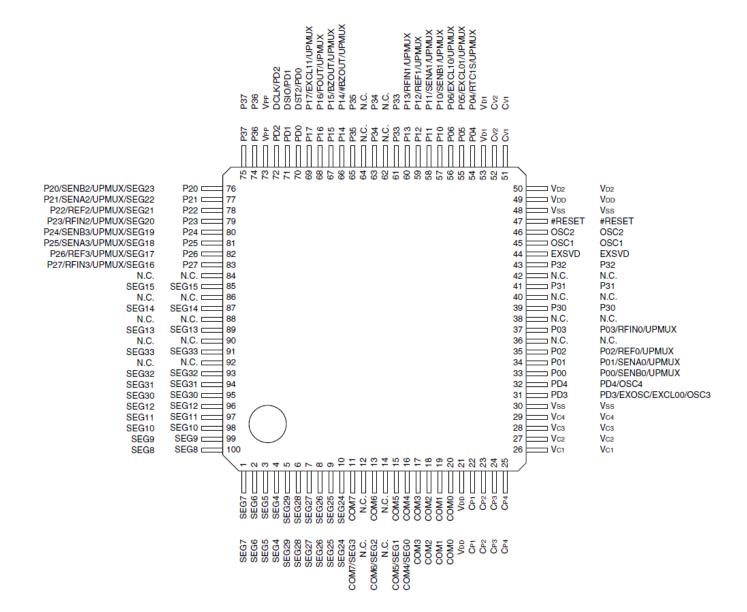
SQFN9-64pin, TQFP13-64pin



QFP14-80pin



QFP15-100pin



■ PIN DESCRIPTIONS

Initial state:

Assigned signal: The signal listed at the top of each pin is assigned in the initial state. The pin function must be switched via software to

assign another signal (see the "I/O Ports" chapter).

I/O:

I = Input
O = Output
I/O = Input/output
P = Power supply
A = Analog signal

Hi-Z = High impedance state
I (Pull-up) = Input with pulled up

I (Pull-down) = Input with pulled down
Hi-Z = High impedance state
O (H) = High level output
O (L) = Low level output

Tolerant fail-safe structure: = Over voltage tolerant fail-safe type I/O cell included (see the "I/O Ports" chapter)

Pin/pad Assigne	Assigned		Initial	Tolerant			Package		
name	signal	I/O	state	fail-safe structure	Function	64pin	80pin	100pin /Chip	
VDD	VDD	Р	-	-	Power supply (+)		1	1	
VSS	VSS	Р	-	-	GND		1	1	
VPP	VPP	Р	-	-	Power supply for Flash programming	1	1	1	
VD1	VD1	Α	-	-	DC-DC converter output		1	1	
VD2	VD2	Α	-	-	DC-DC converter stabilization capacitor connect pin	-	1	1	
CV1-2	CV1-2	Α	-	-	DC-DC converter charge pump capacitor connect pins	-	1	1	
VC1-4	VC1-4	Р	-	-	LCD panel driver power supply	1	1	1	
CP1-4	CP1-4	Α	-	-	LCD power supply booster capacitor connect pins	1	1	1	
OSC1	OSC1	Α	-	-	OSC1 oscillator circuit input	1	1	1	
OSC2	OSC2	Α	-	-	OSC1 oscillator circuit output	1	1	1	
#RESET	#RESET	- 1	I (Pull-up)	-	Reset input	1	1	1	
P00	P00	I/O	Hi-Z	-	I/O port	1	1	1	
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1	
	SENB0	I/O/A			R/F converter Ch.0 sensor B oscillator pin	1	1	1	
P01	P01	I/O	Hi-Z	-	I/O port	1	1	1	
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1	
	SENA0	I/O/A			R/F converter Ch.0 sensor A oscillator pin	1	1	1	
P02	P02	I/O	Hi-Z	-	I/O port		1	1	
	UPMUX	I/O			User-selected I/O (universal port multiplexer)		1	1	
	REF0	I/O/A			R/F converter Ch.0 reference oscillator pin	1	1	1	
P03	P03	I/O	Hi-Z	-	I/O port	1	1	1	
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1	
	RFIN0	I/O/A			R/F converter Ch.0 oscillation input	1	1	1	
P04	P04	I/O	Hi-Z	-	I/O port	1	1	1	
	RTC1S	0			Real-time clock 1-second cycle pulse output		1	1	
	UPMUX	I/O			User-selected I/O (universal port multiplexer)		1	1	
P05	P05	I/O	Hi-Z	-	I/O port	1	1	1	
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1	
	EXCL01	1			16-bit PWM timer Ch.0 event counter input 1	1	1	1	
P06	P06	I/O	Hi-Z	-	I/O port	1	1	1	
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1	
	EXCL10	ı			16-bit PWM timer Ch.1 event counter input 0	1	1	1	
P10	P10	I/O	Hi-Z	-	I/O port	1	1	1	
	UPMUX	I/O			User-selected I/O (universal port multiplexer)		1	1	
	SENB1	I/O			R/F converter Ch.1 sensor B oscillator pin		1	1	
P11	P11	I/O	Hi-Z	-	I/O port	1	1	1	
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1	
	SENA1	I/O			R/F converter Ch.1 sensor A oscillator pin	/	/	1	

Pin/pad name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function	64pin	Package 80pin	100pin /Chip
P12	P12	I/O	Hi-Z	-	I/O port	1	1	1
	UPMUX	I/O	1		User-selected I/O (universal port multiplexer)	1	1	1
	REF1	I/O			R/F converter Ch.1 reference oscillator pin	1	1	1
P13	P13	I/O	Hi-Z	-	I/O port	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1
	RFIN1	0			R/F converter Ch.1 oscillation input	1	1	1
P14	P14	I/O	Hi-Z	-	I/O port	1	1	1
	#BZOUT	0			Sound generator inverted output	1	1	1
	UPMUX	I/O	1		User-selected I/O (universal port multiplexer)	1	1	1
P15	P15	I/O	Hi-Z	-	I/O port	1	1	1
	BZOUT	0			Sound generator output	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1
P16	P16	I/O	Hi-Z	-	I/O port	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1
	FOUT	0			Clock external output	1	1	1
P17	P17	I/O	Hi-Z	-	I/O port	1	1	1
	UPMUX	I/O	1		User-selected I/O (universal port multiplexer)	1	1	1
	EXCL11	Α	1		16-bit PWM timer Ch.1 event counter input 1	1	1	1
P20	P20	I/O	Hi-Z	/	I/O port	1	1	1
	UPMUX	I/O	1		User-selected I/O (universal port multiplexer)	/	/	1
	SENB2	I/O	1		R/F converter Ch.2 sensor B oscillator pin	/	/	1
	SEG23	Α	1		LCD segment output	1	1	1
P21	P21	I/O	Hi-Z	/	I/O port	1	1	1
	UPMUX	I/O	1		User-selected I/O (universal port multiplexer)	/	/	1
	SENA2	I/O	1		R/F converter Ch.2 sensor A oscillator pin	1	1	1
	SEG22	Α			LCD segment output	1	1	1
P22	P22	I/O	Hi-Z	/	I/O port	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1
	REF2	I/O			R/F converter Ch.2 reference oscillator pin	1	1	1
	SEG21	Α			LCD segment output	1	1	1
P23	P23	I/O	Hi-Z	/	I/O port	1	1	1
	UPMUX	I/O	1		User-selected I/O (universal port multiplexer)	/	/	1
	RFIN2	I/O			R/F converter Ch.2 oscillation input	1	1	1
	SEG20	Α	1		LCD segment output	/	1	1
P24	P24	I/O	Hi-Z	/	I/O port	1	1	1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	1	1	1
	SENB3	I/O			R/F converter Ch.3 sensor B oscillator pin	1	1	1
	SEG19	Α	1		LCD segment output	/	/	1
P25	P25	I/O	Hi-Z	1	I/O port	/	/	1
	UPMUX	I/O	1		User-selected I/O (universal port multiplexer)	/	1	1
	SENA3	I/O	1		R/F converter Ch.3 sensor A oscillator pin	1	1	1
	SEG18	Α	1		LCD segment output	/	1	1
P26	P26	I/O	Hi-Z	/	I/O port	1	1	1
	UPMUX	I/O	1		User-selected I/O (universal port multiplexer)	/	1	1
	REF3	Α	1		R/F converter Ch.3 reference oscillator pin	/	1	1
	SEG17	Α	1		LCD segment output	/	1	1
P27	P27	I/O	Hi-Z	/	I/O port	1	1	1
	UPMUX	I/O	1		User-selected I/O (universal port multiplexer)	1	1	1
	RFIN3	I/O	1		R/F converter Ch.3 oscillation input	/	1	1
	SEG16	Α	†		LCD segment output	1	1	1

Din/nod	Assigned		Initial	Tolerant		Package		
Pin/pad name	Assigned signal	I/O	state	fail-safe structure	Function	64pin	80pin	100pin /Chip
P30	P30	I/O	Hi-Z	-	I/O port	-	1	✓
P31	P31	I/O	Hi-Z	-	I/O port	-	1	✓
P32	P32	I/O	Hi-Z	-	I/O port	-	1	✓
P33	P33	I/O	Hi-Z	-	I/O port	-	1	✓
P34	P34	I/O	Hi-Z	-	I/O port	-	1	✓
P35	P35	I/O	Hi-Z	-	I/O port	-	-	✓
P36	P36	I/O	Hi-Z	-	I/O port	-	-	✓
P37	P37	I/O	Hi-Z	-	I/O port	-	-	✓
PD0	DST2	0	O (L)	-	On-chip debugger status output	/	1	1
	PD0	I/O			I/O port	/	1	✓
PD1	DSIO	I/O	I (Pull-up)	-	On-chip debugger data input/output	/	1	✓
	PD1	I/O			I/O port	✓	1	1
PD2	DCLK	I/O	O(H)	-	On-chip debugger clock output	✓	1	1
	PD2	0			Output port		1	1
PD3	PD3	I/O	Hi-Z	-	I/O port	1	1	1
	EXOSC	ı			Clock generator external clock input	✓	1	1
	EXCL00	ı			16-bit PWM timer Ch.0 event counter input 0	✓	1	1
	OSC3	Α			OSC3 oscillator circuit input	1	1	1
PD4	PD4	I/O	Hi-Z	-	I/O port	✓	1	1
	OSC4	Α			OSC3 oscillator circuit output	✓	1	1
COM0-3	COM0-3	Α	Hi-Z	-	LCD common output	✓	1	1
COM4	COM4	Α	Hi-Z	-	LCD common output	✓	1	1
	SEG0	Α			LCD segment output		1	1
COM5	COM5	Α	Hi-Z	- LCD common output		✓	1	1
	SEG1	Α		LCD segment output		✓	1	1
COM6	COM6	Α	Hi-Z	-	LCD common output	✓	1	1
	SEG2	Α			LCD segment output	✓	1	1
COM7	COM7	Α	Hi-Z	-	LCD common output	1	1	1
	SEG3	Α			LCD segment output	✓	1	1
SEG4-15	SEG4-15	Α	Hi-Z	-	LCD segment output	1	1	1
SEG24-27	SEG24-27	Α	Hi-Z	-	LCD segment output - ✓		1	
SEG28-29	SEG28-29	Α	Hi-Z	-	, ,		1	
SEG30-33	SEG30-33	Α	Hi-Z	-			1	
EXSVD	EXSVD	Α	A (I)	-	External power supply voltage detection input	✓	1	1

Note: In the peripheral circuit descriptions, the assigned signal name is used as the pin name.

Universal port multiplexer (UPMUX)

The universal port multiplexer (UPMUX) allows software to select the peripheral circuit input/output function to be assigned to each pin from those listed below.

Peripheral circuit	Signal to be assigned	I/O	Channel number n	Function
Synchronous serial	SDIn	I	<i>n</i> =0	SPIA Ch.n data input
interface (SPIA)	SDOn	0		SPIA Ch.n data output
(SFIA)	SPICLKn	I/O		SPIA Ch.n clock input/output
	#SPISSn	I		SPIA Ch.n slave-select input
I ² C	SCLn	I/O	<i>n</i> =0	I2C Ch.n clock input/output
(I2C)	SDAn	I/O		I2C Ch.n data input/output
UART (UART)	USINn	I	<i>n</i> =0,1	UART Ch.n data input
	USOUTn	0		UART Ch.n data output
16-bit PWM timer	TOUTn0/CAPn0	I/O	<i>n</i> -0,1	T16B Ch.n PWM output/capture input 0
(T16B)	TOUTn1/CAPn1	I/O		T16B Ch.n PWM output/capture input 1

Note: Do not assign a function to two or more pins simultaneously.

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