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S1C63 Family Application Note

S1C6F016 Software Development Supplementary Document

Target Products: S1C63016/008/004/003

SEIKO EPSON CORPORATION

Rev.1.0

Evaluation board/kit and Development tool important notice

1. This evaluation board/kit or development tool is designed for use for engineering evaluation, demonstration, or development purposes only. Do not use it for other purpose. It is not intended to meet the requirement of design for finished product.
2. This evaluation board/kit or development tool is intended for use by an electronics engineer, and it is not the product for consumer. The user should use this goods properly and safely. Seiko Epson dose not assume any responsibility and liability of any kind of damage and/or fire coursed by usage of it. User should cease to use it when any abnormal issue occurs even during proper and safe use.
3. The part used for this evaluation board/kit or development tool is changed without any notice.

NOTICE

Table of Contents

1. Overview

The S1C6F016 has all the required characteristics as a program development tool for the targets, S1C63016, S1C63008, S1C63004, and S1C63003. It has all the built-in peripherals those targets have. But it has to be noted that some functions including the setting of the SVD criteria voltage are not compatible between S1C6F016 and the targets. The purpose of this note is to clarify the difference of the features and specifications between S1C6F016 and the targets and to facilitate development of application programs using S1C6F016.

(Note): S1C6F016 corresponds to the largest-scale product in the target products. The functions that are unavailable with some target products can be used with S1C6F016. When developing application programs using S1C6F016, confirm the target product specifications and create the programs so as not to use the unavailable functions.

2. Features

A comparison table of the features of the Flash type microcomputer (S1C6F016) and the mask ROM type microcomputers (S1C63016/ 008/ 004/ 003) is shown below.

Function		S1C6F016	S1C63016	S1C63008	S1C63004	S1C63003
Core		4-bit core CPU S1C63000				
OSC1 oscillation circuit		32.768kHz (Typ.) crystal oscillation circuit				
OSC3 oscillation circuit		・Ceramic oscillation circuit 4.0MHz ・CR oscillation circuit (external R) 1.8MHz ・CR oscillation circuit (built-in R) 500kHz (*1)	・Ceramic oscillation circuit 4.0MHz (Typ., 3 V model) / 1.0MHz (Typ., 1.5 V model) ・CR oscillation circuit (external R) 1.8MHz (Typ., 3 V model) / 500kHz (Typ., 1.5 V model) ・CR oscillation (built-in R) 500kHz (Typ., 3 V model) / 500kHz (Typ., 1.5 V model) (*1)			・CR oscillation (built-in R) 550kHz (Typ., 3 V model) / 550kHz (Typ., 1.5 V model) (*1)
Instruction set		Basic instructions: 47 (411 instructions in total) / Addressing Mode: 8 types				
Instruction execution time		61µsec, 122µsec, 183µsec (32.768kHz When running at)				
		0.50µsec, 1.00µsec, 1.50µsec (4MHz When running at)				
ROM capacity	Code ROM	16384 × 13 bits (FLASH)	16384 × 13 bits (MASK)	8192 × 13 bits (MASK)	4096 × 13 bits (MASK)	
	Data ROM	4096 × 4 bits (FLASH)	4096 × 4 bits (MASK)	2048 × 4 bits (MASK)	1024 × 4 bits (MASK)	—
RAM capacity	Data Memory	2048 × 4 bits	2048 × 4 bits	1024 × 4 bits	512 × 4 bits	256 × 4 bits
	Display Memory	448 bits	448 bits	400 bits	288 bits	110 bits
I/O ports		24 ports (16 pins: shared with SEG pins (*1))	24 ports (16 pins: shared with SEG pins (*1))	24 ports (16 pins: shared with SEG pins (*1))	20 ports (12 pins: shared with SEG pins (*1))	16 ports (8 pins: shared with SEG pins (*1))
LCD Driver		56 seg (Max. *1) × 8-3 com	56 seg (Max. *1) × 8-3 com	50 seg (Max. *1) × 8-3 com	36 seg (Max. *1) × 8-3 com	22 seg (Max. *1) × 5-3 com
Serial interface		1 port (8-bit clock synchronous type, with SPI supported)				—
Clock timer		Built-in				
Stopwatch timer		1/1000 sec, with direct key input function				Input direct key No function
Programmable timer (Event input / PWM output)		8-bit timer × 4-channel		8-bit timer × 3-channel		8-bit timer × 1-channel
Watchdog timer		Built-in				
Sound generator		With envelope and 1-shot output functions				
R/F converter		DC × 1-channel, DC/AC × 1-channel, with 20-bit counter / channel (supporting resistive humidity sensors) (8 pins for R/F converter: shared with SEG pins (*1))				
This function is not included		8-bit accumulator × 1 channel Multiplication: 8 bits × 8 bits → 16-bit product Division: 16 bits / 8 bits → 8-bit quotient and 8-bit remainder			—	
Supply voltage detection (SVD) circuit		Programmable 16 detection levels	Programmable 29 detection levels			—
External interrupt		Key input : 8 systems				4 systems
Internal interrupt		Watchdog timer (NMI) : 1 system				
		Clock timer : 8 systems				4 systems
		Stopwatch timer : 4 systems				2 systems
		Programmable timer : 8 systems		6 systems		1 system
		Serial Interface : 1 system				—
		R/F converter : 3 systems				

(*1) : Can be selected with mask option.

Product Specification	S1C6F016	S1C63016	S1C63008	S1C63004	S1C63003
Chip size	4.037mm ×3.775mm	2.655mm × 2.677mm	2.459mm × 2.501mm	2.195mm × 2.500mm	1.890mm × 1.900mm
Chip thickness	400µm	400µm	400µm	400µm	400µm
Pad spacing (Min.)	100µm	90µm			
Pad opening	85×87µm	77×85µm			
Power supply voltage	1.8 V to 3.6 V	1.8 to 5.5V (3V normal type) / 1.1 to 1.7V (1.5V low-voltage type) (*1)			
Operating temperature	-20 °C to 70 °C	-40 °C to 85 °C			
Current consumption In SLEEP	0.7µA	0.1µA			
In HALT (32kHz)	2.0µA	0.5µA			
In HALT and LCD On (32kHz)	2.8µA (*2)	0.98µA (*2)	0.95µA (*2)	0.9µA (*2)	0.62µA (*2)
During operation (32kHz)	9.0µA	2.3µA (3V model) / 2.0µA (1.5V model)			
During operation (4MHz / 1MHz)	950µA(4MHz)	220µA (4MHz, 3V model) / 60µA (1MHz, 1.5V model)			40µA (550kHz, 3V model) / 30µA (550kHz,1.5Vmodel)
Shipment form	Chip / QFP15-100	Chip / QFP15-100 / TQFP14-100		Chip / QFP14-80/ TQFP14-100	Chip / QFP12-48
Development tool	ICE : S5U1C63000H2 or S5U1C63000H6 PRC: S5U1C63000P6100 Add-on board : S5U1C6F016P2100 Flash Writer : S5U1C88000W4100 (only S1C6F016)				

(*1) : Can be selected with mask option.

(*2) : Varies depending on the number of segments
The values are in the following cases, respectively: 36 segments × 8 commons (S1C6F016 / 63016), 30 segments × 8 commons (S1C63008) , 20 segments × 8 commons (S1C63004). and 10 segments × 5 commons (S1C63003)

<Notes for target product selections and program developments>

(1) S1C6F016 is package-compatible with S1C63016 / 008 (QFP15-100 only), but not compatible with other target products. However, the alignment sequence of functional pins is the same.
(2) For the chip size and the pad location, S1C6F016 is not compatible with all target products. However, the alignment sequence of functional pads is the same.
(3) The operating supply voltage range of S1C6F016 is different from that of all target products. (For the target products, the range of 1.8 to 5.5V (3V normal type) or 1.1 to 1.7V (1.5V low-voltage type) can be selected by the mask option.) Refer to “Recommended Operating Conditions” in Technical Manual for details.
(4) The electrical characteristics of S1C6F016 are different from those of all target products, due to the differences of manufacturing processes. Refer to “Electrical Characteristics” in Technical Manual of the target product, for details.
(5) When developing programs using S1C6F016, make enough considerations on the following functional differences, and confirm the operations.

- The capacities of code ROM, data ROM, work RAM and display memory are different among each product.
  Develop programs in consideration of the capacities of the target product.
- Note the differences of the stack area.
- The number of available SEG pins is different according to the target product.
- Do not access the unavailable peripheral circuit registers with each target product. These unavailable registers cannot operate normally.
- The SVD function of S1C6F016 is different from that of target products. For S1C6F016 the voltage setting with only 16 levels is available by using 4 bits of the comparison voltage setting register SVDS[3:0] of FF04. On the other hand, for the target products, the voltage setting with 29 levels is available by using 5 bits of the comparison voltage setting register SVDS[4:0] of FF04 and FF05(D2). For the target products, when setting the comparison voltage to the level that is available with S1C6F016, set the bit of SVDS[4] of FF05(D2) to “1”. When setting the comparison voltage to the level that is available only with the target products in a lower voltage range, set the bit of SVDS[4] of FF05(D2) to “0” at program developments, though this function is not implemented in S1C6F016.

3. Pins and Packages

PIN / PAD correspondence tables of S1C6F016 and the target products (S1C63016 / 008 / 004 / 003) and the handling for unused pins in user systems are described below. For the detailed functional descriptions of each pin, refer to “2.2 Pin Description” in Technical Manual of S1C6F016 and target products.

Table 3.1 Comparison table of functional pins

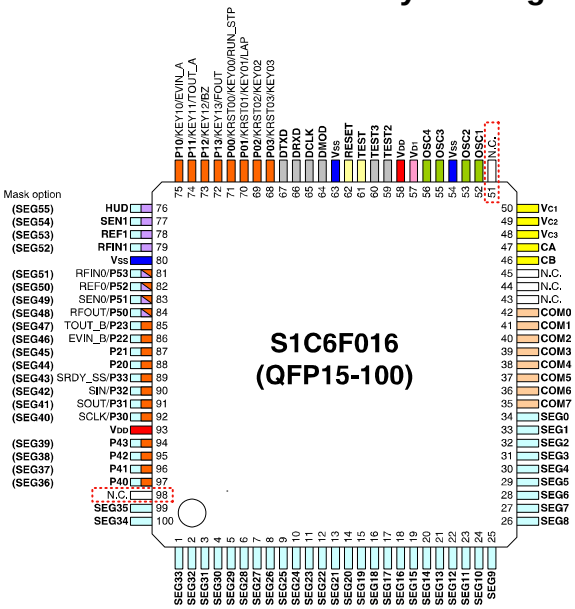
Pin/Pad Name	S1C6F016	S1C63016	S1C63008	S1C63004	S1C63003
V_{DD}	○	○	○	○	○
V_{SS}	○	○	○	○	○
V_{OSC}	—	○	○	○	○
V_{D1}	○	○	○	○	○
V_{C1}- V_{C3}	○	○	○	○	○
CA-CB	○	○	○	○	○
OSC1	○	○	○	○	○
OSC2	○	○	○	○	○
OSC3	○	○	○	○	—
OSC4	○	○	○	○	—
RESET	○	○	○	○	○
TEST	○	○	○	○	○
TEST1	○	—	—	—	—
TEST2	○	—	—	—	—
TEST3	○	—	—	—	—
DMOD	○	—	—	—	—
DCLK	○	—	—	—	—
DRXD	○	—	—	—	—
DTXD	○	—	—	—	—
COM0-4	○	○	○	○	○
COM5-7	○	○	○	○	—
SEG0-9	○	○	○	○	○
SEG10-19	○	○	○	○	—
SEG20-29	○	○	○	—	—
SEG30-35	○	○	—	—	—
HUD / SEG55	○	○	○	○	○
SEN1 / SEG54	○	○	○	○	○
REF1 / SEG53	○	○	○	○	○
RFIN1 / SEG52	○	○	○	○	○
RFIN0/ P53 / SEG51	○	○	○	○	○
REF0/ P52 / SEG50	○	○	○	○	○
SEN0/ P51 / SEG49	○	○	○	○	○
RFOUT/ P50 / SEG48	○	○	○	○	○

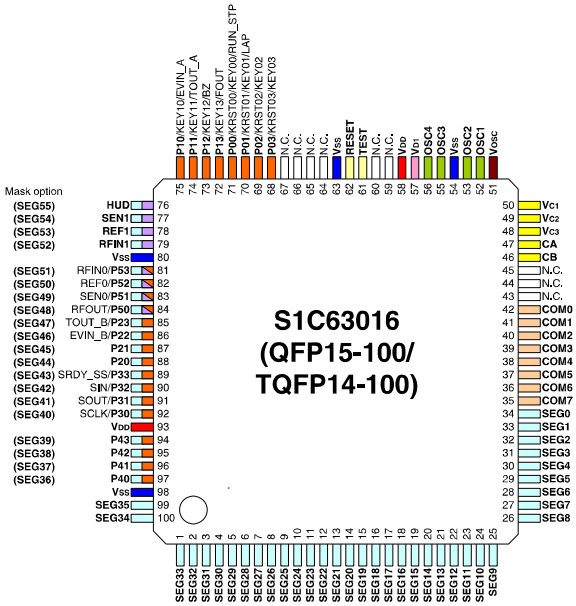
Pin/Pad Name	S1C6F016	S1C63016	S1C63008	S1C63004	S1C63003
P00/ KRST00/ KEY00/ RUN_STOP	○	○	○	○	○
P01/ KRST01/ KEY01/ LAP	○	○	○	○	○
P02/ KRST02/ KEY02	○	○	○	○	○
P03 / KRST03/ KEY03	○	○	○	○	○
P10/ KEY10/ EVIN_A	○	○	○	○	○
P11/ KEY11/ TOUT_A	○	○	○	○	○
P12/ KEY12/ BZ	○	○	○	○	○
P13/ KEY13/ FOUT	○	○	○	○	○
P20 / SEG44	○	○	○	○	○
P21 / SEG45	○	○	○	○	○
P22/ EVIN_B / SEG46	○	○	○	○	○ *1
P23/ TOUT_B / SEG47	○	○	○	○	○ *2
P30/ SCLK / SEG40	○	○	○	○	—
P31/ SOUT / SEG41	○	○	○	○	—
P32/ SIN / SEG42	○	○	○	○	—
P33/ SRDY-SS / SEG43	○	○	○	○	—
P40 / SEG36	○	○	○	—	—
P41 / SEG37	○	○	○	—	—
P42 / SEG38	○	○	○	—	—
P43 / SEG39	○	○	○	—	—

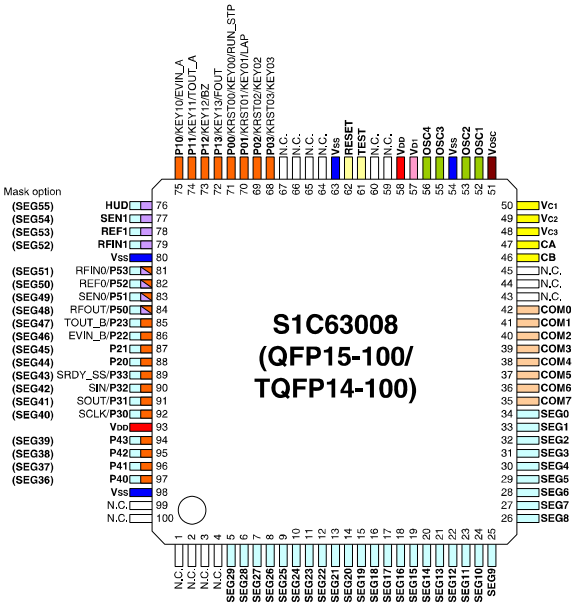
*1: EVIN_B is not included

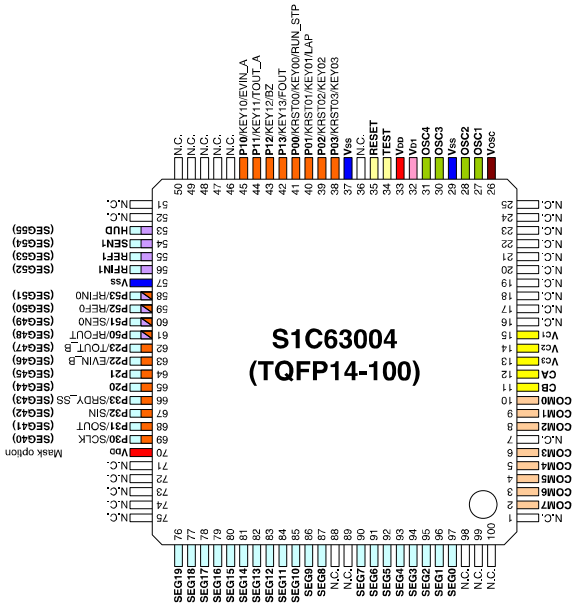
*2: TOUT_B is not included

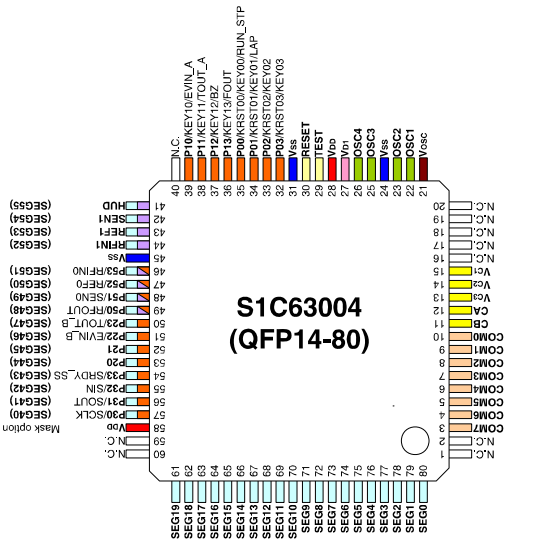
3.1 C63000 Series Pin Layout Diagrams

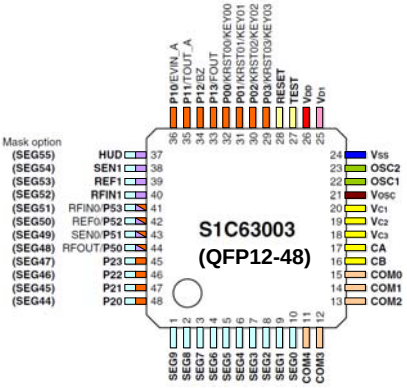


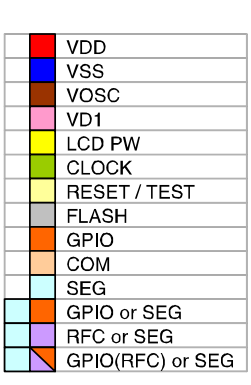




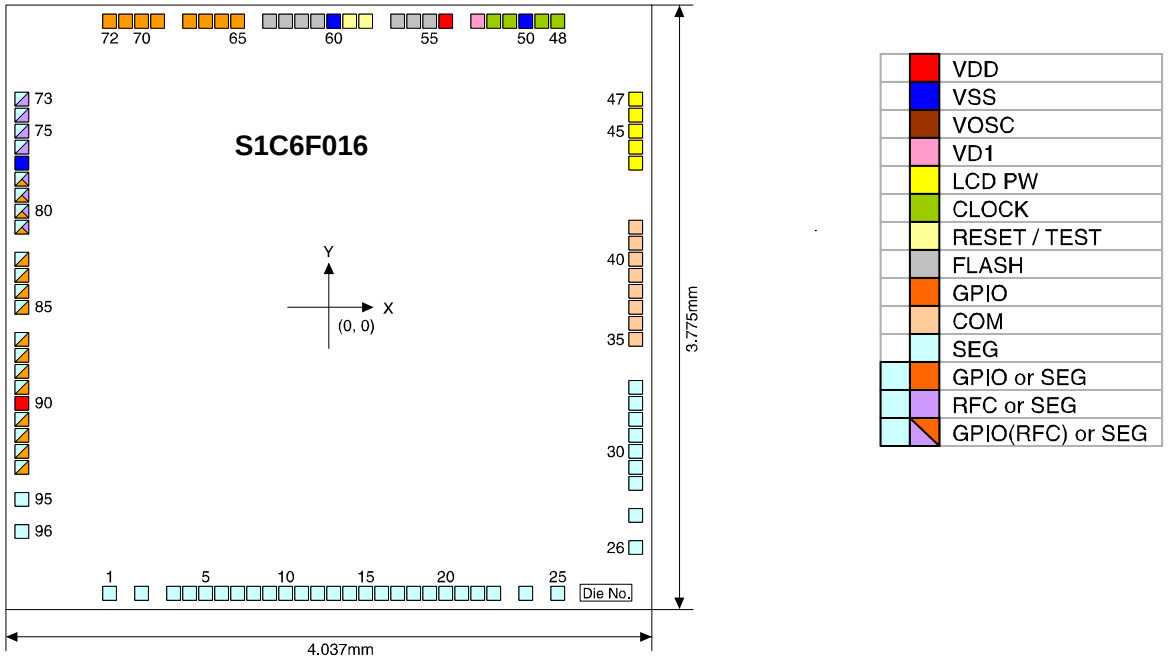


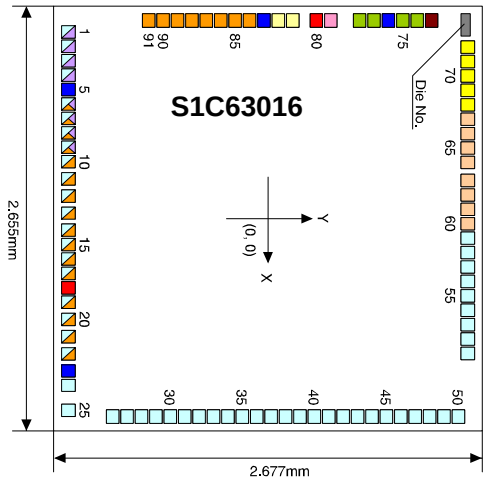


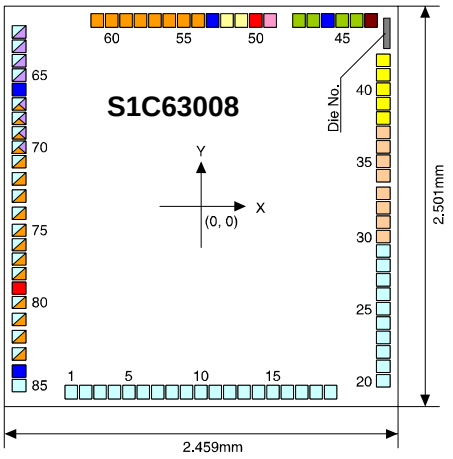


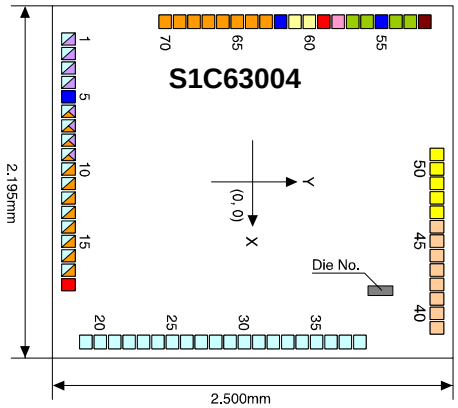


3.2 C63000 Series Pad Layout Diagrams









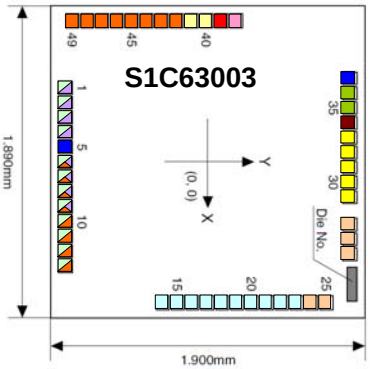


Table 3.2 Pad correspondence table of S1C6F016 and target products (S1C63016 / 008 / 004 / 003) (1)

S1C6F016				S1C63016			
PAD No.	Signal Name	Pad center coordinate X	Pad center coordinate Y	PAD No.	Signal Name	Pad center coordinate X	Pad center coordinate Y
1	SEG33	-1369.0	-1786.5	26	SEG33	1236.5	-971.0
2	SEG32	-1169.0	-1786.5	27	SEG32	1236.5	-881.0
3	SEG31	-969.0	-1786.5	28	SEG31	1236.5	-791.0
4	SEG30	-869.0	-1786.5	29	SEG30	1236.5	-701.0
5	SEG29	-769.0	-1786.5	30	SEG29	1236.5	-611.0
6	SEG28	-669.0	-1786.5	31	SEG28	1236.5	-521.0
7	SEG27	-569.0	-1786.5	32	SEG27	1236.5	-431.0
8	SEG26	-469.0	-1786.5	33	SEG26	1236.5	-341.0
9	SEG25	-369.0	-1786.5	34	SEG25	1236.5	-251.0
10	SEG24	-269.0	-1786.5	35	SEG24	1236.5	-161.0
11	SEG23	-169.0	-1786.5	36	SEG23	1236.5	-71.0
12	SEG22	-69.0	-1786.5	37	SEG22	1236.5	19.0
13	SEG21	31.0	-1786.5	38	SEG21	1236.5	109.0
14	SEG20	131.0	-1786.5	39	SEG20	1236.5	199.0
15	SEG19	231.0	-1786.5	40	SEG19	1236.5	289.0
16	SEG18	331.0	-1786.5	41	SEG18	1236.5	379.0
17	SEG17	431.0	-1786.5	42	SEG17	1236.5	469.0
18	SEG16	531.0	-1786.5	43	SEG16	1236.5	559.0
19	SEG15	631.0	-1786.5	44	SEG15	1236.5	649.0
20	SEG14	731.0	-1786.5	45	SEG14	1236.5	739.0
21	SEG13	831.0	-1786.5	46	SEG13	1236.5	829.0
22	SEG12	931.0	-1786.5	47	SEG12	1236.5	919.0
23	SEG11	1031.0	-1786.5	48	SEG11	1236.5	1009.0
24	SEG10	1231.0	-1786.5	49	SEG10	1236.5	1099.0
25	SEG9	1431.0	-1786.5	50	SEG9	1236.5	1189.0
26	SEG8	1917.5	-1500.0	51	SEG8	842.0	1247.5
27	SEG7	1917.5	-1300.0	52	SEG7	752.0	1247.5
28	SEG6	1917.5	-1100.0	53	SEG6	662.0	1247.5
29	SEG5	1917.5	-1000.0	54	SEG5	572.0	1247.5
30	SEG4	1917.5	-900.0	55	SEG4	482.0	1247.5
31	SEG3	1917.5	-800.0	56	SEG3	392.0	1247.5
32	SEG2	1917.5	-700.0	57	SEG2	302.0	1247.5
33	SEG1	1917.5	-600.0	58	SEG1	212.0	1247.5
34	SEG0	1917.5	-500.0	59	SEG0	122.0	1247.5
35	COM7	1917.5	-200.0	60	COM7	32.0	1247.5
36	COM6	1917.5	-100.0	61	COM6	-58.0	1247.5
37	COM5	1917.5	0.0	62	COM5	-148.0	1247.5
38	COM4	1917.5	100.0	63	COM4	-238.0	1247.5
39	COM3	1917.5	200.0	64	COM3	-351.0	1247.5
40	COM2	1917.5	300.0	65	COM2	-441.0	1247.5
41	COM1	1917.5	400.0	66	COM1	-531.0	1247.5
42	COM0	1917.5	500.0	67	COM0	-621.0	1247.5
43	CB	1917.5	900.0	68	CB	-711.0	1247.5
44	CA	1917.5	1000.0	69	CA	-801.0	1247.5
45	V_{C3}	1917.5	1100.0	70	V_{C3}	-891.0	1247.5
46	V_{C2}	1917.5	1200.0	71	V_{C2}	-981.0	1247.5
47	V_{C1}	1917.5	1300.0	72	V_{C1}	-1071.0	1247.5
—	—	—	—	73	V_{OSC}	-1236.5	1023.0
48	OSC1	1431.0	1786.5	74	OSC1	-1236.5	933.0
49	OSC2	1331.0	1786.5	75	OSC2	-1236.5	843.0
50	V_{SS}	1231.0	1786.5	76	V_{SS}	-1236.5	753.0
51	OSC3	1131.0	1786.5	77	OSC3	-1236.5	663.0
52	OSC4	1031.0	1786.5	78	OSC4	-1236.5	573.0
53	V_{D1}	931.0	1786.5	79	V_{D1}	-1236.5	393.0
54	V_{DD}	731.0	1786.5	80	V_{DD}	-1236.5	303.0
55	TEST1	631.0	1786.5	—	—	—	—
56	TEST2	531.0	1786.5	—	—	—	—
57	TEST3	431.0	1786.5	—	—	—	—
58	TEST	231.0	1786.5	81	TEST	-1236.5	154.0
59	RESET	131.0	1786.5	82	RESET	-1236.5	64.0
60	V_{SS}	31.0	1786.5	83	V_{SS}	-1236.5	-26.0
61	DM0D	-69.0	1786.5	—	—	—	—
62	DCLK	-169.0	1786.5	—	—	—	—
63	DRXD	-269.0	1786.5	—	—	—	—
64	DTXD	-369.0	1786.5	—	—	—	—
65	P03(KRST03/KEY03)	-569.0	1786.5	84	P03(KRST03/KEY03)	-1236.5	-116.0
66	P02(KRST02/KEY02)	-669.0	1786.5	85	P02(KRST02/KEY02)	-1236.5	-206.0
67	P01(KRST01/KEY01/LAP)	-769.0	1786.5	86	P01(KRST01/KEY01/LAP)	-1236.5	-296.0
68	P00(KRST00/KEY00/RUN)	-869.0	1786.5	87	P00(KRST00/KEY00/RUN)	-1236.5	-386.0
69	P13(KEY13/FOUT)	-1069.0	1786.5	88	P13(KEY13/FOUT)	-1236.5	-476.0
70	P12(KEY12/BZ)	-1169.0	1786.5	89	P12(KEY12/BZ)	-1236.5	-566.0
71	P11(KEY11/TOUT_A)	-1269.0	1786.5	90	P11(KEY11/TOUT_A)	-1236.5	-656.0
72	P10(KEY10/EVIN_A)	-1369.0	1786.5	91	P10(KEY10/EVIN_A)	-1236.5	-746.0
73	SEG55(HUD)	-1917.5	1300.0	1	SEG55(HUD)	-1165.0	-1247.5
74	SEG54(SEN1)	-1917.5	1200.0	2	SEG54(SEN1)	-1075.0	-1247.5
75	SEG53(REF1)	-1917.5	1100.0	3	SEG53(REF1)	-985.0	-1247.5
76	SEG52(RFIN1)	-1917.5	1000.0	4	SEG52(RFIN1)	-895.0	-1247.5
77	V_{SS}	-1917.5	900.0	5	V_{SS}	-805.0	-1247.5
78	SEG51(P53/RFIN0)	-1917.5	800.0	6	SEG51(P53/RFIN0)	-715.0	-1247.5
79	SEG50(P52/REF0)	-1917.5	700.0	7	SEG50(P52/REF0)	-625.0	-1247.5
80	SEG49(P51/SEN0)	-1917.5	600.0	8	SEG49(P51/SEN0)	-535.0	-1247.5
81	SEG48(P50/RFOUT)	-1917.5	500.0	9	SEG48(P50/RFOUT)	-445.0	-1247.5
82	SEG47(P23/TOUT_B)	-1917.5	300.0	10	SEG47(P23/TOUT_B)	-355.0	-1247.5
83	SEG46(P22/EVIN1_B)	-1917.5	200.0	11	SEG46(P22/EVIN_B)	-248.0	-1247.5
84	SEG45(P21)	-1917.5	100.0	12	SEG45(P21)	-141.0	-1247.5
85	SEG44(P20)	-1917.5	0.0	13	SEG44(P20)	-34.0	-1247.5
86	SEG43(P33/SRDY-SS)	-1917.5	-200.0	14	SEG43(P33/SRDY-SS)	73.0	-1247.5
87	SEG42(P32/SIN)	-1917.5	-300.0	15	SEG42(P32/SIN)	163.0	-1247.5
88	SEG41(P31/SOUT)	-1917.5	-400.0	16	SEG41(P31/SOUT)	253.0	-1247.5
89	SEG40(P30/SCLK)	-1917.5	-500.0	17	SEG40(P30/SCLK)	343.0	-1247.5
90	V_{DD}	-1917.5	-600.0	18	V_{DD}	433.0	-1247.5
91	SEG39(P43)	-1917.5	-700.0	19	SEG39(P43)	523.0	-1247.5
92	SEG38(P42)	-1917.5	-800.0	20	SEG38(P42)	630.0	-1247.5
93	SEG37(P41)	-1917.5	-900.0	21	SEG37(P41)	737.0	-1247.5
94	SEG36(P40)	-1917.5	-1000.0	22	SEG36(P40)	844.0	-1247.5
—	—	—	—	23	V_{SS}	951.0	-1247.5
95	SEG35	-1917.5	-1200.0	24	SEG35	1041.0	-1247.5
96	SEG34	-1917.5	-1400.0	25	SEG34	1197.0	—

Table 3.2 Pad correspondence table of S1C6F016 and target products (S1C63016 / 008 / 004 / 003) (2)

S1C6F016				S1C63008			
PAD No.	Signal Name	Pad center coordinate X	Pad center coordinate Y	PAD No.	Signal Name	Pad center coordinate X	Pad center coordinate Y
1	SEG33	-1369.0	-1786.5	—	—	—	—
2	SEG32	-1169.0	-1786.5	—	—	—	—
3	SEG31	-969.0	-1786.5	—	—	—	—
4	SEG30	-869.0	-1786.5	—	—	—	—
5	SEG29	-769.0	-1786.5	85	SEG29	-1138.5	-1118.0
6	SEG28	-669.0	-1786.5	1	SEG28	-812.0	-1159.5
7	SEG27	-569.0	-1786.5	2	SEG27	-722.0	-1159.5
8	SEG26	-469.0	-1786.5	3	SEG26	-632.0	-1159.5
9	SEG25	-369.0	-1786.5	4	SEG25	-542.0	-1159.5
10	SEG24	-269.0	-1786.5	5	SEG24	-452.0	-1159.5
11	SEG23	-169.0	-1786.5	6	SEG23	-362.0	-1159.5
12	SEG22	-69.0	-1786.5	7	SEG22	-272.0	-1159.5
13	SEG21	31.0	-1786.5	8	SEG21	-182.0	-1159.5
14	SEG20	131.0	-1786.5	9	SEG20	-92.0	-1159.5
15	SEG19	231.0	-1786.5	10	SEG19	-2.0	-1159.5
16	SEG18	331.0	-1786.5	11	SEG18	88.0	-1159.5
17	SEG17	431.0	-1786.5	12	SEG17	178.0	-1159.5
18	SEG16	531.0	-1786.5	13	SEG16	268.0	-1159.5
19	SEG15	631.0	-1786.5	14	SEG15	358.0	-1159.5
20	SEG14	731.0	-1786.5	15	SEG14	448.0	-1159.5
21	SEG13	831.0	-1786.5	16	SEG13	538.0	-1159.5
22	SEG12	931.0	-1786.5	17	SEG12	628.0	-1159.5
23	SEG11	1031.0	-1786.5	18	SEG11	718.0	-1159.5
24	SEG10	1231.0	-1786.5	19	SEG10	808.0	-1159.5
25	SEG9	1431.0	-1786.5	20	SEG9	1138.5	-1089.0
26	SEG8	1917.5	-1500.0	21	SEG8	1138.5	-999.0
27	SEG7	1917.5	-1300.0	22	SEG7	1138.5	-909.0
28	SEG6	1917.5	-1100.0	23	SEG6	1138.5	-819.0
29	SEG5	1917.5	-1000.0	24	SEG5	1138.5	-729.0
30	SEG4	1917.5	-900.0	25	SEG4	1138.5	-639.0
31	SEG3	1917.5	-800.0	26	SEG3	1138.5	-549.0
32	SEG2	1917.5	-700.0	27	SEG2	1138.5	-459.0
33	SEG1	1917.5	-600.0	28	SEG1	1138.5	-369.0
34	SEG0	1917.5	-500.0	29	SEG0	1138.5	-279.0
35	COM7	1917.5	-200.0	30	COM7	1138.5	-189.0
36	COM6	1917.5	-100.0	31	COM6	1138.5	-99.0
37	COM5	1917.5	0.0	32	COM5	1138.5	-9.0
38	COM4	1917.5	100.0	33	COM4	1138.5	81.0
39	COM3	1917.5	200.0	34	COM3	1138.5	191.0
40	COM2	1917.5	300.0	35	COM2	1138.5	281.0
41	COM1	1917.5	400.0	36	COM1	1138.5	371.0
42	COM0	1917.5	500.0	37	COM0	1138.5	461.0
43	CB	1917.5	900.0	38	CB	1138.5	551.0
44	CA	1917.5	1000.0	39	CA	1138.5	641.0
45	V_{C3}	1917.5	1100.0	40	V_{C3}	1138.5	731.0
46	V_{C2}	1917.5	1200.0	41	V_{C2}	1138.5	821.0
47	V_{C1}	1917.5	1300.0	42	V_{C1}	1138.5	911.0
—	—	—	—	43	V_{OSC}	1062.0	1159.5
48	OSC1	1431.0	1786.5	44	OSC1	972.0	1159.5
49	OSC2	1331.0	1786.5	45	OSC2	882.0	1159.5
50	V_{SS}	1231.0	1786.5	46	V_{SS}	792.0	1159.5
51	OSC3	1131.0	1786.5	47	OSC3	702.0	1159.5
52	OSC4	1031.0	1786.5	48	OSC4	612.0	1159.5
53	V_{D1}	931.0	1786.5	49	V_{D1}	432.0	1159.5
54	V_{DD}	731.0	1786.5	50	V_{DD}	342.0	1159.5
55	TEST1	631.0	1786.5	—	—	—	—
56	TEST2	531.0	1786.5	—	—	—	—
57	TEST3	431.0	1786.5	—	—	—	—
58	TEST	231.0	1786.5	51	TEST	252.0	1159.5
59	RESET	131.0	1786.5	52	RESET	162.0	1159.5
60	V_{SS}	31.0	1786.5	53	V_{SS}	72.0	1159.5
61	DM0D	-69.0	1786.5	—	—	—	—
62	DCLK	-169.0	1786.5	—	—	—	—
63	DRXD	-269.0	1786.5	—	—	—	—
64	DTXD	-369.0	1786.5	—	—	—	—
65	P03(KRST03/KEY03)	-569.0	1786.5	54	P03(KRST03/KEY03)	-18.0	1159.5
66	P02(KRST02/KEY02)	-669.0	1786.5	55	P02(KRST02/KEY02)	-108.0	1159.5
67	P01(KRST01/KEY01/LAP)	-769.0	1786.5	56	P01(KRST01/KEY01/LAP)	-198.0	1159.5
68	P00(KRST00/KEY00/RUN)	-869.0	1786.5	57	P00(KRST00/KEY00/RUN)	-288.0	1159.5
69	P13(KEY13/FOUT)	-1069.0	1786.5	58	P13(KEY13/FOUT)	-378.0	1159.5
70	P12(KEY12/BZ)	-1169.0	1786.5	59	P12(KEY12/BZ)	-468.0	1159.5
71	P11(KEY11/TOUT_A)	-1269.0	1786.5	60	P11(KEY11/TOUT_A)	-558.0	1159.5
72	P10(KEY10/EVIN_A)	-1369.0	1786.5	61	P10(KEY10/EVIN_A)	-648.0	1159.5
73	SEG55(HUD)	-1917.5	1300.0	62	SEG55(HUD)	-1138.5	1088.0
74	SEG54(SEN1)	-1917.5	1200.0	63	SEG54(SEN1)	-1138.5	998.0
75	SEG53(REF1)	-1917.5	1100.0	64	SEG53(REF1)	-1138.5	908.0
76	SEG52(RFIN1)	-1917.5	1000.0	65	SEG52(RFIN1)	-1138.5	818.0
77	V_{SS}	-1917.5	900.0	66	V_{SS}	-1138.5	728.0
78	SEG51(P53/RFIN0)	-1917.5	800.0	67	SEG51(P53/RFIN0)	-1138.5	638.0
79	SEG50(P52/REF0)	-1917.5	700.0	68	SEG50(P52/REF0)	-1138.5	548.0
80	SEG49(P51/SEN0)	-1917.5	600.0	69	SEG49(P51/SEN0)	-1138.5	458.0
81	SEG48(P50/RFOUT)	-1917.5	500.0	70	SEG48(P50/RFOUT)	-1138.5	368.0
82	SEG47(P23/TOUT_B)	-1917.5	300.0	71	SEG47(P23/TOUT_B)	-1138.5	278.0
83	SEG46(P22/EVIN1_B)	-1917.5	200.0	72	SEG46(P22/EVIN_B)	-1138.5	171.0
84	SEG45(P21)	-1917.5	100.0	73	SEG45(P21)	-1138.5	64.0
85	SEG44(P20)	-1917.5	0.0	74	SEG44(P20)	-1138.5	-43.0
86	SEG43(P33/SRDY-SS)	-1917.5	-200.0	75	SEG43(P33/SRDY-SS)	-1138.5	-150.0
87	SEG42(P32/SIN)	-1917.5	-300.0	76	SEG42(P32/SIN)	-1138.5	-240.0
88	SEG41(P31/SOUT)	-1917.5	-400.0	77	SEG41(P31/SOUT)	-1138.5	-330.0
89	SEG40(P30/SCLK)	-1917.5	-500.0	78	SEG40(P30/SCLK)	-1138.5	-420.0
90	V_{DD}	-1917.5	-600.0	79	V_{DD}	-1138.5	-510.0
91	SEG39(P43)	-1917.5	-700.0	80	SEG39(P43)	-1138.5	-600.0
92	SEG38(P42)	-1917.5	-800.0	81	SEG38(P42)	-1138.5	-707.0
93	SEG37(P41)	-1917.5	-900.0	82	SEG37(P41)	-1138.5	-814.0
94	SEG36(P40)	-1917.5	-1000.0	83	SEG36(P40)	-1138.5	-921.0
—	—	—	—	84	V_{SS}	-1138.5	-1028.0
95	SEG35	-1917.5	-1200.0	—	—	—	—
96	SEG34	-1917.5	-1400.0	—	—	—	—

Table 3.2 Pad correspondence table of S1C6F016 and target products (S1C63016 / 008 / 004 / 003) (3)

S1C6F016				S1C63004			
PAD No.	Signal Name	Pad center coordinate X	Pad center coordinate Y	PAD No.	Signal Name	Pad center coordinate X	Pad center coordinate Y
1	SEG33	-1369.0	-1786.5	—	—	—	—
2	SEG32	-1169.0	-1786.5	—	—	—	—
3	SEG31	-969.0	-1786.5	—	—	—	—
4	SEG30	-869.0	-1786.5	—	—	—	—
5	SEG29	-769.0	-1786.5	—	—	—	—
6	SEG28	-669.0	-1786.5	—	—	—	—
7	SEG27	-569.0	-1786.5	—	—	—	—
8	SEG26	-469.0	-1786.5	—	—	—	—
9	SEG25	-369.0	-1786.5	—	—	—	—
10	SEG24	-269.0	-1786.5	—	—	—	—
11	SEG23	-169.0	-1786.5	—	—	—	—
12	SEG22	-69.0	-1786.5	—	—	—	—
13	SEG21	31.0	-1786.5	—	—	—	—
14	SEG20	131.0	-1786.5	—	—	—	—
15	SEG19	231.0	-1786.5	19	SEG19	996.5	-1040.5
16	SEG18	331.0	-1786.5	20	SEG18	996.5	-950.5
17	SEG17	431.0	-1786.5	21	SEG17	996.5	-860.5
18	SEG16	531.0	-1786.5	22	SEG16	996.5	-770.5
19	SEG15	631.0	-1786.5	23	SEG15	996.5	-680.5
20	SEG14	731.0	-1786.5	24	SEG14	996.5	-590.5
21	SEG13	831.0	-1786.5	25	SEG13	996.5	-500.5
22	SEG12	931.0	-1786.5	26	SEG12	996.5	-410.5
23	SEG11	1031.0	-1786.5	27	SEG11	996.5	-320.5
24	SEG10	1231.0	-1786.5	28	SEG10	996.5	-230.5
25	SEG9	1431.0	-1786.5	29	SEG9	996.5	-140.5
26	SEG8	1917.5	-1500.0	30	SEG8	996.5	-50.5
27	SEG7	1917.5	-1300.0	31	SEG7	996.5	39.5
28	SEG6	1917.5	-1100.0	32	SEG6	996.5	129.5
29	SEG5	1917.5	-1000.0	33	SEG5	996.5	219.5
30	SEG4	1917.5	-900.0	34	SEG4	996.5	309.5
31	SEG3	1917.5	-800.0	35	SEG3	996.5	399.5
32	SEG2	1917.5	-700.0	36	SEG2	996.5	489.5
33	SEG1	1917.5	-600.0	37	SEG1	996.5	579.5
34	SEG0	1917.5	-500.0	38	SEG0	996.5	669.5
35	COM7	1917.5	-200.0	39	COM7	907.5	1149.0
36	COM6	1917.5	-100.0	40	COM6	817.5	1149.0
37	COM5	1917.5	0.0	41	COM5	727.5	1149.0
38	COM4	1917.5	100.0	42	COM4	637.5	1149.0
39	COM3	1917.5	200.0	43	COM3	547.5	1149.0
40	COM2	1917.5	300.0	44	COM2	457.5	1149.0
41	COM1	1917.5	400.0	45	COM1	367.5	1149.0
42	COM0	1917.5	500.0	46	COM0	277.5	1149.0
43	CB	1917.5	900.0	47	CB	187.5	1149.0
44	CA	1917.5	1000.0	48	CA	97.5	1149.0
45	V_{C3}	1917.5	1100.0	49	V_{C3}	7.5	1149.0
46	V_{C2}	1917.5	1200.0	50	V_{C2}	-82.5	1149.0
47	V_{C1}	1917.5	1300.0	51	V_{C1}	-172.5	1149.0
—	—	—	—	52	V_{OSC}	-996.5	1074.0
48	OSC1	1431.0	1786.5	53	OSC1	-996.5	984.0
49	OSC2	1331.0	1786.5	54	OSC2	-996.5	894.0
50	V_{SS}	1231.0	1786.5	55	V_{SS}	-996.5	804.0
51	OSC3	1131.0	1786.5	56	OSC3	-996.5	714.0
52	OSC4	1031.0	1786.5	57	OSC4	-996.5	624.0
53	V_{D1}	931.0	1786.5	58	V_{D1}	-996.5	534.0
54	V_{DD}	731.0	1786.5	59	V_{DD}	-996.5	444.0
55	TEST1	631.0	1786.5	—	—	—	—
56	TEST2	531.0	1786.5	—	—	—	—
57	TEST3	431.0	1786.5	—	—	—	—
58	TEST	231.0	1786.5	60	TEST	-996.5	354.0
59	RESET	131.0	1786.5	61	RESET	-996.5	264.0
60	V_{SS}	31.0	1786.5	62	V_{SS}	-996.5	174.0
61	DM0D	-69.0	1786.5	—	—	—	—
62	DCLK	-169.0	1786.5	—	—	—	—
63	DRXD	-269.0	1786.5	—	—	—	—
64	DTXD	-369.0	1786.5	—	—	—	—
65	P03(KRST03/KEY03)	-569.0	1786.5	63	P03(KRST03/KEY03)	-996.5	84.0
66	P02(KRST02/KEY02)	-669.0	1786.5	64	P02(KRST02/KEY02)	-996.5	-6.0
67	P01(KRST01/KEY01/LAP)	-769.0	1786.5	65	P01(KRST01/KEY01/LAP)	-996.5	-96.0
68	P00(KRST00/KEY00/RUN)	-869.0	1786.5	66	P00(KRST00/KEY00/RUN)	-996.5	-186.0
69	P13(KEY13/FOUT)	-1069.0	1786.5	67	P13(KEY13/FOUT)	-996.5	-276.0
70	P12(KEY12/BZ)	-1169.0	1786.5	68	P12(KEY12/BZ)	-996.5	-366.0
71	P11(KEY11/TOUT_A)	-1269.0	1786.5	69	P11(KEY11/TOUT_A)	-996.5	-456.0
72	P10(KEY10/EVIN_A)	-1369.0	1786.5	70	P10(KEY10/EVIN_A)	-996.5	-546.0
73	SEG55(HUD)	-1917.5	1300.0	1	SEG55(HUD)	-889.5	-1149.0
74	SEG54(SEN1)	-1917.5	1200.0	2	SEG54(SEN1)	-799.5	-1149.0
75	SEG53(REF1)	-1917.5	1100.0	3	SEG53(REF1)	-709.5	-1149.0
76	SEG52(RFIN1)	-1917.5	1000.0	4	SEG52(RFIN1)	-619.5	-1149.0
77	V_{SS}	-1917.5	900.0	5	VSS	-529.5	-1149.0
78	SEG51(P53/RFIN0)	-1917.5	800.0	6	SEG51(P53/RFIN0)	-439.5	-1149.0
79	SEG50(P52/REF0)	-1917.5	700.0	7	SEG50(P52/REF0)	-349.5	-1149.0
80	SEG49(P51/SEN0)	-1917.5	600.0	8	SEG49(P51/SEN0)	-259.5	-1149.0
81	SEG48(P50/RFOUT)	-1917.5	500.0	9	SEG48(P50/RFOUT)	-169.5	-1149.0
82	SEG47(P23/TOUT_B)	-1917.5	300.0	10	SEG47(P23/TOUT_B)	-79.5	-1149.0
83	SEG46(P22/EVIN_B)	-1917.5	200.0	11	SEG46(P22/EVIN_B)	10.5	-1149.0
84	SEG45(P21)	-1917.5	100.0	12	SEG45(P21)	100.5	-1149.0
85	SEG44(P20)	-1917.5	0.0	13	SEG44(P20)	190.5	-1149.0
86	SEG43(P33/SRDY-SS)	-1917.5	-200.0	14	SEG43(P33/SRDY-SS)	280.5	-1149.0
87	SEG42(P32/SIN)	-1917.5	-300.0	15	SEG42(P32/SIN)	370.5	-1149.0
88	SEG41(P31/SOUT)	-1917.5	-400.0	16	SEG41(P31/SOUT)	460.5	-1149.0
89	SEG40(P30/SCLK)	-1917.5	-500.0	17	SEG40(P30/SCLK)	550.5	-1149.0
90	V_{DD}	-1917.5	-600.0	18	V_{DD}	640.5	-1149.0
91	SEG39(P43)	-1917.5	-700.0	—	—	—	—
92	SEG38(P42)	-1917.5	-800.0	—	—	—	—
93	SEG37(P41)	-1917.5	-900.0	—	—	—	—
94	SEG36(P40)	-1917.5	-1000.0	—	—	—	—
—	—	—	—	—	—	—	—
95	SEG35	-1917.5	-1200.0	—	—	—	—
96	SEG34	-1917.5	-1400.0	—	—	—	—

Table 3.2 Pad correspondence table of S1C6F016 and target products (S1C63016 / 008 / 004 / 003) (4)

S1C6F016				S1C63003			
PAD No.	Signal Name	Pad center coordinate X	Pad center coordinate Y	PAD No.	Signal Name	Pad center coordinate X	Pad center coordinate Y
1	SEG33	-1369.0	-1786.5	—	—	—	—
2	SEG32	-1169.0	-1786.5	—	—	—	—
3	SEG31	-969.0	-1786.5	—	—	—	—
4	SEG30	-869.0	-1786.5	—	—	—	—
5	SEG29	-769.0	-1786.5	—	—	—	—
6	SEG28	-669.0	-1786.5	—	—	—	—
7	SEG27	-569.0	-1786.5	—	—	—	—
8	SEG26	-469.0	-1786.5	—	—	—	—
9	SEG25	-369.0	-1786.5	—	—	—	—
10	SEG24	-269.0	-1786.5	—	—	—	—
11	SEG23	-169.0	-1786.5	—	—	—	—
12	SEG22	-69.0	-1786.5	—	—	—	—
13	SEG21	31.0	-1786.5	—	—	—	—
14	SEG20	131.0	-1786.5	—	—	—	—
15	SEG19	231.0	-1786.5	—	—	—	—
16	SEG18	331.0	-1786.5	—	—	—	—
17	SEG17	431.0	-1786.5	—	—	—	—
18	SEG16	531.0	-1786.5	—	—	—	—
19	SEG15	631.0	-1786.5	—	—	—	—
20	SEG14	731.0	-1786.5	—	—	—	—
21	SEG13	831.0	-1786.5	—	—	—	—
22	SEG12	931.0	-1786.5	—	—	—	—
23	SEG11	1031.0	-1786.5	—	—	—	—
24	SEG10	1231.0	-1786.5	—	—	—	—
25	SEG9	1431.0	-1786.5	14	SEG9	854.0	-272.8
26	SEG8	1917.5	-1500.0	15	SEG8	854.0	-182.8
27	SEG7	1917.5	-1300.0	16	SEG7	854.0	-92.8
28	SEG6	1917.5	-1100.0	17	SEG6	854.0	-2.8
29	SEG5	1917.5	-1000.0	18	SEG5	854.0	87.2
30	SEG4	1917.5	-900.0	19	SEG4	854.0	177.2
31	SEG3	1917.5	-800.0	20	SEG3	854.0	267.2
32	SEG2	1917.5	-700.0	21	SEG2	854.0	357.2
33	SEG1	1917.5	-600.0	22	SEG1	854.0	447.2
34	SEG0	1917.5	-500.0	23	SEG0	854.0	537.2
35	COM7	1917.5	-200.0	—	—	—	—
36	COM6	1917.5	-100.0	—	—	—	—
37	COM5	1917.5	0.0	—	—	—	—
38	COM4	1917.5	100.0	24	COM4	854.0	627.2
39	COM3	1917.5	200.0	25	COM3	854.0	717.2
40	COM2	1917.5	300.0	26	COM2	560.1	859.0
41	COM1	1917.5	400.0	27	COM1	470.1	859.0
42	COM0	1917.5	500.0	28	COM0	380.1	859.0
43	CB	1917.5	900.0	29	CB	214	859.0
44	CA	1917.5	1000.0	30	CA	124	859.0
45	V_{C3}	1917.5	1100.0	31	V_{C3}	34	859.0
46	V_{C2}	1917.5	1200.0	32	V_{C2}	-56	859.0
47	V_{C1}	1917.5	1300.0	33	V_{C1}	-146	859.0
—	—	—	—	34	V_{OSC}	-236	859.0
48	OSC1	1431.0	1786.5	35	OSC1	-326	859.0
49	OSC2	1331.0	1786.5	36	OSC2	-416	859.0
50	V_{SS}	1231.0	1786.5	37	V_{SS}	-506	859.0
51	OSC3	1131.0	1786.5	—	—	—	—
52	OSC4	1031.0	1786.5	—	—	—	—
53	V_{D1}	931.0	1786.5	38	V_{D1}	-854.0	171.5
54	V_{DD}	731.0	1786.5	39	V_{DD}	-854.0	81.5
55	TEST1	631.0	1786.5	—	—	—	—
56	TEST2	531.0	1786.5	—	—	—	—
57	TEST3	431.0	1786.5	—	—	—	—
58	TEST	231.0	1786.5	40	TEST	-854.0	-8.5
59	RESET	131.0	1786.5	41	RESET	-854.0	-98.5
60	V_{SS}	31.0	1786.5	—	—	—	—
61	DM0D	-69.0	1786.5	—	—	—	—
62	DCLK	-169.0	1786.5	—	—	—	—
63	DRXD	-269.0	1786.5	—	—	—	—
64	DTXD	-369.0	1786.5	—	—	—	—
65	P03(KRST03/KEY03)	-569.0	1786.5	42	P03(KRST03/KEY03)	-854.0	-188.5
66	P02(KRST02/KEY02)	-669.0	1786.5	43	P02(KRST02/KEY02)	-854.0	-278.5
67	P01(KRST01/KEY01/LAP)	-769.0	1786.5	44	P01(KRST01/KEY01/LAP)	-854.0	-368.5
68	P00(KRST00/KEY00/RUN)	-869.0	1786.5	45	P00(KRST00/KEY00/RUN)	-854.0	-458.5
69	P13(KEY13/FOUT)	-1069.0	1786.5	46	P13(KEY13/FOUT)	-854.0	-548.5
70	P12(KEY12/BZ)	-1169.0	1786.5	47	P12(KEY12/BZ)	-854.0	-638.5
71	P11(KEY11/TOUT_A)	-1269.0	1786.5	48	P11(KEY11/TOUT_A)	-854.0	-728.5
72	P10(KEY10/EVIN_A)	-1369.0	1786.5	49	P10(KEY10/EVIN_A)	-854.0	-818.5
73	SEG55(HUD)	-1917.5	1300.0	1	SEG55(HUD)	-447.6	-859.0
74	SEG54(SEN1)	-1917.5	1200.0	2	SEG54(SEN1)	-357.6	-859.0
75	SEG53(REF1)	-1917.5	1100.0	3	SEG53(REF1)	-267.6	-859.0
76	SEG52(RFIN1)	-1917.5	1000.0	4	SEG52(RFIN1)	-177.6	-859.0
77	V_{SS}	-1917.5	900.0	5	V_{SS}	-87.6	-859.0
78	SEG51(P53/RFIN0)	-1917.5	800.0	6	SEG51(P53/RFIN0)	2.4	-859.0
79	SEG50(P52/REF0)	-1917.5	700.0	7	SEG50(P52/REF0)	92.4	-859.0
80	SEG49(P51/SEN0)	-1917.5	600.0	8	SEG49(P51/SEN0)	182.4	-859.0
81	SEG48(P50/RFOUT)	-1917.5	500.0	9	SEG48(P50/RFOUT)	272.4	-859.0
82	SEG47(P23/TOUT_B)	-1917.5	300.0	10	SEG47(P23)	362.4	-859.0
83	SEG46(P22/EVIN_B)	-1917.5	200.0	11	SEG46(P22)	452.4	-859.0
84	SEG45(P21)	-1917.5	100.0	12	SEG45(P21)	542.4	-859.0
85	SEG44(P20)	-1917.5	0.0	13	SEG44(P20)	632.4	-859.0
86	SEG43(P33/SRDY-SS)	-1917.5	-200.0	—	—	—	—
87	SEG42(P32/SIN)	-1917.5	-300.0	—	—	—	—
88	SEG41(P31/SOUT)	-1917.5	-400.0	—	—	—	—
89	SEG40(P30/SCLK)	-1917.5	-500.0	—	—	—	—
90	V_{DD}	-1917.5	-600.0	—	—	—	—
91	SEG39(P43)	-1917.5	-700.0	—	—	—	—
92	SEG38(P42)	-1917.5	-800.0	—	—	—	—
93	SEG37(P41)	-1917.5	-900.0	—	—	—	—
94	SEG36(P40)	-1917.5	-1000.0	—	—	—	—
—	—	—	—	—	—	—	—
95	SEG35	-1917.5	-1200.0	—	—	—	—
96	SEG34	-1917.5	-1400.0	—	—	—	—

3.3 Handling of Unused Pins

For the pins of S1C6F016 that are unavailable with the target products and the pins that are unused in application systems, the following handling is needed.

3.3.1 FLASH ROM Test Pins (TEST1 / TEST2 / TEST3)

FLASH ROM test pins (TEST1 / TEST2 / TEST3) are not available with target products. However, when S1C6F016 is used for developments, leave the TEST1 and TEST3 pins open and connect the TEST2 pin to V_{DD}.

3.3.2 FLASH Programming Pins (DMOD / DCLK / DRXD / DTXD)

FLASH programming pins (DMOD / DCLK / DRXD / DTXD) are not available with target products. However, when S1C6F016 is used for developments, refer to the "Flash EEPROM Programming" in S1C6F016 Technical Manual to control properly.

3.3.3 Crystal Oscillation Circuit Operating Voltage Output Pin (V_{OSC})

For developments, leave V_{OSC} pin open, because S1C6F016 does not have this pin. For the target products, a capacitor should be connected to the V_{OSC} pin.

3.3.4 LCD System Power Supply Pins

When the LCD circuit is not used, leave the pins of V_{C1}, V_{C2}, V_{C3}, CA and CB open. Also, leave the pins of COM0 to COM7 and SEG0 to SEG55 open.

3.3.5 Unused COM / SEG Pins

Leave the unused pins of COM and SEG open.

3.3.6 Unused I/O Pins

Leave the unused I/O pins open. However, if "Without pull-down resistor" in the input mode is selected by the mask option, an external pull-down resistor should be connected to each pin, to avoid floating states.

4. Mask Options

Table 4 Mask option comparison table between S1C6F016 and target products (S1C63016 / 008 / 004 / 003) (1)

Item		Option			
		S1C6F016	S1C63016/008	S1C63004	S1C63003
Operating power supply voltage			☐ 1. Normal Type (1.8–5.5V) ☐ 2. Low Voltage Type (1.1–1.7V)	☐ 1. Normal Type (1.8–5.5V) ☐ 2. Low Voltage Type (1.1–1.7V)	☐ 1. Normal Type (1.8–5.5V) ☐ 2. Low Voltage Type (1.1–1.7V)
OSC3 oscillation circuit		☐ 1. CR (built-in R) ☐ 2. CR (external R) ☐ 3. Ceramic (4.0MHz)	☐ 1. CR (built-in R) ☐ 2. CR (external R) ☐ 3. Ceramic (4.0MHz)	☐ 1. CR (built-in R) ☐ 2. CR (external R) ☐ 3. Ceramic (4.0MHz)	☐ 1. CR (built-in R)
RESET pin pull-down resistor		☐ 1. Use ☐ 2. Not Use	☐ 1. Use ☐ 2. Not Use	☐ 1. Use ☐ 2. Not Use	☐ 1. Use ☐ 2. Not Use
SEG/ GPIO/ RFC selector	P20	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG
	P21	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG
	P22	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG
	P23	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG
	P30	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	
	P31	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	
	P32	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	
	P33	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	
	P40	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG		
	P41	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG		
	P42	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG		
	P43	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG		
	P50	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG
	P51	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG
	P52	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG
	P53	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG
	RFIN1	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG
	REF1	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG
	SEN1	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG
	HUD	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG	☐ 1. I/O ☐ 2. SEG

Table 4 Mask option comparison table between S1C6F016 and target products (S1C63016 / 008 / 004 / 003) (2)

Item		Option			
		S1C6F016	S1C63016/008	S1C63004	S1C63003
I/O port pull-down resistor	P00	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use
	P01	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use
	P02	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use
	P03	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use
	P10	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use
	P11	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use
	P12	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use
	P13	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use
	P20	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use
	P21	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use
	P22	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use
	P23	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use
	P30	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	
	P31	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	
	P32	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	
	P33	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	
	P40	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use		
	P41	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use		
	P42	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use		
	P43	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use		
	P50	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use
	P51	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use
	P52	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use
	P53	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use	□ 1. Use □ 2. Not Use

Table 4 Mask option comparison table between S1C6F016 and target products (S1C63016 / 008 / 004 / 003) (3)

Item		Option			
		S1C6F016	S1C63016/008	S1C63004	S1C63003
I/O port output specification	P00	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain
	P01	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain
	P02	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain
	P03	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain
	P10	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain
	P11	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain
	P12	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain
	P13	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain
	P20	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain
	P21	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain
	P22	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain
	P23	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain
	P30	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	
	P31	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	
	P32	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	
	P33	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	
	P40	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain		
	P41	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain		
	P42	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain		
	P43	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain		
	P50	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain
	P51	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain
	P52	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain
	P53	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain	□ 1. Complementary □ 2. Pch Open Drain

Table 4 Mask option comparison table between S1C6F016 and target products (S1C63016 / 008 / 004 / 003) (4)

Item	Option			
	S1C6F016	S1C63016/008	S1C63004	S1C63003
P1x port multiple-y key entry reset combination	□ 1. Not Use □ 2. Use <P00, P01> □ 3. Use <P00, P01, P02> □ 4. Use <P00, P01, P02, P03>	□ 1. Not Use □ 2. Use <P00, P01> □ 3. Use <P00, P01, P02> □ 4. Use <P00, P01, P02, P03>	□ 1. Not Use □ 2. Use <P00, P01> □ 3. Use <P00, P01, P02> □ 4. Use <P00, P01, P02, P03>	□ 1. Not Use □ 2. Use <P00, P01> □ 3. Use <P00, P01, P02> □ 4. Use <P00, P01, P02, P03>
P1x port multiple-key entry reset time authorization	□ 1. Not Use □ 2. Use	□ 1. Not Use □ 2. Use	□ 1. Not Use □ 2. Use	□ 1. Not Use □ 2. Use
LCD drive power supply	□ 1. Internal 1/3 bias □ 2. Ext. 1/3 bias, VDD = VC2 (4.5 V panel) □ 3. Ext.1/3 bias, VDD = VC3 (3.0 V panel) □ 4. Ext. 1/2 bias, VDD = VC3, VC1 = VC2 (3.0 V panel)	□ 1. Internal 1/3 bias □ 2. Ext. 1/3 bias, VDD = VC2 (4.5 V panel) □ 3. Ext.1/3 bias, VDD = VC3 (3.0 V panel) □ 4. Ext. 1/2 bias, VDD = VC3, VC1 = VC2 (3.0 V panel)	□ 1. Internal 1/3 bias □ 2. Ext. 1/3 bias, VDD = VC2 (4.5 V panel) □ 3. Ext.1/3 bias, VDD = VC3 (3.0 V panel) □ 4. Ext. 1/2 bias, VDD = VC3, VC1 = VC2 (3.0 V panel)	□ 1. Internal VC2, 1/3 bias □ 2. Internal VC1, 1/3 bias □ 3. Ext. 1/3 bias, VDD = VC2 (4.5 V panel) □ 4. Ext.1/3 bias, VDD = VC3 (3.0 V panel) □ 5. Ext. 1/2 bias, VDD = VC3, VC1 = VC2 (3.0 V panel)

5. Memories

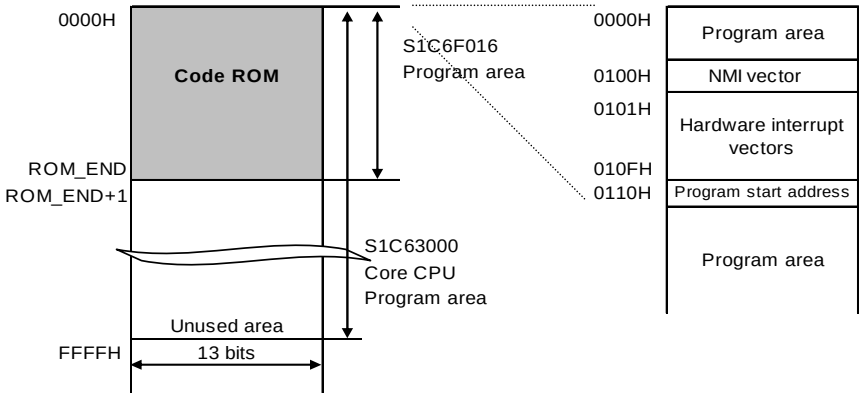
	S1C6F016	S1C63016	S1C63008	S1C63004	S1C63003
Code ROM	0000H to 3FFFH	0000H to 3FFFH	0000H to 1FFFH	0000H to 0FFFH	0000H to 0FFFH
RAM	0000H to 07FFH	0000H to 07FFH	0000H to 03FFH	0000H to 01FFH	"0000H to 007FH 0100H to 017FH"
SP1 address	0100H to 01FFH	0100H to 01FFH	0100H to 01FFH	0100H to 01FFH	0100H to 017FH
SP2 address	0000H to 00FFH	0000H to 00FFH	0000H to 00FFH	0000H to 00FFH	0000H to 007FH
Data ROM	8000H to 8FFFH	8000H to 8FFFH	8000H to 87FFH	8000H to 83FFH	—
Display RAM	F000H to F07FH	F000H to F07FH	F000H to F07FH	F000H to F07FH	F000H to F03FH
IO memory	FF00H to FFFFH	FF00H to FFFFH	FF00H to FFFFH	FF00H to FFFFH	FF00H to FFFFH

5.1 Code Memory Area

5.1.1 Code ROM

Products	Capacity	Address
S1C6F016	16,384 words × 13 bits	0000H to 3FFFH
S1C63016	16,384 words × 13 bits	0000H to 3FFFH
S1C63008	8,192 words × 13 bits	0000H to 1FFFH
S1C63004	4,096 words × 13 bits	0000H to 0FFFH
S1C63003	4,096 words × 13 bits	0000H to 0FFFH

The core CPU can access the program area step 0000H to step FFFFH linearly. However, the program area of S1C6F016 is step 0000H to step 3FFFH. The program start address after the initial reset is assigned to step 0110H. The non-maskable interrupt (NMI) vector is assigned to step 0100H, and hardware interrupt vectors are assigned to steps 0101H to 010FH respectively.



Products	ROM_END
S1C6F016	3FFFH
S1C63016	3FFFH
S1C63008	1FFFH
S1C63004	0FFFH
S1C63003	0FFFH

Figure 5.1 Code ROM configuration

(Note): S1C6F016 has a built-in code ROM with the capacity corresponding to S1C63016. When using S1C6F016 for the developments of other target products (S1C63008 / 004 / 003), create programs within the upper limit of each target product memory.

5.2 Data Memory Area

The data memory of S1C63016 / 008 / 004 / 003 consists of RAM, data ROM, display memory and peripheral I/O memory.

Figure 3.3.1 shows the overall data memory map.

(Note): Memories are not incorporated in the unused areas within the memory map. Further, there are some non-incorporated areas and unused (access prohibited) areas in the peripheral I/O area. Normal operations cannot be guaranteed for the programs that access these areas.

For details of the peripheral I/O area, refer to Appendix (I/O memory maps) in Technical Manual.

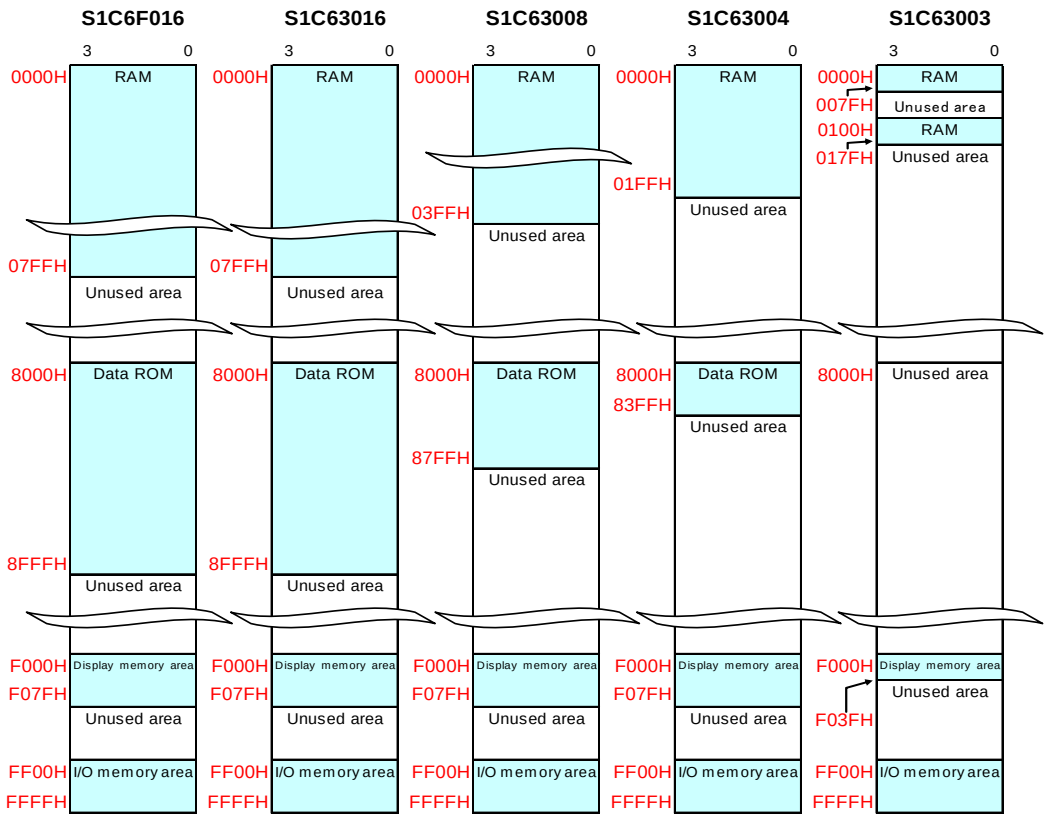


Figure 5.2 Data memory configuration

5.2.1 RAM

Products	Capacity	Address
S1C6F016	2048 words × 13 bits	0000H to 07FFH
S1C63016	2048 words × 13 bits	0000H to 07FFH
S1C63008	1024 words × 13 bits	0000H to 03FFH
S1C63004	512 words × 13 bits	0000H to 01FFH
S1C63003	256 words × 13 bits	0000H to 007FH 0100H to 017FH

S1C6F016 has some RAM areas that are unavailable with target products (S1C63008 / 004 / 003). Create programs not to access these unavailable areas.

S1C63016/008/004 have the same stack area as S1C6F016 does but S1C63003 uses a different stack area. This should be noted when you program.

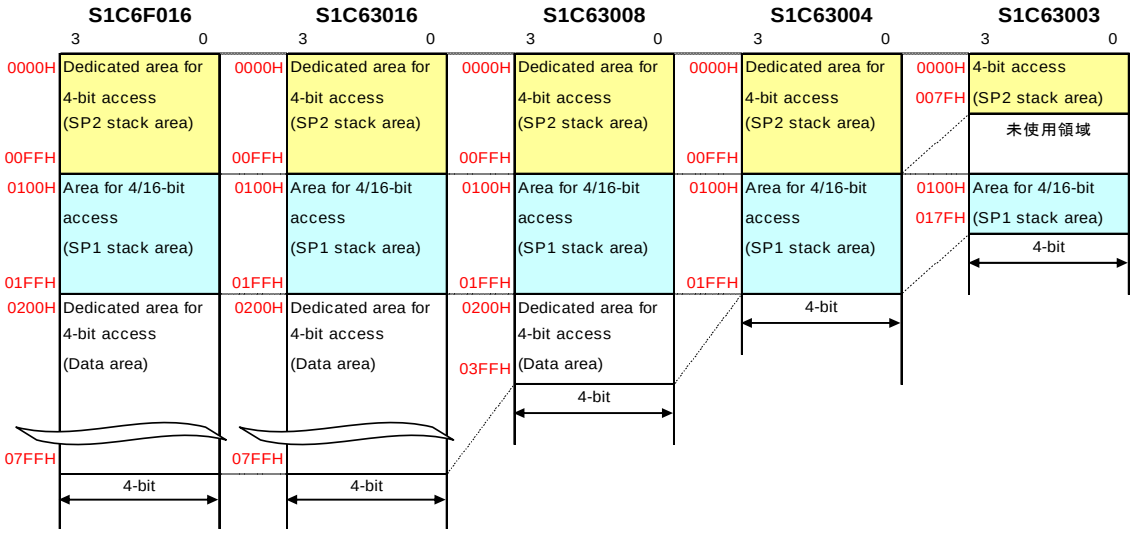


Figure 5.3 Stack area configuration

<Example of a confirmation method>
Use an in-circuit emulator during software debug to fill in a fixed value (for example, 0xA) to the whole RAM area before the test. After the test, check whether any data are written to the supposedly unused RAM area. If there was unintended access to the area, you can find values other than the fixed value (0xA) in the area. Therefore, by checking whether such values exist in the area, you can tell if there was unintended access.

Also, when you develop software for S1C63003 using the Peripheral Circuit Board for S1C6F016 (S5U1C63000P6 and S5U1C6F016P2), keep in mind that the behavior of the microcontroller is different from the actual S1C63003 chip as follows.

(Accessing the undefined address space)

S1C63003 does not generate a program break when accessing to the undefined address space between 0080H and 00FFH. When data is written to/read from the undefined address space that is not assigned to any of the built-in ROM/RAM and I/O of the actual S1C63003 chip, the written/read value is undefined. Note carefully that the written/read value in this case is different between the tool and the actual chip.

Because of this, always confirm before the ROM release that there is no illegal access to the undefined address space. If there is any illegal access to the undefined address space, correct program execution is not guaranteed.

<Checking whether there is any illegal access to the undefined address space in S1C63003>

Follow the procedure below to check whether there is any illegal access to the undefined address space in S1C63003.

1. Selecting the project file

    1-1. Start up the WorkBench63.
    [Start]-[Program]-[EPSON MCU]-[S1C63 Assembler]-[WorkBench63]

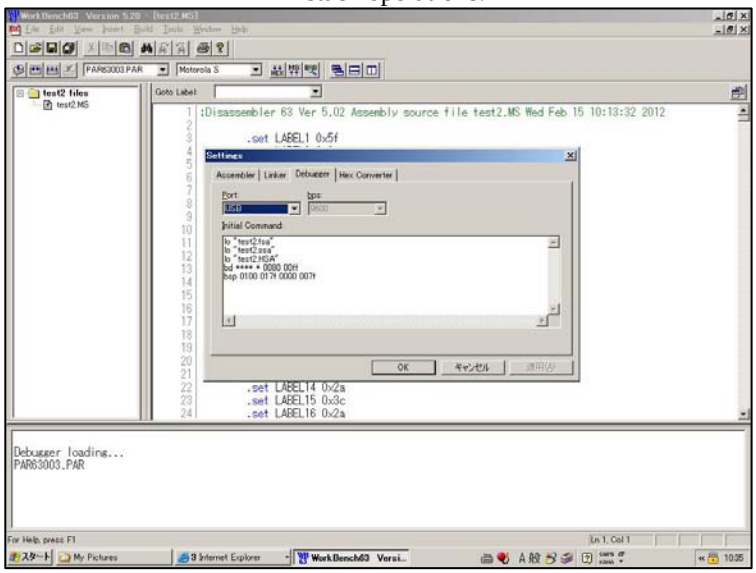
    1-2. Select and load the project file you want to check.
    [File]-[Open Workspace]-select the project file in focus

2. Setting up break commands to check whether there is any illegal access to the undefined address space

    2-1. Open the window to specify commands to be executed when the debugger starts up.
    [Build] - [Settings] - [Debugger]

    2-2. Type in break commands to be executed when the debugger starts up to check whether there is any illegal access.

lo “test.fsa”	←	Loading the function option file
lo “test.ssa”	←	Loading the LCD Segment option file
lo “test.HSA”	←	Loading the program file
bd **** * 0080 00ff	←	A break occurs when any data is read from or written to the undefined address space between 0080H and 00FFH.
bsp 0100 017f 0000 007f	←	The address space between 0100H and 017FH is assigned to SP1 and the address space between 0000H and 007FH is assigned to SP2. A break occurs by accessing outside the assigned stack area during stack operations.



3. Checking whether there is any illegal access to the undefined address space

    3-1. Start up the debugger.
    [Build] - [Debug]

    3-2. Do a test run. If there is any illegal access to the undefined address space, a break occurs. Confirm that no break occurs.

5.2.2 Data ROM

The data PROM with the capacity of 2,048 words × 4 bits incorporates a Flash EEPROMs for loading various kinds of static data such as character generators. The data PROM is assigned to steps 8000H to 8FFFH on the data memory map, and the data can be read by data memory access instructions, in the same way as RAM.

(Note): S1C6F016 has the data ROM with the capacity corresponding to S1C63016. When using S1C6F016 for the developments of other target products that have different ROM capacities, create programs within the upper limit of each target product memory.

Products	Capacity	Address
S1C6F016	4096 words × 4 bits	8000H to 8FFFH
S1C63016	4096 words × 4 bits	8000H to 8FFFH
S1C63008	2048 words × 4 bits	8000H to 87FFH
S1C63004	1024 words × 4 bits	8000H to 83FFH
S1C63003	—	—

5.2.3 Display Memory

Products	Capacity	Address
S1C6F016	448 bits	F000H to F07FH
S1C63016	448 bits	F000H to F07FH
S1C63008	400 bits	F000H to F07FH
S1C63004	288 bits	F000H to F07FH
S1C63003	110 bits	F000H to F03FH

This is the number of bits that can be assigned for the output data to the segments. For S1C6F016 and also for S1C63016/008/004, any address between F000H and F07FH can be specified. For S1C63003, any address between F000H and F03FH can be specified.

5.2.4 I/O Memory

The peripheral circuits (timer, I/O and others) of S1C6F016 are interfaced with the CPU with the memory mapped I/O system. As a result, all the peripheral circuits can be controlled by accessing the I/O memories on the memory map using the memory manipulation instructions.

The details of each peripheral circuit operation are described below.

5.2.4.1 Memory Map

The I/O map of S1C6F016 is different from that of target products. The differences are shown in the tables of Chapter 6.

Create programs not to access the registers that are not incorporated in the target product.

6. Differences of I/O Registers

(○: Same, △: Partially different, ×: Not available)
△: Partially different: Refer to Chapter 7, for details.

*1: Initial value at initial reset *2: Not set in the circuits *3: Always "0" in reading *4: Unused for S1C63003 / 004 / 008
*5: Unused for S1C63003 / 004 *6: Unused for S1C63003

FF00H Oscillation Circuit

Address		Register name	R/W	Default	Setting / data				Function	F016	016	008	004	003
FF00H	D3	**CLKCHG**	R/W	0	1	OSC3	0	OSC1	CPU clock switch	○	○	○	○	○
	D2	**OSCC**	R/W	0	1	On	0	Off	OSC3 oscillation On / Off	○	○	○	○	○
	D1	0 (*3)	R	– (*2)	1		0		Unused	○	○	○	○	○
	D0	0 (*3)	R	– (*2)	1		0		Unused	○	○	○	○	○

FF01H Watchdog Timer

Address		Register name	R/W	Default	Setting / data				Function	F016	016	008	004	003
FF01H	D3	0 (*3)	R	– (*2)	—				Unused	○	○	○	○	○
	D2	0 (*3)	R	– (*2)	—				Unused	○	○	○	○	○
	D1	**WDEN**	R/W	1	1	Enable	0	Disable	Watchdog timer enable	○	○	○	○	○
	D0	**WDRST**(*3)	W	(Reset)	1	Reset	0	Invalid	Watchdog timer reset (writing)	○	○	○	○	○

FF02H- FF03H Power Supply Circuit

Address		Register name	R/W	Default	Setting / data				Function	F016	016	008	004	003
FF02H	D3	**VDSEL**	R/W	0	1	1	0	0	General-purpose register	○	○	○	○	○
	D2	**VCSEL**	R/W	0	1	1	0	0	General-purpose register	○	○	○	○	○
	D1	**HLON**	R/W	0	1	1	0	0	General-purpose register	○	○	○	○	○
	D0	**DBON**	R/W	0	1	1	0	0	General-purpose register	○	○	○	○	○
FF03H	D3	**VCHLMOD**	R/W	0	1	On	0	Off	VC regulator heavy load protection mode On / Off	○	○	○	○	○
	D2	**VDHLMOD**	R/W	0	1	On	0	Off	VD regulator heavy load protection mode On / Off	○	○	○	○	○
	D1	**VCREF**(*6)	R/W	0	1	VC2	0	VC1	VC regulator reference voltage selection	○	○	○	○	×
	D0	**LPWR**	R/W	0	1	On	0	Off	VC regulator On / Off	○	○	○	○	○

FF04H- FF05H SVD

Address		Register name	R/W	Default	Setting / data								Function	F016	016	008	004	003
FF04H (*6)	D3	**SVDS3**	R/W	0	F	3.2	B	2.8	7	2.4	3	2.0	SVD criteria voltage (V) selection	○	△	△	△	×
	D2	**SVDS2**	R/W	0	E	3.1	A	2.7	6	2.3	2	1.9		○	△	△	△	×
	D1	**SVDS1**	R/W	0	D	3.0	9	2.6	5	2.2	1	1.8		○	△	△	△	×
	D0	**SVDS0**	R/W	0	C	2.9	8	2.5	4	2.1	0	1.7		○	△	△	△	×
FF05H (*6)	D3	0 (*3)	R	– (*2)	—								Unused	○	○	○	○	○
	D2	**SVDS4**	R/W	0	1	1	0	0					General-purpose register	○	△	△	△	×
	D1	**SVDDT**	R	0	1	Low	0	Normal					SVD evaluation data	○	○	○	○	×
	D0	**SVDON**	R/W	0	1	On	0	Off					SVD circuit On / Off	○	○	○	○	×

FF10H- FF1BH					Clock Manager		F016	016	008	004	003
Address		Register name	R/W	Default	Setting / data	Function					
FF10H	D3	FOUT3	R/W	0	F f3 / B f3/16 / 7 f1 / 3 f1/32	FOUT frequency selection (f1 = fOSC1, f3 = fOSC3)	○	○	○	○	○
	D2	FOUT2	R/W	0	E f3/2 / A f3/32 / 6 f1/2 / 2 f1/64		○	○	○	○	○
	D1	FOUT1	R/W	0	D f3/4 / 9 f3/64 / 5 f1/4 / 1 f1/256		○	○	○	○	○
	D0	FOUT0	R/W	0	C f3/8 / 8 f3/256 / 4 f1/16 / 0 Off		○	○	○	○	○
FF11H	D3	NRSP11 (*6)	R/W	0	3 f1/256 / 1 f1/16	P1 key input interrupt noise reduction frequency selection (f1 = fosc1, f3 = fosc3)	○	○	○	○	×
	D2	NRSP10 (*6)	R/W	0	2 f1/64 / 0 Off		○	○	○	○	×
	D1	NRSP01	R/W	0	3 f1/256 / 1 f1/16	P0 key input interrupt noise reduction frequency selection (f1 = fosc1, f3 = fosc3)	○	○	○	○	○
	D0	NRSP00	R/W	0	2 f1/64 / 0 Off		○	○	○	○	○
FF12H	D3	FLCKS1	R/W	0	3 — / 1 21.3	Frame frequency (Hz) selection	○	○	○	○	○
	D2	FLCKS0	R/W	0	2 16.0 / 0 32.0		○	○	○	○	○
	D1	VCCKS1	R/W	0	3 — / 1 2048	VC boost frequency (Hz) selection	○	○	○	○	○
	D0	VCCKS0	R/W	0	2 — / 0 Off		○	○	○	○	○
FF14H (*6)	D3	0 (*3)	R	– (*2)	—	Unused	○	○	○	○	○
	D2	SIFCKS2	R/W	0	7 f3/4 / 4 PT1 / 1 f1	Serial I/F clock frequency selection (f1 = fosc1, f3 = fosc3)	○	○	○	○	×
	D1	SIFCKS1	R/W	0	6 f3/2 / 3 f1/4 / 0 Off/		○	○	○	○	×
	D0	SIFCKS0	R/W	0	5 f3 / 2 f1/2 / External		○	○	○	○	×
FF15H	D3	0 (*3)	R	– (*2)	—	Unused	○	○	○	○	○
	D2	RFCKS2	R/W	0	7 f3/4 / 4 PT1 / 1 f1	R/F converter clock frequency selection (f1 = fosc1, f3 = fosc3)	○	○	○	○	○
	D1	RFCKS1	R/W	0	6 f3/2 / 3 f1/4 / 0 Off/		○	○	○	○	○
	D0	RFCKS0	R/W	0	5 f3 / 2 f1/2		○	○	○	○	○
FF16H	D3	MDCKE (*5)	R/W	0	1 Enable / 0 Disable	Integer multiplier clock enable	○	○	○	×	×
	D2	SGCKE	R/W	0	1 Enable / 0 Disable	Sound generator clock enable	○	○	○	○	○
	D1	SWCKE	R/W	0	1 Enable / 0 Disable	Stopwatch timer clock enable	○	○	○	○	○
	D0	RTCKE	R/W	0	1 Enable / 0 Disable	Clock timer clock enable	○	○	○	○	○
FF18H	D3	PTPS03	R/W	0	F f3 / B f3/16 / 7 f1 / 3 f1/32	Programmable timer 0 count clock frequency selection (f1 = fosc1, f3 = fosc3)	○	○	○	○	○
	D2	PTPS02	R/W	0	E f3/2 / A f3/32 / 6 f1/2 / 2 f1/64		○	○	○	○	○
	D1	PTPS01	R/W	0	D f3/4 / 9 f3/64 / 5 f1/4 / 1 f1/256		○	○	○	○	○
	D0	PTPS00	R/W	0	C f3/8 / 8 f3/256 / 4 f1/16 / 0 Off		○	○	○	○	○
FF19H (*6)	D3	PTPS13	R/W	0	F f3 / B f3/16 / 7 f1 / 3 f1/32	Programmable timer 1 count clock frequency selection (f1 = fosc1, f3 = fosc3)	○	○	○	○	×
	D2	PTPS12	R/W	0	E f3/2 / A f3/32 / 6 f1/2 / 2 f1/64		○	○	○	○	×
	D1	PTPS11	R/W	0	D f3/4 / 9 f3/64 / 5 f1/4 / 1 f1/256		○	○	○	○	×
	D0	PTPS10	R/W	0	C f3/8 / 8 f3/256 / 4 f1/16 / 0 Off		○	○	○	○	×
FF1AH (*6)	D3	PTPS23	R/W	0	F f3 / B f3/16 / 7 f1 / 3 f1/32	Programmable timer 2 count clock frequency selection (f1 = fosc1, f3 = fosc3)	○	○	○	○	×
	D2	PTPS22	R/W	0	E f3/2 / A f3/32 / 6 f1/2 / 2 f1/64		○	○	○	○	×
	D1	PTPS21	R/W	0	D f3/4 / 9 f3/64 / 5 f1/4 / 1 f1/256		○	○	○	○	×
	D0	PTPS20	R/W	0	C f3/8 / 8 f3/256 / 4 f1/16 / 0 Off		○	○	○	○	×
FF1BH (*4)	D3	PTPS33	R/W	0	F f3 / B f3/16 / 7 f1 / 3 f1/32	Programmable timer 3 count clock frequency selection (f1 = fosc1, f3 = fosc3)	○	○	×	×	×
	D2	PTPS32	R/W	0	E f3/2 / A f3/32 / 6 f1/2 / 2 f1/64		○	○	×	×	×
	D1	PTPS31	R/W	0	D f3/4 / 9 f3/64 / 5 f1/4 / 1 f1/256		○	○	×	×	×
	D0	PTPS30	R/W	0	C f3/8 / 8 f3/256 / 4 f1/16 / 0 Off		○	○	×	×	×

FF20H- FF3FH									I/O Ports				
Address		Register name	R/W	Default	Setting / data				Function	F016	016	008	004	003
FF20H	D3	**P03**	R/W	1	1	High	0	Low	P03 I/O port data	○	○	○	○	○
	D2	**P02**	R/W	1	1	High	0	Low	P02 I/O port data	○	○	○	○	○
	D1	**P01**	R/W	1	1	High	0	Low	P01 I/O port data	○	○	○	○	○
	D0	**P00**	R/W	1	1	High	0	Low	P00 I/O port data	○	○	○	○	○
FF21H	D3	**IOC03**	R/W	0	1	Output	0	Input	P03 I/O control register	○	○	○	○	○
	D2	**IOC02**	R/W	0	1	Output	0	Input	P02 I/O control register	○	○	○	○	○
	D1	**IOC01**	R/W	0	1	Output	0	Input	P01 I/O control register	○	○	○	○	○
	D0	**IOC00**	R/W	0	1	Output	0	Input	P00 I/O control register	○	○	○	○	○
FF22H	D3	**PUL03**	R/W	1	1	Enable	0	Disable	P03 pull-down control register	○	○	○	○	○
	D2	**PUL02**	R/W	1	1	Enable	0	Disable	P02 pull-down control register	○	○	○	○	○
	D1	**PUL01**	R/W	1	1	Enable	0	Disable	P01 pull-down control register	○	○	○	○	○
	D0	**PUL00**	R/W	1	1	Enable	0	Disable	P00 pull-down control register	○	○	○	○	○
FF23H	D3	**SMT03**	R/W	1	1	Schmitt	0	CMOS	P03 input I/F level select register	○	○	○	○	○
	D2	**SMT02**	R/W	1	1	Schmitt	0	CMOS	P02 input I/F level select register	○	○	○	○	○
	D1	**SMT01**	R/W	1	1	Schmitt	0	CMOS	P01 input I/F level select register	○	○	○	○	○
	D0	**SMT00**	R/W	1	1	Schmitt	0	CMOS	P00 input I/F level select register	○	○	○	○	○
FF24H	D3	**P13**	R/W	1	1	High	0	Low	P13 I/O port data	○	○	○	○	○
	D2	**P12**	R/W	1	1	High	0	Low	P12 I/O port data	○	○	○	○	○
	D1	**P11**	R/W	1	1	High	0	Low	P11 I/O port data	○	○	○	○	○
	D0	**P10**	R/W	1	1	High	0	Low	P10 I/O port data	○	○	○	○	○
FF25H	D3	**IOC13**	R/W	0	1	Output	0	Input	P13 I/O control register	○	○	○	○	○
	D2	**IOC12**	R/W	0	1	Output	0	Input	P12 I/O control register	○	○	○	○	○
	D1	**IOC11**	R/W	0	1	Output	0	Input	P11 I/O control register	○	○	○	○	○
	D0	**IOC10**	R/W	0	1	Output	0	Input	P10 I/O control register	○	○	○	○	○
FF26H	D3	**PUL13**	R/W	1	1	Enable	0	Disable	P13 pull-down control register	○	○	○	○	○
	D2	**PUL12**	R/W	1	1	Enable	0	Disable	P12 pull-down control register	○	○	○	○	○
	D1	**PUL11**	R/W	1	1	Enable	0	Disable	P11 pull-down control register	○	○	○	○	○
	D0	**PUL10**	R/W	1	1	Enable	0	Disable	P10 pull-down control register	○	○	○	○	○
FF27H	D3	**SMT13**	R/W	1	1	Schmitt	0	CMOS	P13 input I/F level select register	○	○	○	○	○
	D2	**SMT12**	R/W	1	1	Schmitt	0	CMOS	P12 input I/F level select register	○	○	○	○	○
	D1	**SMT11**	R/W	1	1	Schmitt	0	CMOS	P11 input I/F level select register	○	○	○	○	○
	D0	**SMT10**	R/W	1	1	Schmitt	0	CMOS	P10 input I/F level select register	○	○	○	○	○

FF20H- FF3FH									I/O Ports	F016	016	008	004	003
Address		Register name	R/W	Default	Setting / data				Function					
FF28H	D3	**P23**	R/W	1	1	High	0	Low	P23 I/O port data	○	○	○	○	○
	D2	**P22**	R/W	1	1	High	0	Low	P22 I/O port data	○	○	○	○	○
	D1	**P21**	R/W	1	1	High	0	Low	P21 I/O port data	○	○	○	○	○
	D0	**P20**	R/W	1	1	High	0	Low	P20 I/O port data	○	○	○	○	○
FF29H	D3	**IOC23**	R/W	0	1	Output	0	Input	P23 I/O control register	○	○	○	○	○
	D2	**IOC22**	R/W	0	1	Output	0	Input	P22 I/O control register	○	○	○	○	○
	D1	**IOC21**	R/W	0	1	Output	0	Input	P21 I/O control register	○	○	○	○	○
	D0	**IOC20**	R/W	0	1	Output	0	Input	P20 I/O control register	○	○	○	○	○
FF2AH	D3	**PUL23**	R/W	1	1	Enable	0	Disable	P23 pull-down control register	○	○	○	○	○
	D2	**PUL22**	R/W	1	1	Enable	0	Disable	P22 pull-down control register	○	○	○	○	○
	D1	**PUL21**	R/W	1	1	Enable	0	Disable	P21 pull-down control register	○	○	○	○	○
	D0	**PUL20**	R/W	1	1	Enable	0	Disable	P20 pull-down control register	○	○	○	○	○
FF2CH (*6)	D3	**P33**	R/W	1	1	High	0	Low	P33 I/O port data	○	○	○	○	×
	D2	**P32**	R/W	1	1	High	0	Low	P32 I/O port data	○	○	○	○	×
	D1	**P31**	R/W	1	1	High	0	Low	P31 I/O port data	○	○	○	○	×
	D0	**P30**	R/W	1	1	High	0	Low	P30 I/O port data	○	○	○	○	×
FF2DH (*6)	D3	**IOC33**	R/W	0	1	Output	0	Input	P33 I/O control register	○	○	○	○	×
	D2	**IOC32**	R/W	0	1	Output	0	Input	P32 I/O control register	○	○	○	○	×
	D1	**IOC31**	R/W	0	1	Output	0	Input	P31 I/O control register	○	○	○	○	×
	D0	**IOC30**	R/W	0	1	Output	0	Input	P30 I/O control register	○	○	○	○	×
FF2EH (*6)	D3	**PUL33**	R/W	1	1	Enable	0	Disable	P33 pull-down control register	○	○	○	○	×
	D2	**PUL32**	R/W	1	1	Enable	0	Disable	P32 pull-down control register	○	○	○	○	×
	D1	**PUL31**	R/W	1	1	Enable	0	Disable	P31 pull-down control register	○	○	○	○	×
	D0	**PUL30**	R/W	1	1	Enable	0	Disable	P30 pull-down control register	○	○	○	○	×
FF30H (*5)	D3	**P43**	R/W	1	1	High	0	Low	P43 I/O port data	○	○	○	×	×
	D2	**P42**	R/W	1	1	High	0	Low	P42 I/O port data	○	○	○	×	×
	D1	**P41**	R/W	1	1	High	0	Low	P41 I/O port data	○	○	○	×	×
	D0	**P40**	R/W	1	1	High	0	Low	P40 I/O port data	○	○	○	×	×
FF31H (*5)	D3	**IOC43**	R/W	0	1	Output	0	Input	P43 I/O control register	○	○	○	×	×
	D2	**IOC42**	R/W	0	1	Output	0	Input	P42 I/O control register	○	○	○	×	×
	D1	**IOC41**	R/W	0	1	Output	0	Input	P41 I/O control register	○	○	○	×	×
	D0	**IOC40**	R/W	0	1	Output	0	Input	P40 I/O control register	○	○	○	×	×
FF32H (*5)	D3	**PUL43**	R/W	1	1	Enable	0	Disable	P43 pull-down control register	○	○	○	×	×
	D2	**PUL42**	R/W	1	1	Enable	0	Disable	P42 pull-down control register	○	○	○	×	×
	D1	**PUL41**	R/W	1	1	Enable	0	Disable	P41 pull-down control register	○	○	○	×	×
	D0	**PUL40**	R/W	1	1	Enable	0	Disable	P40 pull-down control register	○	○	○	×	×

FF20H- FF3FH					I/O Ports										
Address		Register name	R/W	Default	Setting / data				Function	F016	016	008	004	003
FF34H	D3	**P53**	R/W	1	1	High	0	Low	P53 I/O port data	○	○	○	○	○
	D2	**P52**	R/W	1	1	High	0	Low	P52 I/O port data	○	○	○	○	○
	D1	**P51**	R/W	1	1	High	0	Low	P51 I/O port data	○	○	○	○	○
	D0	**P50**	R/W	1	1	High	0	Low	P50 I/O port data	○	○	○	○	○
FF35H	D3	**IOC53**	R/W	0	1	Output	0	Input	P53 I/O control register	○	○	○	○	○
	D2	**IOC52**	R/W	0	1	Output	0	Input	P52 I/O control register	○	○	○	○	○
	D1	**IOC51**	R/W	0	1	Output	0	Input	P51 I/O control register	○	○	○	○	○
	D0	**IOC50**	R/W	0	1	Output	0	Input	P50 I/O control register	○	○	○	○	○
FF36H	D3	**PUL53**	R/W	1	1	Enable	0	Disable	P53 pull-down control register	○	○	○	○	○
	D2	**PUL52**	R/W	1	1	Enable	0	Disable	P52 pull-down control register	○	○	○	○	○
	D1	**PUL51**	R/W	1	1	Enable	0	Disable	P51 pull-down control register	○	○	○	○	○
	D0	**PUL50**	R/W	1	1	Enable	0	Disable	P50 pull-down control register	○	○	○	○	○
FF3CH	D3	**SIP03**	R/W	0	1	Enable	0	Disable	P03 (KEY03) interrupt select register	○	○	○	○	○
	D2	**SIP02**	R/W	0	1	Enable	0	Disable	P02 (KEY02) interrupt select register	○	○	○	○	○
	D1	**SIP01**	R/W	0	1	Enable	0	Disable	P01 (KEY01) interrupt select register	○	○	○	○	○
	D0	**SIP00**	R/W	0	1	Enable	0	Disable	P00 (KEY00) interrupt select register	○	○	○	○	○
FF3DH	D3	**PCP03**	R/W	1	1	↓ (falling edge)	0	↑ (rising edge)	P03 (KEY03) interrupt polarity select register	○	○	○	○	○
	D2	**PCP02**	R/W	1	1	↓ (falling edge)	0	↑ (rising edge)	P02 (KEY02) interrupt polarity select register	○	○	○	○	○
	D1	**PCP01**	R/W	1	1	↓ (falling edge)	0	↑ (rising edge)	P01 (KEY01) interrupt polarity select register	○	○	○	○	○
	D0	**PCP00**	R/W	1	1	↓ (falling edge)	0	↑ (rising edge)	P00 (KEY00) interrupt polarity select register	○	○	○	○	○
FF3EH (*6)	D3	**SIP13**	R/W	0	1	Enable	0	Disable	P13 (KEY13) interrupt select register	○	○	○	○	×
	D2	**SIP12**	R/W	0	1	Enable	0	Disable	P12 (KEY12) interrupt select register	○	○	○	○	×
	D1	**SIP11**	R/W	0	1	Enable	0	Disable	P11 (KEY11) interrupt select register	○	○	○	○	×
	D0	**SIP10**	R/W	0	1	Enable	0	Disable	P10 (KEY10) interrupt select register	○	○	○	○	×
FF3FH (*6)	D3	**PCP13**	R/W	1	1	↓ (falling edge)	0	↑ (rising edge)	P13 (KEY13) interrupt polarity select register	○	○	○	○	×
	D2	**PCP12**	R/W	1	1	↓ (falling edge)	0	↑ (rising edge)	P12 (KEY12) interrupt polarity select register	○	○	○	○	×
	D1	**PCP11**	R/W	1	1	↓ (falling edge)	0	↑ (rising edge)	P11 (KEY11) interrupt polarity select register	○	○	○	○	×
	D0	**PCP10**	R/W	1	1	↓ (falling edge)	0	↑ (rising edge)	P10 (KEY10) interrupt polarity select register	○	○	○	○	×

FF40H- FF42H					Clock Timer									
Address		Register name	R/W	Default	Setting / data				Function	F016	016	008	004	003
FF40H	D3	0 (*3)	R	– (*2)	—				Unused	○	○	○	○	○
	D2	0 (*3)	R	– (*2)	—				Unused	○	○	○	○	○
	D1	**TMRST** (*3)	W	(Reset)	1	Reset	0	Invalid	Clock timer reset (writing)	○	○	○	○	○
	D0	**TMRUN**	R/W	0	1	Run	0	Stop	Clock timer Run / Stop	○	○	○	○	○
FF41H	D3	**TM3**	R	0	0H–FH				Clock timer data (16Hz)	○	○	○	○	○
	D2	**TM2**	R	0					Clock timer data (32Hz)	○	○	○	○	○
	D1	**TM1**	R	0					Clock timer data (64Hz)	○	○	○	○	○
	D0	**TM0**	R	0					Clock timer data (128Hz)	○	○	○	○	○
FF42H	D3	**TM7**	R	0	0H–FH				Clock timer data (1Hz)	○	○	○	○	○
	D2	**TM6**	R	0					Clock timer data (2Hz)	○	○	○	○	○
	D1	**TM5**	R	0					Clock timer data (4Hz)	○	○	○	○	○
	D0	**TM4**	R	0					Clock timer data (8Hz)	○	○	○	○	○

FF44H- FF47H Sound Generator

Address		Register name	R/W	Default	Setting / data	Function	F016	016	008	004	003
FF44H	D3	**ENRTM**	R/W	0	1: 1 sec / 0: 0.5 sec	Envelope releasing time selection	○	○	○	○	○
	D2	**ENRST** (*3)	W	(Reset)	1: Reset / 0: Invalid	Envelope reset (writing)	○	○	○	○	○
	D1	**ENON**	R/W	0	1: On / 0: Off	Envelope On / Off	○	○	○	○	○
	D0	**BZE**	R/W	0	1: Enable / 0: Disable	Buzzer output enable	○	○	○	○	○
FF45H	D3	0 (*3)	R	– (*2)	—	Unused	○	○	○	○	○
	D2	**BZSTP** (*3)	W	0	1: Stop / 0: Invalid	1-shot buzzer stop (writing)	○	○	○	○	○
	D1	**BZSHT**	R/W	0	1: Trigger (W) Busy (R) / 0: Invalid (W) Ready (R)	1-shot buzzer trigger (writing) 1-shot buzzer status (reading)	○	○	○	○	○
	D0	**SHTPW**	R/W	0	1: 125 msec / 0: 31.25 msec	1-shot buzzer pulse width selection	○	○	○	○	○
FF46H	D3	0 (*3)	R	– (*2)	—	Unused	○	○	○	○	○
	D2	**BZFQ2**	R/W	0	7: 1170.3 / 4: 2048.0 / 1: 3276.8	Buzzer frequency (Hz) selection	○	○	○	○	○
	D1	**BZFQ1**	R/W	0	6: 1365.3 / 3: 2340.6 / 0: 4096.0		○	○	○	○	○
	D0	**BZFQ0**	R/W	0	5: 1638.4 / 2: 2730.7		○	○	○	○	○
FF47H	D3	0 (*3)	R	– (*2)	—	Unused	○	○	○	○	○
	D2	**BDTY2**	R/W	0	7: Level 8 / 4: Level 5 / 1: Level 2	Buzzer signal duty ratio selection	○	○	○	○	○
	D1	**BDTY1**	R/W	0	6: Level 7 / 3: Level 4 / 0: Level 1		○	○	○	○	○
	D0	**BDTY0**	R/W	0	5: Level 6 / 2: Level3		○	○	○	○	○

FF48H- FF4DH Stopwatch Timer

Address		Register name	R/W	Default	Setting / data	Function	F016	016	008	004	003
FF48H (*6)	D3	0 (*3)	R	– (*2)	—	Unused	○	○	○	○	○
	D2	0 (*3)	R	– (*2)	—	Unused	○	○	○	○	○
	D1	**SWDIR**	R/W	0	1: P00=Lap P01=Run/Stop / 0: P00=Run/Stop P01=Lap	Stopwatch direct input switch	○	○	○	○	×
	D0	**EDIR**	R/W	0	1: Enable / 0: Disable	Direct input enable	○	○	○	○	×
FF49H (*6)	D3	0 (*3)	R	– (*2)	—	Unused	○	○	○	○	○
	D2	**DKM2**	R/W	0	7: P10–13 / 4: P10 / 1: P02	Key mask selection	○	○	○	○	×
	D1	**DKM1**	R/W	0	6: P10–12 / 3: P02–03,10 / 0: No mask		○	○	○	○	×
	D0	**DKM0**	R/W	0	5: P10–11 / 2: P02–03		○	○	○	○	×
FF4AH	D3	**LCURF** (*6)	R	0	1: Request / 0: No	Lap data carry-up request flag	○	○	○	○	×
	D2	**CRNWF** (*6)	R	0	1: Renewal / 0: No	Capture renewal flag	○	○	○	○	×
	D1	**SWRUN**	R/W	0	1: Run / 0: Stop	Stopwatch timer Run / Stop	○	○	○	○	○
	D0	**SWRST** (*3)	W	(Reset)	1: Reset / 0: Invalid	Stopwatch timer reset (writing)	○	○	○	○	○
FF4BH	D3	**SWD3**	R	0	0-9	Stopwatch timer data BCD(1/1000 sec)	○	○	○	○	○
	D2	**SWD2**	R	0			○	○	○	○	○
	D1	**SWD1**	R	0			○	○	○	○	○
	D0	**SWD0**	R	0			○	○	○	○	○
FF4CH	D3	**SWD7**	R	0	0-9	Stopwatch timer data BCD(1/100 sec)	○	○	○	○	○
	D2	**SWD6**	R	0			○	○	○	○	○
	D1	**SWD5**	R	0			○	○	○	○	○
	D0	**SWD4**	R	0			○	○	○	○	○
FF4DH	D3	**SWD11**	R	0	0-9	Stopwatch timer data BCD(1/10 sec)	○	○	○	○	○
	D2	**SWD10**	R	0			○	○	○	○	○
	D1	**SWD9**	R	0			○	○	○	○	○
	D0	**SWD8**	R	0			○	○	○	○	○

FF50H- FF52H LCD Driver

Address		Register name	R/W	Default	Setting / data	Function	F016	016	008	004	003
FF50H	D3	0 (*3)	R	– (*2)	—	Unused	○	○	○	○	○
	D2	0 (*3)	R	– (*2)	—	Unused	○	○	○	○	○
	D1	**DSPC1**	R/W	1	3 All on 1 All on	LCD display mode selection	○	○	○	○	○
	D0	**DSPC0**	R/W	0	2 All off 0 Normal		○	○	○	○	○
FF51H	D3	**STCD**	R/W	0	1 Static 0 Dynamic	LCD drive mode switch	○	○	○	○	○
	D2	**LDUTY2**	R/W	0	7 1/8 4 1/7 1 1/4	LCD drive duty selection	○	○	○	○	○
	D1	**LDUTY1**	R/W	0	6 1/7 3 1/6 0 1/3		○	○	○	○	○
	D0	**LDUTY0**	R/W	0	5 1/8 2 1/5		○	○	○	○	○
FF52H (*6)	D3	**LC3**	R/W	0	0H(light)–FH(dark)	LCD contrast adjustment	○	○	○	○	×
	D2	**LC2**	R/W	0			○	○	○	○	×
	D1	**LC1**	R/W	0			○	○	○	○	×
	D0	**LC0**	R/W	0			○	○	○	○	×

FF58H- FF5CH Serial Interface

Address		Register name	R/W	Default	Setting / data	Function	F016	016	008	004	003
FF58H (*6)	D3	0 (*3)	R	– (*2)	—	Unused	○	○	○	○	○
	D2	**ESOUT**	R/W	0	1 Enable 0 Disable	SOUT enable	○	○	○	○	×
	D1	**SCTRG**	R/W	0	1 Trigger (W) Run (R) 0 Invalid (W) Stop (R)	Serial I/F clock trigger (writing) Serial I/F clock status (reading)	○	○	○	○	×
	D0	**ESIF**	R/W	0	1 SIF 0 I/O	Serial I/F enable (P3 port function selection)	○	○	○	○	×
FF59H (*6)	D3	**SCPS1**	R/W	0	3 Negative ↑ 1 Positive ↓	Serial I/F clock format selection	○	○	○	○	×
	D2	**SCPS0**	R/W	0	2 Negative ↓ 0 Positive ↑	(polarity, phase)	○	○	○	○	×
	D1	**SDP**	R/W	0	1 MSB first 0 LSB first	Serial I/F data input / output permutation	○	○	○	○	×
	D0	**SMOD**	R/W	0	1 Master 0 Slave	Serial I/F mode selection	○	○	○	○	×
FF5AH (*6)	D3	0 (*3)	R	– (*2)	—	Unused	○	○	○	○	○
	D2	0 (*3)	R	– (*2)	—	Unused	○	○	○	○	○
	D1	**ESREADY**	R/W	0	1 SRDY 0 SS	SRDY_SS function selection (ENCS = "1")	○	○	○	○	×
	D0	**ENCS**	R/W	0	1 SRDY_SS 0 P33	SRDY_SS enable (P33 port function selection)	○	○	○	○	×
FF5BH (*6)	D3	**SD3**	R/W	×	0H–FH	Serial I/F transmit / receive data (low-order 4 bits) SD0 = LSB	○	○	○	○	×
	D2	**SD2**	R/W	×			○	○	○	○	×
	D1	**SD1**	R/W	×			○	○	○	○	×
	D0	**SD0**	R/W	×			○	○	○	○	×
FF5CH (*6)	D3	**SD7**	R/W	×	0H–FH	Serial I/F transmit / receive data (high-order 4 bits) SD7 = MSB	○	○	○	○	×
	D2	**SD6**	R/W	×			○	○	○	○	×
	D1	**SD5**	R/W	×			○	○	○	○	×
	D0	**SD4**	R/W	×			○	○	○	○	×

6. Differences of I/O Registers

FF60H- FF6BH									RF Converter	F016	016	008	004	003
Address		**Register name**	**R/W**	**Default**	**Setting / data**				**Function**					
FF60H	D3	**RFCNT**	R/W	0	1	Continuous	0	Normal	Continuous oscillation enable	○	○	○	○	○
	D2	**RFOUT**	R/W	0	1	Enable	0	Disable	RFOUT enable	○	○	○	○	○
	D1	**ERF1**	R/W	0	3	Ch.1 DC	1	Ch.0 DC	R/F conversion selection	○	○	○	○	○
	D0	**ERF0**	R/W	0	2	Ch.1 AC	0	I/O		○	○	○	○	○
FF61H	D3	**OVTC**	R/W	0	1	Overflow error	0	No error	Time base counter overflow flag	○	○	○	○	○
	D2	**OVMC**	R/W	0	1	Overflow error	0	No error	Measurement counter overflow flag	○	○	○	○	○
	D1	**RFRUNR**	R/W	0	1	Run	0	Stop	Reference oscillation Run control / status	○	○	○	○	○
	D0	**RFRUNS**	R/W	0	1	Run	0	Stop	Sensor oscillation Run control / status	○	○	○	○	○
FF62H	D3	**MC3**	R/W	×	0H–FH				Measurement counter MC0–MC3 MC0 = LSB	○	○	○	○	○
	D2	**MC2**	R/W	×						○	○	○	○	○
	D1	**MC1**	R/W	×						○	○	○	○	○
	D0	**MC0**	R/W	×						○	○	○	○	○
FF63H	D3	**MC7**	R/W	×	0H–FH				Measurement counter MC4–MC7	○	○	○	○	○
	D2	**MC6**	R/W	×						○	○	○	○	○
	D1	**MC5**	R/W	×						○	○	○	○	○
	D0	**MC4**	R/W	×						○	○	○	○	○
FF64H	D3	**MC11**	R/W	×	0H–FH				Measurement counter MC8–MC11	○	○	○	○	○
	D2	**MC10**	R/W	×						○	○	○	○	○
	D1	**MC9**	R/W	×						○	○	○	○	○
	D0	**MC8**	R/W	×						○	○	○	○	○
FF65H	D3	**MC15**	R/W	×	0H–FH				Measurement counter MC12–MC15	○	○	○	○	○
	D2	**MC14**	R/W	×						○	○	○	○	○
	D1	**MC13**	R/W	×						○	○	○	○	○
	D0	**MC12**	R/W	×						○	○	○	○	○
FF66H	D3	**MC19**	R/W	×	0H–FH				Time base counter TC16–TC19 TC19 = MSB	○	○	○	○	○
	D2	**MC18**	R/W	×						○	○	○	○	○
	D1	**MC17**	R/W	×						○	○	○	○	○
	D0	**MC16**	R/W	×						○	○	○	○	○
FF67H	D3	**TC3**	R/W	×	0H–FH				Time base counter TC0–TC3 TC0 = LSB	○	○	○	○	○
	D2	**TC2**	R/W	×						○	○	○	○	○
	D1	**TC1**	R/W	×						○	○	○	○	○
	D0	**TC0**	R/W	×						○	○	○	○	○
FF68H	D3	**TC7**	R/W	×	0H–FH				Time base counter TC4–TC7	○	○	○	○	○
	D2	**TC6**	R/W	×						○	○	○	○	○
	D1	**TC5**	R/W	×						○	○	○	○	○
	D0	**TC4**	R/W	×						○	○	○	○	○
FF69H	D3	**TC11**	R/W	×	0H–FH				Time base counter TC8–TC11	○	○	○	○	○
	D2	**TC10**	R/W	×						○	○	○	○	○
	D1	**TC9**	R/W	×						○	○	○	○	○
	D0	**TC8**	R/W	×						○	○	○	○	○
FF6AH	D3	**TC15**	R/W	×	0H–FH				Time base counter TC12–TC15	○	○	○	○	○
	D2	**TC14**	R/W	×						○	○	○	○	○
	D1	**TC13**	R/W	×						○	○	○	○	○
	D0	**TC12**	R/W	×						○	○	○	○	○
FF6BH	D3	**TC19**	R/W	×	0H–FH				Time base counter TC16–TC19 TC19 = MSB	○	○	○	○	○
	D2	**TC18**	R/W	×						○	○	○	○	○
	D1	**TC17**	R/W	×						○	○	○	○	○
	D0	**TC16**	R/W	×						○	○	○	○	○

FF70H- FF76H										Integer Multiplier	F016	016	008	004	003
Address		**Register name**	**R/W**	**Default**		**Setting / data**				**Function**					
FF70H (*5)	D3	**SR3**	R/W	×		0H–FH				Source register (low-order 4 bits) SR0 = LSB	○	○	○	×	×
	D2	**SR2**	R/W	×							○	○	○	×	×
	D1	**SR1**	R/W	×							○	○	○	×	×
	D0	**SR0**	R/W	×							○	○	○	×	×
FF71H (*5)	D3	**SR7**	R/W	×		0H–FH				Source register (high-order 4 bits) SR7 = MSB	○	○	○	×	×
	D2	**SR6**	R/W	×							○	○	○	×	×
	D1	**SR5**	R/W	×							○	○	○	×	×
	D0	**SR4**	R/W	×							○	○	○	×	×
FF72H (*5)	D3	**DRL3**	R/W	×		0H–FH				Low-order 8-bit destination register (low-order 4 bits) DRL0 = LSB	○	○	○	×	×
	D2	**DRL2**	R/W	×							○	○	○	×	×
	D1	**DRL1**	R/W	×							○	○	○	×	×
	D0	**DRL0**	R/W	×							○	○	○	×	×
FF73H (*5)	D3	**DRL7**	R/W	×		0H–FH				Low-order 8-bit destination register (high-order 4 bits) DRL7 = MSB	○	○	○	×	×
	D2	**DRL6**	R/W	×							○	○	○	×	×
	D1	**DRL5**	R/W	×							○	○	○	×	×
	D0	**DRL4**	R/W	×							○	○	○	×	×
FF74H (*5)	D3	**DRH3**	R/W	×		0H–FH				High-order 8-bit destination register (low-order 4 bits) DRH0 = LSB	○	○	○	×	×
	D2	**DRH2**	R/W	×							○	○	○	×	×
	D1	**DRH1**	R/W	×							○	○	○	×	×
	D0	**DRH0**	R/W	×							○	○	○	×	×
FF75H (*5)	D3	**DRH7**	R/W	×		0H–FH				High-order 8-bit destination register (high-order 4 bits) DRH7 = MSB	○	○	○	×	×
	D2	**DRH6**	R/W	×							○	○	○	×	×
	D1	**DRH5**	R/W	×							○	○	○	×	×
	D0	**DRH4**	R/W	×							○	○	○	×	×
FF76H (*5)	D3	**NF**	R	0	1	Negative	0	Positive		Negative flag	○	○	○	×	×
	D2	**VF**	R	0	1	Overflow	0	No		Overflow flag	○	○	○	×	×
	D1	**ZF**	R	0	1	Zero	0	No		Zero flag	○	○	○	×	×
	D0	**CALMD**	R/W	0	1	Division (W) Run (R)	0	Multiplication (W) Stop (R)		Calculation mode selection (writing) Operation status (reading)	○	○	○	×	×

FF80H- FF8FH					Programmable Timer A						F016	016	008	004	003
Address		Register name	R/W	Default	Setting / data					Function					
FF80H	D3	**MOD16_A** (*6)	R/W	0	1	16 bits	0	8 bits		PTM0–1 16-bit mode selection	○	○	○	○	×
	D2	**EVCNT_A**	R/W	0	1	Event counter	0	Timer		PTM0 counter mode selection	○	○	○	○	○
	D1	**FCSEL_A**	R/W	0	1	With noise reject	0	No noise reject		PTM0 function selection (for event counter mode)	○	○	○	○	○
	D0	**PLPUL_A**	R/W	0	1	↑ (positive)	0	↓ (negative)		PTM0 pulse polarity selection (for event counter mode)	○	○	○	○	○
FF81H	D3	**PTSEL1** (*6)	R/W	0	1	PWM	0	Normal		Programmable timer 1 PWM output selection	○	○	○	○	×
	D2	**PTSEL0** (*6)	R/W	0	1	PWM	0	Normal		Programmable timer 0 PWM output selection	○	○	○	○	×
	D1	**CHSEL_A** (*6)	R/W	0	1	Timer 1	0	Timer 0		PTM0–1 TOUT_A output selection	○	○	○	○	×
	D0	**PTOUT_A**	R/W	0	1	On	0	Off		PTM0–1 TOUT_A output selection	○	○	○	○	○
FF82H	D3	**PTRST1** (*3, *6)	W	– (*2)	1	Reset	0	Invalid		Programmable timer 1 reset (reload)	○	○	○	○	×
	D2	**PTRUN1** (*6)	R/W	0	1	Run	0	Stop		Programmable timer 1 Run / Stop	○	○	○	○	×
	D1	**PTRST0** (*3)	W	– (*2)	1	Reset	0	Invalid		Programmable timer 0 reset (reload)	○	○	○	○	○
	D0	**PTRUN0**	R/W	0	1	Run	0	Stop		Programmable timer 0 Run / Stop	○	○	○	○	○
FF84H	D3	**RLD03**	R/W	0	0H–FH					Programmable timer 0 reload data (low-order 4 bits) RLD00 = LSB	○	○	○	○	○
	D2	**RLD02**	R/W	0							○	○	○	○	○
	D1	**RLD01**	R/W	0							○	○	○	○	○
	D0	**RLD00**	R/W	0							○	○	○	○	○
FF85H	D3	**RLD07**	R/W	0	0H–FH					Programmable timer 0 reload data (high-order 4 bits) RLD07 = MSB	○	○	○	○	○
	D2	**RLD06**	R/W	0							○	○	○	○	○
	D1	**RLD05**	R/W	0							○	○	○	○	○
	D0	**RLD04**	R/W	0							○	○	○	○	○
FF86H (*6)	D3	**RLD13**	R/W	0	0H–FH					Programmable timer 0 reload data (low-order 4 bits) RLD10 = LSB	○	○	○	○	×
	D2	**RLD12**	R/W	0							○	○	○	○	×
	D1	**RLD11**	R/W	0							○	○	○	○	×
	D0	**RLD10**	R/W	0							○	○	○	○	×
FF87H (*6)	D3	**RLD17**	R/W	0	0H–FH					Programmable timer 0 reload data (low-order 4 bits) RLD17 = MSB	○	○	○	○	×
	D2	**RLD16**	R/W	0							○	○	○	○	×
	D1	**RLD15**	R/W	0							○	○	○	○	×
	D0	**RLD14**	R/W	0							○	○	○	○	×
FF88H	D3	**PTD03**	R	0	0H–FH					Programmable timer 0 data (low-order 4 bits) PTD00 = LSB	○	○	○	○	○
	D2	**PTD02**	R	0							○	○	○	○	○
	D1	**PTD01**	R	0							○	○	○	○	○
	D0	**PTD00**	R	0							○	○	○	○	○
FF89H	D3	**PTD07**	R	0	0H–FH					Programmable timer 0 data (high-order 4 bits) PTD07 = MSB	○	○	○	○	○
	D2	**PTD06**	R	0							○	○	○	○	○
	D1	**PTD05**	R	0							○	○	○	○	○
	D0	**PTD04**	R	0							○	○	○	○	○
FF8AH (*6)	D3	**PTD13**	R	0	0H–FH					Programmable timer 1 data (low-order 4 bits) PTD10 = LSB	○	○	○	○	×
	D2	**PTD12**	R	0							○	○	○	○	×
	D1	**PTD11**	R	0							○	○	○	○	×
	D0	**PTD10**	R	0							○	○	○	○	×
FF8BH (*6)	D3	**PTD17**	R	0	0H–FH					Programmable timer 1 data (high-order 4 bits) PTD17 = MSB	○	○	○	○	×
	D2	**PTD16**	R	0							○	○	○	○	×
	D1	**PTD15**	R	0							○	○	○	○	×
	D0	**PTD14**	R	0							○	○	○	○	×

FF80H- FF8FH Programmable Timer A

Address		Register name	R/W	Default	Setting / data	Function	F016	016	008	004	003
FF8CH (*6)	D3	**CD03**	R/W	0	0H–FH	Programmable timer 0 compare data (low-order 4 bits) CD00 = LSB	○	○	○	○	×
	D2	**CD02**	R/W	0			○	○	○	○	×
	D1	**CD01**	R/W	0			○	○	○	○	×
	D0	**CD00**	R/W	0			○	○	○	○	×
FF8DH (*6)	D3	**CD07**	R/W	0	0H–FH	Programmable timer 0 compare data (high-order 4 bits) CD07 = MSB	○	○	○	○	×
	D2	**CD06**	R/W	0			○	○	○	○	×
	D1	**CD05**	R/W	0			○	○	○	○	×
	D0	**CD04**	R/W	0			○	○	○	○	×
FF8EH (*6)	D3	**CD13**	R/W	0	0H–FH	Programmable timer 1 compare data (low-order 4 bits) CD10 = LSB	○	○	○	○	×
	D2	**CD12**	R/W	0			○	○	○	○	×
	D1	**CD11**	R/W	0			○	○	○	○	×
	D0	**CD10**	R/W	0			○	○	○	○	×
FF8FH (*6)	D3	**CD17**	R/W	0	0H–FH	Programmable timer 1 compare data (high-order 4 bits) CD17 = MSB	○	○	○	○	×
	D2	**CD16**	R/W	0			○	○	○	○	×
	D1	**CD15**	R/W	0			○	○	○	○	×
	D0	**CD14**	R/W	0			○	○	○	○	×

FF90H- FF9FH Programmable Timer B

Address		Register name	R/W	Default	Setting / data				Function	F016	016	008	004	003
FF90H (*6)	D3	**MOD16_B** (*4)	R/W	0	1	16 bits	0	8 bits	PTM2–3 16-bit mode selection	○	○	×	×	×
	D2	**EVCNT_B**	R/W	0	1	Event counter	0	Timer	PTM2 counter mode selection	○	○	○	○	×
	D1	**FCSEL_B**	R/W	0	1	With noise reject	0	No noise reject	PTM2 function selection (for event counter mode)	○	○	○	○	×
	D0	**PLPUL_B**	R/W	0	1	↑ (positive)	0	↓ (negative)	PTM2 pulse polarity selection (for event counter mode)	○	○	○	○	×
FF91H (*6)	D3	**PTSEL3** (*4)	R/W	0	1	PWM	0	Normal	Programmable timer 3 PWM output selection	○	○	×	×	×
	D2	**PTSEL2**	R/W	0	1	PWM	0	Normal	Programmable timer 2 PWM output selection	○	○	○	○	×
	D1	**CHSEL_B** (*4)	R/W	0	1	Timer 3	0	Timer 2	PTM2–13 TOUT_B output selection	○	○	×	×	×
	D0	**PTOUT_B**	R/W	0	1	On	0	Off	PTM2–3 TOUT_B output control	○	○	○	○	×
FF92H (*6)	D3	**PTRST3**(*3, *4)	W	– (*2)	1	Reset	0	Invalid	Programmable timer 3 reset (reload)	○	○	×	×	×
	D2	**PTRUN3**(*4)	R/W	0	1	Run	0	Stop	Programmable timer 3 Run / Stop	○	○	×	×	×
	D1	**PTRST2** (*3)	W	– (*2)	1	Reset	0	Invalid	Programmable timer 2 reset (reload)	○	○	○	○	×
	D0	**PTRUN2**	R/W	0	1	Run	0	Stop	Programmable timer 2 Run / Stop	○	○	○	○	×
FF94H (*6)	D3	**RLD23**	R/W	0	0H–FH				Programmable timer 2 reload data (low-order 4 bit) RLD20 = LSB	○	○	○	○	×
	D2	**RLD22**	R/W	0						○	○	○	○	×
	D1	**RLD21**	R/W	0						○	○	○	○	×
	D0	**RLD20**	R/W	0						○	○	○	○	×
FF95H (*6)	D3	**RLD27**	R/W	0	0H–FH				Programmable timer 2 reload data (high-order 4 bit) RLD27 = MSB	○	○	○	○	×
	D2	**RLD26**	R/W	0						○	○	○	○	×
	D1	**RLD25**	R/W	0						○	○	○	○	×
	D0	**RLD24**	R/W	0						○	○	○	○	×

FF90H- FF9FH					Programmable Timer B		F016	016	008	004	003
Address		**Register name**	**R/W**	**Default**	**Setting / data**	**Function**					
FF96H (*4)	D3	**RLD33**	R/W	0	0H–FH	Programmable timer 3 reload data (low-order 4 bits) RLD30 = LSB	○	○	×	×	×
	D2	**RLD32**	R/W	0			○	○	×	×	×
	D1	**RLD31**	R/W	0			○	○	×	×	×
	D0	**RLD30**	R/W	0			○	○	×	×	×
FF97H (*4)	D3	**RLD37**	R/W	0	0H–FH	Programmable timer 3 reload data (high-order 4 bits) RLD37 = MSB	○	○	×	×	×
	D2	**RLD36**	R/W	0			○	○	×	×	×
	D1	**RLD35**	R/W	0			○	○	×	×	×
	D0	**RLD34**	R/W	0			○	○	×	×	×
FF98H (*6)	D3	**PTD23**	R	0	0H–FH	Programmable timer 2 data (low-order 4 bits) PTD20 = LSB	○	○	○	○	×
	D2	**PTD22**	R	0			○	○	○	○	×
	D1	**PTD21**	R	0			○	○	○	○	×
	D0	**PTD20**	R	0			○	○	○	○	×
FF99H (*6)	D3	**PTD27**	R	0	0H–FH	Programmable timer 2 data (high-order 4 bits) PTD27 = MSB	○	○	○	○	×
	D2	**PTD26**	R	0			○	○	○	○	×
	D1	**PTD25**	R	0			○	○	○	○	×
	D0	**PTD24**	R	0			○	○	○	○	×
FF9AH (*4)	D3	**PTD33**	R	0	0H–FH	Programmable timer 3 data (low-order 4 bits) PTD30 = LSB	○	○	×	×	×
	D2	**PTD32**	R	0			○	○	×	×	×
	D1	**PTD31**	R	0			○	○	×	×	×
	D0	**PTD30**	R	0			○	○	×	×	×
FF9BH (*4)	D3	**PTD37**	R	0	0H–FH	Programmable timer 3 data (high-order 4 bits) PTD37 = MSB	○	○	×	×	×
	D2	**PTD36**	R	0			○	○	×	×	×
	D1	**PTD35**	R	0			○	○	×	×	×
	D0	**PTD34**	R	0			○	○	×	×	×
FF9CH (*6)	D3	**CD23**	R/W	0	0H–FH	Programmable timer 2 compare data (low-order 4 bits) CD20 = LSB	○	○	○	○	×
	D2	**CD22**	R/W	0			○	○	○	○	×
	D1	**CD21**	R/W	0			○	○	○	○	×
	D0	**CD20**	R/W	0			○	○	○	○	×
FF9DH (*6)	D3	**CD27**	R/W	0	0H–FH	Programmable timer 2 compare data (high-order 4 bits) CD27 = MSB	○	○	○	○	×
	D2	**CD26**	R/W	0			○	○	○	○	×
	D1	**CD25**	R/W	0			○	○	○	○	×
	D0	**CD24**	R/W	0			○	○	○	○	×
FF9EH (*4)	D3	**CD33**	R/W	0	0H–FH	Programmable timer 3 compare data (low-order 4 bits) CD30 = LSB	○	○	×	×	×
	D2	**CD32**	R/W	0			○	○	×	×	×
	D1	**CD31**	R/W	0			○	○	×	×	×
	D0	**CD30**	R/W	0			○	○	×	×	×
FF9FH (*4)	D3	**CD37**	R/W	0	0H–FH	Programmable timer 3 (high-order 4 bits) CD37 = MSB	○	○	×	×	×
	D2	**CD36**	R/W	0			○	○	×	×	×
	D1	**CD35**	R/W	0			○	○	×	×	×
	D0	**CD34**	R/W	0			○	○	×	×	×

FFE1H- FFFFH					Interrupt Controller										
Address		Register name	R/W	Default	Setting / data					Function	F016	016	008	004	003
FFE1H	D3	0 (*3)	R	– (*2)	—					Unused	○	○	○	○	○
	D2	**EIRFE**	R/W	0	1	Enable	0	Mask		Interrupt mask register (RFC error)	○	○	○	○	○
	D1	**EIRFR**	R/W	0	1	Enable	0	Mask		Interrupt mask register (RFC REF completion)	○	○	○	○	○
	D0	**EIRFS**	R/W	0	1	Enable	0	Mask		Interrupt mask register (RFC SEN completion)	○	○	○	○	○
FFE2H	D3	0 (*3)	R	– (*2)	—					Unused	○	○	○	○	○
	D2	0 (*3)	R	– (*2)	—					Unused	○	○	○	○	○
	D1	**EIPT0**	R/W	0	1	Enable	0	Mask		Interrupt mask register (PT0 underflow)	○	○	○	○	○
	D0	**EICTC0**(*6)	R/W	0	1	Enable	0	Mask		Interrupt mask register (PT0 compare match)	○	○	○	○	×
FFE3H (*6)	D3	0 (*3)	R	– (*2)	—					Unused	○	○	○	○	○
	D2	0 (*3)	R	– (*2)	—					Unused	○	○	○	○	○
	D1	**EIPT1**	R/W	0	1	Enable	0	Mask		Interrupt mask register (PT1 underflow)	○	○	○	○	×
	D0	**EICTC1**	R/W	0	1	Enable	0	Mask		Interrupt mask register (PT1 compare match)	○	○	○	○	×
FFE4H (*6)	D3	0 (*3)	R	– (*2)	—					Unused	○	○	○	○	○
	D2	0 (*3)	R	– (*2)	—					Unused	○	○	○	○	○
	D1	**EIPT2**	R/W	0	1	Enable	0	Mask		Interrupt mask register (PT2 underflow)	○	○	○	○	×
	D0	**EICTC2**	R/W	0	1	Enable	0	Mask		Interrupt mask register (PT2 compare match)	○	○	○	○	×
FFE5H (*4)	D3	0 (*3)	R	– (*2)	—					Unused	○	○	○	○	○
	D2	0 (*3)	R	– (*2)	—					Unused	○	○	○	○	○
	D1	**EIPT3**	R/W	0	1	Enable	0	Mask		Interrupt mask register (PT3 underflow)	○	○	×	×	×
	D0	**EICTC3**	R/W	0	1	Enable	0	Mask		Interrupt mask register (PT3 compare match)	○	○	×	×	×
FFEAH (*6)	D3	0 (*3)	R	– (*2)	—					Unused	○	○	○	○	○
	D2	0 (*3)	R	– (*2)	—					Unused	○	○	○	○	○
	D1	0 (*3)	R	– (*2)	—					Unused	○	○	○	○	○
	D0	**EISIF**	R/W	0	1	Enable	0	Mask		Interrupt mask register (serial I/F)	○	○	○	○	×
FFEBH	D3	**EIK03**	R/W	0	1	Enable	0	Mask		Interrupt mask register (KEY03<P03>)	○	○	○	○	○
	D2	**EIK02**	R/W	0	1	Enable	0	Mask		Interrupt mask register (KEY02<P02>)	○	○	○	○	○
	D1	**EIK01**	R/W	0	1	Enable	0	Mask		Interrupt mask register (KEY01<P01>)	○	○	○	○	○
	D0	**EIK00**	R/W	0	1	Enable	0	Mask		Interrupt mask register (KEY00<P00>)	○	○	○	○	○
FFECH (*6)	D3	**EIK13**	R/W	0	1	Enable	0	Mask		Interrupt mask register (KEY13<P13>)	○	○	○	○	×
	D2	**EIK12**	R/W	0	1	Enable	0	Mask		Interrupt mask register (KEY12<P12>)	○	○	○	○	×
	D1	**EIK11**	R/W	0	1	Enable	0	Mask		Interrupt mask register (KEY11<P11>)	○	○	○	○	×
	D0	**EIK10**	R/W	0	1	Enable	0	Mask		Interrupt mask register (KEY10<P10>)	○	○	○	○	×
FFEDH	D3	**EIRUN**(*6)	R/W	0	1	Enable	0	Mask		Interrupt mask register (SW direct RUN)	○	○	○	○	×
	D2	**EILAP** (*6)	R/W	0	1	Enable	0	Mask		Interrupt mask register (SW direct LAP)	○	○	○	○	×
	D1	**EISW1**	R/W	0	1	Enable	0	Mask		Interrupt mask register (SW direct RUN)	○	○	○	○	○
	D0	**EISW10**	R/W	0	1	Enable	0	Mask		Interrupt mask register (stopwatch 10Hz)	○	○	○	○	○
FFEEH	D3	**EIT3** (*6)	R/W	0	1	Enable	0	Mask		Interrupt mask register (clock timer 16Hz)	○	○	○	○	×
	D2	**EIT2**	R/W	0	1	Enable	0	Mask		Interrupt mask register (clock timer 32Hz)	○	○	○	○	○
	D1	**EIT1** (*6)	R/W	0	1	Enable	0	Mask		Interrupt mask register (clock timer 64Hz)	○	○	○	○	×
	D0	**EIT0** (*6)	R/W	0	1	Enable	0	Mask		Interrupt mask register (clock timer 128Hz)	○	○	○	○	×
FFEFH	D3	**EIT7**	R/W	0	1	Enable	0	Mask		Interrupt mask register (clock timer 1Hz)	○	○	○	○	○
	D2	**EIT6**	R/W	0	1	Enable	0	Mask		Interrupt mask register (clock timer 2Hz)	○	○	○	○	○
	D1	**EIT5**(*6)	R/W	0	1	Enable	0	Mask		Interrupt mask register (clock timer 4Hz)	○	○	○	○	×
	D0	**EIT4**	R/W	0	1	Enable	0	Mask		Interrupt mask register (clock timer 8Hz)	○	○	○	○	○

FFE1H- FFFFH					Interrupt Controller						F016	016	008	004	003
Address		Register name	R/W	Default	Setting / data					Function					
FFF1H	D3	0 (*3)	R	– (*2)	—					Unused	○	○	○	○	○
	D2	**IRFE**	R/W	0	1	Occurred (R) Reset (W)	0	Not occurred (R) Invalid (W)		Interrupt factor flag (RFC Error)	○	○	○	○	○
	D1	**IRFR**	R/W	0						Interrupt factor flag (RFC REF completion)	○	○	○	○	○
	D0	**IRFS**	R/W	0						Interrupt factor flag (RFC SEN completion)	○	○	○	○	○
FFF2H	D3	0 (*3)	R	– (*2)	—					Unused	○	○	○	○	○
	D2	0 (*3)	R	– (*2)	—					Unused	○	○	○	○	○
	D1	**IPT0**	R/W	0	1	Occurred (R) Reset (W)	0	Not occurred (R) Invalid (W)		Interrupt factor flag (PT0 underflow)	○	○	○	○	○
	D0	**ICTC0** (*6)	R/W	0						Interrupt factor flag (PT0 compare match)	○	○	○	○	×
FFF3H (*6)	D3	0 (*3)	R	– (*2)	—					Unused	○	○	○	○	○
	D2	0 (*3)	R	– (*2)	—					Unused	○	○	○	○	○
	D1	**IPT1**	R/W	0	1	Occurred (R) Reset (W)	0	Not occurred (R) Invalid (W)		Interrupt factor flag (PT1 underflow)	○	○	○	○	×
	D0	**ICTC1**	R/W	0						Interrupt factor flag (PT1 compare match)	○	○	○	○	×
FFF4H (*6)	D3	0 (*3)	R	– (*2)	—					Unused	○	○	○	○	○
	D2	0 (*3)	R	– (*2)	—					Unused	○	○	○	○	○
	D1	**IPT2**	R/W	0	1	Occurred (R) Reset (W)	0	Not occurred (R) Invalid (W)		Interrupt factor flag (PT2 underflow)	○	○	○	○	×
	D0	**ICTC2**	R/W	0						Interrupt factor flag (PT2 compare match)	○	○	○	○	×
FFF5H (*4)	D3	0 (*3)	R	– (*2)	—					Unused	○	○	○	○	○
	D2	0 (*3)	R	– (*2)	—					Unused	○	○	○	○	○
	D1	**IPT3**	R/W	0	1	Occurred (R) Reset (W)	0	Not occurred (R) Invalid (W)		Interrupt factor flag (PT3 underflow)	○	○	×	×	×
	D0	**ICTC3**	R/W	0						Interrupt factor flag (PT3 compare match)	○	○	×	×	×
FFFAH (*6)	D3	0 (*3)	R	– (*2)	—					Unused	○	○	○	○	○
	D2	0 (*3)	R	– (*2)	—					Unused	○	○	○	○	○
	D1	0 (*3)	R	– (*2)	—					Unused	○	○	○	○	○
	D0	**ISIF**	R/W	0	1	Occurred (R) Reset (W)	0	Not occurred (R) Invalid (W)		Interrupt factor flag (serial I/F)	○	○	○	○	×
FFFBH	D3	**IK03**	R/W	0	1	Occurred (R) Reset (W)	0	Not occurred (R) Invalid (W)		Interrupt factor flag (KEY03<P03>)	○	○	○	○	○
	D2	**IK02**	R/W	0						Interrupt factor flag (KEY02<P02>)	○	○	○	○	○
	D1	**IK01**	R/W	0						Interrupt factor flag (KEY01<P01>)	○	○	○	○	○
	D0	**IK00**	R/W	0						Interrupt factor flag (KEY00<P00>)	○	○	○	○	○
FFFCH (*6)	D3	**IK13**	R/W	0	1	Occurred (R) Reset (W)	0	Not occurred (R) Invalid (W)		Interrupt factor flag (KEY13<P13>)	○	○	○	○	×
	D2	**IK12**	R/W	0						Interrupt factor flag (KEY12<P12>)	○	○	○	○	×
	D1	**IK11**	R/W	0						Interrupt factor flag (KEY11<P11>)	○	○	○	○	×
	D0	**IK10**	R/W	0						Interrupt factor flag (KEY10<P10>)	○	○	○	○	×
FFFDH	D3	**IRUN** (*6)	R/W	0	1	Occurred (R) Reset (W)	0	Not occurred (R) Invalid (W)		Interrupt factor flag (SW direct RUN)	○	○	○	○	×
	D2	**ILAP** (*6)	R/W	0						Interrupt factor flag (SW direct LAP)	○	○	○	○	×
	D1	**ISW1**	R/W	0						Interrupt factor flag (stopwatch 1Hz)	○	○	○	○	○
	D0	**ISW10**	R/W	0						Interrupt factor flag (stopwatch 10Hz)	○	○	○	○	○
FFFEH	D3	**IT3** (*6)	R/W	0	1	Occurred (R) Reset (W)	0	Not occurred (R) Invalid (W)		Interrupt factor flag (clock timer 16Hz)	○	○	○	○	×
	D2	**IT2**	R/W	0						Interrupt factor flag (clock timer 32Hz)	○	○	○	○	○
	D1	**IT1** (*6)	R/W	0						Interrupt factor flag (clock timer 64Hz)	○	○	○	○	×
	D0	**IT0** (*6)	R/W	0						Interrupt factor flag (clock timer 128Hz)	○	○	○	○	×
FFFFH	D3	**IT7**	R/W	0	1	Occurred (R) Reset (W)	0	Not occurred (R) Invalid (W)		Interrupt factor flag (clock timer 1Hz)	○	○	○	○	○
	D2	**IT6**	R/W	0						Interrupt factor flag (clock timer 2Hz)	○	○	○	○	○
	D1	**IT5** (*6)	R/W	0						Interrupt factor flag (clock timer 4Hz)	○	○	○	○	×
	D0	**IT4**	R/W	0						Interrupt factor flag (clock timer 8Hz)	○	○	○	○	○

7. Notes For Programming With Target Products

For application developments with target products, do not use the unavailable peripheral circuits. The peripheral circuits, for which the configurations are different between S1C6F016 and target products or specific controls are necessary, are described below.

7.1 SVD Circuit

The SVD function is different between S1C6F016 and the target products. For S1C6F016 the voltage setting with only 16 levels is available by using 4 bits of the SVD comparison voltage setting register SVDS [3:0] of FF04. On the other hand, for the target products, the voltage setting with 29 levels is available by using 5 bits of the SVD comparison voltage setting register SVDS [4:0] of FF04 and FF05(D2).

For the target products, when setting the SVD comparison voltage to the level that is available with S1C6F016, set the bit of SVDS [4] of FF05 (D2) to "1". When setting the SVD comparison voltage to the level that is available only with the target products in lower voltage range, set the bit of SVDS [4] of FF05 (D2) to "0" at program developments, though this function is not implemented in S1C6F016.

(S1C63003 does not have the SVD function.)

7.2 RESET Circuit (CPU Operation Startup Time)

For S1C6F016, when the internal initial reset is released, the hardware initialization process (takes 21,515/f_{OSC1} sec. (657ms at f_{OSC1} = 32.768 kHz)) is executed. After this process, the CPU starts operations. However, for the target products, the above hardware initialization process is not executed. The CPU starts operations immediately after the internal initial reset is released. As a result, the program startup time is different between S1C6F016 and the target products. For the reset release time, refer to "Initial Reset" in Technical Manual.

8. Differences Of Electrical Characteristics

8.1 Oscillation Characteristics

The oscillation circuit characteristics of S1C6F016 are almost the same as those of target products.

OSC1 Crystal Oscillation Circuit

S1C6F016: Unless otherwise specified: V_{DD}=1.8 to 3.6V, V_{SS}=0V, T_a=25°C,
Crystal oscillator: C-002RX (R1=30kΩ Typ., CL=12.5pF), CG1 = 25pF (external), CD1=built-in

S1C63016 / 008 / 004 / 003: Unless otherwise specified: V_{DD}=1.1 to 5.5V, V_{SS} 0V, T_a=25°C,
Crystal oscillator: C-002RX (R1=30kΩ Typ., CL=12.5pF), CG1=25pF (external), CD1=built-in

Item	Symbol	Condition	S1C6F016/ S1C63016/008/004/003			Unit
			Min.	Typ.	Max.	
Oscillation start time	tsta		—	—	3	s
External gate capacitance	CG1	Including board capacitance	0	—	25	pF
Built-in drain capacitance	CD1	In case of chip	—	20	—	pF
Frequency / IC deviation	Δf/ΔIC	V_{DD}=constant	-10	—	10	ppm
Frequency / power supply voltage deviation	Δf/ΔV		—	—	1	ppm/V
Frequency adjustment range	Δf/ΔCG	V_{DD}=constant, CG=0 to 25pF	25	—	—	ppm

OSC3 Ceramic Oscillation Circuit

S1C6F016: Unless otherwise specified, V_{DD}=1.8 to 3.6V, V_{SS}=0V, T_a=25°C, CG3=CD3=30pF

S1C63016 / 008 / 004 3V normal type: Unless otherwise specified, V_{DD}=1.8 to 5.5V, V_{SS}=0V, T_a=25°C, CG3=CD3=30pF
1.5V low-voltage type: Unless otherwise specified, V_{DD}=1.1 to 1.7V, V_{SS}=0V, T_a=25°C, CG3=CD3=30pF

Item	Symbol	Condition	S1C6F016/ S1C63016/008/004 3V type			S1C63016/008/004 1.5V type			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Oscillation start time	tsta		—	—	1	—	—	3	ms

OSC3 CR Oscillation Circuit (external R)

S1C6F016: Unless otherwise specified, V_{DD}=1.8 to 3.6V, V_{SS}=0V, T_a=25°C

S1C63016 / 008 / 004 3V normal type: Unless otherwise specified, V_{DD}=1.8 to 5.5V, V_{SS}=0V, T_a=25°C, CG3=CD3=30pF
1.5V low-voltage type: Unless otherwise specified: V_{DD}=1.1 to 1.7V, V_{SS}=0V, T_a=25°C, CG3=CD3=30pF

Item	Symbol	Condition	S1C6F016/ S1C63016/008/004 3V type			S1C63016/008/004 1.5V type			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Oscillation start time	tsta		—	—	1	—	—	1	ms
Frequency / IC deviation	Δf/ΔIC		-25	—	25	-33	—	33	%

OSC3 CR Oscillation Circuit (built-in R)

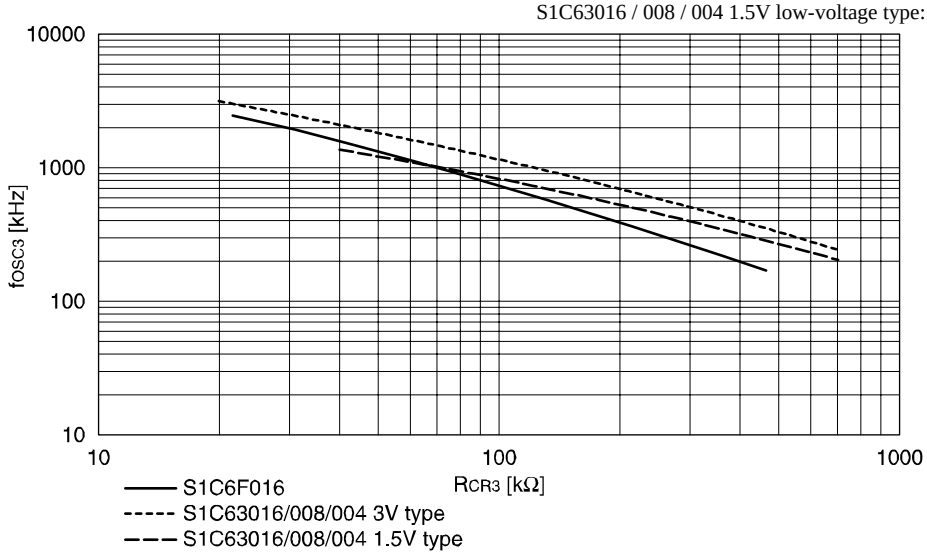
S1C6F016: Unless otherwise specified, V_{DD}=1.8 to 3.6V, V_{SS}=0V, T_a=25°C

S1C63016 / 008 / 004 / 003: Unless otherwise specified, V_{DD}=1.1 to 5.5V, V_{SS}=0V, T_a=25°C

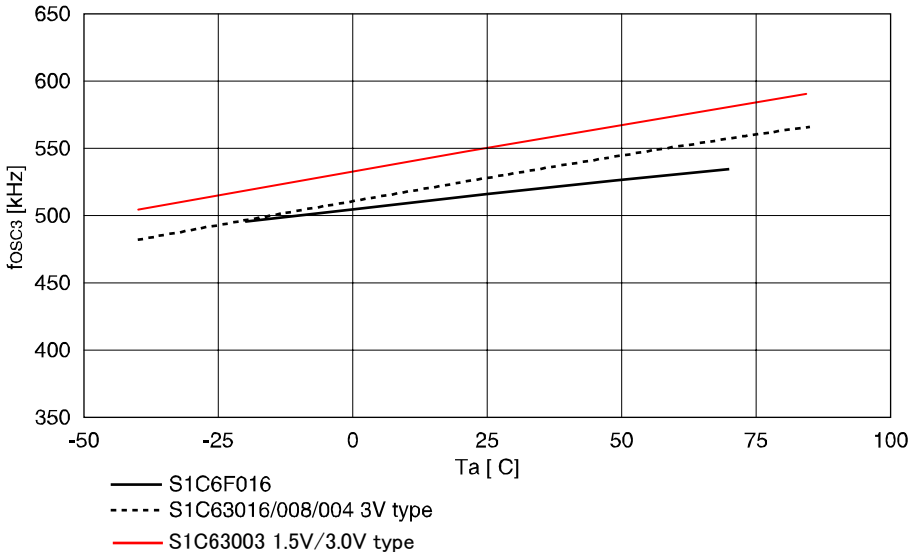
Item	Symbol	Condition	S1C6F016/ S1C63016/008/004			S1C63003			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Oscillation frequency	fOSC3		Typ. × 0.75	500	Typ. × 1.25	Typ. × 0.75	550	Typ. × 1.25	kHz
Oscillation start time	tsta		—	—	20	—	—	20	μs

Characteristics Curves (reference value)

Oscillation frequency - resistor characteristics (OSC3) S1C6F016: V_{DD}=3.6V, T_a=25°C, typical value
<CR oscillation (external R)> S1C63016 / 008 / 004 3V normal type: V_{DD}=5.5V, T_a=25°C, typical value
S1C63016 / 008 / 004 1.5V low-voltage type: V_{DD}=1.7V, T_a=25°C, typical value



Oscillation frequency − temperature characteristics (OSC3) S1C6F016: V_{DD}=3.6V, typical value
<CR oscillation (built-in R)> S1C63016 / 008 / 004 3V normal type: V_{DD}=5.5V, typical value



8.2 DC Characteristics

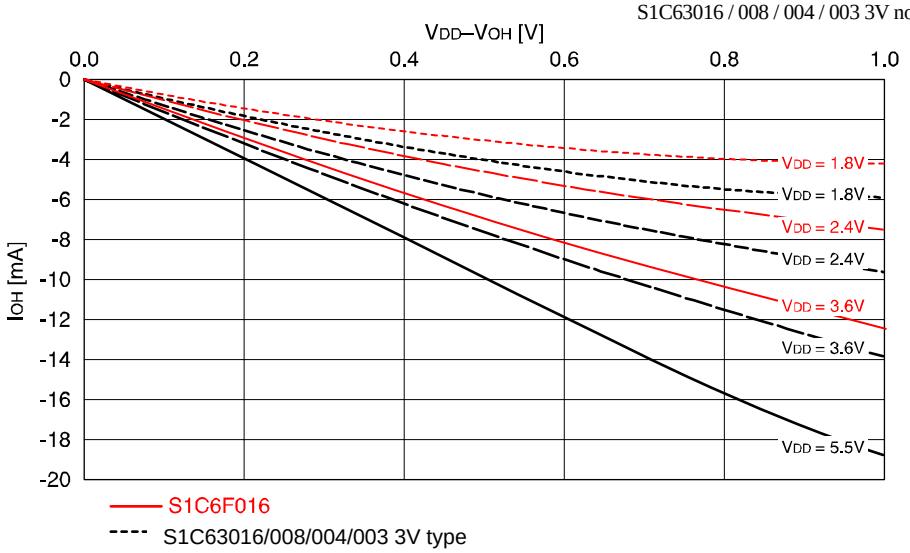
The driving power (maximum output current) of S1C6F016 is slightly higher than the targets. Especially when you use the R/F converter with small external resistance, you cannot neglect the difference. In particular, the difference is significant for the 1.5V low voltage type. If you use this type, make sure you evaluate the R/F converter carefully before using it. The variance of the reference oscillation and sensor oscillation frequencies among ICs can be larger due to the effect of the variance in resistance, capacitance, PCB, and so on.
For information about the voltage variance, see “19 Electrical Characteristics” > “Characteristics Graph (RFC reference oscillation/sensor oscillation frequencies vs. resistance)”.

8. Differences Of Electrical Characteristics

Characteristics Curves (reference value)

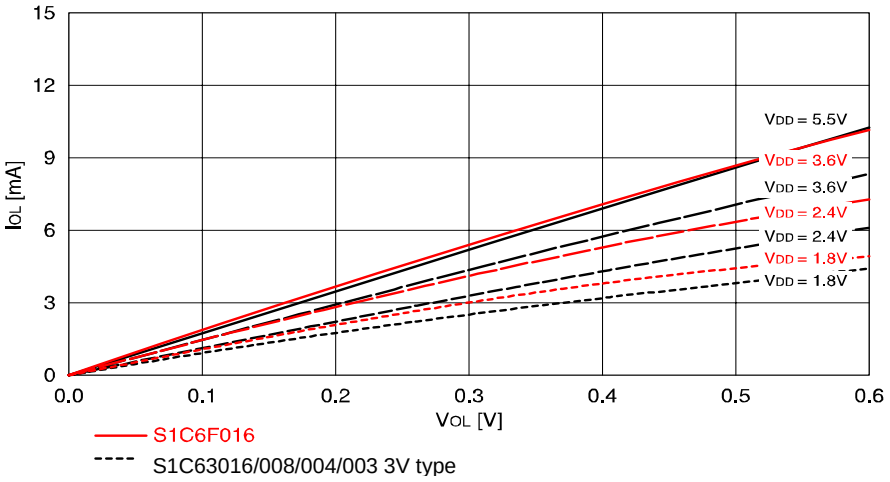
High level output current characteristics

S1C6F016: Ta=70°C, maximum value
S1C63016 / 008 / 004 / 003 3V normal type: Ta=85°C, maximum value



Low level output current characteristics

S1C6F016: Ta=70°C, maximum value
S1C63016 / 008 / 004 / 003 3V normal type: Ta=85°C, maximum value



8.3 LCD Characteristics

LCD drive voltage (reference: V_{C1})

S1C6F016: Unless otherwise specified, V_{DD}=1.8 to 3.6V, V_{SS}=0V, T_a=25°C, C_1 to C_5=0.1µF, checker pattern display, no panel load, 1MΩ load resistor is connected between V_{SS} and V_{C1}, V_{C2}, V_{C3}, respectively.

S1C63016 / 008 / 004 / 003: Unless otherwise specified, V_{DD}=1.2 to 1.7V (1.5V low-voltage type) or V_{DD}=1.8 to 5.5V (3V normal type), V_{SS}=0V, T_a=25°C, C_1 to C_6=0.1µF, checker pattern display, no panel load, 1MΩ load resistor is connected between V_{SS} and V_{C1}, V_{C2}, V_{C3}, respectively.

Item	Symbol	Condition	S1C6F016			S1C63016/008/004			S1C63003			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
LCD Drive Voltage	V_{C1}		0.334 × V_{C3}(typ.)	—	0.364 × V_{C3}(typ.)	0.335 × V_{C3}(typ.)	—	0.363 × V_{C3}(typ.)	0.347 × V_{C3}(typ.)	—	0.350 × V_{C3}(typ.)	V
	V_{C2}		0.653 × V_{C3}(typ.)	—	0.693 × V_{C3}(typ.)	0.646 × V_{C3}(typ.)	—	0.700 × V_{C3}(typ.)	0.665 × V_{C3}(typ.)	—	0.670 × V_{C3}(typ.)	V
	V_{C3}	LC[3:0]=0H	Typ. × 0.96	2.75	Typ. × 1.04							V
		LC[3:0]=1H		2.84					Typ. × 0.96	2.947	Typ. × 1.04	V
		LC[3:0]=2H		2.92								V
		LC[3:0]=3H		3.00								V
		LC[3:0]=4H		3.08								V
		LC[3:0]=5H		3.17								V
		LC[3:0]=6H		3.25								V
		LC[3:0]=7H		3.34		Same as S1C6F016						V
		LC[3:0]=8H		3.42								V
		LC[3:0]=9H		3.50								V
		LC[3:0]=AH		3.58								V
		LC[3:0]=BH		3.67								V
		LC[3:0]=CH		3.75								V
		LC[3:0]=DH		3.83								V
		LC[3:0]=EH		3.91								V
		LC[3:0]=FH		4.00								V

LCD drive voltage (reference: V_{C2})

S1C6F016 : Unless otherwise specified, V_{DD}=3.6V, V_{SS}=0V, T_a=25°C, C_1 to C_5=0.1µF, checker pattern display, no panel load, 1MΩ load resistor is connected between V_{SS} and V_{C1}, V_{C2}, V_{C3}, respectively.

S1C63016 / 008 / 004: Unless otherwise specified, V_{DD}=1.8 to 5.5V, V_{SS}=0V, T_a=25°C, C_1 to C_6=0.1µF, checker pattern display, no panel load, 1MΩ load resistor is connected between V_{SS} and V_{C1}, V_{C2}, V_{C3}, respectively.

Item	Symbol	Condition	S1C6F016			S1C63016/008/004 3V type			S1C63003 3V type			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
LCD Drive Voltage	V_{C1}		0.317 × V_{C3}(typ.)	—	0.357 × V_{C3}(typ.)	0.323 × V_{C3}(typ.)	—	0.349 × V_{C3}(typ.)	0.329 × V_{C3}(typ.)	—	0.340 × V_{C3}(typ.)	V
	V_{C2}		0.656 × V_{C3}(typ.)	—	0.706 × V_{C3}(typ.)	0.650 × V_{C3}(typ.)	—	0.704 × V_{C3}(typ.)	0.660 × V_{C3}(typ.)	—	0.683 × V_{C3}(typ.)	V
	V_{C3}	LC[3:0]=0H	Typ. × 0.96	2.84	Typ. × 1.04							V
		LC[3:0]=1H		2.92					Typ. × 0.96	3.022	Typ. × 1.04	V
		LC[3:0]=2H		3.01								V
		LC[3:0]=3H		3.09								V
		LC[3:0]=4H		3.17								V
		LC[3:0]=5H		3.26								V
		LC[3:0]=6H		3.34								V
		LC[3:0]=7H		3.43		Same as S1C6F016						V
		LC[3:0]=8H		3.51								V
		LC[3:0]=9H		3.60								V
		LC[3:0]=AH		3.68								V
		LC[3:0]=BH		3.77								V
		LC[3:0]=CH		3.85								V
		LC[3:0]=DH		3.94								V
		LC[3:0]=EH		4.02								V
		LC[3:0]=FH		4.11								V

8.4 SVD Characteristics

Refer to the SVD voltage in “19.4 Analog Circuit Characteristics and Current Consumption” in Technical Manual for details.

SVD Circuit

S1C6F016: Unless otherwise specified, V_{DD}=1.8 to 3.6V, V_{SS}=0V, T_a=25°C

S1C63016 / 008 / 004: Unless otherwise specified, V_{DD}=1.1 to 1.7V (1.5V low-voltage type) or V_{DD}=1.8 to 5.5V (3V normal type), V_{SS}=0V, T_a=25°C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	
SVD voltage	V_{SVD}		SVDS[4:0]=00H	Typ. ×0.97	1.05	Typ. ×1.03	V	
			SVDS[4:0]=01H		1.05		V	S1C63016/008/004 1.5V type
			SVDS[4:0]=02H		1.05		V	
			SVDS[4:0]=03H		1.05		V	
			SVDS[4:0]=04H		1.10		V	
			SVDS[4:0]=05H		1.15		V	
			SVDS[4:0]=06H		1.20		V	
			SVDS[4:0]=07H		1.25		V	
			SVDS[4:0]=08H		1.30		V	
			SVDS[4:0]=09H		1.35		V	
			SVDS[4:0]=0AH		1.40		V	
			SVDS[4:0]=0BH		1.45		V	
			SVDS[4:0]=0CH		1.50		V	
			SVDS[4:0]=0DH		1.55		V	
			SVDS[4:0]=0EH		1.60		V	
			SVDS[4:0]=0FH		1.65		V	
		SVDS[3:0]=0H	SVDS[4:0]=10H	Typ. ×0.97	1.70	Typ. ×1.03	V	
		SVDS[3:0]=1H	SVDS[4:0]=11H		1.80		V	S1C6F016/ S1C63016/008/004 3V type
		SVDS[3:0]=2H	SVDS[4:0]=12H		1.90		V	
		SVDS[3:0]=3H	SVDS[4:0]=13H		2.00		V	
		SVDS[3:0]=4H	SVDS[4:0]=14H		2.10		V	
		SVDS[3:0]=5H	SVDS[4:0]=15H		2.20		V	
		SVDS[3:0]=6H	SVDS[4:0]=16H		2.30		V	
		SVDS[3:0]=7H	SVDS[4:0]=17H		2.40		V	
		SVDS[3:0]=8H	SVDS[4:0]=18H		2.50		V	
		SVDS[3:0]=9H	SVDS[4:0]=19H		2.60		V	
		SVDS[3:0]=AH	SVDS[4:0]=1AH		2.70		V	
		SVDS[3:0]=BH	SVDS[4:0]=1BH		2.80		V	
		SVDS[3:0]=CH	SVDS[4:0]=1CH		2.90		V	
		SVDS[3:0]=DH	SVDS[4:0]=1DH		3.00		V	
		SVDS[3:0]=EH	SVDS[4:0]=1EH		3.10		V	
		SVDS[3:0]=FH	SVDS[4:0]=1FH		3.20		V	
SVD circuit response time	t_{SVD}			—	—	500	µs	

8.5 Operating Power Supply Voltage Range

The operating voltage range of S1C6F016 is different from that of target products. Refer to "19.2 Recommended Operating Conditions" in Technical Manual for details.

For S1C6F016, all circuit blocks, except OSC1 and OSC3 oscillation circuits and LCD driver, operate with the power supply voltage V_{DD} – V_{SS}. As a result, the current consumption is different from that of target products.

Absolute Maximum Rating (items with difference only)

Item	Symbol	Condition	Rated value			Unit
			S1C6F016	S1C63016/008/004/003		
				3V type	1.5V type	
Power supply voltage	V_{DD}	—	-0.3 to +4.0	-0.3 to +6.0	-0.3 to +3.0	V
LCD power supply voltage	V_{C3}	—	-0.3 to +6.0	←	←	V
Operating temperature	T_a	—	-20 to +70	-40 to +85	←	°C

Recommended Operating Conditions (items with difference only)

Item	Symbol	Condition	S1C6F016			S1C63016/008/004						Unit
						3V type			1.5V type			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Power supply voltage	V_{DD}	Normal operation mode	1.8	—	3.6	1.8	—	5.5	1.1	—	1.7	V
		Flash programming mode	2.7	—	3.6	—	—	—	—	—	—	V
Operating frequency	f_{OSC1}	Crystal oscillation	—	32.768	—	←			←			kHz
	f_{OSC3}	Ceramic oscillation *1	30	—	4,200	←			30	—	1,000	kHz
		CR oscillation (external R) *1	30	—	2,200	←			30	—	500	kHz

*1 S1C6F016/S1C63016/008/004 only

Revision History

Attachment-1

Code No.	Page	Contents
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EPSON

International Sales Operations

AMERICA

EPSON ELECTRONICS AMERICA, INC.
214 Devcon Drive,
San Jose, CA 95112, USA
Phone: +1-800-228-3964 FAX: +1-408-922-0238

EUROPE

EPSON EUROPE ELECTRONICS GmbH
Riesstrasse 15, 80992 Munich,
GERMANY
Phone: +49-89-14005-0 FAX: +49-89-14005-110

ASIA

EPSON (CHINA) CO., LTD.
7F, Jinbao Bldg., No.89 Jinbao St.,
Dongcheng District,
Beijing 100005, CHINA
Phone: +86-10-8522-1199 FAX: +86-10-8522-1125

SHANGHAI BRANCH
7F, Block B, Hi-Tech Bldg., 900 Yishan Road,
Shanghai 200233, CHINA
Phone: +86-21-5423-5577 FAX: +86-21-5423-4677

SHENZHEN BRANCH
12F, Dawning Mansion, Keji South 12th Road,
Hi-Tech Park, Shenzhen 518057, CHINA
Phone: +86-755-2699-3828 FAX: +86-755-2699-3838

EPSON HONG KONG LTD.
20/F, Harbour Centre, 25 Harbour Road,
Wanchai, Hong Kong
Phone: +852-2585-4600 FAX: +852-2827-4346
Telex: 65542 EPSCO HX

EPSON TAIWAN TECHNOLOGY & TRADING LTD.
14F, No. 7, Song Ren Road,
Taipei 110, TAIWAN
Phone: +886-2-8786-6688 FAX: +886-2-8786-6660

EPSON SINGAPORE PTE., LTD.
1 HarbourFront Place,
#03-02 HarbourFront Tower One, Singapore 098633
Phone: +65-6586-5500 FAX: +65-6271-3182

SEIKO EPSON CORP.
KOREA OFFICE
50F, KLI 63 Bldg., 60 Yoido-dong,
Youngdeungpo-Ku, Seoul 150-763, KOREA
Phone: +82-2-784-6027 FAX: +82-2-767-3677

SEIKO EPSON CORP.
SEMICONDUCTOR OPERATIONS DIVISION

IC Sales Dept.
IC International Sales Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-42-587-5814 FAX: +81-42-587-5117

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