EPSON
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Interlace / Progressive Conversion IC

S2S65P10
Technical Manual

SEIKO EPSON CORPORATION

Rev.1.1

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1. DESCRIPTION

S2S65P10 is an IC which converts the interlace signals into the progressive signals. Combining S2S65P10 with S1S65010 (or S2S65A00) makes it possible to convert the digital signals sent from the NTSC/PAL video decoder into the JPEG format. S2S65P10 has a large-capacity SRAM built in, so it requires no external RAM. S2S65P10 has four channels of video input, and provides versatile screen outputs, including fixed, auto-scan, and 4-input-merge screen outputs. It has also the moving-object detection function built in. It interrupts the host CPU upon detecting a moving object, so it saves power consumption of the system.

2. FEATURES

- Video input
  - 4 channel inputs (any one of them can be set to an output)
  - 8 bit input
  - Compatible with ITU-R BT.601 (4:2:2) / ITU-R BT.656
  - Compatible with NTSC / PAL
  - Compatible with the interlace / progressive inputs
- Video output
  - 2 channel outputs (one of them is shared by video input)
  - 8 bit output
  - Compatible with ITU-R BT.601 (4:2:2) / ITU-R BT.656
  - Compatible with progressive output
  - VGA 30frame/sec(Max.)
  - 4 - 1 Intelligent Image Switch Function
  - Compatible with 4-inputs-merged screen (QVGA × 4 = VGA)
- Host Interface
  - I^2C Interface
  - Interrupt pin (Interrupted upon detection by area sensor)
- Image Processing
  - Interlace / progressive conversion
  - Aspect conversion
  - Area sensor (Detects moving objects and brightness)
- I^2C Through Function (Camera Control or Video Decoder Control) / GPIO
- No external RAM required
- Guaranteed operating temperature -40 to $+105^oC(T_a)$
- CMOS 0.18μm Process
- Supply voltage IO: 2.4 to 3.6V / Internal: 1.8±0.15V
- Package QFP15-100pin (0.5mm pitch)

3. BLOCK DIAGRAM

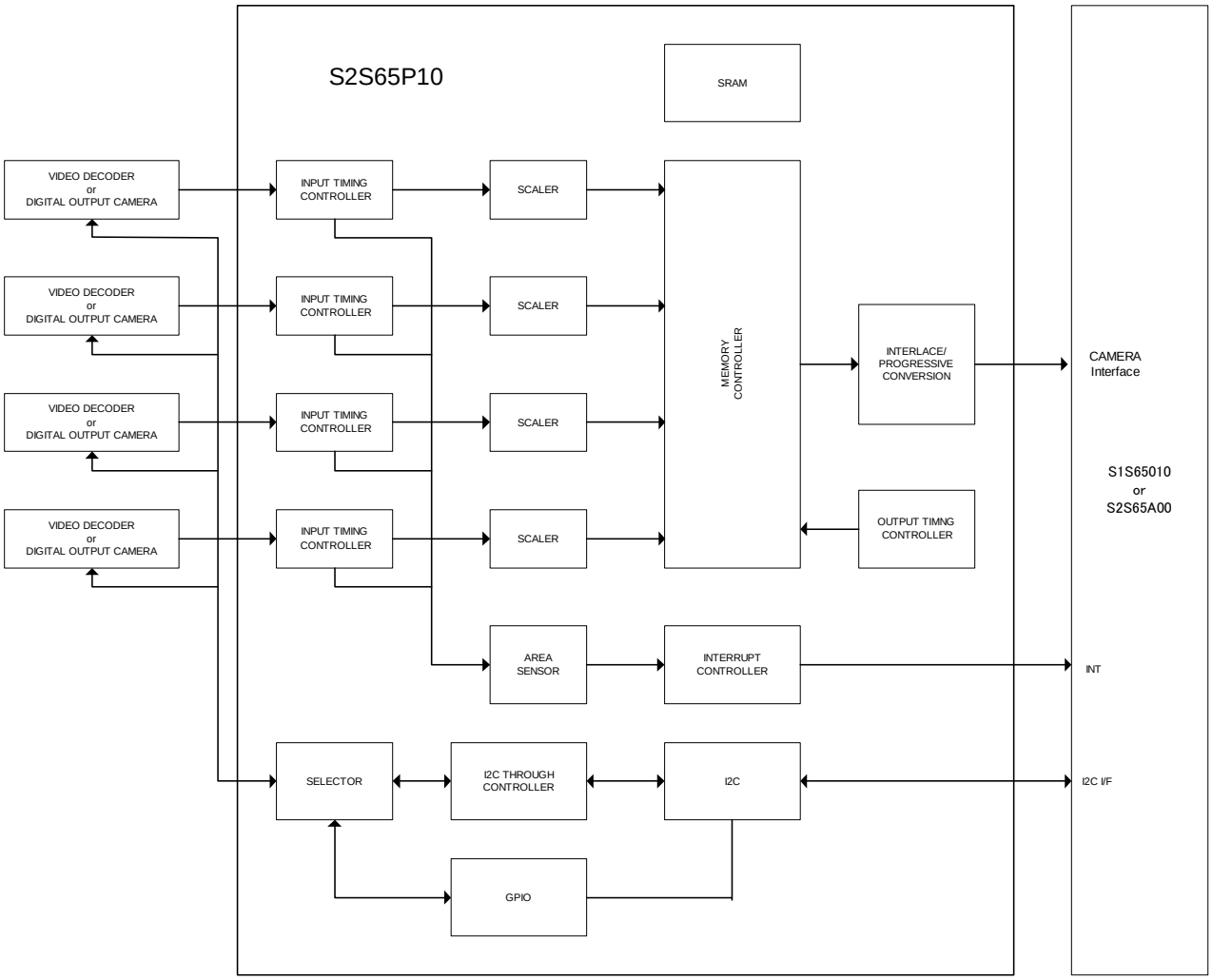


Fig.3.1 S2S65P10 Block Diagram

4. PIN DESCRIPTION

4.1 Pin Assignment

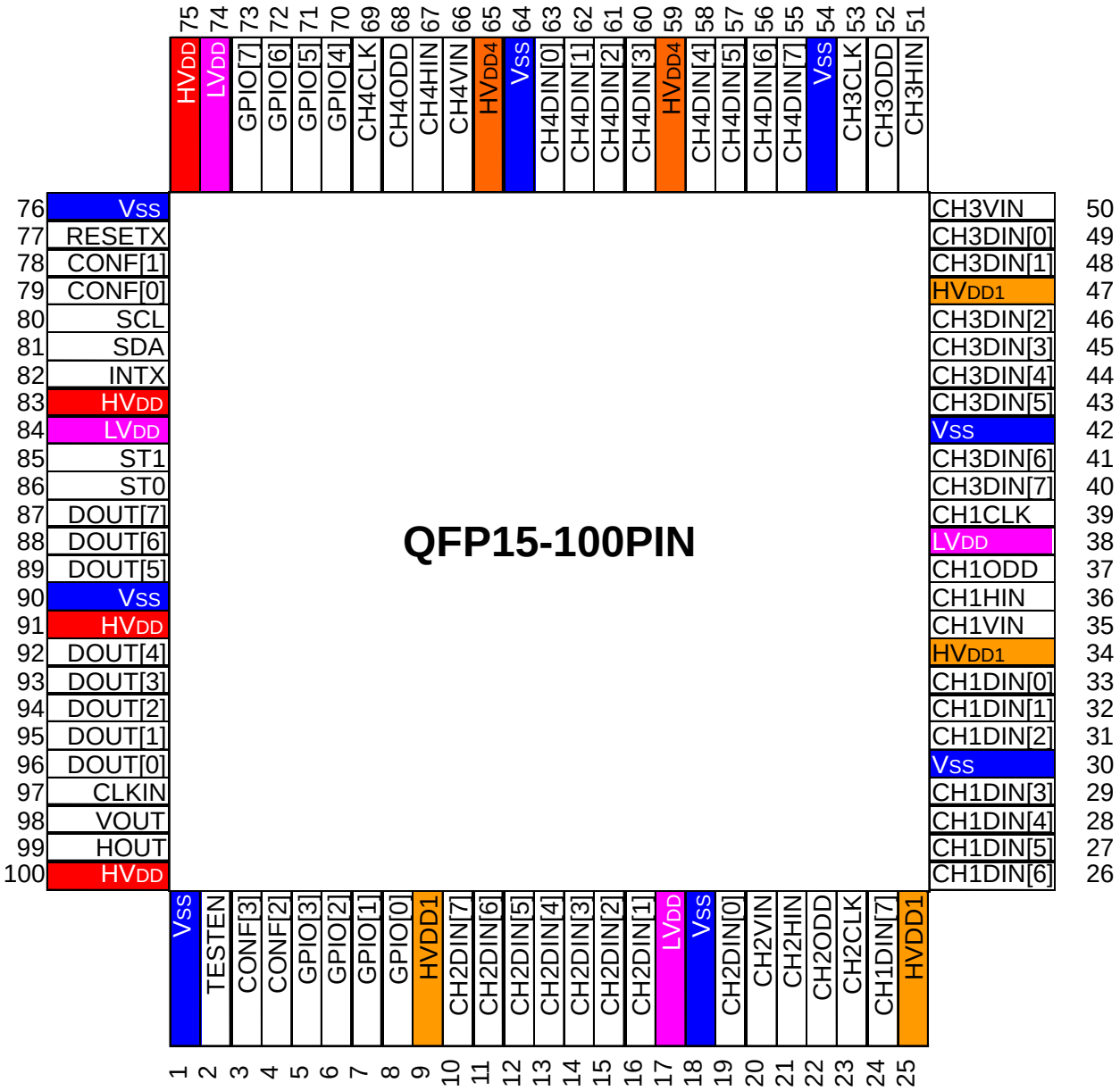


Fig.4.1 Pin assignment (Top View)

4.2 Pin Functions

Reset / Clock

Pin Name	Pin No.	Type	Input Level	Output Current	Description
RESETX	77	I	LVCMOS SCHMITT	—	System Reset Input
CLKIN	97	I	LVCMOS	—	System Clock Input(from S1S65010,S2S65A00)

Video Interface

Pin Name	Pin No.	Type	Input Level	Output Current	Description
CH1CLK	39	I	LVCMOS SCHMITT	—	Video1 Clock input
CH1VIN CH1VOUT	35	I/O	LVCMOS SCHMITT	2mA	Video1 Vertical Synchronization input/output
CH1HIN CH1HOUT	36	I/O	LVCMOS SCHMITT	2mA	Video1 Horizontal Synchronization input/output
CH1DIN[7:0] CH1DOUT[7:0]	33,32,31,29, 28,27,26,24	I/O	LVCMOS SCHMITT	2mA	Video1 Data input/output
CH1ODD	37	I	LVCMOS SCHMITT	—	Video1 Field Signal input
CH2CLK	23	I	LVCMOS SCHMITT	—	Video2 Clock input
CH2VIN CH2VOUT	20	I/O	LVCMOS SCHMITT	2mA	Video2 Vertical Synchronization input/output
CH2HIN CH2HOUT	21	I/O	LVCMOS SCHMITT	2mA	Video2 Horizontal Synchronization input/output
CH2DIN[7:0] CH2DOUT[7:0]	19,16,15,14, 13,12,11,10	I/O	LVCMOS SCHMITT	2mA	Video2 Data input/output
CH2ODD	22	I	LVCMOS SCHMITT	—	Video2 Field Signal input
CH3CLK	53	I	LVCMOS SCHMITT	—	Video3 Clock input
CH3VIN CH3VOUT	50	I/O	LVCMOS SCHMITT	2mA	Video3 Vertical Synchronization input/output
CH3HIN CH3HOUT	51	I/O	LVCMOS SCHMITT	2mA	Video3 Horizontal Synchronization input/output
CH3DIN[7:0] CH3DOUT[7:0]	49,48,46,45, 44,43,41,40	I/O	LVCMOS SCHMITT	2mA	Video3 Data input/output
CH3ODD	52	I	LVCMOS SCHMITT	—	Video3 Field Signal input
CH4CLK	69	I	LVCMOS SCHMITT	—	Video4 Clock input
CH4VIN CH4VOUT	66	I/O	LVCMOS SCHMITT	2mA	Video4 Vertical Synchronization input/output
CH4HIN CH4HOUT	67	I/O	LVCMOS SCHMITT	2mA	Video4 Horizontal Synchronization input/output
CH4DIN[7:0] CH4DOUT[7:0]	63,62,61,60, 58,57,56,55	I/O	LVCMOS SCHMITT	2mA	Video4 Data input/output
CH4ODD	68	I	LVCMOS SCHMITT	—	Video4 Field Signal input
VOUT	98	O	—	2mA	Video Vertical Synchronization output
HOUT	99	O	—	2mA	Video Horizontal Synchronization output
DOUT[7:0]	96,95,94,93, 92,89,88,87	O	—	2mA	Video Data output

* Input and output are switched to each other by the setting of internal register with I^2C.

Host Interface

Pin Name	Pin No.	Type	Input Level	Output Current	Description
SDA	81	I/O	LVCMOS	2mA	I^2C Data I/O
SCL	80	I	LVCMOS	—	I^2C Clock
INTX	82	O	—	2mA	Interrupt Output
ST[1:0]	86,85	O	—	2mA	Status Output

Others

Pin Name	Pin No.	Type	Input Level	Output Current	Description
CONF[3:0]	79,78,4,3	I	LVCMOS SCHMITT	—	System configuration input Sets the functions which configure the system when it is booted.
GPIO0	8	I/O	LVCMOS SCHMITT	2mA	GPIO0 I^2C Through function SCL(Clock)
GPIO1	7	I/O	LVCMOS SCHMITT	2mA	GPIO1 I^2C Through function SDA(Data)
GPIO2	6	I/O	LVCMOS SCHMITT	2mA	GPIO2 I^2C Through function SCL(Clock)
GPIO3	5	I/O	LVCMOS SCHMITT	2mA	GPIO3 I^2C Through function SDA(Data)
GPIO4	70	I/O	LVCMOS SCHMITT	2mA	GPIO4 I^2C Through function SCL(Clock)
GPIO5	71	I/O	LVCMOS SCHMITT	2mA	GPIO5 I^2C Through function SDA(Data)
GPIO6	72	I/O	LVCMOS SCHMITT	2mA	GPIO6 I^2C Through function SCL(Clock)
GPIO7	73	I/O	LVCMOS SCHMITT	2mA	GPIO7 I^2C Through function SDA(Data)

* The GPIO functions are switched to each other by the setting of internal register with I^2C.

Test

Pin Name	Pin No.	Type	Input Level	Output Current	Description
TESTEN	2	I	LVCMOS	—	Test pin for the IC; connect it to V_{SS}. Connect this to the V_{SS} pin.

Power Supply

Pin Name	Pin No.	Type	Input Level	Output Current	Description
HV_{DD}	75,83, 91,100	P	—	—	I/O power supply (2.4V to 3.6V)
HV_{DD1}	9,25, 34,47	P	—	—	I/O power supply for video inputs 1 to 3 (2.4V to 3.6V)
HV_{DD4}	59,65	P	—	—	I/O power supply for video input 4 (2.4V to 3.6V)
LV_{DD}	17,38, 74,84	P	—	—	Power supply for internal logic. (1.8V±0.15V)
V_{SS}	1,18,30, 42,54,64, 76,90	P	—	—	GND

5. REGISTER MAP

5.1 Register Table

Address (h)	Register Name	Register Abbreviation	Default Value	R/W	Register Size (bit)
System setting registers					
0000	Chip ID register	SYS_CHIPID	1000h	RO	16
0004 to 000C	Reserved				
0010	Input image 1 setting register	SYS_CH1INMODE	10000xxxb	R/W	8
0014	Input image 2 setting register	SYS_CH2INMODE	00000xxxb	R/W	8
0018	Input image 3 setting register	SYS_CH3INMODE	00000xxxb	R/W	8
001C	Input image 4 setting register	SYS_CH4INMODE	00000xxxb	R/W	8
0020	Video 1 input setting register	SYS_CH1INCONFIG	000x0001b	R/W	8
0024	Video 2 input setting register	SYS_CH2INCONFIG	000x0001b	R/W	8
0028	Video 3 input setting register	SYS_CH3INCONFIG	000x0001b	R/W	8
002C	Video 4 input setting register	SYS_CH4INCONFIG	000x0001b	R/W	8
0030	Output image setting register	SYS_OUTMODE	80h	R/W	8
0034	Video output setting register	SYS_OUTCONFIG	00000011_ 000x0000b	R/W	16
0038	Output image selection register (Fixed mode)	SYS_OUTCH	00h	R/W	8
003C	Reserved				
0040	Video 1 output cycle setting register (Scan mode)	SYS_CH1OUTCYCLE	30h	R/W	8
0044	Video 2 output cycle setting register (Scan mode)	SYS_CH2OUTCYCLE	30h	R/W	8
0048	Video 3 output cycle setting register (Scan mode)	SYS_CH3OUTCYCLE	30h	R/W	8
004C	Video 4 output cycle setting register (Scan mode)	SYS_CH4OUTCYCLE	30h	R/W	8
0050	Video 1 input pull-down control register	SYS_CH1PCCTRL	0000h	R/W	16
0054	Video 2 input pull-down control register	SYS_CH2PCCTRL	0000h	R/W	16
0058	Video 3 input pull-down control register	SYS_CH3PCCTRL	0000h	R/W	16
005C	Video 4 input pull-down control register	SYS_CH4PCCTRL	0000h	R/W	16
0060	GPIO pin pull-up control register	SYS_GPIOPCCTRL	00h	R/W	8
0064	CONF pin pull-down control register	SYS_CONFPCCTRL	00h	R/W	8
I^2C registers					
0400	I^2C setting register	I2C_CONTROL	00h	R/W	8
0404	I^2C Slave address setting register	I2C_SLAVE_ADRS	0011011xb	R/W	8
0408	Software reset register	I2C_SOFTRESET	00h	WO	8
040C	I^2C bus through function control register	I2C_THR_ENABLE	00h	R/W	8
0410	I^2C bus through address setting register	I2C_THR_ADRS	00h	R/W	8
0414	I^2C bus through ID setting register	I2C_THR_DEVID	00h	R/W	8
0418	Reserved				
041C	I^2C bus through hold counter setting register	I2C_THR_HOLD	00h	R/W	8
Video input 1 registers					
0800 to 0804	Reserved				
0808	Video 1 input capture position setting register (X)	VIN1_XSTART	xxh	R/W	8
080C	Video 1 input capture position setting register (Y ODD)	VIN1_YSTART_O	01h	R/W	8
0810	Video 1 input capture position setting register (Y EVEN)	VIN1_YSTART_E	01h	R/W	8
0814	Video 1 input interrupt setting register	VIN1_INTSEL	00h	R/W	8
Video input 2 registers					
0C00 to 0C04	Reserved				
0C08	Video 2 input capture position setting register (X)	VIN2_XSTART	xxh	R/W	8
0C0C	Video 2 input capture position setting register (Y ODD)	VIN2_YSTART_O	01h	R/W	8
0C10	Video 2 input capture position setting register (Y EVEN)	VIN2_YSTART_E	01h	R/W	8
0C14	Video 2 input interrupt setting register	VIN2_INTSEL	00h	R/W	8
Video input 3 registers					
1000 to 1004	Reserved				
1008	Video 3 input capture position setting register (X)	VIN3_XSTART	xxh	R/W	8
100C	Video 3 input capture position setting register (Y ODD)	VIN3_YSTART_O	01h	R/W	8
1010	Video 3 input capture position setting register (Y EVEN)	VIN3_YSTART_E	01h	R/W	8
1014	Video 3 input interrupt setting register	VIN3_INTSEL	00h	R/W	8

Address (h)	Register Name	Register Abbreviation	Default Value	R/W	Register Size (bit)
Video input 4 registers					
1400 to 1404	Reserved				
1408	Video 4 input capture position setting register (X)	VIN4_XSTART	xxh	R/W	8
140C	Video 4 input capture position setting register (Y ODD)	VIN4_YSTART_O	01h	R/W	8
1410	Video 4 input capture position setting register (Y EVEN)	VIN4_YSTART_E	01h	R/W	8
1414	Video 4 input interrupt setting register	VIN4_INTSEL	01h	R/W	8
Video output registers					
1800	Video output HSYNC front porch setting register	VOUT_HF	00h	R/W	8
1804	Video output HSYNC width setting register	VOUT_HP	01h	R/W	8
1808	Video output HSYNC back porch setting register	VOUT_HB	00h	R/W	8
180C to 181C	Reserved				
1820	Video output X-direction length setting register 1	VOUT_HT1	xxxxh	R/W	16
1824	Video output X-direction length setting register 2	VOUT_HT2	xxxxh	R/W	16
1828	Video output X-direction length setting register 3	VOUT_HT3	xxxxh	R/W	16
182C	Video output X-direction length setting register 4	VOUT_HT4	xxxxh	R/W	16
1830	Video output VSYNC front porch setting register	VOUT_VF	0Ah	R/W	8
1834	Video output VSYNC width setting register	VOUT_VP	0Ah	R/W	8
1838	Video output VSYNC back porch setting register	VOUT_VB	00h	R/W	8
183C to 184C	Reserved				
Area sensor registers					
1C00	Area sensor setting register 1	ARS_CONTROL1	00h	R/W	8
1C04	Area sensor setting register 2	ARS_CONTROL2	01h	R/W	8
1C08	Area sensor setting register 3	ARS_CONTROL3	08h	R/W	8
1C0C	Area sensor setting register 4	ARS_CONTROL4	00h	R/W	8
1C10 to 1C14	Reserved				
1C18	Area sensor X-direction size setting register	ARS_XSIZE	00h	R/W	8
1C1C	Area sensor Y-direction size setting register	ARS_YSIZE	00h	R/W	8
1C20	Area sensor control register 1	ARS_SELECT1	00h	R/W	8
1C24	Area sensor control register 2	ARS_SELECT2	00h	R/W	8
1C28	Area sensor control register 3	ARS_SELECT3	00h	R/W	8
1C2C	Area sensor control register 4	ARS_SELECT4	00h	R/W	8
1C30	Area sensor control register 5	ARS_SELECT5	00h	R/W	8
1C34	Area sensor control register 6	ARS_SELECT6	00h	R/W	8
1C38 to 1C3C	Reserved				
1C40	Area sensor interrupt control register	ARS_INTCTRL	00h	R/W	8
1C44	Area sensor interrupt status register	ARS_INTSTAT	00h	RO	8
1C48 to 1C5C	Reserved				
1C60	Area sensor interrupt detail status register 1	ARS_INT1	00h	RO	8
1C64	Area sensor interrupt detail status register 2	ARS_INT2	00h	RO	8
1C68	Area sensor interrupt detail status register 3	ARS_INT3	00h	RO	8
1C6C	Area sensor interrupt detail status register 4	ARS_INT4	00h	RO	8
1C70	Area sensor interrupt detail status register 5	ARS_INT5	00h	RO	8
1C74	Area sensor interrupt detail status register 6	ARS_INT6	00h	RO	8
1C78 to 1CBC	Reserved				
Interlace/progressive conversion registers					
3000	Interlace/progressive conversion mode setting register	IPC_MODE	80h	R/W	8
3004 to 3030	Reserved				
Interrupt controller registers					
3800	Interrupt status register	INTC_STAT	00h	RO	8
3804	Interrupt raw status register	INTC_RAWSTAT	00h	RO	8
3808	Interrupt enable setting register	INTC_ENABLE	00h	RO	8
380C	Interrupt enable clear register	INTC_EN_CLEAR	00h	WO	8
3810 to 387C	Reserved				

Address (h)	Register Name	Register Abbreviation	Default Value	R/W	Register Size (bit)
3880	Interrupt trigger setting register	INTC_LEVEL	00h	R/W	8
3884	Reserved				
3888	Trigger interrupt factor clear register	INTC_TRIG_CLEAR	00h	WO	8
GPIO registers					
3C00	GPIO data register	GPIO_DATA	00h	R/W	8
3C04	GPIO function switching register	GPIO_FUNC	0000h	R/W	16

* Registers reserved or not described are not subject to writing.

5.2 Register Description

Chip ID Register (SYS_CHIPID)

[0000h] Default value = 1000h Read Only

PRODUCT ID [7:0]							
15	14	13	12	11	10	9	8
Reserved					REVISION CODE[2:0]		
7	6	5	4	3	2	1	0

Bits[15:8]: **Product ID Code**
This IC contains 10h in hexadecimal notation.

Bits[7:3]: **Reserved**

Bits[2:0]: **Revision Code**
Indicates the revision of this IC. The first chip REV0 is set to 00h, which is incremented by one each time this IC is revised.

Input image 1 setting register (SYS_CH1INMODE)

[0010h] Default value = 10000xxxb Read/Write

EN	Reserved				MODE[2:0]		
7	6	5	4	3	2	1	0

Input image 2 setting register (SYS_CH2INMODE)

[0014h] Default value = 00000xxxb Read/Write

EN	Reserved				MODE[2:0]		
7	6	5	4	3	2	1	0

Input image 3 setting register (SYS_CH3INMODE)

[0018h] Default value = 00000xxxb Read/Write

EN	Reserved				MODE[2:0]		
7	6	5	4	3	2	1	0

Input image 4 setting register (SYS_CH4INMODE)

[001Ch] Default value = 00000xxxb Read/Write

EN	Reserved				MODE[2:0]		
7	6	5	4	3	2	1	0

Bit[7]: **Video Input Enable**

Controls video input ON/OFF.
Video 1 is only turned on after resetting.

0: Video input OFF
1: Video input ON

Bits[6:3]: **Reserved**

Bits[2:0]: **Video Input Mode select**

Sets the video input mode.
This bit has the state after resetting that varies depending on the setting of the CONF[1:0] pin.

000: NTSC(720)
001: NTSC(704)
010: PAL
011: Reserved
100: VGA
101: Reserved
110: Reserved
111: Reserved

Video 1 input setting register (SYS_CH1INCONFIG)

[0020h] Default value = 000x0001b Read/Write

Reserved	TYPE[1:0]		601 / 656	ODD_POL	HSYNC_POL	VSYNC_POL	CLK_POL
7	6	5	4	3	2	1	0

Video 2 input setting register (SYS_CH2INCONFIG)

[0024h] Default value = 000x0001b Read/Write

Reserved	TYPE[1:0]		601 / 656	ODD_POL	HSYNC_POL	VSYNC_POL	CLK_POL
7	6	5	4	3	2	1	0

Video 3 input setting register (SYS_CH3INCONFIG)

[0028h] Default value = 000x0001b Read/Write

Reserved	TYPE[1:0]		601 / 656	ODD_POL	HSYNC_POL	VSYNC_POL	CLK_POL
7	6	5	4	3	2	1	0

Video 4 input setting register (SYS_CH4INCONFIG)

[002Ch] Default value = 000x0001b Read/Write

Reserved	TYPE[1:0]		601 / 656	ODD_POL	HSYNC_POL	VSYNC_POL	CLK_POL
7	6	5	4	3	2	1	0

Bit[7]: **Reserved**

Bits[6:5]: **Video Input Data Type**

Sets the alignment sequence of YUV data that is input by byte.

00: (1st)Cb-Y0-Cr-Y1(last) (Set to this state after resetting.)
01: (1st)Cr-Y0-Cb-Y1(last)
10: (1st)Y0-Cb-Y1-Cr(last)
11: (1st)Y0-Cr-Y1-Cb(last)

Bit[4]: **Video Input Data Format Select**

Sets the video input format.
This bit has the state after resetting that varies depending on the setting of the CONF[2] pin.

0: BT601 mode
1: BT656 mode

Bit[3]: **ODD Input Polarity**

Sets the ODDIN polarity.

0: Negative logic (Set to this state after resetting.)
1: Positive logic

Bit[2]: **Hsync Input Polarity**

Sets the HIN polarity.

0: Negative logic (Set to this state after resetting.)
1: Positive logic

Bit[1]: **Vsync Input Polarity**

Sets the VIN polarity.

0: Negative logic (Set to this state after resetting.)
1: Positive logic

Bit[0]: **Dot Clock Input Polarity**

Sets the valid edge for input clock.

0: Data is read when the clock changes from High to Low.
1: Data is read when the clock changes from Low to High. (Set to this state after resetting.)

Output image setting register (SYS_OUTMODE)

[0030h] Default value = 80h Read/Write

EN	Reserved					MODE[1:0]	
7	6	5	4	3	2	1	0

Bit[7]: **Video Output Enable**

Controls video output ON/OFF.

0: Video output OFF

1: Video output ON (Set to this state after resetting.)

Bit[6]: **Reserved (Write Only)**

Be sure to set “1”.

Bits[5:2]: **Reserved**

Bits[1:0]: **Video Output Mode**

Sets the video output mode.

00: Fixed mode (Set to this state after resetting.)

01: Auto scan mode

10: Compress mode

11: Merge mode

Video output setting register (SYS_OUTCONFIG)							
[0034h] Default value = 00000011_000x0000b							Read/Write
CH4SEL	CH3SEL	CH2SEL	CH1SEL	Reserved		HSYNC_SEL	VSYNC_SEL
15	14	13	12	11	10	9	8
Reserved	TYPE[1:0]		601 / 656	Reserved	HSYNC_POL	VSYNC_POL	Reserved
7	6	5	4	3	2	1	0

Bit[15]: **Video 4 Input / Output Select**

Sets the I/O direction of the video 4 pin.

0: Video input (Set to this state after resetting.)
1: Video output

Bit[14]: **Video 3 Input / Output Select**

Sets the I/O direction of the video 3 pin.

0: Video input (Set to this state after resetting.)
1: Video output

Bit[13]: **Video 2 Input / Output Select**

Sets the I/O direction of the video 2 pin.

0: Video input (Set to this state after resetting.)
1: Video output

Bit[12]: **Video 1 Input / Output Select**

Sets the I/O direction of the video 1 pin.

0: Video input (Set to this state after resetting.)
1: Video output

Bits[11:10]: **Reserved**

Be sure to set “00”.

Bit[9]: **Hsync Output Select**

Sets the signal output from the HOUT pin.

0: HSYNC signal
1: HVALID signal (Set to this state after resetting.)

Bit[8]: **Vsync Output Select**

Sets the signal output from the VOUT pin.

0: VSYNC signal
1: VVALID signal (Set to this state after resetting.)

Bit[7]: **Reserved**

Bits[6:5]: **Video Output Data Type**

Sets the alignment sequence of YUV data that is input by byte.

00: (1st)Cb-Y0-Cr-Y1(last) (Set to this state after resetting.)
01: (1st)Cr-Y0-Cb-Y1(last)
10: (1st)Y0-Cb-Y1-Cr(last)
11: (1st)Y0-Cr-Y1-Cb(last)

Bit[4]: **Video Output Data Format Select**

Sets the video output format.
This bit has the state after resetting that varies depending on the setting of the CONF[2] pin.

0: BT601 mode
1: BT656 mode

Bit[3]: **Reserved**

Bit[2]: **Hsync Output Polarity**

Sets the polarity of the signal output from the HOUT pin.

0: Negative logic (Set to this state after resetting.)

1: Positive logic

Bit[1]: **Vsync Output Polarity**

Sets the polarity of the signal output from the VOUT pin.

0: Negative logic (Set to this state after resetting.)

1: Positive logic

Bit[0]: **Reserved**

Output image selection register (SYS_OUTCH)

[0038h] Default value = 00h Read/Write

Reserved						OUTCH[1:0]	
7	6	5	4	3	2	1	0

Bits[7:2]: **Reserved**

Bits[1:0]: **Output Channel for Fix Mode**

Sets the video input to be output in the fixed mode.

00: Video 1 (Set to this state after resetting.)

01: Video 2

10: Video 3

11: Video 4

Video 1 output cycle setting register (SYS_CH1OUTCYCLE)

[0040h] Default value = 30h Read/Write

CYCLE[7:0]							
7	6	5	4	3	2	1	0

Video 2 output cycle setting register (SYS_CH2OUTCYCLE)

[0044h] Default value = 30h Read/Write

CYCLE[7:0]							
7	6	5	4	3	2	1	0

Video 3 output cycle setting register (SYS_CH3OUTCYCLE)

[0048h] Default value = 30h Read/Write

CYCLE[7:0]							
7	6	5	4	3	2	1	0

Video 4 output cycle setting register (SYS_CH4OUTCYCLE)

[004Ch] Default value = 30h Read/Write

CYCLE[7:0]							
7	6	5	4	3	2	1	0

Bits[7:0]: **Video 1(2, 3, 4) Output Cycle for Auto Scan Mode**

Sets the cycle count for each video input in the auto scan mode.

Ex.) 0 = To the next video input without outputting any screen

1 = To the next video input after outputting one screen

2 = To the next video input after outputting two screens

Video 1 input pull-down control register (SYS_CH1PCCTRL)

[0050h] Default value = 0000h Read/Write

Reserved				CH1PCCTRL[11:0]			
15	14	13	12	11	10	9	8
CH1PCCTRL[11:0]							
7	6	5	4	3	2	1	0

Video 2 input pull-down control register (SYS_CH2PCCTRL)

[0054h] Default value = 0000h Read/Write

Reserved				CH2PCCTRL[11:0]			
15	14	13	12	11	10	9	8
CH2PCCTRL[11:0]							
7	6	5	4	3	2	1	0

Video 3 input pull-down control register (SYS_CH3PCCTRL)

[0058h] Default value = 0000h Read/Write

Reserved				CH3PCCTRL[11:0]			
15	14	13	12	11	10	9	8
CH3PCCTRL[11:0]							
7	6	5	4	3	2	1	0

Video 4 input pull-down control register (SYS_CH4PCCTRL)

[005Ch] Default value = 0000h Read/Write

Reserved				CH4PCCTRL[11:0]			
15	14	13	12	11	10	9	8
CH4PCCTRL[11:0]							
7	6	5	4	3	2	1	0

Bits[15:12]: **Reserved**

Bits[11:0]: **Video 1(2, 3, 4) Pull-Down Control**

Controls the connection or disconnection of the pull-down resistor built in the video input pin. The bits correspond to the following pins respectively.

[11] CH1CLK, CH2CLK, CH3CLK, CH4CLK
[10] CH1ODDIN, CH2ODDIN, CH3ODDIN, CH4ODDIN
[9] CH1HIN, CH2HIN, CH3HIN, CH4HIN
[8] CH1VIN, CH2VIN, CH3VIN, CH4VIN
[7:0] CH1DIN[7:0], CH2DIN[7:0], CH3DIN[7:0], CH4DIN[7:0],

0: Pull-down resistor enable (Set to this state after resetting.)
1: Pull-down resistor disable

GPIO pin pull-up control register (SYS_GPIOPCCTRL)

[0060h] Default value = 00h Read/Write

GPIOPCCTRL[7:0]							
7	6	5	4	3	2	1	0

Bits[11:0]: **GPIO Pull-Up Control**

Controls the connection or disconnection of the pull-up resistor built in the GPIO pin. The bits correspond to the GPIO[7:0] pins respectively.

0: Pull-up resistor enable (Set to this state after resetting.)

1: Pull-up resistor disable

CONF pin pull-down control register (SYS_CONFPCCTRL)

[0064h] Default value = 00h Read/Write

Reserved				CONFPCCTRL[3:0]			
7	6	5	4	3	2	1	0

Bits[8:4]: **Reserved**

Bits[3:0]: **CONF Pull-Down Control**

Controls the connection or disconnection of the pull-down resistor built in the CONF[3:0] pin. The bits correspond to the CONF[3:0] pins respectively.

0: Pull-down resistor enable (Set to this state after resetting.)

1: Pull-down resistor disable

I²C setting register (I2C_CONTROL)

[0400h] Default value = 00h Read/Write

Reserved		THR_TYPE	THR_HI	I2C_ HI	Reserved	STEP[1:0]	
7	6	5	4	3	2	1	0

Bits[7:6]: **Reserved**

Be sure to set “00”.

Bit[5]: **Transform Format Type for Through bus**

Sets the transfer format that supports the device connected to Through Bus.

0: Compound format (Set to this state after resetting.)

1: Normal format

Bit[4]: **HIGH drive enable to Through bus**

Sets whether or not to enable H drive for the SDA signal of Through Bus with a High signal.

0: Hz signal (Set to this state after resetting.)

1: High signal

Bit[3]: **HIGH drive enable to I²C bus**

Sets whether or not to enable H drive for the SDA signal of I²C bus with a High signal.

0: Hz signal (Set to this state after resetting.)

1: High signal

Bit[2]: **Reserved**

Be sure to set “0”.

Bits[1:0]: **Access Step**

Sets the number of steps in the continuous access mode.

00: 32 steps (Set to this state after resetting.)

01: 16 steps

10: 8 steps

11: Reserved

I²C slave address setting register (I2C_SLAVE_ADRS)

[0404 h] Default value = 36h or 37h Read/Write

Reserved	SLAVE_ADRS[6:0]						
7	6	5	4	3	2	1	0

Bit[7]: **Reserved**

Bits[6:0]: **Slave Device ID**

Sets the I²C slave address of this I²C. The default value of Bits[6:1] is 011011b. Capturing the CONF[3] pin just after resetting initializes bit 0 in this register, resulting in 36h or 37h being used as an I²C slave address of this IC.

Software reset register (I2C_SOFTRST)

[0408h] Default value = —— Write Only

SOFTRST [7:0]							
7	6	5	4	3	2	1	0

Bits[7:0]: **Software Reset**

Generates software reset. Writing 5Ah will result in software reset being generated.

I²C bus through function control register (I2C_THR_ENABLE)

[040Ch] Default value = 00h Read/Write

Reserved							THR_EN
7	6	5	4	3	2	1	0

Bits[7:1]: **Reserved**

Bit[0]: **Through Bus Enable**

Controls whether or not to permit Through Bus Access. When this bit is 0, Through Bus is in the Hz output state.

0: Disable (Set to this state after resetting.)

1: Enable

I²C bus through address setting register (I2C_THR_ADRS)

[0410h] Default value = 00h Read/Write

Reserved	THR_ADRS						
7	6	5	4	3	2	1	0

Bit[7]: **Reserved**

Bits[6:0]: **Through Bus Address**

A register used to store the ID for Through Bus Access. This register must be set before enabling the THR_EN bit in the I²C bus through function control register (I2C_THR_ENABLE [040Ch]).

I²C bus through ID setting register (I2C_THR_DEVID)

[0414h] Default value = 00h Read/Write

Reserved	THR_DEVID[6:0]						
7	6	5	4	3	2	1	0

Bit[7]: **Reserved**

Bits[6:0]: **Through Bus Device ID**

A register used to store the ID of the device to be connected to Through Bus. This register must be set before enabling the THR_EN bit in the I²C bus through function control register (I2C_THR_ENABLE [040Ch]).

I^2C bus through hold counter setting register (I2C_THR_HOLD)

[041Ch] Default value = 00h Read/Write

7	6	5	4	3	2	1	0
Reserved	THR_HOLD[6:0]						

Bit[7]: **Reserved**

Bits[6:0]: **Through Bus Hold Count**

A register used to store the hold time adjustment value of Through Bus. This register assures the following hold time.

Hold time = Clock Cycle time × Value of this register

Ex.) When f=25MHz(Clock Cycle = 40ns), the following hold time will be assured.
Set value 0Dh・・・Hold time: Approx. 500 ns
Set value 19h・・・Hold time: Approx. 1 μs
Set value 32h・・・Hold time: Approx. 2 μs

Supplemental remarks)
When using Through Bus, check the hold time of the device to be connected before setting this register. when not using Through Bus, specify the default value.

Video 1 input capture position setting register (VIN1_XSTART)

[0808h] Default value = 01h(CONF[1:0] = 00/10/11), 09h(CONF[1:0] = 01) Read/Write

7	6	5	4	3	2	1	0
XSTART[7:0]							

Bits[7:0]: **Horizontal Start**

Sets the X-direction capture position of video 1 input. In the BT601 mode, specify the number of pixels after the HIN pin has been set to High (at setting of the negative logic). In the BT656 mode, specify the number of pixels after SAV has been completed. Be sure to specify “1” or more.

Ex.) 1 = Captures pixels from the first.
2 = Captures pixels from the second.

Video 1 input capture position setting register (VIN1_YSTART_O)

[080Ch] Default value = 01h Read/Write

7	6	5	4	3	2	1	0
YSTART_O[7:0]							

Bits[7:0]: **Odd Line Vertical Start**

Sets the Y-direction capture position in the interlace (or progressive) odd field of video 1 input. In the BT601 mode, specify the number of HSYNCs after the VIN pin has been set to High (at setting of the negative logic). In the BT656 mode, specify the number of SAVs after the V bit has been set to 0. Be sure to specify “1” or more.

Ex.) 1 = Captures data from the first line.
2 = Captures data from the second line.

Video 1 input capture position setting register (VIN1_YSTART_E)							
[0810h] Default value = 01h							Read/Write
YSTART_E[7:0]							
7	6	5	4	3	2	1	0

Bits[7:0]: **Even Line Vertical Start**

Sets the Y-direction capture position in the interlace even field of video 1 input. In the BT601 mode, specify the number of HSYNCs after the VIN pin has been set to High (at setting of the negative logic). In the BT656 mode, specify the number of SAVs after the V bit has been set to 0. Be sure to specify "1" or more.

Ex.) 1 = Captures data from the first line.
2 = Captures data from the second line.

Video 1 input interrupt setting register (VIN1_INTSEL)							
[0814h] Default value = 00h							Read/Write
Reserved						HSYNC	VSYNC
7	6	5	4	3	2	1	0

Bits[8:2]: **Reserved**

Be sure to set "0".

Bit[1]: **Hsync Interrupt Enable**

Controls the Hsync interrupt of video 1 input. In the BT601 mode, an interrupt is generated at a timing when the HIN pin has changed from Low to High (at setting of the negative logic). In the BT656 mode, an interrupt is generated at a timing when the H bit has changed from "1" to "0".

0: Disable (Set to this state after resetting.)
1: Enable

Bit[0]: **Vsync Interrupt Enable**

Controls the Vsync interrupt of video 1 input. In the BT601 mode, an interrupt is generated at a timing when the VIN pin has changed from Low to High (at setting of the negative logic). In the BT656 mode, an interrupt is generated at a timing when the V bit has changed from "1" to "0".

0: Disable (Set to this state after resetting.)
1: Enable

Video 2 input capture position setting register (VIN2_XSTART)							
[0C08h] Default value = 01h(CONF[1:0] = 00/10/11), 09h(CONF[1:0] = 01)							Read/Write
XSTART[7:0]							
7	6	5	4	3	2	1	0

Bits[7:0]: **Horizontal Start**

Sets the X-direction capture position of video 2 input. In the BT601 mode, specify the number of pixels after the HIN pin has been set to High (at setting of the negative logic). In the BT656 mode, specify the number of pixels after SAV has been completed. Be sure to specify "1" or more.

Ex.) 1 = Captures pixels from the first.
2 = Captures pixels from the second.

Video 2 input capture position setting register (VIN2_YSTART_O)							
[0C0Ch] Default value = 01h							Read/Write
YSTART_O[7:0]							
7	6	5	4	3	2	1	0

Bits[7:0]: **Odd Line Vertical Start**

Sets the Y-direction capture position in the interlace (or progressive) odd field of video 2 input. In the BT601 mode, specify the number of HSYNCs after the VIN pin has been set to High (at setting of the negative logic). In the BT656 mode, specify the number of SAVs after the V bit has been set to 0. Be sure to specify "1" or more.

Ex.) 1 = Captures data from the first line.
2 = Captures data from the second line.

Video 2 input capture position setting register (VIN2_YSTART_E)							
[0C10h] Default value = 01h							Read/Write
YSTART_E[7:0]							
7	6	5	4	3	2	1	0

Bits[7:0]: **Even Line Vertical Start**

Sets the Y-direction capture position in the interlace even field of video 2 input. In the BT601 mode, specify the number of HSYNCs after the VIN pin has been set to High (at setting of the negative logic). In the BT656 mode, specify the number of SAVs after the V bit has been set to "0". Be sure to specify "1" or more.

Ex.) 1 = Captures data from the first line.
2 = Captures data from the second line.

Video 2 input interrupt setting register (VIN2_INTSEL)							
[0C14h] Default value = 00h							Read/Write
Reserved						HSYNC	VSYNC
7	6	5	4	3	2	1	0

Bits[8:2]: **Reserved**

Be sure to set "0".

Bit[1]: **Hsync Interrupt Enable**

Controls the Hsync interrupt of video 2 input. In the BT601 mode, an interrupt is generated at a timing when the HIN pin has changed from Low to High (at setting of the negative logic). In the BT656 mode, an interrupt is generated at a timing when the H bit has changed from "1" to "0".

0: Disable (Set to this state after resetting.)
1: Enable

Bit[0]: **Vsync Interrupt Enable**

Controls the Vsync interrupt of video 2 input. In the BT601 mode, an interrupt is generated at a timing when the VIN pin has changed from Low to High (at setting of the negative logic). In the BT656 mode, an interrupt is generated at a timing when the V bit has changed from "1" to "0".

0: Disable (Set to this state after resetting.)
1: Enable

Video 3 input capture position setting register (VIN3_XSTART)							
[1008h] Default value = 01h(CONF[1:0] = 00/10/11), 09h(CONF[1:0] = 01)							Read/Write
XSTART[7:0]							
7	6	5	4	3	2	1	0

Bits[7:0]: **Horizontal Start**

Sets the X-direction capture position of video 3 input. In the BT601 mode, specify the number of pixels after the HIN pin has been set to High (at setting of the negative logic). In the BT656 mode, specify the number of pixels after SAV has been completed. Be sure to specify "1" or more.

Ex.) 1 = Captures pixels from the first.
2 = Captures pixels from the second.

Video 3 input capture position setting register (VIN3_YSTART_O)							
[100Ch] Default value = 01h							Read/Write
YSTART_O[7:0]							
7	6	5	4	3	2	1	0

Bits[7:0]: **Odd Line Vertical Start**

Sets the Y-direction capture position in the interlace (or progressive) odd field of video 3 input. In the BT601 mode, specify the number of HSYNCs after the VIN pin has been set to High (at setting of the negative logic). In the BT656 mode, specify the number of SAVs after the V bit has been set to 0. Be sure to specify "1" or more.

Ex.) 1 = Captures data from the first line.
2 = Captures data from the second line.

Video 3 input capture position setting register (VIN3_YSTART_E)							
[1010h] Default value = 01h							Read/Write
YSTART_E[7:0]							
7	6	5	4	3	2	1	0

Bits[7:0]: **Even Line Vertical Start**

Sets the Y-direction capture position in the interlace even field of video 3 input. In the BT601 mode, specify the number of HSYNCs after the VIN pin has been set to High (at setting of the negative logic). In the BT656 mode, specify the number of SAVs after the V bit has been set to 0. Be sure to specify "1" or more.

Ex.) 1 = Captures data from the first line.
2 = Captures data from the second line.

Video 3 input interrupt setting register (VIN3_INTSEL)

[1014h] Default value = 00h — Read/Write

Reserved						HSYNC	VSYNC
7	6	5	4	3	2	1	0

Bits[8:2]: **Reserved**

Be sure to set "0".

Bit[1]: **Hsync Interrupt Enable**

Controls the Hsync interrupt of video 3 input. In the BT601 mode, an interrupt is generated at a timing when the HIN pin has changed from Low to High (at setting of the negative logic). In the BT656 mode, an interrupt is generated at a timing when the H bit has changed from "1" to "0".

0: Disable (Set to this state after resetting.)
1: Enable

Bit[0]: **Vsync Interrupt Enable**

Controls the Vsync interrupt of video 3 input. In the BT601 mode, an interrupt is generated at a timing when the VIN pin has changed from Low to High (at setting of the negative logic). In the BT656 mode, an interrupt is generated at a timing when the V bit has changed from "1" to "0".

0: Disable (Set to this state after resetting.)
1: Enable

Video 4 input capture position setting register (VIN4_XSTART)

[1408h] Default value = 01h(CONF[1:0] = 00/10/11), 09h(CONF[1:0] = 01) — Read/Write

XSTART[7:0]							
7	6	5	4	3	2	1	0

Bits[7:0]: **Horizontal Start**

Sets the X-direction capture position of video 4 input. In the BT601 mode, specify the number of pixels after the HIN pin has been set to High (at setting of the negative logic). In the BT656 mode, specify the number of pixels after SAV has been completed. Be sure to specify "1" or more.

Ex.) 1 = Captures pixels from the first.
2 = Captures pixels from the second.

Video 4 input capture position setting register (VIN4_YSTART_O)

[140Ch] Default value = 01h — Read/Write

YSTART_O[7:0]							
7	6	5	4	3	2	1	0

Bits[7:0]: **Odd Line Vertical Start**

Sets the Y-direction capture position in the interlace (or progressive) odd field of video 4 input. In the BT601 mode, specify the number of HSYNCs after the VIN pin has been set to High (at setting of the negative logic). In the BT656 mode, specify the number of SAVs after the V bit has been set to 0. Be sure to specify "1" or more.

Ex.) 1 = Captures data from the first line.
2 = Captures data from the second line.

Video 4 input capture position setting register (VIN4_YSTART_E)

[1410h] Default value = 01h — Read/Write

YSTART_E[7:0]							
7	6	5	4	3	2	1	0

Bits[7:0]: **Even Line Vertical Start**

Sets the Y-direction capture position in the interlace even field of video 4 input. In the BT601 mode, specify the number of HSYNCs after the VIN pin has been set to High (at setting of the negative logic). In the BT656 mode, specify the number of SAVs after the V bit has been set to "0". Be sure to specify "1" or more.

Ex.) 1 = Captures data from the first line.
2 = Captures data from the second line.

Video 4 input interrupt setting register (VIN4_INTSEL)

[1414h] Default value = 00h — Read/Write

Reserved						HSYNC	VSYNC
7	6	5	4	3	2	1	0

Bits[8:2]: **Reserved**

Be sure to set "0".

Bit[1]: **Hsync Interrupt Enable**

Controls the Hsync interrupt of video 4 input. In the BT601 mode, an interrupt is generated at a timing when the HIN pin has changed from Low to High (at setting of the negative logic). In the BT656 mode, an interrupt is generated at a timing when the H bit has changed from "1" to "0".

0: Disable (Set to this state after resetting.)
1: Enable

Bit[0]: **Vsync Interrupt Enable**

Controls the Vsync interrupt of video 4 input. In the BT601 mode, an interrupt is generated at a timing when the VIN pin has changed from Low to High (at setting of the negative logic). In the BT656 mode, an interrupt is generated at a timing when the V bit has changed from "1" to "0".

0: Disable (Set to this state after resetting.)
1: Enable

Video output HSYNC front porch setting register (VOUT_HF)

[1800h] Default value = 00h — Read/Write

HF[7:0]							
7	6	5	4	3	2	1	0

Bits[7:0]: **Hsync Front Porch**

Sets the Hsync front porch of video output on a pixel basis.

Video output HSYNC width setting register (VOUT_HP)

[1804h] Default value = 01h Read/Write

HP[7:0]							
7	6	5	4	3	2	1	0

Bits[7:0]: **Hsync Width**

Sets the Hsync value of video output on a pixel basis. Be sure to specify “1” or more.

Video output HSYNC back porch setting register (VOUT_HB)

[1808h] Default value = 00h Read/Write

HB[7:0]							
7	6	5	4	3	2	1	0

Bits[7:0]: **Hsync Back Porch**

Sets the Hsync back porch of video output on a pixel basis.

Video 1 output X-direction length setting register (VOUT_HT1)

[1820h] Default value = 031Ah(CONF[1:0] = 00/01), 0320h(CONF[1:0] = 10/11) Read/Write

Reserved					HT1[10:0]		
15	14	13	12	11	10	9	8
HT1[10:0]							
7	6	5	4	3	2	1	0

Video 2 output X-direction length setting register (VOUT_HT2)

[1824h] Default value = 031Ah(CONF[1:0] = 00/01), 0320h(CONF[1:0] = 10/11) Read/Write

Reserved					HT2[10:0]		
15	14	13	12	11	10	9	8
HT2[10:0]							
7	6	5	4	3	2	1	0

Video 3 output X-direction length setting register (VOUT_HT3)

[1828h] Default value = 031Ah(CONF[1:0] = 00/01), 0320h(CONF[1:0] = 10/11) Read/Write

Reserved					HT3[10:0]		
15	14	13	12	11	10	9	8
HT3[10:0]							
7	6	5	4	3	2	1	0

Video 4 output X-direction length setting register (VOUT_HT4)

[182Ch] Default value = 031Ah(CONF[1:0] = 00/01), 0320h(CONF[1:0] = 10/11) Read/Write

Reserved					HT4[10:0]		
15	14	13	12	11	10	9	8
HT4[10:0]							
7	6	5	4	3	2	1	0

Bits[15:11]: **Reserved**

Bits[10:0]: **Horizontal Total Pixel**

Sets the X-direction length for each video output on a pixel basis. Specify the value for each video output mode, referring to the following.

● When video output is in the fixed, auto scan, or merge mode:

Specify the time when 1-line data is input from a video input.

Ex.) When the CLKIN clock frequency is 25MHz in BT601 NTSC input:
858[Pixel] / 27[MHz] × 25[MHz] = 794[Pixel]

● When the video output mode is the compress mode:

Specify the time when 1/2-line data is input from a video input.

Ex.) When the CLKIN clock frequency is set in BT601 PAL input:
864[Pixel]/ 27[MHz]/ 2 × 25[MHz] = 400[Pixel]

Video output VSYNC front porch setting register (VOUT_VF)

[1830h] Default value = 0Ah Read/Write

VF[7:0]							
7	6	5	4	3	2	1	0

Bits[7:0]: **Vsync Front Porch**

Sets the Vsync front porch of video output on a line basis. Be sure to specify “1” or more.

Video output VSYNC width setting register (VOUT_VP)

[1834h] Default value = 0Ah Read/Write

VP[7:0]							
7	6	5	4	3	2	1	0

Bits[7:0]: **Vsync Width**

Sets the Vsync width of video output on a line basis. Be sure to specify “1” or more.

Video output VSYNC back porch setting register (VOUT_VB)

[1838h] Default value = 00 Read/Write

VB[7:0]							
7	6	5	4	3	2	1	0

Bits[7:0]: **Vsync Back Porch**

Sets the Vsync back porch of video output on a line basis.

Area sensor setting register 1 (ARS_CONTROL1)

[1C00h] Default value = 00h Read/Write

7	6	5	4	3	2	1	0
SWRST	Reserved				ARSDS[1:0]		ARSEN

Bit[7]: **ARS Software Reset (Write Only)**

Resets the software of the area sensor.

0: Unchanged (Set to this state after resetting.)

1: Resets the area sensor module.

Bits[6:3]: **Reserved**

Bits[2:1]: **Data select**

Sets which YUV component of an image is used for integration.

00: Integrates Y0. (Set to this state after resetting.)

01: Integrates Y1.

10: Integrates U.

11: Integrates V.

Bit[0]: **ARS Enable**

Controls the area sensor. Writing "1" to this bit will start the integration from the next frame.

00: Area sensor disable (Set to this state after resetting.)

01: Area sensor enable

Area sensor setting register 2 (ARS_CONTROL2)

[1C04h] Default value = 01h Read/Write

7	6	5	4	3	2	1	0
Reserved			ARSMCC[4:0]				

Bits[7:5]: **Reserved**

Be sure to set "0".

Bits[4:0]: **ARS Multiplying Compare Cycle**

Specifies the integration cycle. The specified integration cycle is used to integrate YUV components of an image sent from the video input, save the results in the integration register, and compare the integrated value of YUV components of a new image with the previous one in the integration register.

00000: Not integrated.

00001: Integrated on a 1-frame basis. (Set to this state after resetting.)

00010: Integrated on a 2-frame basis.

:

111111: Integrated on a 31-frame basis.

Area sensor setting register 3 (ARS_CONTROL3)

[1C08h] Default value = 08h Read/Write

ARSFRN	ARSCRT[2:0]			ARSODM	Reserved	ARSCSL[1:0]	
7	6	5	4	3	2	1	0

Bit[7]: **ARS Free Run mode**

Specifies the operation mode.

0: Stops the comparison if detected. (Set to this state after resetting.)

1: Continues comparison.

Bits[6:4]: **ARS Change Rate**

Specifies the amount of change to be detected.

000: 1.5% (Set to this state after resetting.)

001: 3%

010: 6%

011: 13%

100: 25%

101: 50%

110: Reserved

111: Control Register 4, set value or more

Bit[3]: **ARS Sampling Field Mode**

Specifies a field to be integrated.

0: Odd field

1: Even field (Set to this state after resetting.)

Bit[2]: **Reserved**

Bits[1:0]: **ARS In-Timing Module (Camera) Select**

Specifies which input is used to integrate image data.

00: Video 1 (Set to this state after resetting.)

01: Video 2

10: Video 3

11: Video 4

Area sensor setting register 4 (ARS_CONTROL4)

[1C0Ch] Default value = 00h Read/Write

ARSCUR[7:0]							
7	6	5	4	3	2	1	0

Bits[7:0]: **ARS Change Upper Rate**

Specifies the amount of change to be detected.

Area sensor X-direction size setting register (ARS_XSIZE)							
[1C18h] Default value = 00h							Read/Write
ARSXSR[7:0]							
7	6	5	4	3	2	1	0

Bits[7:0]: **ARS Divided Area X Size**

Specifies the X-direction size of the detected area.

Ex.) NTSC 720/8 = 90(Dec.) = 5A(Hex.)
PAL 720/8 = 90(Dec.) = 5A(Hex.)
VGA 640/8 = 80(Dec.) = 50(Hex.)

Area sensor Y-direction size setting register (ARS_YSIZE)							
[1C1Ch] Default value = 00h							Read/Write
ARSYSR[7:0]							
7	6	5	4	3	2	1	0

Bits[7:0]: **ARS Divided Area Y Size**

Specifies the Y-direction size of the detected area.

Ex.) NTSC 480/6 = 80(Dec.) = 50(Hex.)
PAL 576/6 = 96(Dec.) = 60(Hex.)
VGA 480/6 = 80(Dec.) = 50(Hex.)

Area sensor control registers 1 to 6 (ARS_SELECT1-6)							
[1C20h] to [1C34h]] Default value = 00h							Read/Write
ARSA07	ARSA06	ARSA05	ARSA04	ARSA03	ARSA02	ARSA01	ARSA00
7	6	5	4	3	2	1	0

Select an area to be detected in each split area. Multiple areas are selectable.

Bit[7]: **ARS Compare Area07 select (same 17,27,37,47,57)**
- 0: Detects no area. (Set to this state after resetting.)
- 1: Detects Area07.

Bit[6]: **ARS Compare Area06 select (same 16,26,36,46,56)**
- 0: Detects no area. (Set to this state after resetting.)
- 1: Detects Area06.

Bit[5]: **ARS Compare Area05 select (same 15,25,35,45,55)**
- 0: Detects no area. (Set to this state after resetting.)
- 1: Detects Area05.

Bit[4]: **ARS Compare Area04 select (same 14,24,34,44,54)**
- 0: Detects no area. (Set to this state after resetting.)
- 1: Detects Area04.

Bit[3]: **ARS Compare Area03 select (same 13,23,33,43,53)**
- 0: Detects no area. (Set to this state after resetting.)
- 1: Detects Area03.

Bit[2]: **ARS Compare Area02 select (same 12,22,32,42,52)**
- 0: Detects no area. (Set to this state after resetting.)
- 1: Detects Area02.

Bit[1]: **ARS Compare Area01 select (same 11,21,31,41,51)**
- 0: Detects no area. (Set to this state after resetting.)
- 1: Detects Area01.

Bit[0]: **ARS Compare Area00 select (same 10,20,30,40,50)**
- 0: Detects no area. (Set to this state after resetting.)
- 1: Detects Area00.

Area sensor interrupt control register (ARS_INTCTRL)							
[1C40h] Default value = 00h							Read/Write
ARSINE	Reserved						ARSDTC
7	6	5	4	3	2	1	0

Bit[7]: **ARS Interrupt Enable**
Controls a detection interrupt.
0: Disable (Set to this state after resetting.)
1: Enable

Bits[6:1]: **Reserved**

Bit[0]: **ARS Detect signal Clear(Write Onlly)**
Writing "1" clears the interrupt signal.

Area sensor interrupt status register (ARS_INTSTAT)							
[1C44h] Default value = 00h							Read Only
ARSINT	Reserved	ARSIH5	ARSIH4	ARSIH3	ARSIH2	ARSIH1	ARSIH0
7	6	5	4	3	2	1	0

Bit[7]: **ARS Interrupt**
Indicates whether an interrupt was detected in one of all the detected areas.
0: Not detected.
1: Detected.

Bit[6]: **Reserved**

Bit[5]: **ARS Interrupt Horizontal direction 5**
0: Not detected in Area05, 15, 25, 35, 45, or 55.
1: Detected in Area05, 15, 25, 35, 45, or 55.

Bit[4]: **ARS Interrupt Horizontal direction 4**
0: Not detected in Area04, 14, 24, 34, 44, or 54.
1: Detected in Area04, 14, 24, 34, 44, or 54.

Bit[3]: **ARS Interrupt Horizontal direction 3**
0: Not detected in Area03, 13, 23, 33, 43, or 53.
1: Detected in Area03, 13, 23, 33, 43, or 53.

Bit[2]: **ARS Interrupt Horizontal direction 2**
0: Not detected in Area02, 12, 22, 32, 42, or 52.
1: Detected in Area02, 12, 22, 32, 42, or 52.

Bit[1]: **ARS Interrupt Horizontal direction 1**
0: Not detected in Area01, 11, 21, 31, 41, or 51.
1: Detected in Area01, 11, 21, 31, 41, or 51.

Bit[0]: **ARS Interrupt Horizontal direction 0**
0: Not detected in Area00, 10, 20, 30, 40, or 50.
1: Detected in Area00, 10, 20, 30, 40, or 50.

Area sensor interrupt detail status registers 1 to 6 (ARS_INT1-6)							
[1C60h] to [1C74h] Default value = 00h							Read Only
ARSD07	ARSD06	ARSD05	ARSD04	ARSD03	ARSD02	ARSD01	ARSD00
7	6	5	4	3	2	1	0

Bit[7]: **ARS Area07 Interrupt occurred (same 17,27,37,47,57)**
- 0: Not detected in Area07.
- 1: Detected in Area07.

Bits[6]: **ARS Area06 Interrupt occurred (same 16,26,36,46,56)**
- 0: Not detected in Area06.
- 1: Detected in Area06.

Bit[5]: **ARS Area05 Interrupt occurred (same 15,25,35,45,55)**
- 0: Not detected in Area05.
- 1: Detected in Area05.

Bit[4]: **ARS Area04 Interrupt occurred (same 14,24,34,44,54)**
- 0: Not detected in Area04.
- 1: Detected in Area04.

Bit[3]: **ARS Area03 Interrupt occurred (same 13,23,33,43,53)**
- 0: Not detected in Area03.
- 1: Detected in Area03.

Bit[2]: **ARS Area02 Interrupt occurred (same 12,22,32,42,52)**
- 0: Not detected in Area02.
- 1: Detected in Area02.

Bit[1]: **ARS Area01 Interrupt occurred (same 11,21,31,41,51)**
- 0: Not detected in Area01.
- 1: Detected in Area01.

Bit[0]: **ARS Area00 Interrupt occurred (same 10,20,30,40,50)**
- 0: Not detected in Area00.
- 1: Detected in Area00.

Interlace/progressive conversion mode setting register (IPC_MODE)

[3000h] Default value = 80h Read/Write

EN	Reserved					MODE[1:0]	
7	6	5	4	3	2	1	0

Bit[7]: **IPC Enable**

Controls the interlace/progressive conversion ON/OFF mode. In this IC, be sure to set "1".

0: OFF

1: ON (Set to this state after resetting.)

Bits[6:2]: **Reserved**

Bits[1:0]: **Mode**

Controls the interlace/progressive conversion mode.

00: Weave Mode (Set to this state after resetting.)

01: Bob Mode

10: Interpolation Mode

11: Reserved

Interrupt status register (INTC_STAT)

[3800h] Default value = 00h Read Only

Reserved			ARSSTAT	VIN4STAT	VIN3STAT	VIN2STAT	VIN1STAT
7	6	5	4	3	2	1	0

Bits[7:5]: **Reserved**

Bit[4]: **ARS Interrupt Status**

Indicates whether an interrupt request is issued from the area sensor after masking. Details are shown in the area sensor interrupt status register (ARS_INTSTAT [1C44h]) and area sensor interrupt detail status registers (ARS_ INT1-6 [1C60h] to [1C74h]).

0: No interrupt request issued.
1: Interrupt request issued.

Bit[3]: **Video4 Interrupt Status**

Indicates whether an interrupt request is issued from the video 4 input after masking.

0: No interrupt request issued.
1: Interrupt request issued.

Bit[2]: **Video3 Interrupt Status**

Indicates whether an interrupt request is issued from the video 3 input after masking.

0: No interrupt request issued.
1: Interrupt request issued.

Bit[1]: **Video2 Interrupt Status**

Indicates whether an interrupt request is issued from the video 2 input after masking.

0: No interrupt request issued.
1: Interrupt request issued.

Bit[0]: **Video1 Interrupt Status**

Indicates whether an interrupt request is issued from the video 1 input after masking.

0: No interrupt request issued.
1: Interrupt request issued.

These status bits indicate whether an interrupt request is issued from an interrupt enabled unit, in the interrupt enable setting register (INTC_ENABLE [3808h]). This bit is not set to “1” even if an interrupt request is issued from an interrupt disabled unit. An interrupt request set to “1” is sent to CPU. These bits are returned to “0” by clearing the corresponding bit in the interrupt raw status register.

Interrupt raw status register (INTC_RAWSTAT)

[3804h] Default value = 00h Read Only

Reserved			ARSRAWSTAT	VIN4RAWSTAT	VIN3RAWSTAT	VIN2RAWSTAT	VIN1RAWSTAT
7	6	5	4	3	2	1	0

Bits[7:5]: **Reserved**

Bit[4]: **ARS Interrupt Pre-MASK Status**

Indicates whether an interrupt factor occurs in the area sensor before masking. Details are shown in the area sensor interrupt status register (ARS_INTSTAT [1C44h]) and area sensor interrupt detail status registers (ARS_ INT1-6 [1C60h] to [1C74h]).

0: No interrupt factor detected.
1: Interrupt factor detected.

Bit[3]: **Video4 Interrupt Pre-MASK Status**

Indicates whether an interrupt factor occurs in the video 4 input before masking.

0: No interrupt factor detected.
1: Interrupt factor detected.

Bit[2]: **Video3 Interrupt Pre-MASK Status**

Indicates whether an interrupt factor occurs in the video 3 input before masking.

0: No interrupt factor detected.
1: Interrupt factor detected.

Bit[1]: **Video2 Interrupt Pre-MASK Status**

Indicates whether an interrupt factor occurs in the video 2 input before masking.

0: No interrupt factor detected.
1: Interrupt factor detected.

Bit[0]: **Video1 Interrupt Pre-MASK Status**

Indicates whether an interrupt factor occurs in the video 1 input before masking.

0: No interrupt factor detected.
1: Interrupt factor detected.

These status bits indicate whether an interrupt factor occurs in an interrupt enabled unit before interrupt masking, in the interrupt enable setting register (INTC_ENABLE [3808h]). This bit is not set to “1” even if an interrupt factor occurs in an interrupt disabled unit. For a level trigger interrupt, these bits are returned to “0” by clearing the interrupt flag for each unit. For an edge trigger interrupt, they are returned to “0” by writing “1” to the corresponding bit in the trigger interrupt factor clear register (INTC_TRIG_CLEAR [3888h]).

Interrupt enable setting register (INTC_ENABLE)

[3808h] Default value = 00h Read/Write

Reserved			ARSEN	VIN4EN	VIN3EN	VIN2EN	VIN1EN
7	6	5	4	3	2	1	0

Bits[7:5]: **Reserved**

Be sure to set “0”.

Bit[4]: **ARS Interrupt Enable**

Controls an interrupt request input from the area sensor. Detailed setting is configured in the area sensor interrupt control register (ARS_INTCTRL [1C40h]).

0 (r) : Interrupt request disable state (Set to this state after resetting.)
1 (r) : Interrupt request enable state
0 (w): Invalid
1 (w): Enables an interrupt request input.

Bit[3]: **Video4 Interrupt Enable**

Controls an interrupt request input from the video 4 input. Detailed setting is configured in the video 1 input interrupt setting register (VIN4_INTSEL [1414h]).

0 (r) : Interrupt request disable state (Set to this state after resetting.)
1 (r) : Interrupt request enable state
0 (w): Invalid
1 (w): Enables an interrupt request input.

Bit[2]: **Video3 Interrupt Enable**

Controls an interrupt request input from the video 3 input. Detailed setting is configured in the video 1 input interrupt setting register (VIN3_INTSEL [1014h]).

0 (r) : Interrupt request disable state (Set to this state after resetting.)
1 (r) : Interrupt request enable state
0 (w): Invalid
1 (w): Enables an interrupt request input.

Bit[1]: **Video2 Interrupt Enable**

Controls an interrupt request input from the video 2 input. Detailed setting is configured in the video 1 input interrupt setting register (VIN2_INTSEL [0C14h]).

0 (r) : Interrupt request disable state (Set to this state after resetting.)
1 (r) : Interrupt request enable state
0 (w): Invalid
1 (w): Enables an interrupt request input.

Bit[0]: **Video1 Interrupt Enable**

Controls an interrupt request input from the video 1 input. Detailed setting is configured in the video 1 input interrupt setting register (VIN1_INTSEL [0814h]).

0 (r) : Interrupt request disable state (Set to this state after resetting.)
1 (r) : Interrupt request enable state
0 (w): Invalid
1 (w): Enables an interrupt request input.

Reading this register enables you to check whether each interrupt request input is currently enabled (bit = “1”) or disabled (bit = “0”).
Writing “1” in the register enables an interrupt request input. The interrupt controller receives an interrupt input corresponding to the bit, and outputs an interrupt request to CPU. Writing “0” sets the invalid state, which will result in an interrupt request input not being disabled by accessing this register. This bit is cleared in the interrupt enable clear register (INTC_EN_CLEAR [380Ch]).
Resetting will result in all interrupts being placed into the disable state.

Interrupt enable clear register (INTC_EN_CLEAR)

[380Ch] Default value = 00h — Write Only

Reserved			ARSENCL	V4ENCL	V3ENCL	V2ENCL	V1ENCL
7	6	5	4	3	2	1	0

Bits[7:5]: **Reserved**
Be sure to set “0”.

Bit[4]: **ARS Interrupt Enable Clear**
Disables (masks) an interrupt request input from the area sensor.
0: Invalid
1: Disables an interrupt request input.

Bit[3]: **Video4 Interrupt Enable Clear**
Disables (masks) an interrupt request input from the video 4 input.
0: Invalid
1: Disables an interrupt request input.

Bit[2]: **Video3 Interrupt Enable Clear**
Disables (masks) an interrupt request input from the video 3 input.
0: Invalid
1: Disables an interrupt request input.

Bit[1]: **Video2 Interrupt Enable Clear**
Disables (masks) an interrupt request input from the video 2 input.
0: Invalid
1: Disables an interrupt request input.

Bit[0]: **Video1 Interrupt Enable Clear**
Disables (masks) an interrupt request input from the video 1 input.
0: Invalid
1: Disables an interrupt request input.

Writing “1” clears the interrupt enable bit in the interrupt enable setting register (INTC_ENABLE [3808h]) corresponding to the bit, and disables an interrupt request input. Writing “0” sets the invalid state.

Interrupt trigger setting register (INTC_LEVEL)

[3880h] Default value = 00h Read/Write

Reserved							
7	6	5	4	3	2	1	0

Bits[7:0]: **Reserved**
Be sure to set “0Fh”.

Trigger interrupt factor clear register (INTC_TRIG_CLEAR)

[3888h] Default value = 00h Write Only

Reserved				V4RAWSTCL	V3RAWSTCL	V2RAWSTCL	V1RAWSTCL
7	6	5	4	3	2	1	0

Bits[7:4]: **Reserved**
Be sure to set “0”.

Bit[3]: **Video4 Interrupt Trigger Set**
Clears an interrupt pre-mask status from the video 4 input.
0: Invalid
1: Clears the interrupt status.

Bit[2]: **Video3 Interrupt Trigger Set**
Clears an interrupt pre-mask status from the video 3 input.
0: Invalid
1: Clears the interrupt status.

Bit[1]: **Video2 Interrupt Trigger Set**
Clears an interrupt pre-mask status from the video 2 input.
0: Invalid
1: Clears the interrupt status.

Bit[0]: **Video1 Interrupt Trigger Set**
Clears an interrupt pre-mask status from the video 1 input.
0: Invalid
1: Clears the interrupt status.

Writing “1” clears the corresponding status bit in the interrupt raw status register (INTC_RAWSTAT [3804h]).

GPIO data register (GPIO_DATA)

[3C00h] Default value = 00h Read/Write

GPIODATA [7:0]							
7	6	5	4	3	2	1	0

Bits[7:0]: **GPIO Data**
GPIO data register This register can be written and read. Setting GPIO to the output mode reads this register; setting GPIO to the input mode reads the pint state.

GPIO pin function register (GPIO_FUNC)

[3C04h] Default value = 0000h Read/Write

GP7MD [1:0]		GP6MD [1:0]		GP5MD [1:0]		GP4MD [1:0]	
15	14	13	12	11	10	9	8
GP3MD [1:0]		GP2MD [1:0]		GP1MD [1:0]		GP0MD [1:0]	
7	6	5	4	3	2	1	0

Bits[15:14]: **GPIO7 Port Function Select**
Sets the function of the GPIO7 pin.
00: GPIO7 port input
01: I^2C Through function SDA (Data)
10: GPIO7 port output
11: Reserved

Bits[13:12]: **GPIO6 Port Function Select**
Sets the function of the GPIO6 pin.
00: GPIO6 port input
01: I^2C Through function SCL (Clock)
10: GPIO6 port output
11: Reserved

Bits[11:10]: **GPIO5 Port Function Select**
Sets the function of the GPIO5 pin.
00: GPIO5 port input
01: I^2C Through function SDA (Data)
10: GPIO5 port output
11: Reserved

Bits[9:8]: **GPIO4 Port Function Select**
Sets the function of the GPIO4 pin.
00: GPIO4 port input
01: I^2C Through function SCL (Clock)
10: GPIO4 port output
11: Reserved

Bits[7:6]: **GPIO3 Port Function Select**
Sets the function of the GPIO3 pin.
00: GPIO3 port input
01: I^2C Through function SDA (Data)
10: GPIO3 port output
11: Reserved

Bits[5:4]: **GPIO2 Port Function Select**
Sets the function of the GPIO2 pin.
00: GPIO2 port input
01: I^2C Through function SCL (Clock)
10: GPIO2 port output
11: Reserved

Bits[3:2]: **GPIO1 Port Function Select**
Sets the function of the GPIO1 pin.
00: GPIO1 port input
01: I^2C Through function SDA (Data)
10: GPIO1 port output
11: Reserved

Bits[1:0]: **GPIO0 Port Function Select**
Sets the function of the GPIO0 pin.
00: GPIO0 port input
01: I^2C Through function SCL (Clock)
10: GPIO0 port output
11: Reserved

6. FUNCTIONAL DESCRIPTION

6.1 Initial Settings

S2S65P10 can use the CONF[3:0] pin to set the initial state after resetting has been released. The CONF[3:0] pin has the following functions: The default values of some registers vary depending on the initial state.

CONF[3]: I^2C Slave Address Select
Sets the I^2C slave address of this I^2C.
0: Sets the I^2C slave address to 36h.
1: Sets the I^2C slave address to 37h.

CONF[2]: Video Input / Output Format Select
Sets the video I/O format.
0: Sets the video I/O format into the BT601 mode.
1: Sets the video I/O format into the BT656 mode.

CONF[1:0]: Video Input Mode Select
Sets the video input mode.
00: Sets all video inputs to NTSC(720).
01: Sets all video inputs to NTSC(704).
10: Sets all video inputs to PAL.
11: Sets all video inputs to VGA.

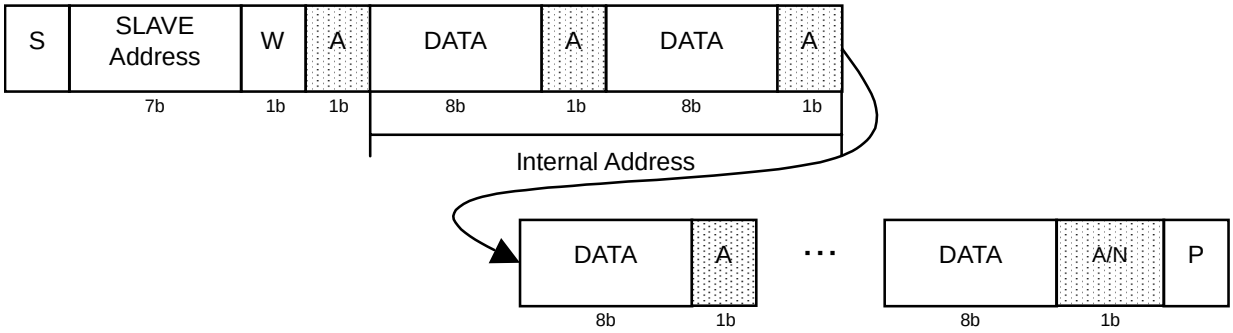
The CONF[3:0] pin contains a pull-down resistor. If necessary, use the CONF pin pull-down control register (SYS_CONFPCCTRL [0064h]) to control the pull-down resistor.

6.2 I^2C

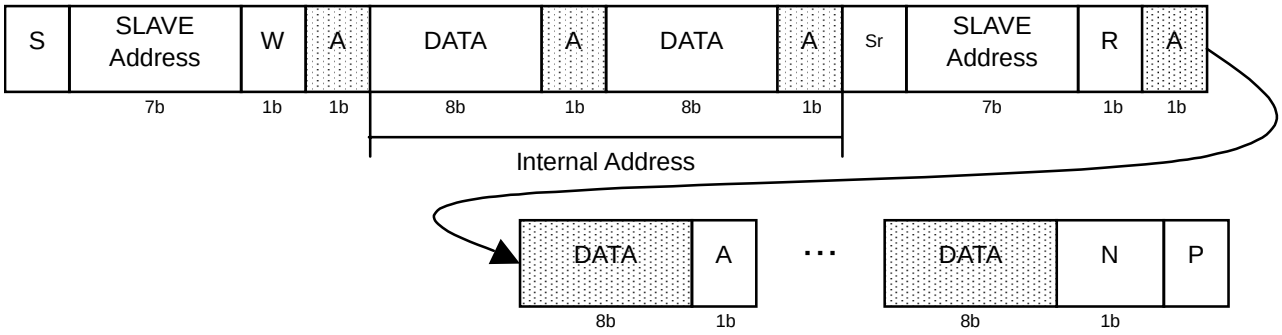
The S2S65P10 internal registers are configured via the I^2C interface. The I^2C slave address, which is switched depending on the state of the CONF[3] pin, is set to 36h or 37h. (It can be changed to any address using the I^2C slave address setting register (I2C_SLAVE_ADRS [0404h]).)

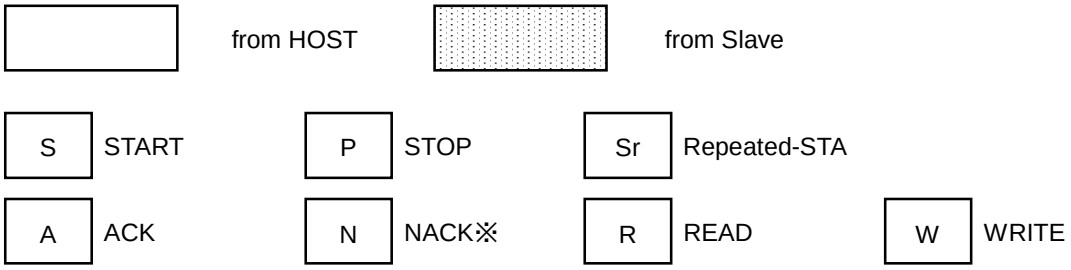
Fig.6.1 shows the data format used to access an internal register. First issue a start condition to start the use of the bus, and specify a slave address of the device. Then send the internal address (2 bytes) of the device as data in the order of high- and low-order bytes. Specifying the write mode continuously sends write data. Specifying the read mode issues a restart condition again, specifies a slave address of the device, and reads data. This function enables the continuous access mode, which automatically increments the internal address. The increment method varies depending on the number of access steps specified in the I^2C setting register (I2C_CONTROL [0400h]). Fig.6.2 shows the address increment image.

The format for data write



The format of data read





※ This Slave Tranffer will finish by NACK replay from Master Receiver.

Fig.6.1 I^2C data format

●Address increment image at continuous access (step 32)

31 24	23 16	15 8	7 0	
			①	0H
			②	4H
			③	8H
			④	CH
			⑤	10H
			⑥	14H

Example: When continuously accessing "0000h" and subsequent addresses in step 32, the 8-bit access order is as follows.
"0000h" → "0004h" → "0008h" → "000Ch" → "0010h" → "0014h"

●Address increment image at continuous access (step 16)

31 24	23 16	15 8	7 0	
		②	①	0H
		④	③	4H
		⑥	⑤	8H

Example: When continuously accessing "0000h" and subsequent addresses in step 16, the 8-bit access order is as follows.
"0000h" → "0001h" → "0004h" → "0005h" → "0008h" → "0009h"

●Address increment image at continuous access (step 8)

31 24	23 16	15 8	7 0	
④	③	②	①	0H
		⑥	⑤	4H

Example: When continuously accessing "0000h" and subsequent addresses in step 8, the 8-bit access order is as follows.
"0000h" → "0001h" → "0002h" → "0003h" → "0004h" → "0005h"

Fig.6.2 Address increment image

The following shows the procedure to access S2S65P10 from the host CPU via I^2C-Bus. In this procedure, symbols S, T, R, and P conform to the basic flow that is composed of the commands issued by S65K series I^2C-Master such as S2S65A00. For more information, see the S65K Series Technical Manual.

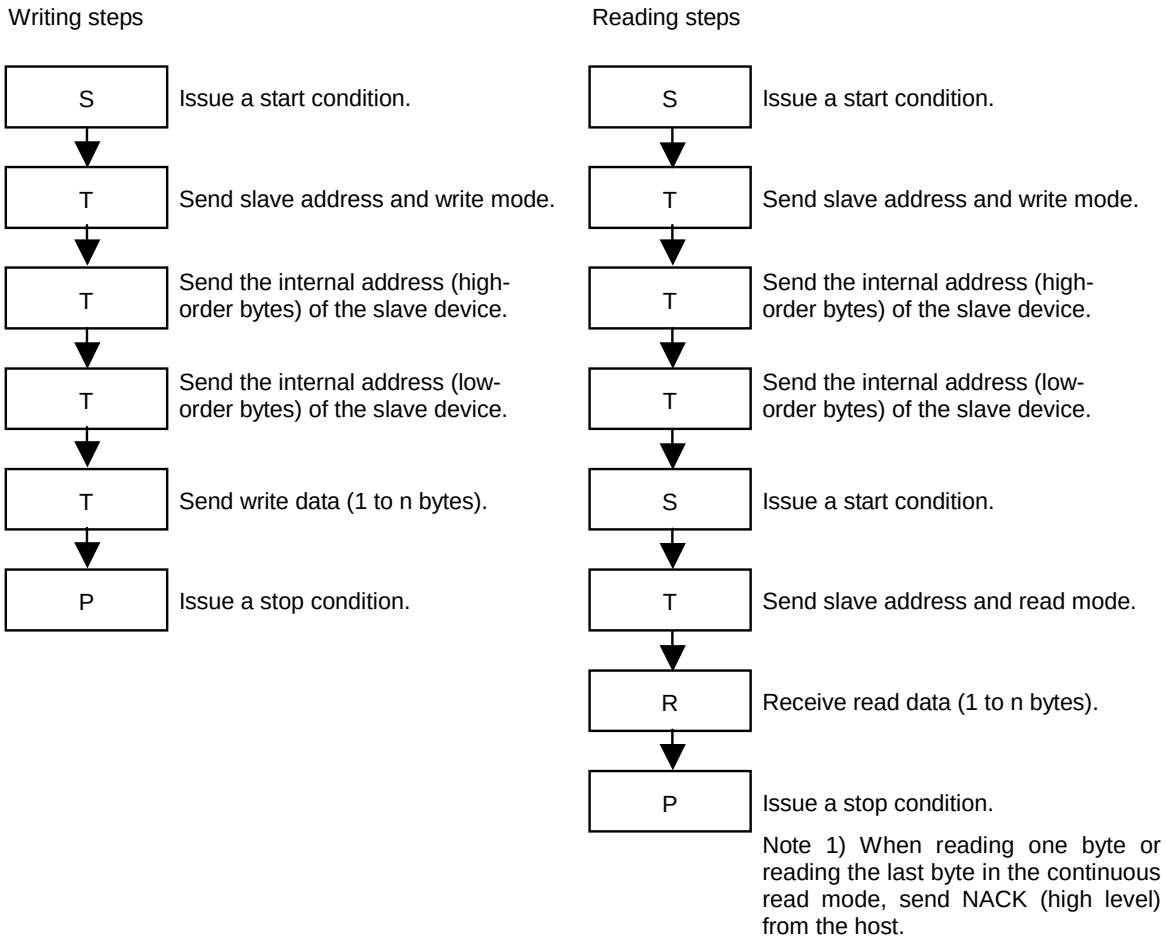


Fig.6.3 I^2C access procedure

6.3 Interlace/Progressive Conversion

S2S65P10 has the following three types of interlace/progressive conversion modes. For setting, use the interlace/progressive conversion mode setting register (IPC_MODE [3000h])

- Weave Mode
  Builds one frame of a combination of odd and even fields.
- Bob Mode
  Doubles each line only in an odd field to build one frame.
- Interpolation Mode
  Interpolates linearly two consecutive horizontal lines only in an odd field to build one frame.

6.4 Video Output and Intelligent Auto Image Switching

S2S65P10 has the following four types of video output modes. For setting, use the output image setting register (SYS_OUTMODE [0030h]).

● Fixed Mode
Fixes to one video input to output data. Video input switching is carried out using the output image selection register (SYS_OUTCH [0038h]). If necessary, video input can be switched while video output is turned on.

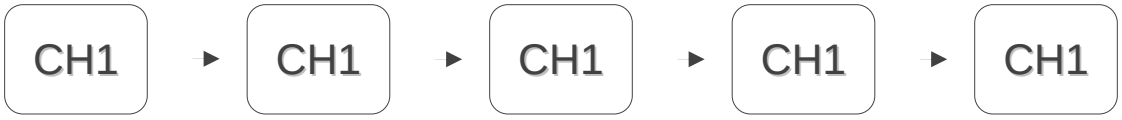


Fig.6.4 Fixed Mode

● Auto Scan Mode
Outputs data while switching video input in the order of 1-2-3-4-1... The cycle count for each video input is specified using the video 1-4 output cycle setting registers (SYS_CH1-4OUTCYCLE [0040h] to [004Ch]). Turning off video input will automatically switch to the next video input. Even if the cycle count is 0, video input will be switched automatically to the next one. The cycle count can be changed while video output is turned on. Which video input is output can be confirmed using the ST[1:0] pin.

Fig.6.5 Auto Scan Mode

● Compress Mode
Resizes to QVGA to output data while switching video input in the order of 1-2-3-4-1... Turning video input off will not output the video input. Which video input is output can be confirmed using the ST[1:0] pin.

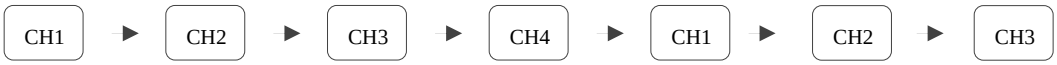


Fig.6.6 Compress Mode

● Merge Mode
Outputs images in each channel resized into QVGA and synthesizing four screens into one. The merge mode is available only when four input mode settings (SYS_CH1-4INMODE[0010h] to [001Ch]) are identical. Each video input can be turned off if necessary.

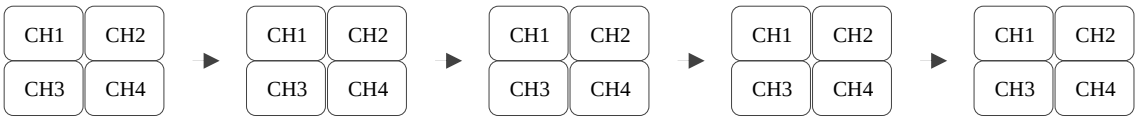


Fig.6.7 Merge Mode

Before changing the video output mode, be sure to turn off video output. The following shows the procedure to change the video output mode.

Ex.) When changing the merge mode to the fixed mode:
① Write 43h to the output image selection register (SYS_OUTMODE[0030h]).
② Write C3h to the output image selection register (SYS_OUTMODE[0030h]).

<Frame rate>

Video output synchronizes with each video input; therefore, the frame rate may reduce when switching video input. The table below lists the minimum and maximum values of the frame rate in each video output mode.

Table 6.1 Frame rate

Video output mode	Video input	Min.[fps]	Max.[fps]
Fixed mode	Interlace	—	30
	Progressive	—	30
Autoscan mode	Interlace	15	30
	Progressive	15	30
Compress mode (QVGA output)	Interlace	60	120
	Progressive	30	60
Merge mode (QVGAx4 output)	Interlace	15	30
	Progressive	7.5	15

*It is a value when the frame rate of the video 1-4 is equal at 30fps.

<ST[1:0] pin>

The ST[1:0] pin shows screen information of video output. The ST[1:0] signal, which changes at a timing when VOUT is output, holds the last output screen information until the next screen is output. The screen information is as follows.

00: Outputs video 1.
01: Outputs video 2.
10: Outputs video 3.
11: Outputs video 4.
* “00” is output in the merge mode.

<Video output>

The video output setting register (SYS_OUTCONFIG [0034h]) enables the following settings.

- Switching the polarity of the signal output from the VOUT pin.
- Switching the polarity of the signal output from the HOUT pin.
- Selecting the video output format
  BT601 or BT656 mode
- Selecting the YUV data alignment sequence
  Cb-Y0-Cr-Y1 / Cr-Y0-Cb-Y1 / Y0-Cb-Y1-Cr / Y0-Cr-Y1-Cb
- Selecting the signal output from the VOUT pin
  VSYNC or VVALID signal
- Selecting the signal output from the HOUT pin
  HSYNC or HVALID signal
- Switching the I/O direction of the video 1 pin
  Video input or video output
- Switching the I/O direction of the video 2 pin
  Video input or video output
- Switching the I/O direction of the video 3 pin
  Video input or video output
- Switching the I/O direction of the video 4 pin
  Video input or video output

* Changing the video 1-4 pin to the output mode will output the same image as for the video output pin.
* When changing the video 1-4 pins to the output mode, set only one pin of them to the output mode.

<Video output timing>

Configuring register settings enables you to change the video output timing. Fig.6.8 shows the set values and output timings. Each setting register is configured as follows.

HF	Common to videos 1 to 4	VOUT_HF [1800h]
HP	Common to videos 1 to 4	VOUT_HP [1804h]
HB	Common to videos 1 to 4	VOUT_HB [1808h]
HD	* Automatically set depending on the video I/O mode.	
HT	Video 1	VOUT_HT1 [1820h]
	Video 2	VOUT_HT2 [1824h]
	Video 3	VOUT_HT3 [1828h]
	Video 4	VOUT_HT4 [182Ch]
VF	Common to videos 1 to 4	VOUT_VF [1830h]
VP	Common to videos 1 to 4	VOUT_VP [1834h]
VB	Common to videos 1 to 4	VOUT_VB [1838h]
VD	* Automatically set depending on the video I/O mode.	

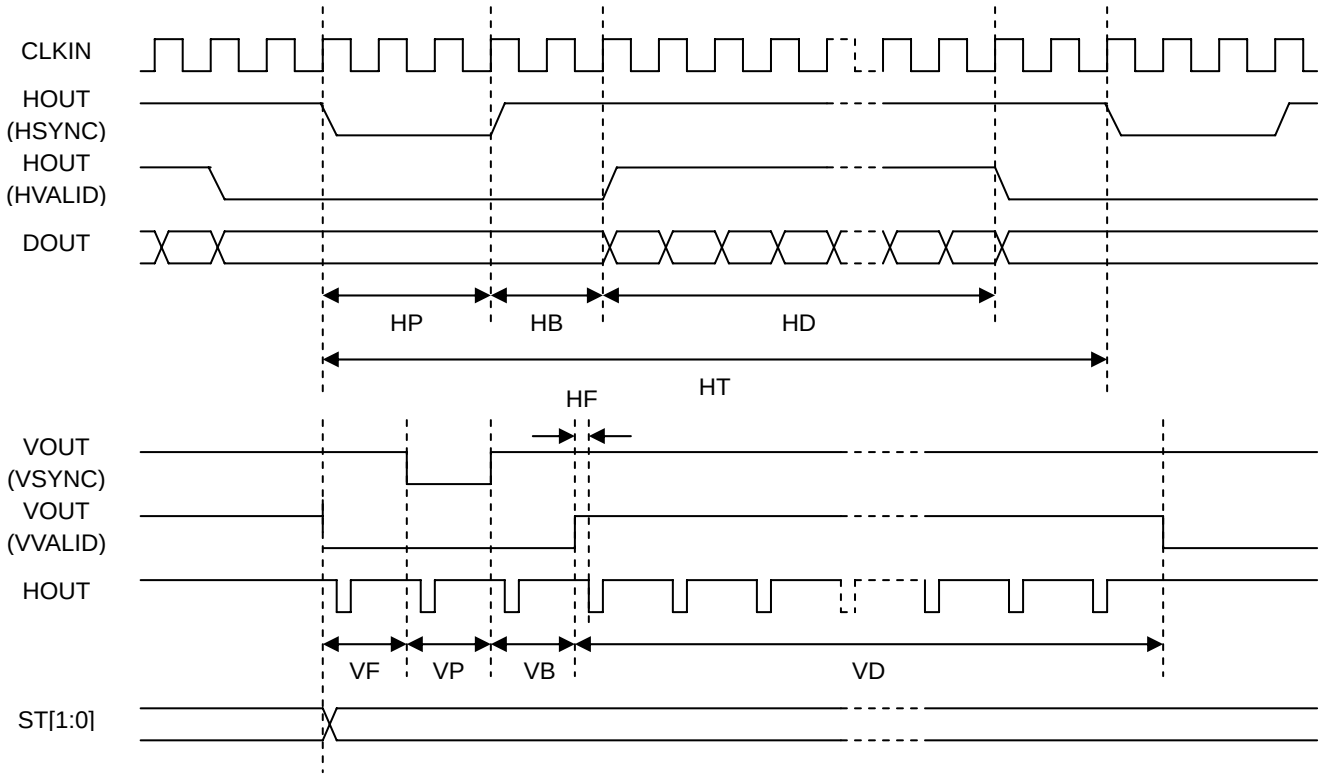


Fig.6.8 Video output timing

<HT>
Specify the HT value for each video output mode, referring to the following.
● When video output is in the fixed, auto scan, or merge mode:
Specify the time when 1-line data is input from a video input.
Ex.) When the CLKIN clock frequency is 25MHz in BT601 NTSC input:
858[Pixel] / 27[MHz] × 25[MHz] = 794[Pixel]

● When video output is in the compress mode:
Specify the time when 1/2-line data is input from a video input.
Ex.) When the CLKIN clock frequency is set in BT601 PAL input:
864[Pixel]/ 27[MHz]/ 2 × 25[MHz] = 400[Pixel]

6.5 Video Input Modes and Aspect Ratio Conversion

S2S65P10 has the following modes. The video input mode is specified using the input image 1-4 setting registers (SYS_CH1-4 INMODE [0010h] to [001Ch]). S2S65P10, which provides the aspect ratio conversion function, automatically converts the aspect ratio depending on the video I/O mode.

● VGA conversion (When video output is in the fixed, auto scan, or merge mode)

Table 6.2 VGA conversion

Video input mode	Pixel Aspect ratio	Number of pixels		After conversion
NTSC(720)	8:9	720:480	--→	640:480
NTSC(704)	10:11	704:480	--→	640:480
PAL	16:15	720:576	--→	768:576
VGA	1:1	640:480	--→	640:480

● QVGA conversion (When video output is in the compress or merge mode)

Table 6.3 QVGA conversion

Video input mode	Pixel Aspect ratio	Number of pixels		After conversion
NTSC(720)	8:9	720:480	--→	320:240
NTSC(704)	10:11	704:480	--→	320:240
PAL	16:15	720:576	--→	384:288
VGA	1:1	640:480	--→	320:240

* This function is available only for either field if video input is in the interlace mode.
* Lines are thinned out vertically if video input is in the progressive mode.

<Video input>

The following setting is configured for each video input using the video 1-4 input setting registers (SYS_CH1-4INCONFIG [0020h] to [002Ch]).

- Switching the valid edge of video input clock
- Switching the VIN polarity
- Switching the HIN polarity
- Switching the ODDIN polarity
- Selecting the video input format
  BT601 or BT656 mode
- Selecting the YUV data alignment sequence
  Cb-Y0-Cr-Y1 / Cr-Y0-Cb-Y1 / Y0-Cb-Y1-Cr / Y0-Cr-Y1-Cb

Interrupt can be generated with a synchronization signal for each video input. Interrupt settings are configured using the following registers.

Video 1 input interrupt setting register	VIN1_INTSEL [0814h]
Video 2 input interrupt setting register	VIN2_INTSEL[0C14h]
Video 3 input interrupt setting register	VIN3_INTSEL[1014h]
Video 4 input interrupt setting register	VIN4_INTSEL[1414h]

Interrupt control is carried out using the interrupt enable setting register (INTC_EBABLE [3808h]) and interrupt enable clear register (INTC_EN_CLEAR [380Ch]), and interrupt check using the interrupt status register (INTC_STAT [3800h]) and interrupt raw status register (INTC_RAWSTAT [3804h]).

The video input pin contains a pull-down resistor. If necessary, use the video 1-4 input pull-down control registers (SYS_CH1-4PCCTRL [0050h] to [005Ch]) to control the pull-down resistor.

<Video input capture position>

Configuring register settings enables you to adjust the video input capture position for each video input. Adjustment is carried out on a pixel basis in the X direction, and on a line basis for each odd or even field in the Y direction. Each setting register is configured as follows. Fig.6.9 shows the set values and capture positions.

Video 1	X direction	VIN1_XSTART [0808h]
	Y direction (Odd field)	VIN1_YSTART_O [080Ch]
	Y direction (Even field)	VIN1_YSTART_E [0810h]
Video 2	X direction	VIN2_XSTART [0C08h]
	Y direction (Odd field)	VIN2_YSTART_O [0C0Ch]
	Y direction (Even field)	VIN2_YSTART_E [0C10h]
Video 3	X direction	VIN3_XSTART [1008h]
	Y direction (Odd field)	VIN3_YSTART_O [100Ch]
	Y direction (Even field)	VIN3_YSTART_E [1010h]
Video 4	X direction	VIN4_XSTART [1408h]
	Y direction (Odd field)	VIN4_YSTART_O [140Ch]
	Y direction (Even field)	VIN4_YSTART_E [1410h]

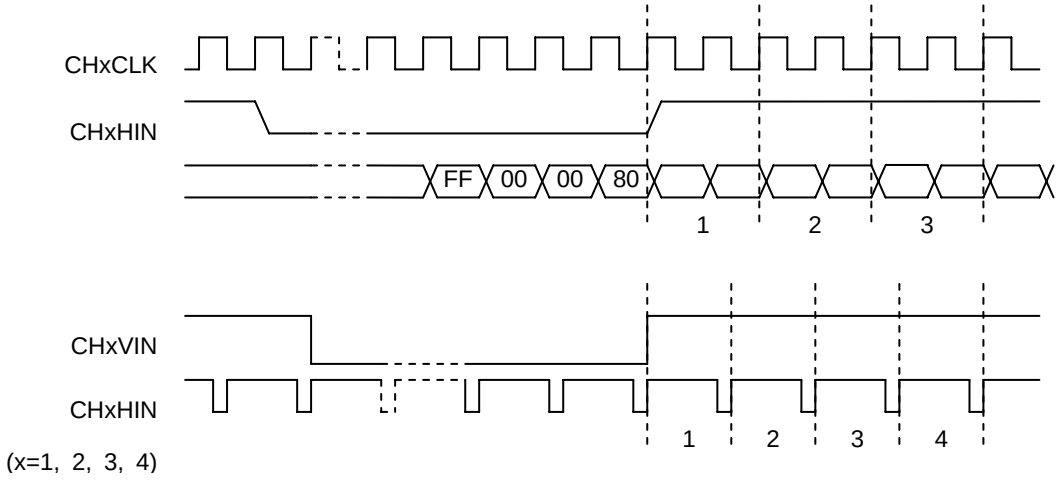


Fig.6.9 Video input capture position

6.6 Area Sensor

S2S65P10 contains an area sensor to detect a moving object. The area sensor divides a screen from any channel into 48 square areas, and gets difference between two consecutive frames for each square area. It outputs an interrupt signal if the difference is greater than a threshold preset.

The area sensor is configured using the area sensor setting registers 1 to 4 (ARS_CONTROL1-4 [1C00h] to [1C0Ch]), area sensor X-direction size setting register (ARS_XSIZE [1C18h]), area sensor Y-direction size setting register (ARS_YSIZE [1C1Ch]), and area sensor control registers 1 to 6 (ARS_SELECT1-6 [1C20h] to [1C34h]).

Interrupt control is carried out using the interrupt enable setting register (INTC_EBABLE [3808h]), interrupt enable clear register (INTC_EN_CLEAR [380Ch]), and area sensor interrupt control register (ARS_INTCTRL [1C40h]).

Interrupt check is carried out using the interrupt status register (INTC_STAT [3800h]), interrupt raw status register (INTC_RAWSTAT [3804h]), area sensor interrupt status register (ARS_INTSTAT [1C44h]), and area sensor interrupt detail status register 1 (ARS_INT1-6 [1C60h] to [1C74h]).

Area 01	Area 02	Area 03	Area 04	Area 05	Area 06	Area 07	Area 08
Area 11	Area 12	Area 13	Area 14	Area 15	Area 16	Area 17	Area 18
Area 21	Area 22	Area 23	Area 24	Area 25	Area 26	Area 27	Area 28
Area 31	Area 32	Area 33	Area 34	Area 34	Area 36	Area 37	Area 38
Area 41	Area 42	Area 43	Area 44	Area 45	Area 46	Area 47	Area 48
Area 51	Area 52	Area 53	Area 54	Area 55	Area 56	Area 57	Area 58

Fig.6.10 Area sensor detection areas (Areas 00 to 57)

6.7 GPIO/I²C Through Function

The GPIO [7:0] pin has two functions: it can work as the general-purpose I/O port, and it can pass through the I²C signals sent from the host CPU. Using the latter function makes it possible to control a device having the same I²C device address from the host CPU. The GPIO pin has a built-in pull-up resistor. If necessary, use the GPIO pin pull-up control register (SYS_GPIOPCCTRL [0060h]) to control the pull-up resistor.

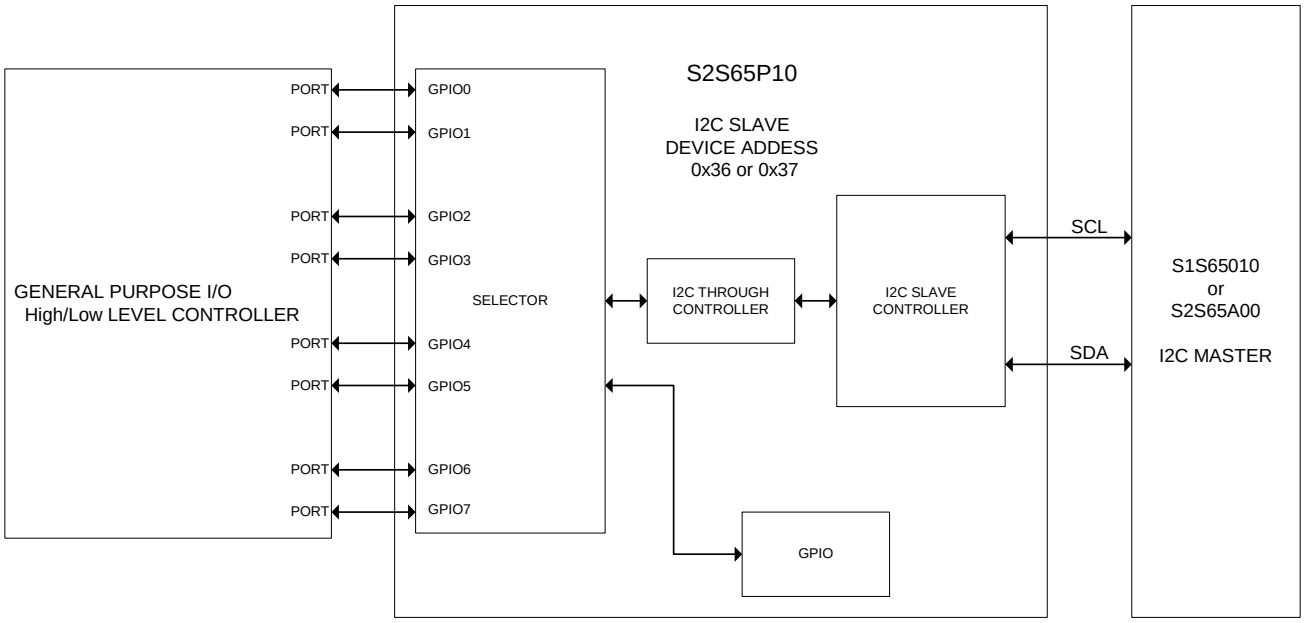


Fig.6.11 GPIO Function

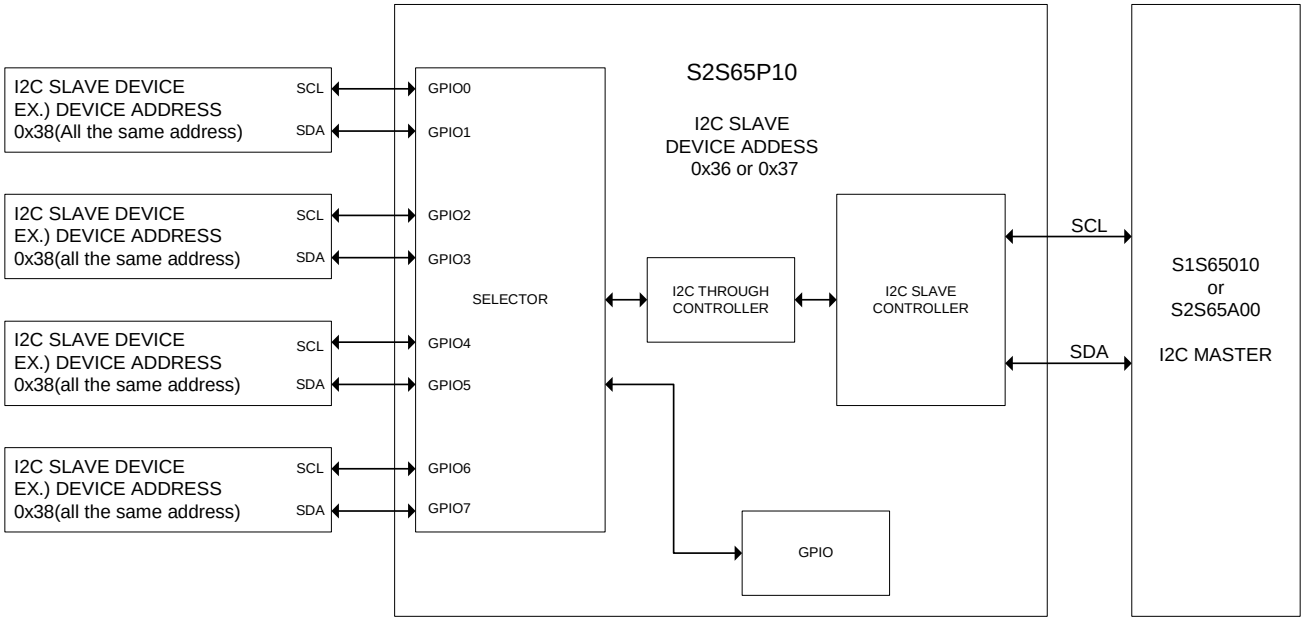
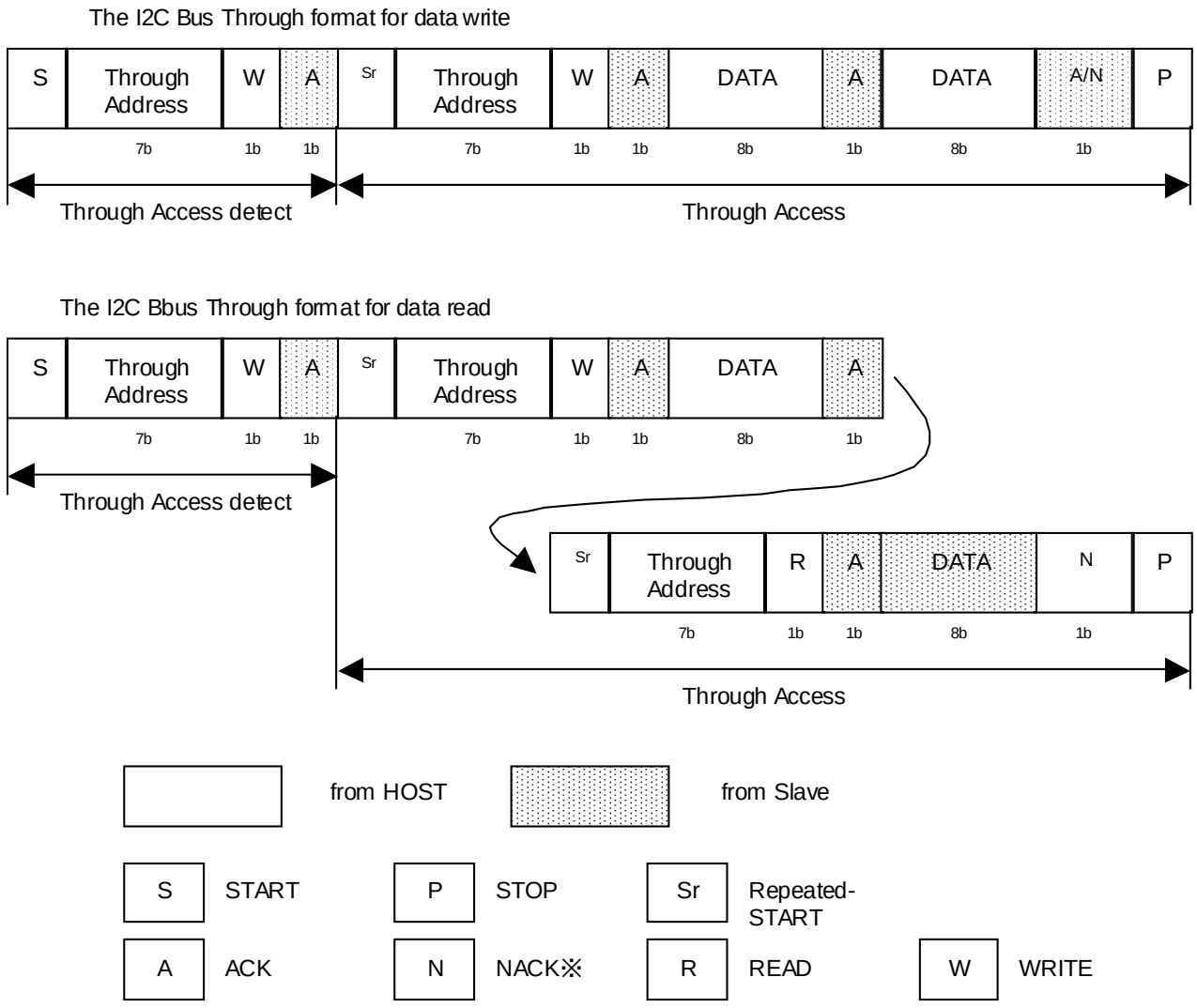


Fig.6.12 I²C through function

Set any value in the I^2C bus through address setting register (I2C_THR_ADRS[0410h]), and also set the ID of the I^2C device connected to the GPIO pin in the I^2C bus through ID setting register (I2C_THR_ADRS[0410h]). When I^2C-accessing the address specified in the I^2C bus through address setting register (I2C_THR_ADRS[0410h]) from the host CPU in the format shown in Fig.6.25, S2S65P10 recognizes it as a through access, and changes the through address to the value specified in the I^2C bus through ID setting register (I2C_THR_DEVID[0414h]) to pass through the I^2C access to the GPIO pin.



F6.13 I^2C Bus Through Data Format

The following shows the procedure to access the device connected to Through-Bus from the host CPU via I^2C-Bus and S2S65P10, giving a case example where you access the device connected to GPIO0 and GPIO1.

Register settings

GPIO settings
- Setting Reg: 3C04h to 0005h ... Set GPIO0 to GPIO1 to the I^2C function, and set GPIO2 to GPIO7 to the GPIO function.

Note) When connecting multiple devices with the same device ID, exclusively control GPIO.

I^2C settings (For Through Instruction Address 2Fh, Through Device Address 38h)
- Setting Reg: 0410h to 2Fh ... Set the Through instruction address in register : [I^2C THROUGH ADDRESS].
- Setting Reg: 0414h to 38h ... Set the through destination device ID in register : [I^2C THROUGH DEV ID].
- Setting Reg : 040Ch to 01h ... Set I^2C into the through mode.

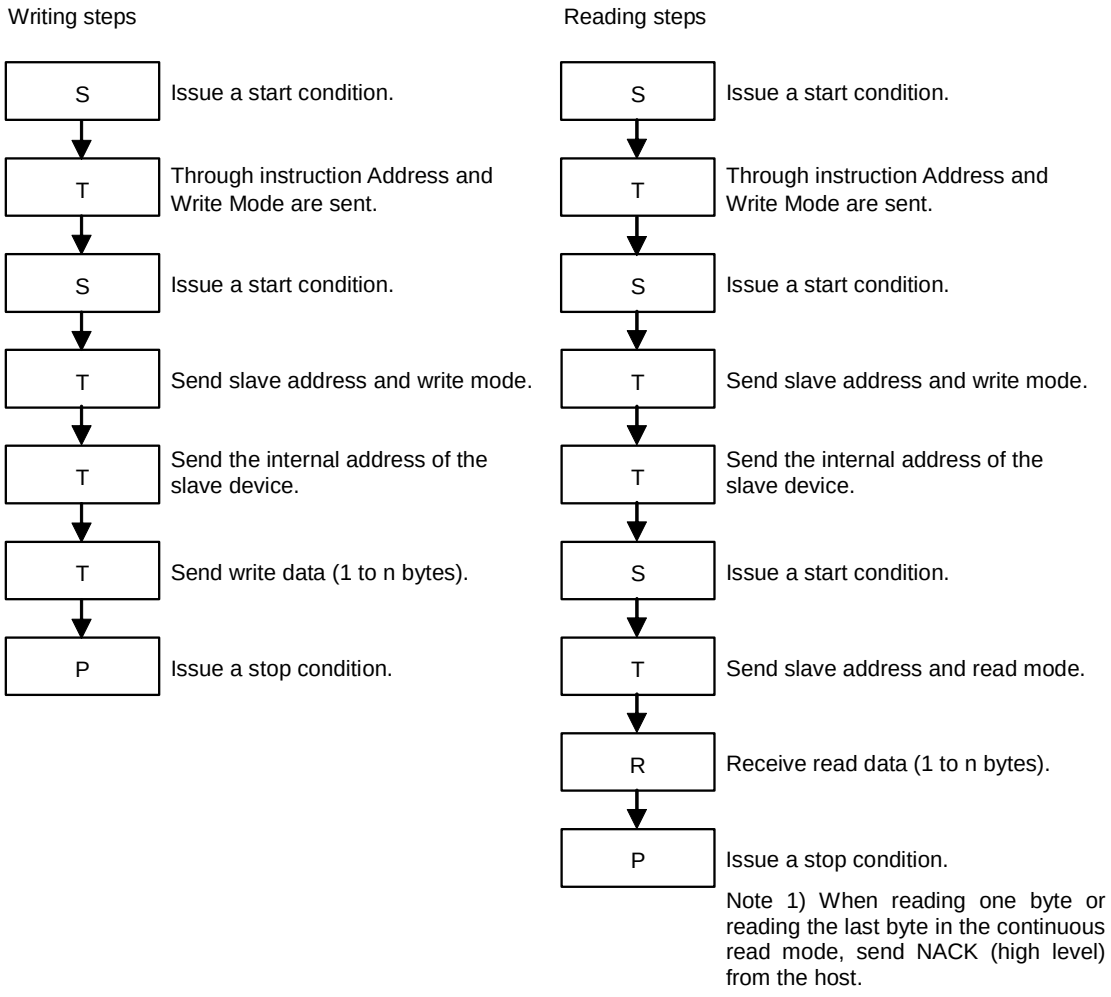


Fig.6.14 I^2C through function setting procedure

7. DC CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 7.1 Absolute maximum ratings

(V_{SS}=0V)

Item	Symbol	Rating	Unit
Supply voltage	HV_{DD}*1	V_{SS}-0.3 to 4.0	V
	HV_{DD1}*1	V_{SS}-0.3 to 4.0	V
	HV_{DD4}*1	V_{SS}-0.3 to 4.0	V
	LV_{DD}*1	V_{SS}-0.3 to 2.5	V
Input voltage	HV_I	V_{SS}-0.3 to HV_{DD},HV_{DD1},HV_{DD4}+0.5	V
	LV_I	V_{SS}-0.3 to LV_{DD}+0.5	V
Output voltage	HV_O	V_{SS}-0.3 to HV_{DD},HV_{DD1},HV_{DD4}+0.5	V
	LV_O	V_{SS}-0.3 to LV_{DD}+0.5	V
Output current/pin	I_{OUT}	±10	mA
Storage temperature	T_{stg}	-65 to +150	°C

(Note) *1 : HV_{DD}, HV_{DD1}, $HV_{DD4} \geq LV_{DD}$

7.2 Recommended Operating Conditions

Table 7.2 Recommended Operating Conditions

(2 Power supply: HV_{DD}, HV_{DD1}, HV_{DD4}/LV_{DD}=3.3/1.8V)

Item	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage (High)	HV_{DD}	2.40	3.30	3.60	V
Power supply voltage (High-voltage video inputs 1, 2, and 3)	HV_{DD1}	2.40	3.30	3.60	V
Power supply voltage (High-voltage video input 4)	HV_{DD4}	2.40	3.30	3.60	V
Power supply voltage (Low)	LV_{DD}	1.65	1.80	1.95	V
Input voltage	HV_I	V_{SS}	—	HV_{DD} HV_{DD1} HV_{DD4}	V
	LV_I	V_{SS}	—	LV_{DD}	V
Ambient temperature	T_a	-40	25	105*1	°C

(Note) *1: This ambient temperature range represents a recommended one assuming Tj = -40 to +125°C.

7.3 DC Characteristics

Table 7.3 DC characteristics

(Under the recommended operating conditions)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Static power consumption (static current between HV_{DD} and V_{SS})						
Static power consumption	I_{DDSH1}	V_{IN}=HV_{DD} or HV_{DD1} or HV_{DD4} or LV_{DD} or V_{SS} HV_{DD}=Max. HV_{DD1}=Max. HV_{DD4}=Max. LV_{DD}=Max. I_{OH}=I_{OL}=0 When T_a(Max.)=105(°C), T_a=T_j=105(°C)	—	—	16	μA
Static power consumption (static current between HV_{DD1} and V_{SS})						
Static power consumption	I_{DDSH2}	V_{IN}=HV_{DD} or HV_{DD1} or HV_{DD4} or LV_{DD} or V_{SS} HV_{DD}=Max. HV_{DD1}=Max. HV_{DD4}=Max. LV_{DD}=Max. I_{OH}=I_{OL}=0 When T_a(Max.)=105(°C), T_a=T_j=105(°C)	—	—	18	μA
Static power consumption (static current between HV_{DD4} and V_{SS})						
Static power consumption	I_{DDSH3}	V_{IN}=HV_{DD} or HV_{DD1} or HV_{DD4} or LV_{DD} or V_{SS} HV_{DD}=Max. HV_{DD1}=Max. HV_{DD4}=Max. LV_{DD}=Max. I_{OH}=I_{OL}=0 When T_a(Max.)=105(°C), T_a=T_j=105(°C)	—	—	6	μA
Static current (static current between LV_{DD} and V_{SS})						
Static power consumption	I_{DDSL}	V_{IN}=HV_{DD} or HV_{DD1} or HV_{DD4} or LV_{DD} or V_{SS} HV_{DD}=Max. HV_{DD1}=Max. HV_{DD4}=Max. LV_{DD}=Max. I_{OH}=I_{OL}=0 When T_a(max)=105(°C), T_a=T_j=105(°C)	—	70	900	μA

7. DC CHARACTERISTICS

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power consumption (current consumption between LV_{DD} and V_{SS})						
Operational power consumption	I_{DDL}	HV_{DD}=3.3V HV_{DD1}=3.3V HV_{DD4}=3.3V LV_{DD}=1.8V T_a=-40 to +105°C CHxCLK=27MHz (x=1, 2, 3, 4) CLKIN=25MHz	—	25	40	mA
Input leak						
Input leak current	I_L	HV_{DD}=Max. HV_{DD1}=Max. HV_{DD4}=Max. LV_{DD}=Max. HV_{IH}=HV_{DD},HV_{DD1}, HV_{DD4} LV_{IH}=LV_{DD} V_{IL}=V_{SS}	-5	—	5	μA
Input characteristics (H-type LVCMOS) CLKIN, SDA, SDC						
HIGH Level input voltage	V_{IH1H}	HV_{DD}=Max. HV_{DD1}=Max. HV_{DD4}=Max.	2.2	—	—	V
LOW Level input voltage	V_{IL1H}	HV_{DD}=Min. HV_{DD1}=Min. HV_{DD4}=Min.	—	—	0.8	V
Input characteristics (L-type LVCMOS) TESTEN						
HIGH Level input voltage	V_{IH1L}	LV_{DD}=Max.	1.27	—	—	V
LOW Level input voltage	V_{IL1L}	LV_{DD}=Min.	—	—	0.57	V
Schmitt input characteristics (H-type LVCMOS) RESETX, CHxCLK, CHxVIN, CHxHIN, CHxDIN[7:0], CHxODD, GPIO[7:0], CONF[3:0] (x=1, 2, 3, 4)						
HIGH Level trigger voltage	V_{T1+}	HV_{DD}=Max. HV_{DD1}=Max. HV_{DD4}=Max. LV_{DD}=Max.	1.4	—	2.7	V
LOW Level trigger voltage	V_{T1-}	HV_{DD}=Min. HV_{DD1}=Min. HV_{DD2}=Min. LV_{DD}=Min.	0.6	—	1.8	V
Hysteresis voltage	ΔV	HV_{DD}=Min. HV_{DD1}=Min. HV_{DD4}=Min. LV_{DD}=Min.	0.3	—	—	V
Input characteristics RESETX, GPIO[7:0]						
Pull-up resistor	RPLU1H	V_I=V_{SS}	25	50	120	kΩ
Input characteristics CHxCLK, CHxVIN, CHxHIN, CHxDIN[7:0], CHxODD, CONF[3:0] (x=1, 2, 3, 4)						
Pull-down resistance	RPLD1H	V_I=HV_{DD},HV_{DD1}, HV_{DD4}	25	50	120	kΩ

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output characteristics CHxVIN, CHxHIN, CHxDIN[7:0], V_{OUT}, HOUT, DOUT[7:0], SDA, INTX, ST[1:0] GPIO[7:0] (x=1, 2, 3, 4)						
HIGH Level output voltage	V_{OH1H}	HV_{DD}=Min. HV_{DD1}=Min. HV_{DD4}=Min. I_{OH}=-2mA	HV_{DD}-0.4 HV_{DD1}-0.4 HV_{DD4}-0.4	—	—	V
LOW Level output voltage	V_{OL1H}	HV_{DD}=Min. HV_{DD1}=Min. HV_{DD4}=Min. I_{OL}=2mA	—	—	V_{SS}+0.4	V
Output characteristics CHxVIN, CHxHIN, CHxDIN[7:0], SDA, GPIO[7:0] (x=1, 2, 3, 4)						
OFF-STATE leak current	I_{OZ}	HV_{DD}=Max. HV_{DD1}=Max. HV_{DD4}=Max. LV_{DD}=Max. HV_{OH}=HV_{DD},HV_{DD1}, HV_{DD4} LV_{OH}=LV_{DD} V_{OL}=V_{SS}	-5	—	5	μA

8. AC CHARACTERISTICS

8.1 Video Input Interface

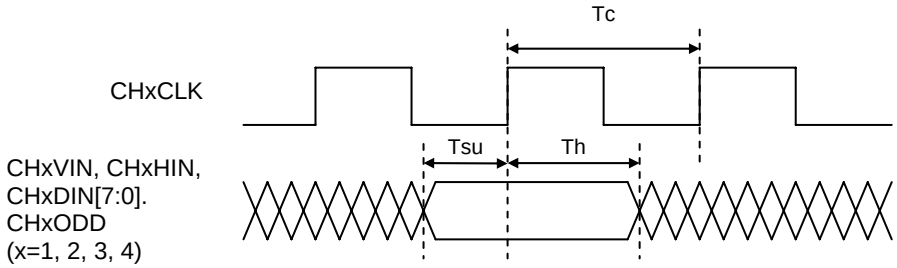


Fig.8.1 Video Input Interface Timing Chart

Table 8.1 Video Input Interface Timing Spec.

Ta = -40 to +105 °C, HV_{DD},HV_{DD1},HV_{DD4} = 2.4 to 3.6 V, LV_{DD} = 1.65 to 1.95 V, V_{SS} = 0 V, CL = 30 pF (Output)

Item	Symbol	Min.	Typ.	Max.	Unit
Video input clock frequency	Tf	—	27	28.5	MHz
Video input clock cycle time	Tc	25	37	—	ns
Data setup time	Tsu	10	—	—	ns
Data hold time	Th	10	—	—	ns

8.2 Video Output Interface

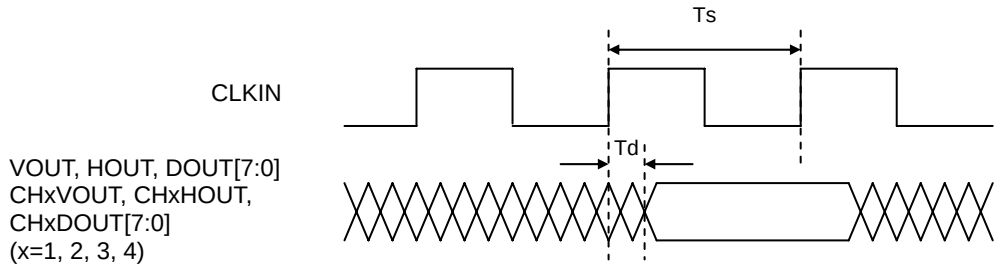


Fig.8.2 Video Output Interface Timing Chart

Table 8.2 Video Output Interface Timing Spec.

Ta = -40 to +105 °C, HV_{DD},HV_{DD1},HV_{DD4} = 2.4 to 3.6 V, LV_{DD} = 1.65 to 1.95 V, V_{SS} = 0 V, CL = 30 pF (Output)

Item	Symbol	Min.	Typ.	Max.	Unit
CLKIN clock frequency	fc	20	25	28.5	MHz
CLKIN clock cycle time	Ts	35	40	50	ns
Data output delay time	Td	5	—	20	ns

8.3 I²C Interface

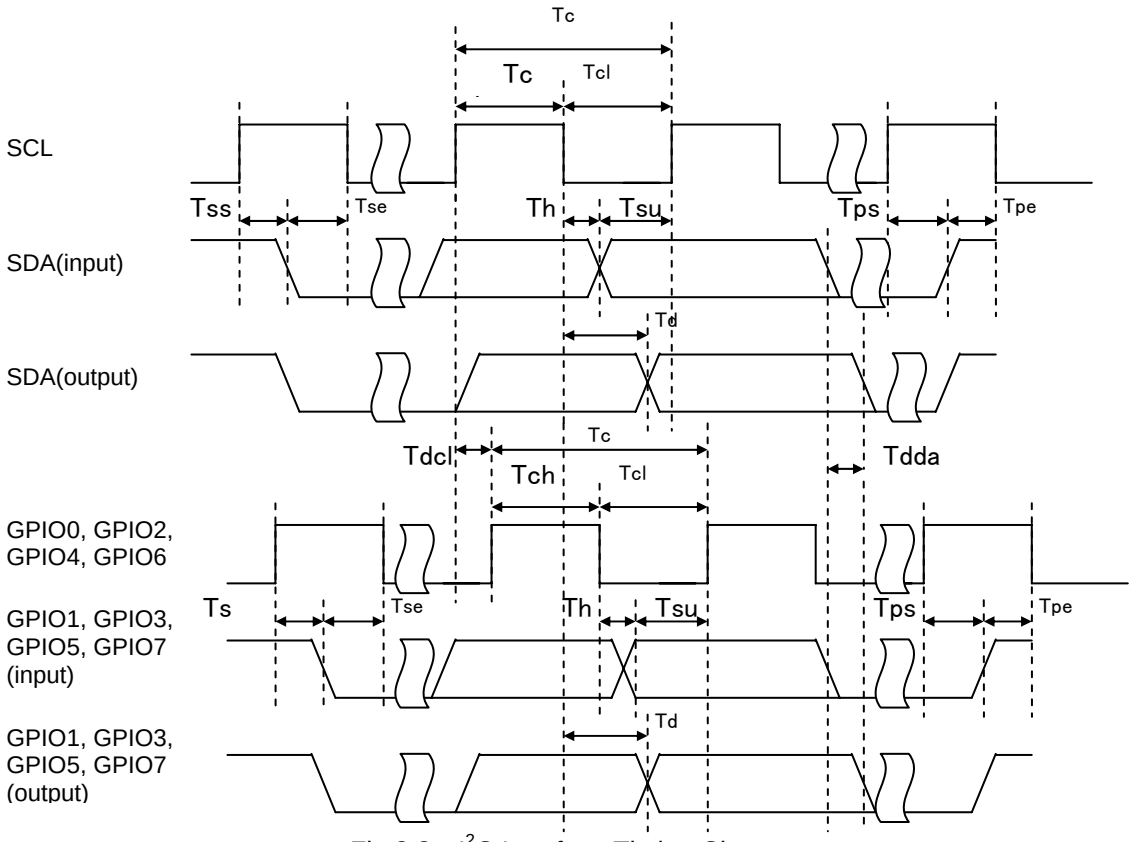


Fig.8.3 I²C Interface Timing Chart

Table 8.3 I²C Interface Timing Spec.

Ta = -40 to +105 °C, HV_{DD},HV_{DD1},HV_{DD4} = 2.4 to 3.6 V, LV_{DD} = 1.65 to 1.95 V, V_{SS} = 0 V, CL = 30 pF (Output)

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	fc	—	—	10^9/(Tc*Ts) ※1,4	Hz
SCL clock cycle time	Tc	25 ※3,4	—	—	Ts※1
SCL clock pulse width (High)	Tch	10	—	—	Ts※1
SCL clock pulse width (Low)	Tcl	15 ※3,4	—	—	Ts※1
SDA input setup time	Tsu	0	—	—	ns
SDA input hold time	Th	0	—	—	ns
SDA output delay time	Td	10	—	※2,3	Ts※1
START condition start time	Tss	5	—	—	Ts※1
START condition end time	Tse	5	—	—	Ts※1
STOP condition start time	Tps	5	—	—	Ts※1
STOP condition end time	Tpe	5	—	—	Ts※1
SCL to GPIO delay time	Tdcl	5	—	6 ※3	Ts※1
SDA(input) to GPIO(output) delay time GPIO(input) to SDA(output) delay time	Tdda	5	—	6 ※3	Ts※1

*1 Ts: CLKIN clock cycle time (Example: Ts=40ns if f=25MHz)
*2 This numeric value can be adjusted up to 4us depending on the set value of I2C HOLD COUNTER [041Ch].
*3 This numeric value is set, assuming that the rising time of the external bus is within 1Ts (40ns if f=25MHz). Note that this numeric value increases if the rising time of the external bus exceeds 1Ts depending on the load capacity and pull-up resistance value.
Reference) At f=25MHz, the numeric value will increase approximately +10Ts when the rising time is 400ns and approximately +25Ts when it is 1000ns.
*4 This numeric value is set, assuming that the set value of I2C HOLD CONUTER [041Ch] is set to "0". Note that this numeric value increases (the clock frequency decreases) as the output delay time increases depending on the set value of I2C HOLD COUNTER.
Reference) At f=25MHz, the numeric value will increase approximately +10Ts when the set value of I2C HOLD COUNTER is 0Ah (approximately 400ns).

8.4 Reset

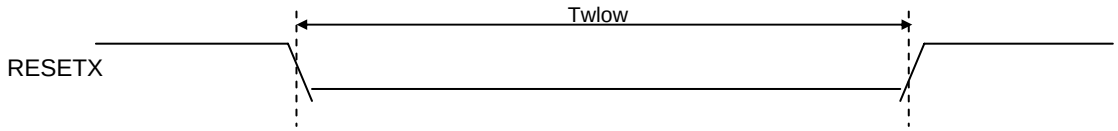


Fig.8.4 Reset Timing Chart

Table 8.4 Reset Timing Spec.

Ta = -40 to +105 °C, HV_{DD},HV_{DD1},HV_{DD4} = 2.4 to 3.6 V, LV_{DD} = 1.65 to 1.95 V, V_{SS} = 0 V, CL = 30 pF (Output)

Item	Symbol	Min.	Typ.	Max.	Unit
Reset pulse width	Twlow	100	—	—	ns

9. APPLICATION DIAGRAM

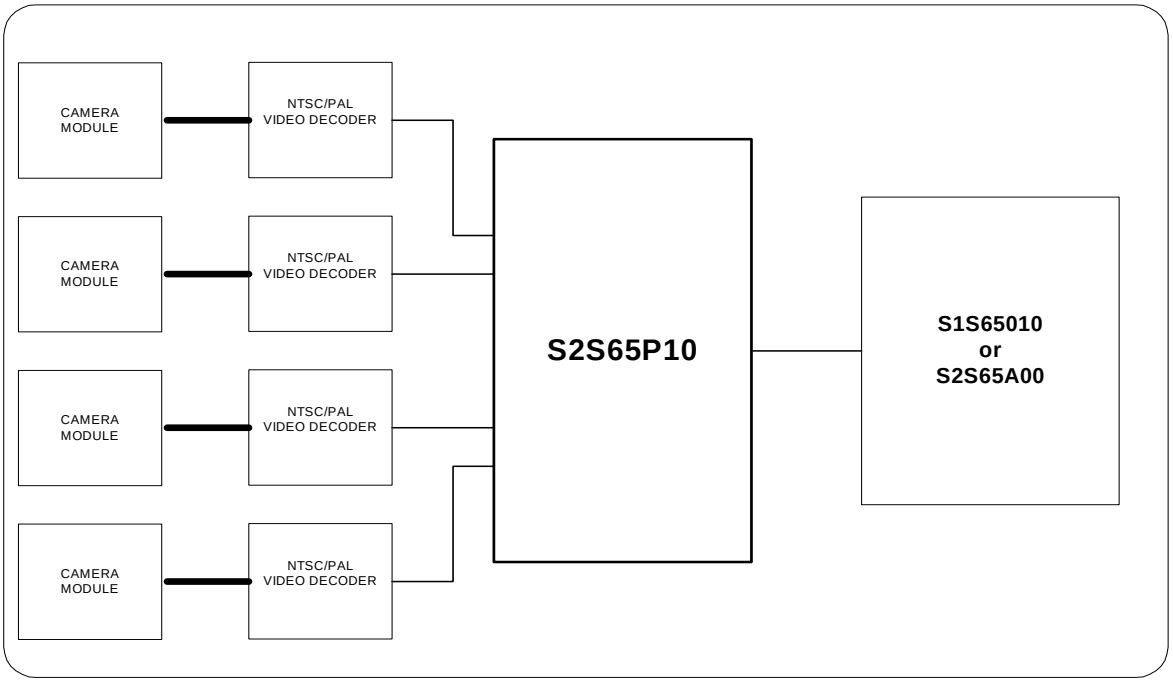


Fig.9.1 System Example 1

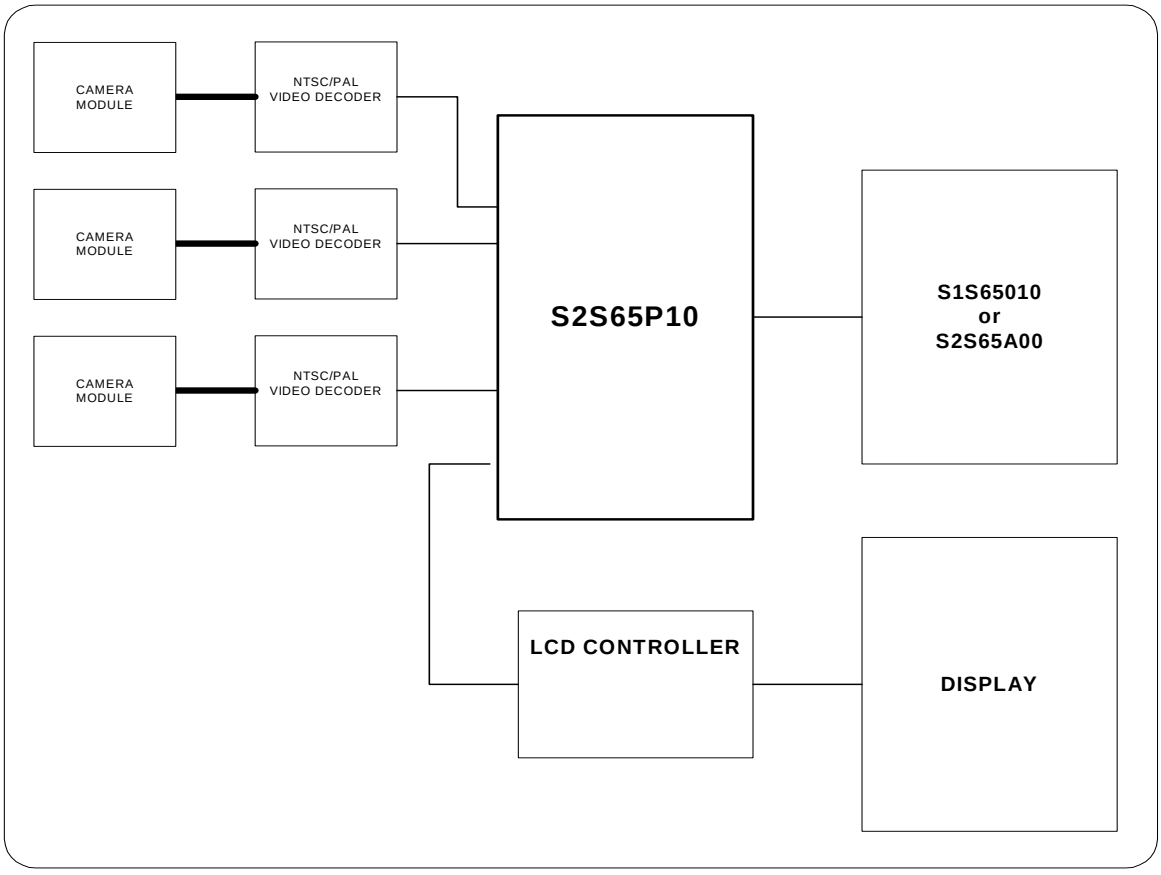
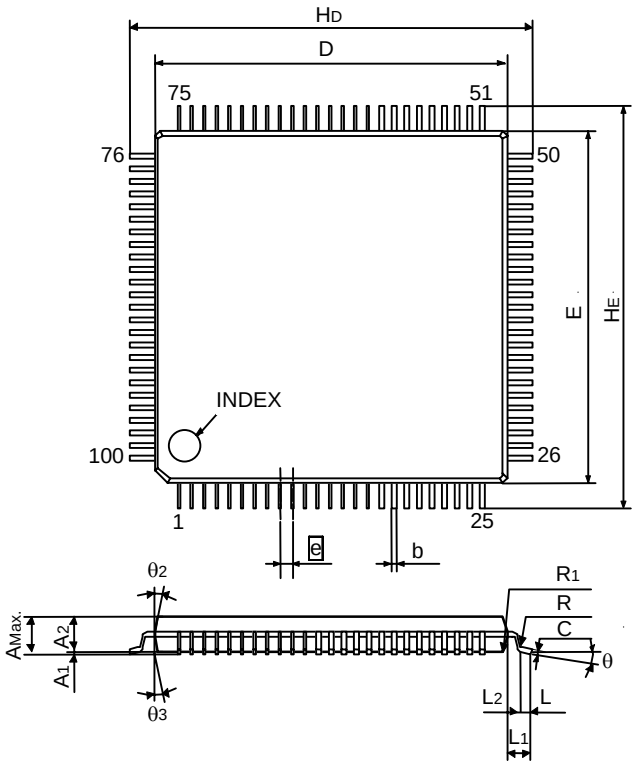


Fig.9.2 System Example 2

10. MECHANICAL DIMENSIONS

* Any information of this manual is subject to change without prior notice according to the continual improvement.



Symbol	Dimension in Milimeters		
	Min.	Nom.	Max.
E	13.9	14	14.1
D	13.9	14	14.1
A			1.7
A_1		0.1	
A_2	1.3	1.4	1.5
e		0.5	
b	0.13	0.18	0.28
C	0.1	0.125	0.175
θ	0°		10°
L	0.3	0.5	0.7
L_1		1	
L_2		0.5	
H_E	15.7	16	16.3
H_D	15.7	16	16.3
θ_2		12°	
θ_3		12°	
R		0.2	
R_1		0.2	

Fig.10.1 QFP15-100pin PACKAGE

REVISION HISTORY

Attachment-1

Rev. No.	Date	Page	Type	Description of revisions (including contents of previous revisions) and reasons		
Rev 0.1	2007/04/06	All pages	New	New establishment		
Rev 1.0	2007/07/27	All pages	Revised	Corrected typographical errors over all; made additions.		
Rev 1.1	2011/10/05		Revised	Corrected typographical errors over all; made additions.		
		Page		Revision data	Before revision	After revision
		4. PIN DESCRIPTION				
		P.4		CH1CLK	Output Current 2mA	Output Current —
				CH1HIN CH1HOUT	Type I	Type I/O
				CH1ODD	Output Current 2mA	Output Current —
				CH2CLK	Output Current 2mA	Output Current —
				CH2HIN CH2HOUT	Type I	Type I/O
				CH2DIN[7:0] CH2DOUT[7:0]	CH2DIN[7:0]	CH2DIN[7:0] CH2DOUT[7:0]
				CH2ODD	Output Current 2mA	Output Current —
				CH3CLK	Output Current 2mA	Output Current —
				CH3ODD	Output Current 2mA	Output Current —
				CH4CLK	CH4DCLK	CH4CLK
					Output Current 2mA	Output Current —
				CH4ODD	Output Current 2mA	Output Current —
				HOUT	Video4 Horizontal Syncronaization output	Video Horizontal Syncronaization output
				ST[1:0]	Input Level LVCMOS	Input Level —
		P.5		GPIO1	GPIO1 TH_I2C_SDA	GPIO1
				GPIO3	GPIO3 TH_I2C_SDA	GPIO3
				GPIO5	GPIO5 TH_I2C_SDA	GPIO5
				GPIO7	GPIO7 TH_I2C_SDA	GPIO7
					SDAL(Data)	SDA (Data)
		P.6		Address(h) 0808	Default Value 01h	Default Value xxh
				Address(h) 0C08	Default Value 01h	Default Value xxh
				Address(h) 1008	Default Value 01h	Default Value xxh
		P.7		Address(h) 1408	Default Value 01h	Default Value xxh
				Address(h) 1820	Default Value 31Ah	Default Value xxxxh
				Address(h) 1824	Default Value 31Ah	Default Value xxxxh
				Address(h) 1828	Default Value 31Ah	Default Value xxxxh
				Address(h) 182C	Default Value 31Ah	Default Value xxxxh
				Address(h) 1830	Default Value 01h	Default Value 0Ah
				Address(h) 1834	Default Value 01h	Default Value 0Ah
		5. REGISTER MAP				
		P.12		Video output setting register	Bits[6:5]: Video Input Data Type	Bits[6:5]: Video Output Data Type
					Bit[4]: Video Input Data Format Select	Bit[4]: Video Output Data Format Select
		P.13			Bit[2]: Hsync Input Polarity	Bit[2]: Hsync Output Polarity
					Bit[1]: Vsync Input Polarity	Bit[1]: Vsync Output Polarity

		P.15		Video 3 input pull-down control register	CH3PCCTRL	SYS_CH3PCCTRL
		P.17		I^2C setting register	DA signal	SDA signal
		P.19 P.20 P.22 P.23		Video 1 input capture position setting register Video 2 input capture position setting register Video 3 input capture position setting register Video 4 input capture position setting register	Default value = 01h	Default value = 01h (CONF[1:0] = 00/10/11), 09h(CONF[1:0] = 01)
		P.26		Video 1 output X-direction length setting register	[1810h]	[1820h]
				Video 2 output X-direction length setting register	[1814h]	[1824h]
				Video 3 output X-direction length setting register	[1818h]	[1828h]
				Video 4 output X-direction length setting register	[181Ch]	[182Ch]
					Default value = 31Ah	Default value = 031Ah (CONF[1:0] = 00/01), 0320h (CONF[1:0] = 10/11)
		P.27		Video output VSYNC front porch setting register	Default value = 01h	Default value = 0Ah
					HF_O	VF[7:0]
				Video output VSYNC width setting register	VOUT_HP	VOUT_VP
					Default value = 01h	Default value = 0Ah
					VP	VP[7:0]
				Video output VSYNC back porch setting registe	HB	VB[7:0]
		P.40		GPIO pin function register	SDAL(Data)	SDA(Data)
		6. FUNCTIONAL DESCRIPTION				
		P.45		Merge Mode	four input settings	our input mode settings (SYS_CH1-4INMODE[0010h] to [001Ch])
		P.46		Table 6.1 Frame rate	Merge mode Progressive Min.[fps] —	Merge mode Progressive Min.[fps] 7.5
					(non)	*It is a value when the frame rate of the video 1-4 is equal at 30fps.
		P.47		<Video output timing>	VOUT_HT1[1810h]	VOUT_HT1[1820h]
					VOUT_HT2[1814h]	VOUT_HT2[1824h]
					VOUT_HT3[1818h]	VOUT_HT3[1828h]
					VOUT_HT4[181Ch]	VOUT_HT4[182Ch]
					VOUT_HP[1834h]	VOUT_VP[1834h]

				Fig 6.8 Video output timing	tHF	HF
		P.49		<Video input capture position>	VIN2_XSTART[0808h]	VIN2_XSTART[0C08h]
					VIN2_YSTART_O[080Ch]	VIN2_YSTART_O[0C0Ch]
					VIN2_YSTART_E[0810h]	VIN2_YSTART_E[0C10h]
					VIN3_XSTART[0808h]	VIN3_XSTART[1008h]
					VIN3_YSTART_O[080Ch]	VIN3_YSTART_O[100Ch]
					VIN3_YSTART_E[0810h]	VIN3_YSTART_E[1010h]
					VIN4_XSTART[0808h]	VIN4_XSTART[1408h]
					VIN4_YSTART_O[080Ch]	VIN4_YSTART_O[140Ch]
					VIN4_YSTART_E[0810h]	VIN4_YSTART_E[1410h]
		7. DC CHARACTERISTICS				
		P.54		Table 7.1 Absolute maximum ratings	LVDS_Vss	(non)
					HVDD3	HVDD4
				Table 7.2 Recommended Operating Conditions	Tj = -40 ～ 105℃	Tj = -40 ～ 125℃
		P.56		Table 7.3 DC characteristics	Pull-up resistor	added RESETX
		P.57			output voltage	added GPIO[7:0]
					OFF-STATE leak current	added SDA
		8. AC CHARACTERISTICS				
		P.58		Table 8.1 Video Input Interface Timing Spec.	Top	Ta
				Table 8.2 Video Output Interface Timing Spec.	Top	Ta
		P.59		Fig 8.3 I^2C Interface Timing Chart	Gpio-SCL	GPIO0, GPIO2, GPIO4, GPIO6
					Gpio-SDA	GPIO1, GPIO3, GPIO5, GPIO7
				Table 8.3 I^2C Interface Timing Spec.	Top	Ta
					Gpio-SCL	GPIO
					Gpio-SDA	GPIO
		P.60		Table 8.4 Reset Timing Spec.	Top	Ta

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