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S7R77024
PCB Design Guide

SEIKO EPSON CORPORATION

Rev.1.0

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1. DESCRIPTION

This Design Guide provides information about designing printed circuit boards using the S1R77024 Analog Front-End (called AFE) with clock generation feature dedicated to Epson's high-speed line sensors. The Guide describes the board design in general including circuit design and layout.

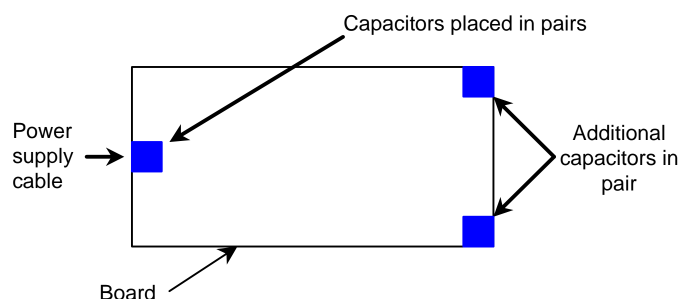
2. CIRCUIT DESIGN

To take full advantage of the performance and characteristics of the AFE, the following description will enable you to effectively design circuits.

(1) High-speed serial transfer by LVDS is available for the output of image data from the AFE.
LVDS should conform to the ANSI/TIA/EIA-644(LVDS) standard that has been regulated by TIA/EIA (Telecommunications Industry Association/Electronic Industries Alliance).

(2) We recommend separate individual designs for the digital circuit (including power supply and GND), the LVDS circuit, and the analog circuit.
The GND line on the digital circuit and the analog circuit must be connected at a single point.
See the relative topics of Section 4.2 "Layout Design" and Section 4.3 "Pattern Design".

(3) On the power supply input area of the board where the AFE will be mounted, place an electrolytic capacitor (or a tantalum capacitor) and a ceramic capacitor in pairs. For any circuit that may be created at a distance from the power supply input, place additional capacitors, also in pairs. To reduce noise in a certain frequency band, use of ceramic capacitors connected in parallel (e.g., 0.1μF, 0.01μF and 0.001μF) may be effective.
See the relevant topic in Section 8.3 "Frequency Characteristics of Capacitors".
[Recommended capacitors for the power supply input]
・Electrolytic capacitor (or tantalum capacitor): 47μF to 4.7μF
・Ceramic Capacitor: 0.1μF to 0.001μF



(4) Assign a bypass capacitor near every power supply pin.
To reduce noise in a certain frequency band, use of the ceramic capacitors connected in parallel (e.g. 0.1μF, 0.01μF and 0.001μF) may be effective.
See the relevant topic of Section 4.3.10 "Bypass Capacitor" and Section 8.3 "Frequency Characteristics of Capacitors".
[Recommended bypass capacitors]
・Ceramic Capacitor: 0.1μF to 0.001μF

2. CIRCUIT DESIGN

2.1 Digital pin

Note that some pins have built-in pull-up/pull-down resistors.
Refer to Technical Manual for details about the built-in resistors.

2.1.1 SDO, SDI, XCS, SCLK Pins

In spite of Schmidt input of the pins, waveform blunting, or other deterioration that occurred before connecting to the AFE may cause a malfunction. Therefore, adequate evaluation carried out by yourself is necessary under actual application conditions.

Attention is required regarding the waveform of clock (SCLK) since the data is latched at the rising edge of the clock. Take waveform blunting into account when designing circuits.

2.1.2 XRST pin

Refer to "System Reset" section of Technical Manual to design your circuit in a way that meets the pulse duration regulated in the specification.

2.1.3 TGCK Pin

TGCK waveform is output to the pin when TGCK is generated internally.

2.1.4 CLKIN pin

When these pins are not used (CLKINP, CLKINN Pins are used), fix them to "LOW".
See the relevant topic in Section 4. "Board Design".

2.1.5 TSTEN, TMOD Pins

Fix these pins to "Open" or "LOW".

2.1.6 CLKINP, CLKINN Pins

When these pins are not used (CLKIN Pins are used), set CLKINP = "LOW", CLKINN = "Open".
See the relevant topic in Section 4. "Board Design".

2.1.7 SNCKn, SHn Pins

If the pins are used as a port for multiple or general use, design your circuit so as not to cause a collision between input and output.

If a sensor to be plugged in has large load carrying capacity (roughly 20pF or more), it is recommended that a buffer circuit for driving be connected.

2.1.8 GPIO Pin (for multiple use)

If the pin is used as a port for multiple or general use, design your circuit so as not to cause a collision between input and output.

2.2 LVDS pin

Impedance consistency is required for the pattern connected to the pin.
See Section 4.3.8 “Impedance Consistency” for details.

2.2.1 TXSYNCP/N, TX[2:0]P/N Pins

Do not connect any other device other than connectors to the transfer line, which must be spliced straight to a pin on the receiver device. For the proper pin assignment of a connector, we recommend P/N be sandwiched by GND.

A terminating resistor must be placed near (within 7mm is recommended) the pin on the receiver device.

See the relevant topics in Section 3.3 “TXSYNCP/N, TX[2:0]P/N” and Section 4. “Board Design”.

2.3 Analog pin

Attention must be paid so that the pin is not affected by noise from digital circuits.

2.3.1 REFP, CM, REFN Pins

A capacitor should be connected to the pins to stabilize their internal behavior.
See the relevant topic in Section 4. “Board Design”.

2.3.2 CLMPLV/INN Pin

For a CCD image sensor, a capacitor should be connected to the pins so that the input signal is properly clamped inside. Place the capacitor close to the pin.

For CIS, a reference voltage level should be input.

See the relevant topic in Section 3.4 “Other External Devices”.

2.3.3 RINP, GINP, BINP Pins

A CCD image sensor should be input through AC coupling capacitor. We recommend the pins be connected to AGND through a capacitor.

See the relevant topics in Section 3.4 “Other External Devices” and Section 4. “Board Design”.

3. SELECTING DEVICES

This section describes the selection of devices that are required for designing a circuit.

For all devices you select, we recommend the smallest possible surface mounting type so as to reduce the effect of lead inductors of the device. Note first that any capacitor with high Equivalent Series Inductance (ESL) or high Equivalent Series Resistance (ESR) may cause unintended adverse effects on the originally designed functions.

Allow for the derating of each device you will select.

We recommend the devices with following characteristics. If your application requires different characteristics, you may determine adequate characteristics based on your evaluation.

- Resistance: ±1% or less
- Ceramic Capacitor: B characteristic

3.1 TXSYNCP/N, TX[2:0]P/N External Devices

Refer to “Terminating Resistors” section of Technical Manual for details about the constants.

3.2 Other External Devices

Refer to Technical Manual for details about the constants.

4. BOARD DESIGN

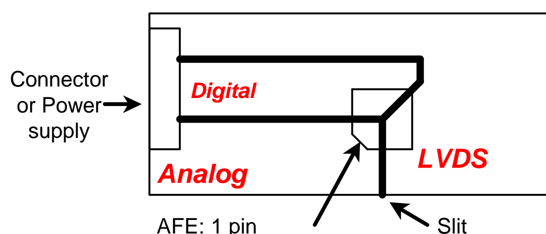
This section describes what is necessary for the board design for the AFE.
Depending on the actual application conditions, the description in this section may not be sufficient to extract adequate characteristics. Your evaluation is therefore required to determine the final design.

4.1 Layers Configuration

We recommend 4 or more layers. Flexible Print Circuit board (FPC), 2-layer board, or single-layer board is not recommended to use for the AFE.
If the components side is where the AFE is mounted, layers should be configured in order of the components side, GND layer, power supply layer, and soldering side. The uniformity of the GND layer and the power supply layer is recommended to stabilize analog characteristics.

4.2 Layout Design

Be sure to separate the digital circuit (including power supply and GND), the LVDS circuit, and the analog circuit individually at the layout design stage so as not to mix these circuits.
Note that the following figure is simply an outline image and is not recommended for use as part of your actual layout.
See the relevant topic in Section 4.3 “Pattern Design”.



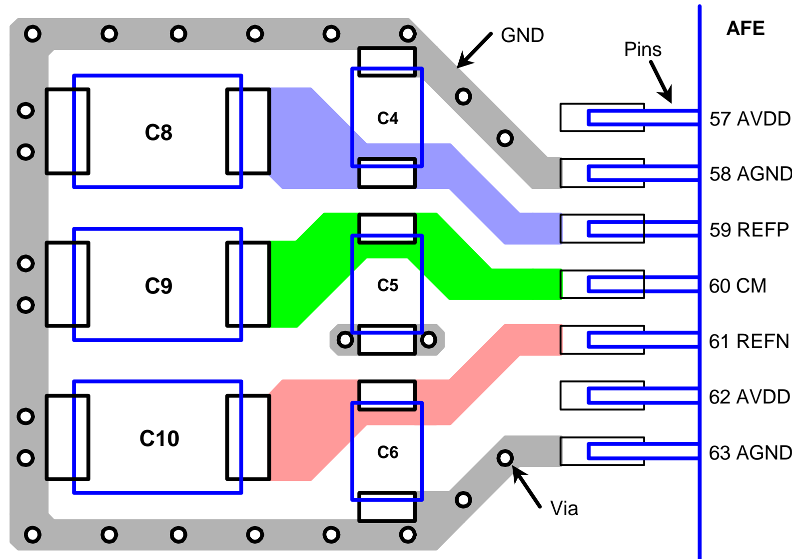
4.2.1 Priority Design

This section describes the priority order of the Digital circuit, the LVDS circuit and the Analog circuit for design purposes.
Proceed with your design according to the order. Parts described in the order include pins and peripheral devices connected to the pins.

No.1 REFP, CM, REFN
No.2 RINP, GINP, BINP
No.3 CLMPLV/INN
No.4 Power supply, GND
No.5 LVDS (TXSYNCP/N, TX[2:0]P/N)

4.2.2 Layout for REFP, CM, REFN

An example of layout and pattern of external devices for REFP, CM, REFN is shown below.
We recommend the layout be drafted on the same side as AFE. Each part number in the figure refers to that described in Technical Manual.

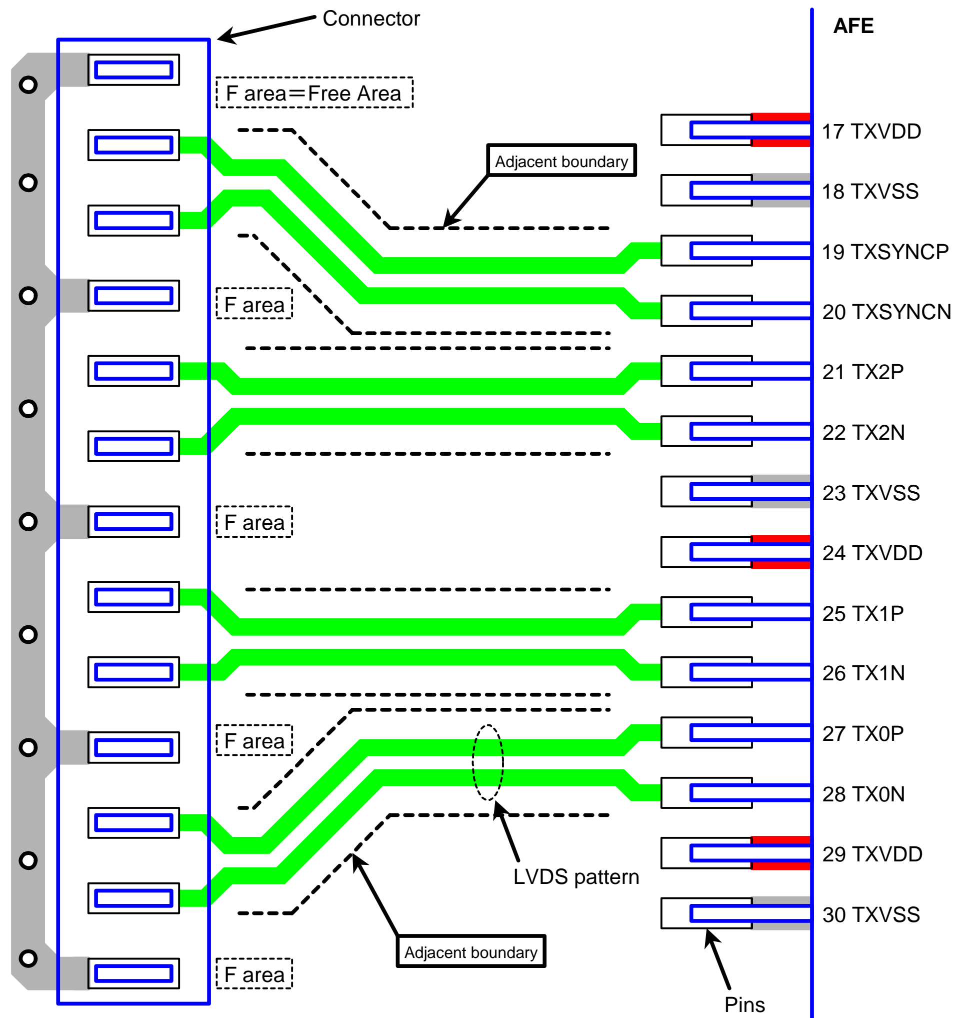


4.2.3 Layout for TXSYNCP/N, TX[2:0]P/N

An example of layout and pattern for TXSYNCP/N, TX[2:0]P/N is shown below.
Our suggestion is as follows.

(1) The layout for the AFE and connector should be drafted on the same side.
(2) See Section 4.3 “Pattern Design” for LVDS pattern.
(3) “Adjacent boundary” refers to a marginal distance from an adjacent LVDS pattern, the gap that should have the same or larger dimensions as described in Section 4.3.8 “Impedance Consistency”.
(4) For “F area”, free space (no conductor) is recommended.
Therefore, connect TXVDD and TXVSS, from inside the AFE, to a bypass capacitor on the soldering side using (2 or more) via holes for a pair of the power supply pins.

(5) For the proper pin assignment of the connector, place GND between a pair and another pair of LVDS. See Section 5.1 “System Connection” for the connection of GND and TXVSS pin on the connector.

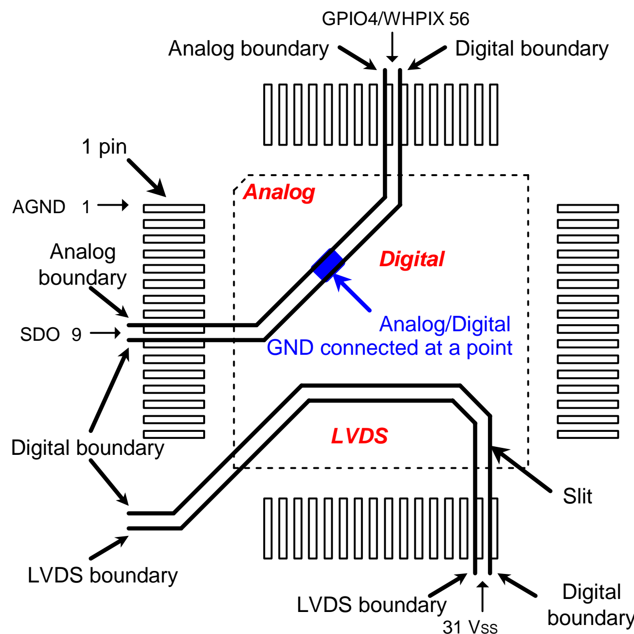


4.3 Pattern Design

Be sure to separate every pattern individually for the digital circuit (including power supply and GND), the LVDS circuit, and the analog circuit.

The GND line on digital and analog must be connected at a single point on the soldering side just beneath the AFE. Into the boundary of separation, put a slit with a width with of 0.5mm or more at the same position of all layers into the boundary of separation.

An example of separation by the slit is shown below. The same positions are applied to all layers.



4.3.1 Basic Wiring

Basic wiring for general patterns is described below.

(1) Be sure to configure wiring for all patterns (such as signal, the power supply and GND) properly so as not to form a loop.
(2) Configure the wiring to take the shortest current path.
(3) Create an adjacent (paralleled) GND pattern (GND shield) to the digital circuit, the analog circuit and the clock related circuit.
(4) Create a GND pattern for free space on the surface layer.
(5) Be sure that the GND pattern described in (3) and (4) does not float.
(6) Do not create unnecessary beta patterns.
(7) Connect the bypass capacitors in the order of the power supply (GND), capacitor, and pin.
(8) Do not add wiring for other signals in the area, for all layers, or for lead type devices (such as a transformer, coil and relay).
(9) Do not add wiring for other signals in the area for surface mounting devices.
(10) Do not place wiring for a clock pattern near other signals or the power supply.
(11) Patterns other than the interlayer connection of the power supply or GND should be wired on the same side whenever possible instead of using via holes.

4.3.2 Pattern Length

The use of via holes should best be avoided for clock related digital patterns. Take the shortest line for the connection. Adopt general basic wiring procedures for other patterns.

See section 4.2.5 “TXSYNCP/N, TX[2:0]P/N Layout” and Section 4.3.8 “Impedance Consistency” for the differential signal pattern.

In general, take the shortest line for wiring on all analog patterns.

Wiring in the same length is required for patterns connected to the following pins.

(1) RINP, GINP, BINP
(2) REFP, CM, REFN

4.3.3 Pattern Width

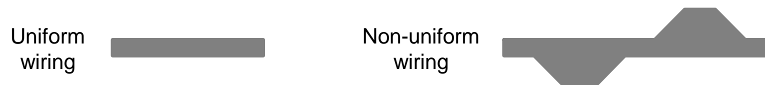
The pattern width of 0.5mm to 1mm is recommended for clock related patterns.

See Section 4.3.8 “Impedance Consistency” for the differential signal pattern.

The pattern width of 0.5mm to 1mm is recommended for analog patterns.

Configure uniform wiring with the uniform width whenever possible for the same pattern.

Note that the extreme wide wiring for patterns other than the power supply and GND may be subject to the adverse effects of noise.



4.3.4 Pattern Bending

Bending by right angles (90°) or acute angles must be avoided for all patterns.

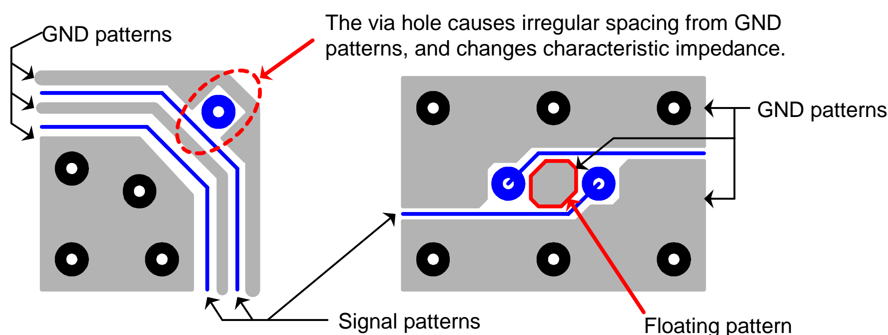
Attention is required also for inner layers including the power supply and GND.

Allow bending to occur only by 45° or in the shape of an arc.

4.3.5 GND Shield

Signal patterns and GND patterns should be spaced out regularly. Via holes except for GND cause irregular spacing, which changes the characteristic impedance of signal patterns.

Place uniformly spaced via holes on GND patterns. Because more widely spaced via holes may cause plane resonance, the smallest possible spacing of the via holes is ideal. If a pattern created as GND shield does not have GND via holes, it may grow to a floating pattern and cause unexpected noise.



4.3.6 Interlayer Connection

Analog patterns should be wired on the same side whenever possible instead of using via holes.

LVDS patterns should be wired on the same side instead of using via holes.

General, basic wiring is allowed for digital patterns, but clock related patterns should be wired on the same side whenever possible instead of using via holes.

Power supply and GND patterns should be connected interlayer using multiple via holes.

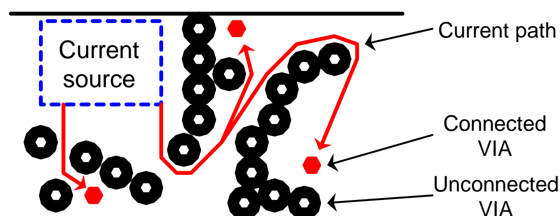
4.3.7 Via Holes and Through Holes

In general, via holes and through holes lead to reduced board reliability.

Allowable current per via hole as well as reliability and inductance should be counted for power and GND patterns (including connection to bypass capacitors) to assign the correct number of via holes.

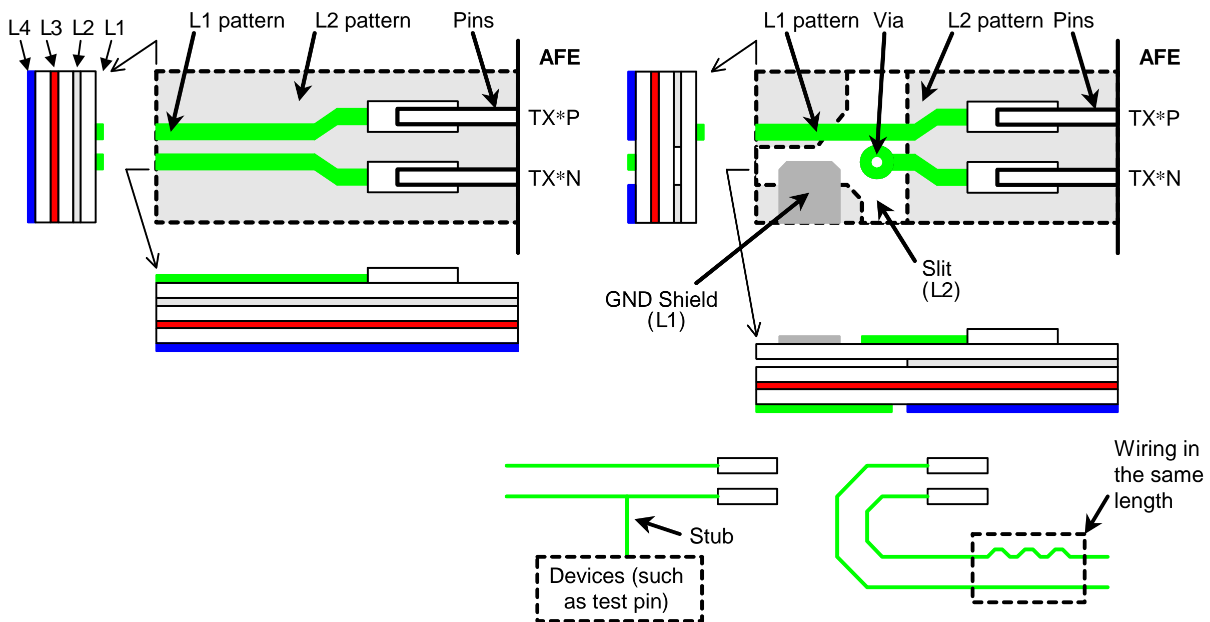
The impedance of a pattern becomes discontinuous by passing through a via hole (or through hole), causing a break in the impedance consistency. Therefore, do not place the via holes on differential signal patterns.

Inappropriate alignment of via holes (or through holes) on a power supply or GND pattern may incur blocking of a current path or uneven current density of the pattern.

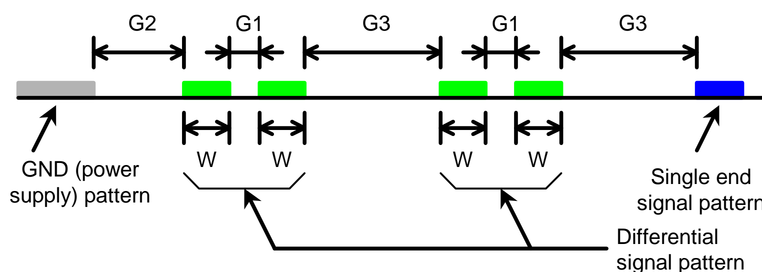


4.3.8 Impedance Consistency

Impedance consistency (with GND) is required for differential signal (LVDS) handled by the AFE.
50 Ω (single end) ±5% is recommended for the characteristic impedance of a differential signal pattern.
The impedance consistency is generally attained by matching the impedance among a differential signal pattern, P/N and a beta pattern created just beneath them. So the impedance for a differential signal pattern may become inconsistent (discontinuous) triggered by adjacent patterns (such as a signal or GND shield) or a beta pattern just beneath the differential signal pattern. Stubs, wiring in the same length, via holes or slits can cause the inconsistency.



The following dimensional requirement should be met to maintain the impedance consistency. Select either the gap between fixed potential adjacent boundaries (G2) or the gap between fluctuating potential adjacent boundaries (G3) depending on an adjacent pattern type. The fixed potential adjacency refers to the power supply or GND, whereas the fluctuating potential adjacency refers to the power exhibiting signal patterns or high-frequency components (such as proximity to a power supply circuit).



W: Width of a differential signal pattern

G1: Gap between differential signal patterns

G2: Gap between fixed potential adjacent boundaries

G3: Gap between fluctuating potential adjacent boundaries

[Dimensional requirement]
- W>G1
- G2=2xW (W>G1)
- G3=3xW (W>G1)

4.3.9 Unwanted Emission Noise

Appropriate board design is the basic factor to reduce unwanted emission noise (EMI).
A board configured for noise reduction implies it has electrically stable characteristics.

(1) A pattern design allowing for the current path of charge supply and return is effective.
Because the current path is a matter that should be reviewed totally as a system, the pin assignment of cable or other components is also important

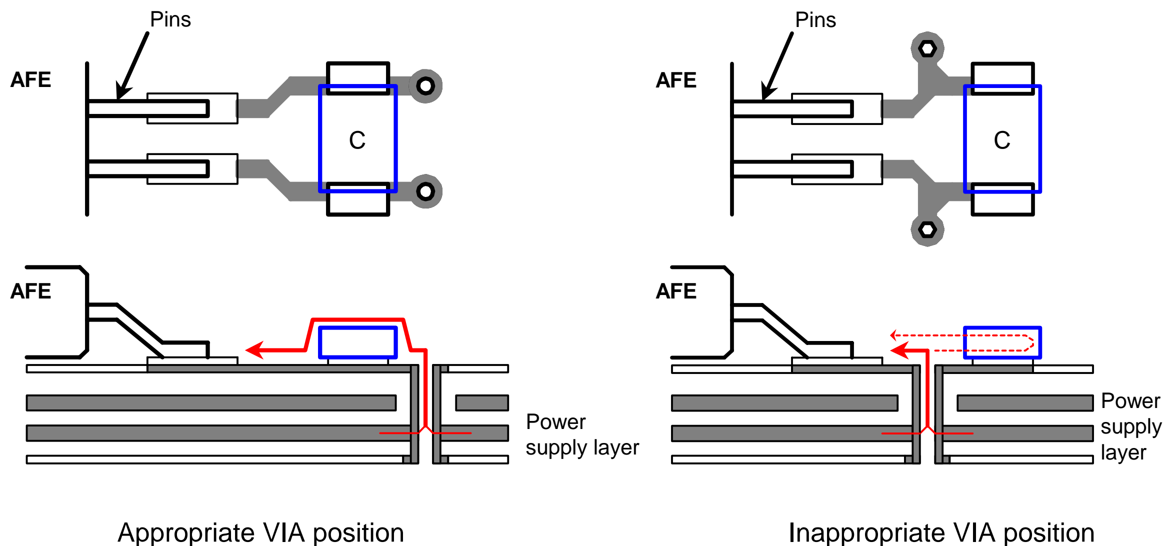
(2) A design that takes into account the electric field that is generated by movement of charges is also effective.
Using GND shield to absorb unwanted emission (non-bonding electric field), or maintaining impedance consistency to block disparity in the electric field can reduce unwanted emissions.

(3) A design that takes into account the intensity of electric field and the electric flux line is also effective.
Unwanted emissions can be reduced from a pattern on the board edge by making the board's periphery into GND beta pattern (also by spacing out via holes). Similarly, unwanted emissions from high-frequency patterns or devices running at high speeds can be reduced by placing them near the center of the board.

4.3.10 Bypass Capacitor

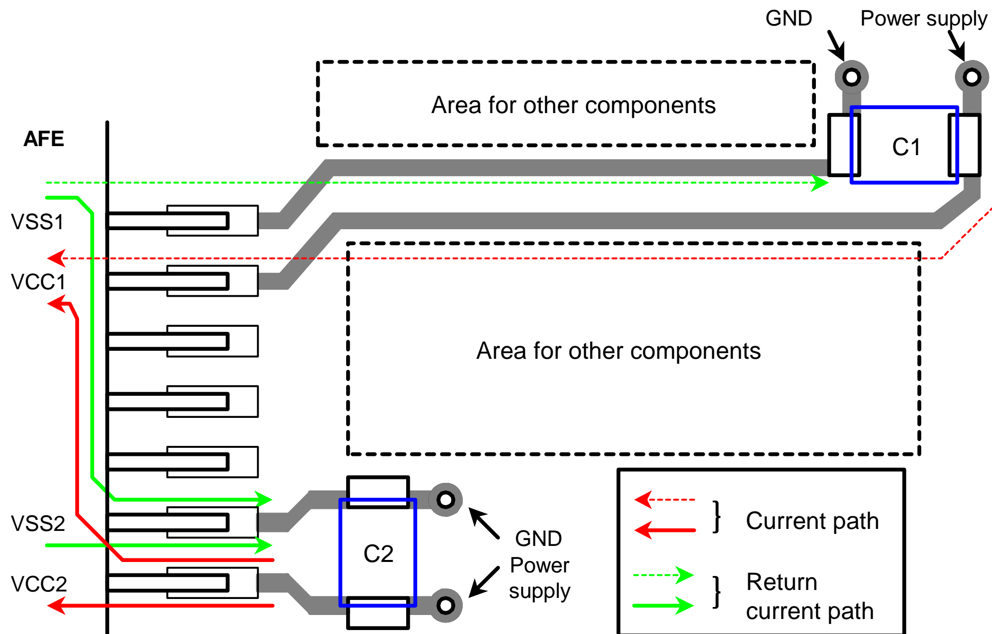
Since bypass capacitors are responsible for the supply of effective current, it is necessary to understand the following in order for your design to enable the stable behavior of the bypass capacitors.

(1) The current path depends on the position of via holes (VIA). It implies that inappropriate placement of via holes (VIA) disable the function of a bypass capacitor.



Appropriate VIA position   Inappropriate VIA position

(2) The distance of a capacitor from pins may not only disable the function of the bypass capacitor but also cause deterioration of its characteristics.
In an example shown below, the current path from C2 has priority over that from C1, which is positioned further from the pins. Internal circuits connected to C1 as well as internal circuits between VCC1 to VCC2 may exhibit characteristic deterioration due to unexpected current.



5. OTHERS

5.1 System Connections

Refer to the description in this Guide for GND related connections (such as shields and connectors) required for your system design. It will be beneficial for you to comply with safety standards or legal restrictions of your country.

5.1.1 Differential Signal Connector

Pin assignment should be optimized depending on the connector being used.

(1) A surface mounting type is recommended for differential signal connectors. However, since the LVDS Standard is required to be met by the system as a whole, it should finally depend on your verification in the actual application conditions.

(2) For the proper pin assignment of the connector, place GND between a pair and another pair of differential signals (LVDS). See Section 5.1 “System Connection” for the connection of GND and TXVSS pin on a connector.

(3) Assign GND to pins on both end of the connector (e.g. for FFC).

(4) Assign GND to unused pins.

(5) If a connector has different length terminal leads (such as right-angle 2-line type), be sure to connect the pair pattern to terminals with the same length.

5.1.2 Cables

To stabilize a board’s behavior, attention is also required for connection cables.

Note that if you shield a cable to reduce unwanted emission noise from the cable, the LVDS standard must be met under the actual application conditions (for the system as a whole).

Ideally, you will allow for the return current to assign GND depending on a signal type (input/output or different driving capabilities) and the power supply system.

Note that ribbon cables are not recommended.

5.2 FG

If a hole used to fix the AFE-mounted board is positioned near a LVDS or Analog circuit, the whole system may be affected by noise when part of a fitted screw comes in contact with chassis or other FG (Frame Ground).

If the AFE-mounted board is shielded by metal to combat unwanted emission noise, the system may also be affected by noise when the shield comes in contact with FG.

Take into account the system as a whole to handle the FG properly.

5.3 ESD

We conduct a test for anti-electrostatic destruction to check the destructive resistant properties of a semiconductor.

The test to check functions and behaviors should be conducted on your side under actual application conditions.

5.4 Thermal Conductance

Maintain the constant ambient temperature during operation of the AFE.

Configure your design to allow the shortest thermal conductance path. You may assume the total thermal resistance of a board based on its pattern and layout. The optimized thermal conductance enables effective heat release, leading to the electrical stability, eventually achieving characteristic improvement.

6. TERMINOLOGY

A

AFE	An acronym standing for Analog Front End. The AFE referred in this Guide is that designed for a scanner system.
AGND	Refers to the ground for analog circuits.
AVDD	Refers to the power supply for analog circuits.

C

CCD	Charge Coupled Device.
CIS	Contact Image Sensor. Also called the Line Sequential Output Sensor. CIS uses LED as a light source, and is characterized by lower power consumption than CCD. CMOS Image Sensor is its third name.

E

EMI	Electro Magnetic Interference, a general term referring to emission phenomena from electronic devices including electromagnetic obstruction and interference.
ESD	Electro-Static Discharge

F

FG	Frame Ground

G

GND	Refers to the ground (including AGND, VSS, TXVSS).

L

LVDS	Low Voltage Differential Signaling (LVDS Interface)

P

PCB	Printed Circuit Board

T

TXVDD	Refers to the power supply for LVDS transmission circuits.
TXVSS	Refers to the ground for LVDS transmission circuits.

V

VDD	Refers to the power supply for digital circuits.
VIA	See the description of Via Hole.
VSS	Refers to ground for digital circuits.

A

Term	Description
Impedance Consistency	To match impedance between output and input on a wiring pattern.

KA

Term	Description
High Frequency Pattern	A wiring pattern for high-frequency signal, higher than a few MHz.

SA

Term	Description
Single End	A data transmission method using a single signal wire.
Skew	Delay in timing affected by e.g. a wiring pattern.
Stub	A stubbed pattern derived from a main wiring pattern.
Slit	An area insulated from electricity and has no copper laminate.
Through Hole	A hole through layers to interconnect the layers for conduction by soldering device leads inserted into the hole.
Ceramic Capacitor	Useful for various applications including denoising and the charge supply if proper characteristics are selected depending on the application.

TA

Term	Description
Tantalum Capacitor	Known for its superior characteristics but also as typical failure mode of a short circuit. Even for a model with a built-in fuse, the short circuit leads to breaking. Therefore, the Tantalum Capacitor should be handled with care.
Derating	The term refers to use of any product with a lower load than the rated value, for the purpose of improving its reliability.
Electrolytic Capacitor	Known for its superior characteristics, which, with its characteristics and life, depend on temperature. Its life is shortened by half with a 10°C rise in temperature according to Arrhenius law.

HA

Term	Description
Via Hole	A through hole only for interconnecting layers.
Surface Layer	Refers to components side or soldering side.
Unwanted Emission Noise	High-frequency noise emitted in addition to primary signal.
Floating	Refers to a pattern electrically unstable (floating)
Beta Pattern	A pattern (area) created with fixed dimensions.

RA

Term	Description
Lead Inductor	The inductance existing in the lead of a lead type device.

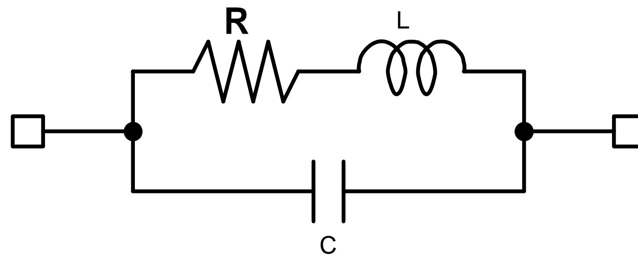
7. TECHNICAL INFORMATION

To find and update technical information related to the AFE, visit the following URL.

[URL] http://www.epsondevice.com/semicon/index.html
[Analog Front End (AFE)] → [AFE Users Site]

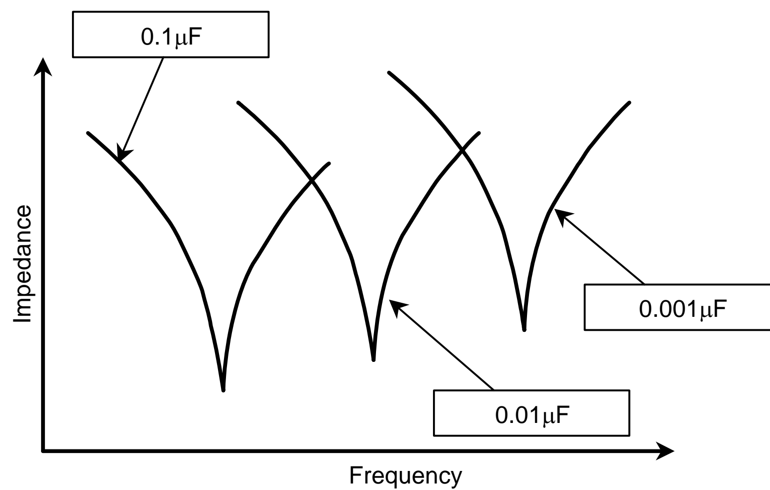
8. APPENDIX

8.1 Equivalent circuit of a resistor

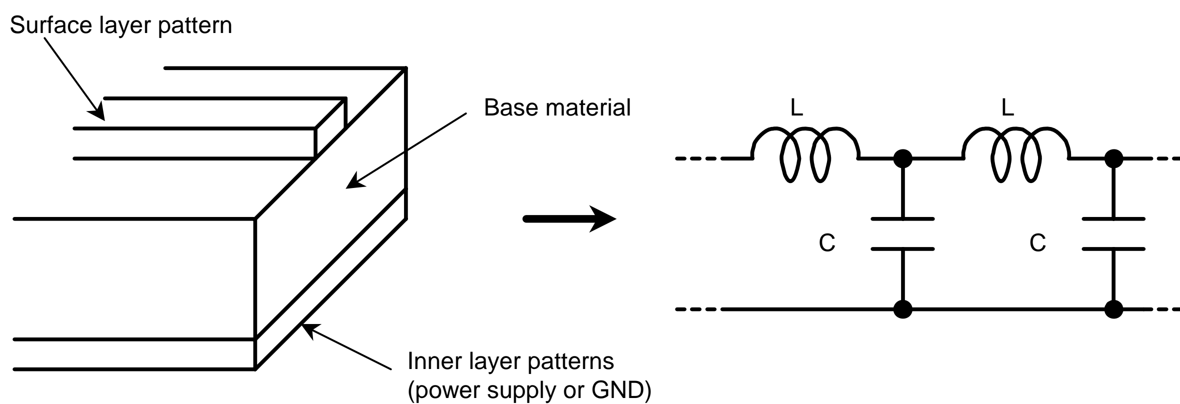


8.2 Equivalent circuit of a capacitor

8.3 Equivalent circuit of a capacitor



8.4 Equivalent circuit of patterns



9. REVISION HISTORY

Rev	Rev Date	Description of revisions
1.0	2007/10/03	First version released.

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