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S1R77022
PCB Design Guide

SEIKO EPSON CORPORATION

Rev.1.0

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1. DESCRIPTION

This Design Guide has been issued for designing the printed circuit boards using the S1R77022 analog front-end ICs (called the AFE) dedicate to Epson's high-speed line sensors. This Guide explains the general circuit board design including circuit design and layout.

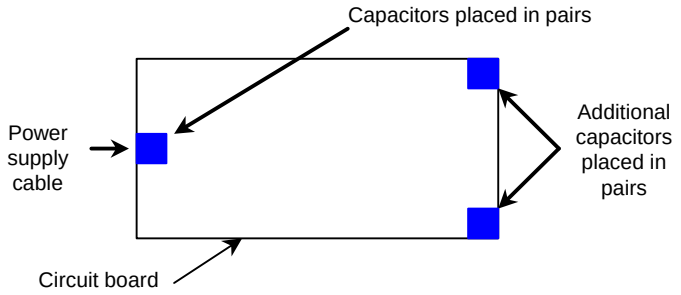
2. CIRCUIT DESIGN

To maximize the performance and characteristics of this AFE, the following points should be considered in the circuit design.

(1) This AFE allows high-speed image data transmission using the low-voltage differential signaling (LVDS) system.
The LVDS standard has been established by the TIA/EIA (The US Telecommunications Industries Association and Electronics Industries Association), and the ANSI/TIA/EIA-644 (LVDS) standards must be conformed.

(2) We recommend the separate design of digital circuit (including the power supply and GND circuits), LVDS circuit, RSDS circuit, and analog circuit.
The digital circuit and analog circuit must be grounded at a single point.
Related items: See Section 4.2 "Designing the Circuit Layout" and Section 4.3 "Designing the Circuit Patterns".

(3) In the power input section of the PC board where the AFE is mounted, place an electrolytic capacitor (or a tantalum capacitor) and a ceramic capacitor in pairs. If it is expected to locate a circuit away from the power input section, place the capacitors also in pairs. To reduce noise in a certain frequency band, the parallel connection of ceramic capacitors (e.g., 0.1µF, 0.01µF and 0.001µF) may be effective.
Related items: See Section 8.3 "Frequency Characteristics of Capacitors".
[Capacitors recommended for power supply input]
・Electrolytic capacitor (or tantalum capacitor): 47µF to 4.7µF
・Ceramic capacitor: 0.1µF to 0.001µF



(4) Install bypass capacitors close to all power pins.
The parallel connection of ceramic capacitors (such as 0.1µF, 0.01µF and 0.001µF capacitors) may be effective to reduce noise in a certain frequency band.
Related items: See Section 4.3.10 "Bypass Capacitors" and Section 8.3 "Frequency Characteristics of Capacitors".
[Recommended bypass capacitors]
・Ceramic capacitor: 0.1µF to 0.001µF

2. CIRCUIT DESIGN

2.1 Digital Pins

Note that some pins contain pull-down resistors.
For the built-in resistors, refer to the Technical Manual.

2.1.1 CK1 and CK2 pins

Signals of these pins are required to use as clock signals similar to the signal connected to the ADCK pin in certain clock frequencies. Also, the circuit pattern layout should be considered to eliminate a noise to the LPF pin.
Related items: See Chapter 4 “Designing the Circuit Boards”.

2.1.2 ADCK pin

The circuit pattern layout should be considered to eliminate a noise to the LPF pin.
Set this pin to logical “LOW” if not used.
Related items: See Chapter 4 “Designing the Circuit Boards”.

2.1.3 LPF pin

The constant of an external resistor needs to be changed according to the selected operation mode of input clocks (ADCK, RXADCKP/N).
The constant is fixed for the external capacitor.
Related items: See Section 3.1 “External LPF device” and Section 4 “Designing the Circuit Boards”.

2.1.4 CLMP pin

The circuit pattern layout should be considered to eliminate a noise to the LPF pin.
Related items: See Chapter 4 “Designing the Circuit Boards”.

2.1.5 TSTEN pin

The TSTEN pin must be fixed to “Open” or logical “LOW”.

2.1.6 TMOD pin

Set the serial access cycle in combination with the ID pin.
If the TMOD pin is fixed to logical “LOW”, 17 access cycles are set. If fixed to logical “HIGH”, 16 access cycles are set.
Related items: See “Serial interface” and “ID pin” section of the Technical Manual.

2.1.7 XRST pin

The circuit must be designed to have the pulse width that has been specified in “System Reset” section of the Technical Manual.

2.1.8 ID pin

The chip identification needs to be set to identify the serial access to this AFE IC. The ID pin must be fixed to logical “HIGH” or “LOW”. Set the chip ID selection bits for serial access according to this setting.

If you have set 16 access cycles by combination with TMOD pin, fix the ID pin to logical LOW (to disable the identification).

Related items: See “Serial interface” and “TMOD pin” section of the Technical Manual.

2.1.9 SDO, SDI, XCS, and SCLK pins

These pins configure the Schmidt input, and the waveform blunting or attenuation occurring before connection to the AFE IC can cause a malfunction. The adequate circuit evaluation is required under actual application conditions.

As the data is latched at the rising edge of SCLK clock, carefully check the waveforms of this SCLK clock. You should consider the waveform attenuation during your circuit design.

2.2 RSDS pin

Match the impedance of signals connected to this pin.

For details, see Section 4.3.8 “Impedance matching”.

2.2.1 RXADCKP/N pin

Set the RXADCKP pin to logical LOW and RXADCKN pin to logical HIGH if not used.

Do not connect any device except for a connecter or a terminating resistor because a straight signal transfer line must be connected from the device terminal of the transmitter. We recommend to jumper between those P and N pins by grounding for proper pin assignment of a connector.

A terminating resistor must be placed close to the pin (within 7 mm).

Related items: See Section 3.2 “External Device of RXADCKP/N pin” and Section 4 “Designing the Circuit Boards”.

2.3 LVDS pin

Match the impedance of signals connected to this pin.

For details, see Section 4.3.8 “Impedance matching”.

2.3.1 TXSYNCP/N and TX[4:0]P/N pins

As a straight signal transfer line must be connected to the device pin of the receiver, do not connect any device except for a connector to the line. We recommend to jumper between those P and N pins by grounding for proper pin assignment of a connector.

A terminating resistor must be placed close (within 7 mm is recommended) to the device pin of the receiver.

Related items: See Section 3.3 “External devices of TXSYNCP/N and TX[4:0]P/N pins” and Chapter 4 “Designing the Circuit Boards”.

2.4 Analog Pins

The analog signal pins must be protected from noise insertion from digital circuit.

2.4.1 REFN and REFP pins

A capacitor should be connected to the pins to stabilize their internal behavior.
Related items: See Chapter 4 “Designing the Circuit Boards”.

2.4.2 CM1 and CM2 pins

The CM1 and CM2 pins must be connected to an external circuit in a position close to those pins.
A capacitor should be connected to the pins to stabilize their internal behavior.
Related items: See Chapter 4 “Designing the Circuit Boards”.

2.4.3 CLMPLV/INN pin

If a CCD image sensor is used, a capacitor should be connected to the pins so that the input signals are properly clamped inside of the system circuit. Place the capacitor close to the pin.
The input at reference voltage level is required in the CIS mode.
Related items: See Section 3.4 “Other External Devices”.

2.4.4 RINP1/2, GINP1/2, and BINP1/2 pins

The CCD image sensor signals should be input through AC coupling capacitor. Unused pins are recommended to ground to the AGND pin via capacitors.
Related items: See Section 3.4 “Other External Devices” and Chapter 4 “Designing the Circuit Boards”.

2.4.5 T[R,G,B]P/N pins

A capacitor should be connected to those pins to stabilize their internal behavior. The customer should also evaluate and use the AGND pin for circuit grounding as it may improve the characteristics in certain applications.
Related items: Refer to the Technical Manual.

3. SELECTING DEVICES

This chapter explains how to select devices that are required for circuit design.

In principle, you should select the smallest possible surface-mounting devices in order to minimize the effect of device lead inductance. Especially, the capacitors having the minimum equivalent series resistance (ESR) or equivalent series inductance (ESL) should be used. If the ESR or ESL is high, those capacitors may not provide the intended functions.

The derating of each device should also be considered during device selection.

The following shows the recommended device characteristics. If your application requires different characteristics, you may determine adequate characteristics based on your evaluation.

- Resistors: ±1% or less
- Ceramic capacitor: B-characteristics

3.1 External LPF devices

For details of constants, refer to “External devices” section of the Technical Manual.

3.2 External Devices of RXADCKP/N pins

For details of constants, refer to “Terminating resistance” section of the Technical Manual.

3.3 External devices of TXSYNCP/N and TX[4:0]P/N pins

For details of constants, refer to “Terminating resistance” section of the Technical Manual.

3.4 Other external devices

For details of constants, refer to the Technical Manual.

4. DESIGNING THE CIRCUIT BOARDS

This chapter provides the basic information that is required for the circuit board design using this AFE.

Depending on the conditions of actual application, our description may not be sufficient to extract adequate characteristics. Your evaluation is required to determine the final design.

4.1 Configuration of layers

A circuit board consisting of 4 or more layers is recommended to design. Flexible printed circuit (FPC) boards, dual-layer boards, and single-layer boards are NOT recommended to design.

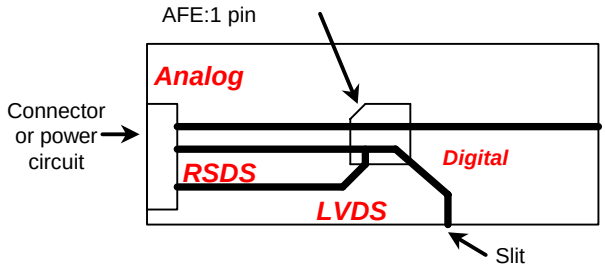
If the components side is where the AFE is mounted, layers should be configured in the order of components side, GND layer, power supply layer, and soldering side. The uniformity of the GND layer and power supply layer is recommended to stabilize analog circuit characteristics.

4.2 Layout design

The separate design should be used for the digital circuit (including power supply and GND circuits), LVDS circuit, RSDS circuit, and analog circuit not to mix them in a closed area. If the RXADCKP/N pin input (RSDS circuit) is not used, the LVDS circuit should be formed with TX_VDD (TX_VSS) and RX_VDD (RX_VSS) pins and those pins should be powered from the same power supply.

Note that the following figure is just an outline image and not recommended for your actual layout.

Related items: See Section 4.3 “Designing the Circuit Patterns”.



4.2.1 Design priority

The following defines the priority of digital, LVDS, RSDS and analog circuit design.

You must proceed the circuit design in this order. Parts described in the order include pins and peripheral devices connected to the pins.

No.1 REFP, REFN, CM1, CM2
No.2 LPF
No.3 RINP1/2, GINP1/2, BINP1/2
No.4 CLMPLV/INN
No.5 Power supply, GND
No.6 RSDS (RXADCKP/N), ADCK(CK1, CK2)
No.7 LVDS (TXSYNCP/N, TX[4:0]P/N)

4.2.2 LPF device layout

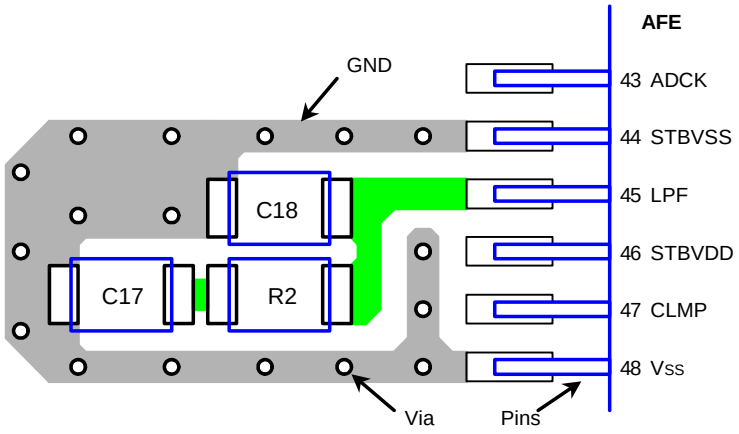
The following gives an example of external LPF device layout and pattern. The device should be shielded with the GND pattern as the recommendation. The LPF device and this AFE must be on the same surface.

The low-pass filter may malfunction due to a noise coming from other circuits including an external device being connected to the LPF pin. Such noise can be caused by intermittent or continuous change of voltage (between high and low voltages) or current. The noise generation by the circuits on the same surface and on another layer should also be checked.

As the ADCK pin (pin 43) and CLMP pin (pin 47) locate closely to each other, appropriate noise shielding is required. Also, the CK1 pin (pin 41) and CK2 pin (pin 42) locate closely and the similar noise shielding is required. The via holes should be formed in appropriate positions if the grounding patterns are used for noise shielding.

Related items: See Section 4.3.5 “Shielding by grounding”.

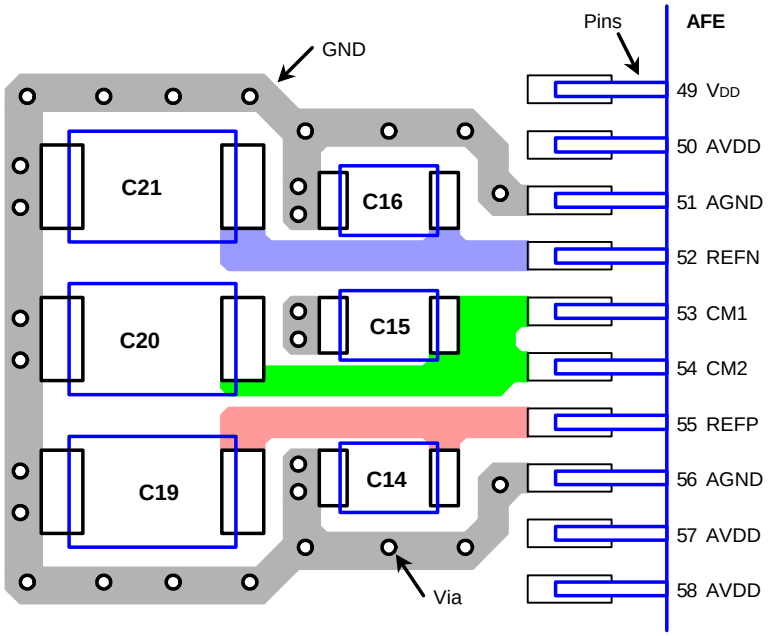
The parts numbers shown in the illustration below correspond to those listed in the Technical Manual.



4.2.3 REFP, REFN, CM1, and CM2 pin layout

The following illustrates the example layout and pattern of external devices connected to REFP, REFN, CM1 and CM2 pins.

These devices and this AFE should be placed on the same surface. The parts numbers shown in the illustration below correspond to those listed in the Technical Manual.

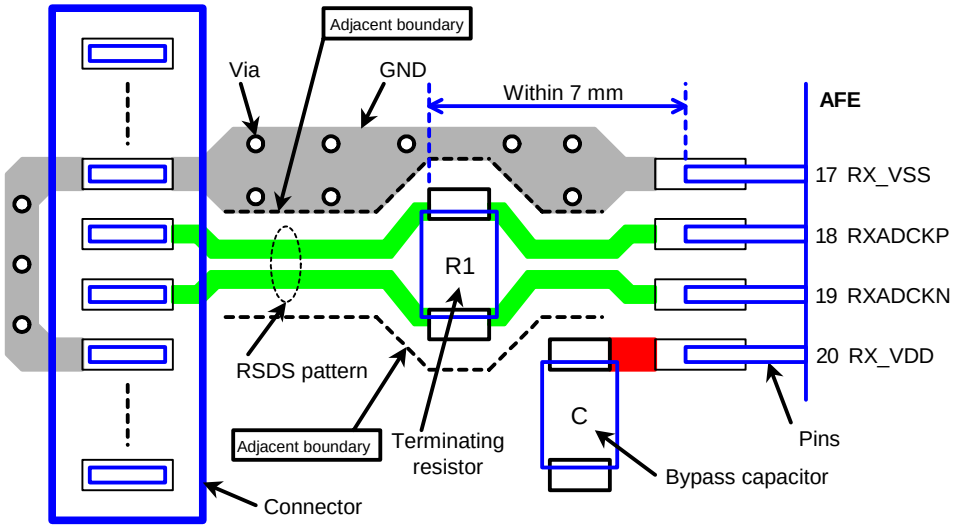


4.2.4 RXADCKP/N pin layout

The following gives the example layout and pattern of the circuit that connects RXADCKP/N pins to the connector. The parts numbers shown in the illustration below correspond to those listed in the Technical Manual.

The following points are recommended to satisfy.

(1) Place the connector and this AFE on the same surface.
(2) For the RSDS circuit pattern, see Section 4.3 “Designing the Circuit Patterns”.
(3) “Adjacent boundary” indicates a marginal distance from the adjacent RSDS circuit pattern. The minimum clearance (or gap) that is larger than the dimensions (G2 or G3) specified in Section 4.3.8 “Impedance matching” must be assigned.
(4) A terminating resistor (R1) must be placed close to the pin (within 7 mm).
(5) The connector must have the GND pin between pairs of RSDS pins.
For the connection between GND and RX_VSS pins of the connector, see section 5.1 “System Connection”.



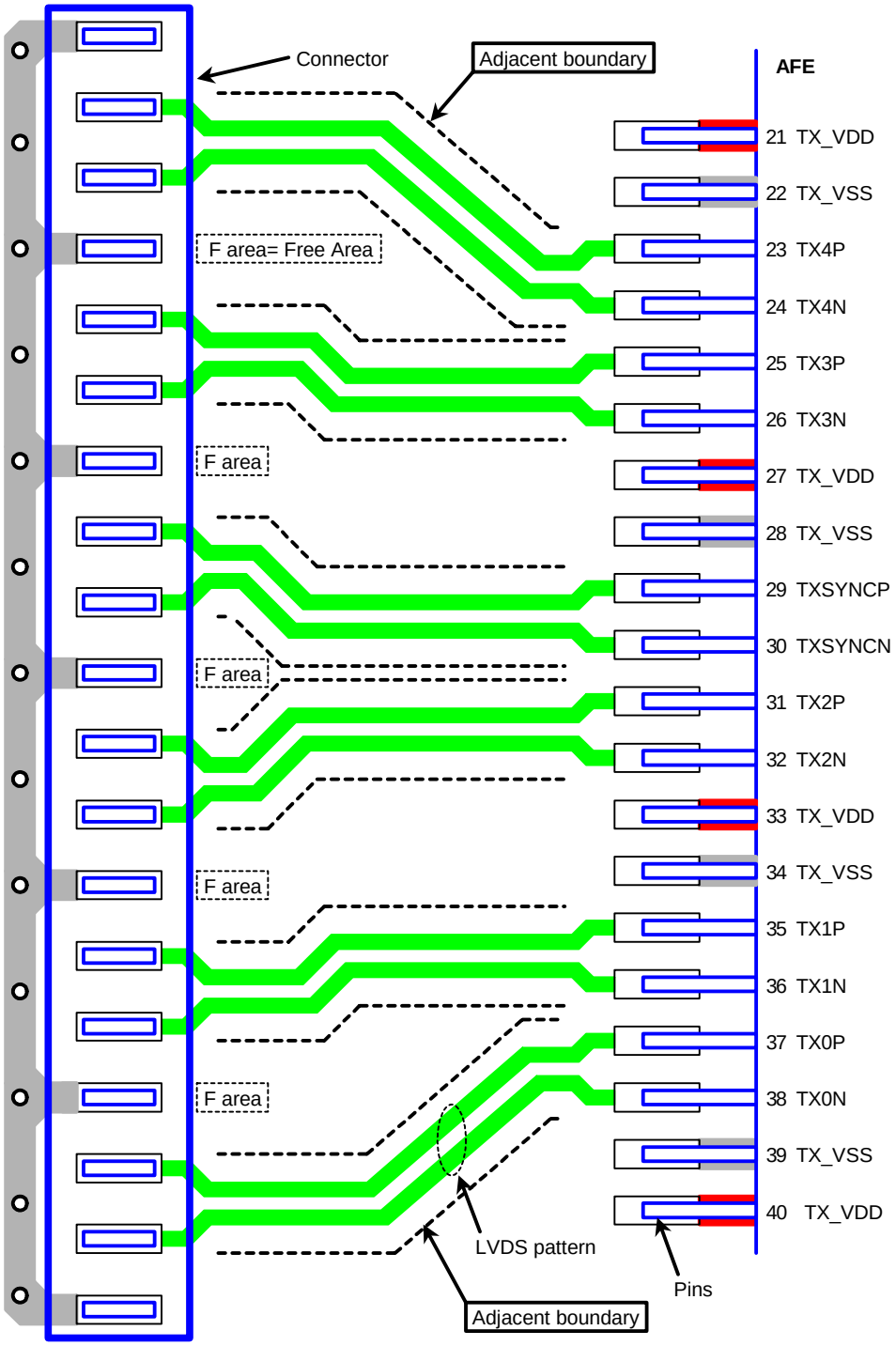
4.2.5 TXSYNCP/N and TX[4:0]P/N pin layout

The following gives an example of TXSYNCP/N and TX[4:0]P/N pin layout and circuit pattern.

The following points are recommended to satisfy.

(1) Place the connector and this AFE on the same surface.
(2) See section 4.3 “Pattern Design” for LVDS pattern.
(3) “Adjacent boundary” indicates a marginal distance from the adjacent LVDS circuit pattern. The minimum clearance (or gap) that is larger than the dimensions (G2 or G3) specified in Section 4.3.8 “Impedance matching” must be assigned.
(4) “F Area” should be a space (having no conductors).
Therefore, the TX_VDD and TX_VSS pins must be connected to the bypass capacitor using two or more via holes from inside of this AFE to the pair of power pins 1.

(5) The connector must have the GND pin between pairs of LVDS pins.
For the connection between GND and TX_VSS pins of the connector, see section 5.1 “System Connection”.

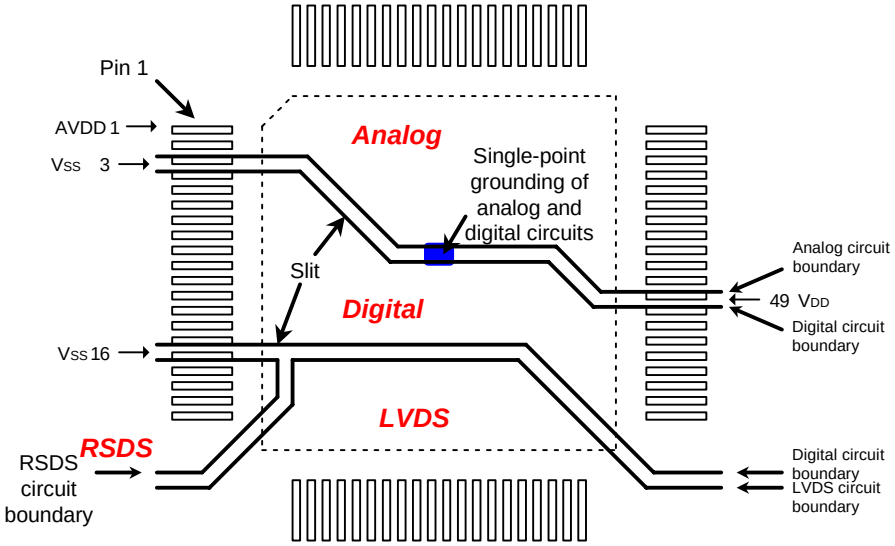


4.3 Designing the Circuit Patterns

Be sure to separate every pattern of digital circuit including power supply and GND circuits, LVDS circuit, RSDS circuit, and analog circuit from each other. If the input of RXADCKP/N pins (RSDS circuit) is not used, the TX_VDD (TX_VSS) pin of LVDS circuit and the RX_VDD (RX_VSS) pin of RSDS circuit need not be separated from each other.

The digital and analog circuits must be grounded at a single point on the soldering side just below this AFE IC. A 0.5-mm or wider slit must be formed at each circuit boundary, and its position must be the same on all layers.

The following gives an example of circuit pattern separation using the slits. Their position is the same on all layers.



4.3.1 Basic pattern layout

The following describes the basic circuit pattern layout.

(1) Avoid a wiring loop of every circuit patterns (such as signal, power supply, and ground circuits).
(2) Design the circuits to have the shortest current path.
(3) Place the GND circuit pattern (for shielding) in parallel to the digital, analog, and clock circuit patterns.
(4) Place a GND pattern in a space on the surface layer.
(5) Avoid a floated GND circuit pattern in areas described in Items (3) and (4).
(6) Avoid a filled pattern of conductors except when necessary.
(7) Insert a bypass capacitor between the power (GND) circuit and IC pins.
(8) If lead-type devices (such as transformers, coils and relays) are mounted, do not place other signal lines in this area of all layers.
(9) Do not place other signal lines in the area that has surface mounting devices.
(10) Do not place the clock circuit pattern in the area close to other signal lines and power supply.
(11) Place all circuit patterns, except for the inter-layer connection of power and GND lines, on the same surface as much as possible without using via holes.

4.3.2 Circuit pattern length

When you design the digital circuit pattern, its clock system circuits must be considered carefully. The circuit pattern length should be minimal, and the minimum via holes should be used as possible. The general wiring patterns should be used for other circuits.

For the differential signal circuit patterns, see Sections 4.2.4 “RXADCKP/N pin layout”, 4.2.5 “TXSYNCP/N and TX[4:0]P/N pin layout”, and 4.3.8 “Impedance matching”.

Basically, the analog circuit patterns must have the minimum connection lines.

Also, the circuit patterns connected to the following pins must have the equal length.

(1) RINP1/2, GINP1/2, BINP1/2

(2) REFP, REFN, CM1, CM2

4.3.3 Circuit pattern width

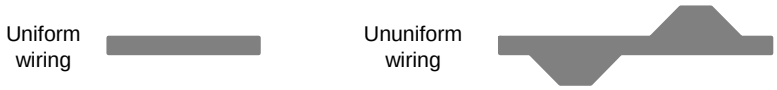
The clock system circuit pattern should be 0.5 mm to 1 mm wide.

For the differential signal circuit patterns, see Section 4.3.8 “Impedance matching”.

The analog circuit patterns should be 0.5 mm to 1 mm wide.

The circuits having the same pattern should have the same width as much as possible.

If a circuit pattern, except for the power and GND circuits, has the very large width, it is susceptive to noise.



4.3.4 Bending of circuit patterns

The angle (90 °) or a sharp bending of circuit patterns is not allowed.

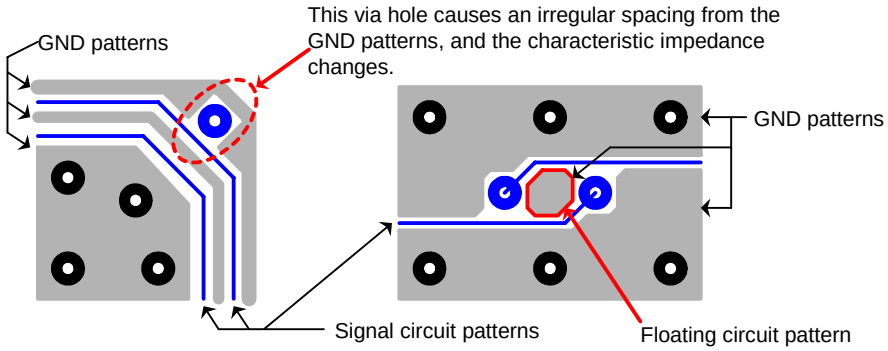
As this rule applies to the power supply and GND circuits, the circuits on the internal layers must also be designed carefully.

If required, you should bend the circuit patterns in 45 ° or larger or along an arc.

4.3.5 Ground (GND) shield

The signal and GND circuit patterns must be separated with a fixed distance from each other. If their distance changes when via holes are used (except for GND circuits), the characteristic impedance of the signal circuit pattern changes.

The GND circuit pattern should have via holes at a fixed distance. As the excessively large space between via holes can cause a plane resonance, their space should be as small as possible. In addition, if the ground circuit pattern placed for shielding has no via holes for grounding, such circuit pattern is floated and it can cause an unexpected noise.



4.3.6 Interlayer connection

Analog circuit patterns should be wired on the same surface without using via holes as much as possible.

The LVDS and RSDS circuit patterns should be wired on the same surface without using via holes.

The digital circuit patterns can be wired in the general way. However, the clock system circuit patterns must be wired on the same surface without using via holes.

The power supply and GND circuit patterns should be connected interlayer using multiple via holes.

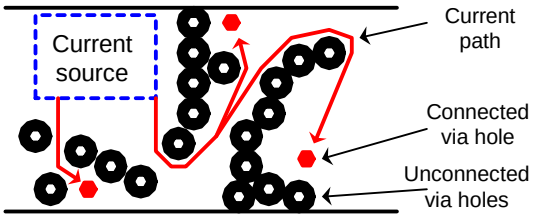
4.3.7 Via holes and through holes

In general, via holes and through holes lead to degrading reliability of the board.

Allowable current per via hole as well as reliability and inductance should be counted for power and GND circuit patterns (including the connection to bypass capacitors) to assign the proper number of via holes.

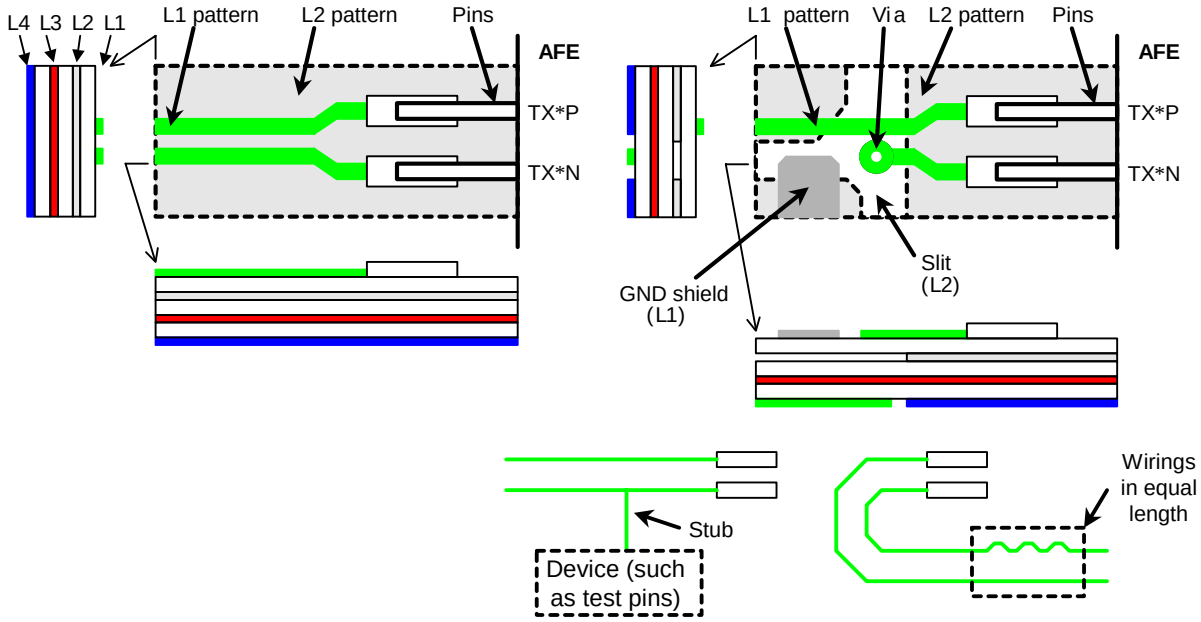
The impedance of a pattern becomes discontinuous by passing a via hole (or through hole), causing an impedance mismatching. Therefore, the differential signal circuit patterns should not have via holes.

Inappropriate alignment of via holes (or through holes) on the power or GND circuit pattern may open the current path or uneven current density. The inner layer current paths should also be considered.

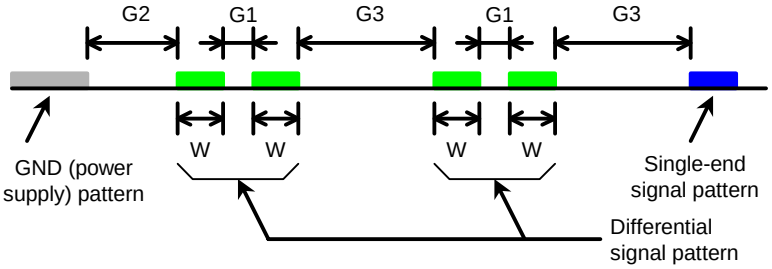


4.3.8 Impedance matching

The differential signals (LVDS and RSDS pin signals) handled by this AFE IC must match their impedance.
The recommended characteristic impedance of differential signal pattern is 50 Ω ±5% (at single end).
Generally, the signal impedance should match between the P and N differential signal patterns and the filled circuit patterns formed immediately below that surface. Therefore, their impedance may mismatch (and become discontinuous) due to the adjacent circuit patterns (such as signal, ground and shielding patterns) and the filled patterns immediately under this surface. Stubs, wirings in equal length, via holes, or slits can cause the impedance mismatching.



The following dimensional requirements must be satisfied to match the signal impedance. The fixed potential adjacent circuit limit gap (G2) or fluctuating potential adjacent circuit limit gap (G3) must be selected according to the type of adjacent circuit patterns used. The fixed potential adjacent circuits are power supply and GND circuits, and the fluctuating potential adjacent circuits are power supply circuits (locating close to the power circuit) having signal patterns or RF signal components.



W: Width of a differential signal pattern

G1: Gap between differential signal patterns

G2: Fixed potential adjacent circuit limit gap

G3: Fluctuating potential adjacent circuit limit gap

[Dimensional requirements]
- W>G1
- G2=2xW (W>G1)
- G3=3xW (W>G1)

4.3.9 Unwanted emission noise

Appropriate board design is the basic factor to reduce unwanted emission noise (EMI).
A board configured for noise reduction implies it has electrically stable characteristics.

(1) A pattern design allowing for the current path of charge supply and return is effective.
Because the current path is a matter that should be reviewed totally as a system, the pin assignment of cable or other components is also important

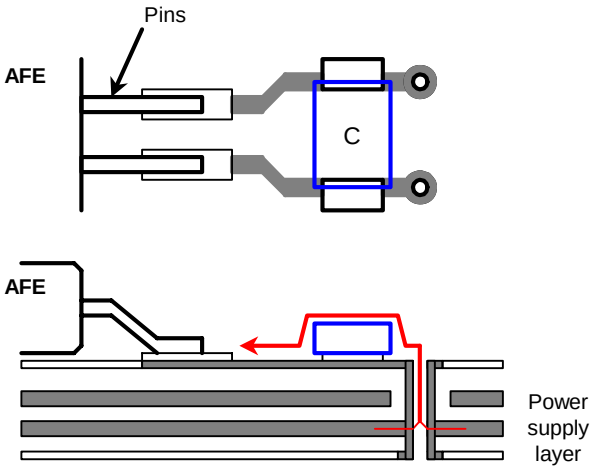
(2) A design that takes into account the electric field that is generated by movement of charges is also effective.
Using the GND shield to absorb unwanted emission (non-bonding electric field), or maintaining impedance matching to block disparity in the electric field can reduce unwanted emissions.

(3) The design that takes into account the intensity of electric field and electric flux line is also effective.
Unwanted emissions can be reduced from a pattern on the board edge by making the board's periphery into filled grounding patterns (also by spacing out via holes). Similarly, unwanted emissions from high-frequency signal patterns and high-speed operating devices can be reduced if those devices are placed close to the center of circuit board.

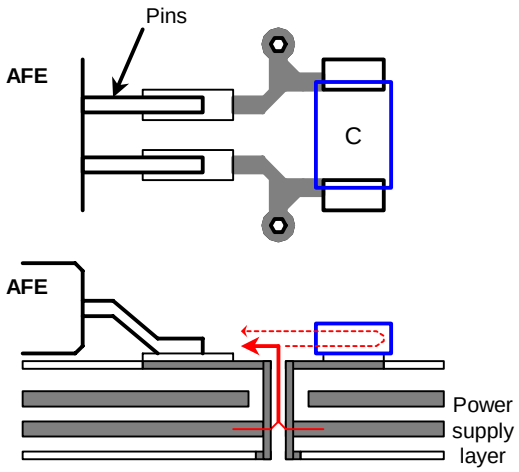
4.3.10 Bypass capacitor

Since bypass capacitors are responsible for the supply of effective current, it is necessary to understand the following in order for your design to enable the stable behavior of the bypass capacitors.

(1) The current path depends on the position of via holes. It implies that inappropriate placement of via holes disable the function of a bypass capacitor.

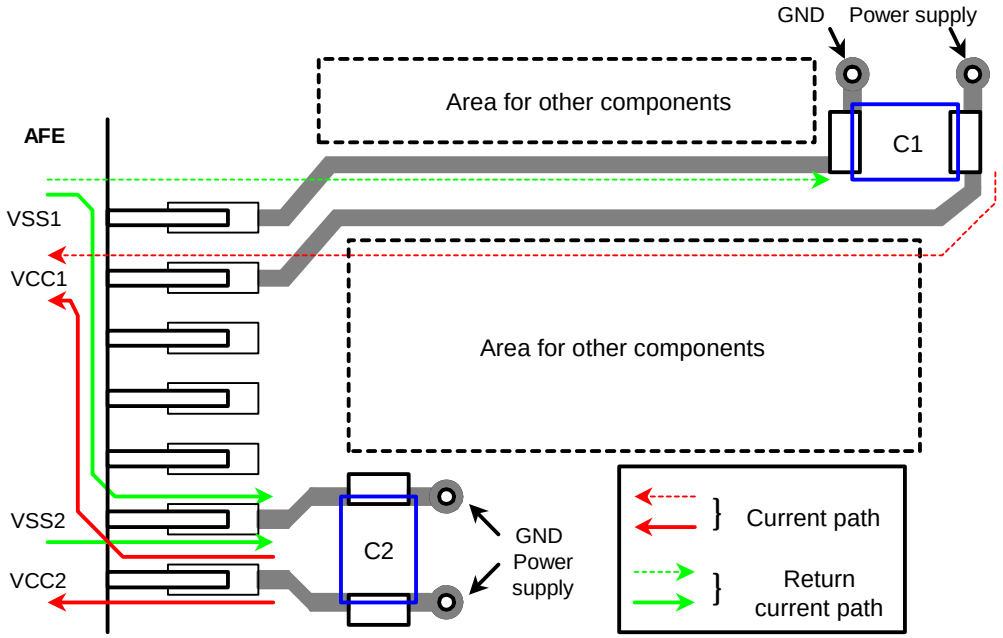


Appropriate via hole position



Inappropriate via hole position

(2) The distance of a capacitor from pins may not only disable the function of the bypass capacitor but also cause deterioration of its characteristics.
In an example shown below, the current path from C2 has priority over that from C1, which is positioned further from the pins. Internal circuits connected to C1 as well as internal circuits between VCC1 to VCC2 may exhibit characteristic deterioration due to unexpected current.



5. OTHERS

5.1 System Connections

Refer to the description in this Guide for GND related connections (such as shields and connectors) required for your system design. It will be beneficial for you to comply with safety standards or legal restrictions of your country.

5.1.1 Differential signal connectors

Pin assignment should be optimized depending on the connector being used.

(1) A surface mounting type is recommended for differential signal connectors. However, since the LVDS Standard is required to be met by the system as a whole, it should finally depend on your verification in the actual application conditions.
(2) The connector must have the GND pin between pairs of differential signal pins (LVDS and RSDS pins). For the connection between GND and TX_VSS pins of the connector, see Section 5.1 “System Connection”.
(3) Assign GND to pins on both end of the connector (e.g. for FFC).
(4) Ground the unused pins.
(5) If the connectors have different lead length (such as right-angle, 2-line connectors), the paired circuit patterns must be connected to the pins in the same length.

5.1.2 Cables

To allow stable PC board operations, the connected cables must carefully be considered.

Note that if you shield a cable to reduce its unwanted emission noise, the LVDS Standard must be satisfied (for the entire system) under the actual application conditions.

Ideally, the GND pins should be assigned by considering the return current, type of signals (such as the difference of I/O and driving capacity), and the power supply system lines.

Note that ribbon cables are not recommended to use.

5.2 FG

If the hole position of the circuit board having this AFE IC is too close to the LVDS or RSDS circuit or the analog signal circuit, the metal surface of setscrews may contact the frame ground (FG) and the entire system may be affected by the noise.

If the circuit board having this AFE IC is shielded by a metallic plate to reduce the unwanted emission noise, this shield itself is connected to the frame ground (FG) and the system may be affected by the noise.

The entire system design should be considered when using the FG.

5.3 ESD

We conduct a test for anti-electrostatic destruction to check the destructive resistant properties of a semiconductor.

The test to check functions and behaviors should be conducted on your side under actual application conditions.

5.4 Thermal Conductance

Maintain the constant ambient temperature during operation of the AFE IC.

The circuit patterns must be designed to have the shortest thermal conductance path by considering the thermal resistance of entire circuit board in different circuit patterns and layout. The optimized thermal conductance allows the effective heat radiation, and stable and improved electric characteristics.

6. TERMINOLOGIES

A

AFE	An abbreviated form of Analog Front End IC. This AFE IC has been designed dedicate to a scanner system.
AGND	The ground pin of analog signal circuit.
AVDD	The power supply pin of analog signal circuit.

C

CCD	An abbreviated form of Charge Coupled Device.
CIS	An abbreviated form of Contact Image Sensor. Also called the Line Sequential Output Sensor. The CIS uses LEDs as the optical source, and it features the less power consumption than the CCD. It is also called the CMOS image sensor.

E

EMI	An abbreviated form of Electro-Magnetic Interference. This is the generic name of electron emission from electronic devices that can cause electromagnetic interference.
ESD	An abbreviated form of Electro-Static Discharge.

F

FG	An abbreviated form of Frame Grounding.

G

GND	An abbreviated form of grounding pins (including AGND, VSS, TX_VSS, and RX_VSS pins).

L

LVDS	An abbreviated form of Low-Voltage Differential Signaling (or LVDS interface).

P

PCB	An abbreviated form of Printed Circuit Board.
PLL	An abbreviated form of Phase-Locked Loop circuit.

R

RSDS	An abbreviated form of Reduced Swing Differential Signaling (or RSDS™ interface) system. This is the driver LSI interfacing standard to reduce the EMI using the reduced swing differential signaling system.
RX_VDD	The power supply pin of RSDS receiver circuit.
RX_VSS	The grounding pin of RSDS receiver circuit.

T

TX_VDD	The power supply pin of LVDS transmission circuit.
TX_VSS	The grounding pin of LVDS transmission circuit.

V

VDD	The power supply pin of digital signal circuit.
VIA	See the description of via holes.
VSS	The grounding pin of digital signal circuit.

A

Impedance matching	Matching between the output impedance and input impedance of a circuit pattern.

KA

RF signal circuit pattern	A circuit pattern that handles several megahertz or higher radio frequency (RF) or high-frequency signals.

SA

Single-end system	A system to transfer data via a single signal line.
Skew	A delay of signal timing that can occur due to an inappropriate wiring pattern.
Stub	A stubbed pattern derived from a main wiring pattern.
Slit	An area insulated from electricity and has no copper laminate.
Through hole	A hole through layers to interconnect the layers for conduction by soldering device leads inserted into the hole.
Ceramic capacitor	Useful for various applications including noise elimination and charge supply if proper characteristics are selected depending on the application.

TA

Tantalum capacitor	Known as its superior characteristics but also as typical failure mode of short circuit. Even for a model with built-in fuse, a short circuit leads to breaking. So the tantalum capacitor should be handled with care.
Derating	The term refers to the use of any product with lower load than the rated value, for the purpose of improving its reliability.
Electrolytic capacitor	Known as its superior characteristics, but its characteristics and life depend on temperature. Its life is shortened by half with 10 °C rise in temperature according to the Arrhenius theory.

HA

Via hole	A through hole only for interconnecting layers.
Surface layer	Refers to components side or soldering side.
Unwanted emission noise	High-frequency noise emitted in addition to primary signals.
Floating	Refers to a pattern electrically unstable (floating).
Filled circuit pattern	A circuit pattern (area) created with the fixed area.

RA

Lead inductance	The inductance existing in the leads of a lead-type device.

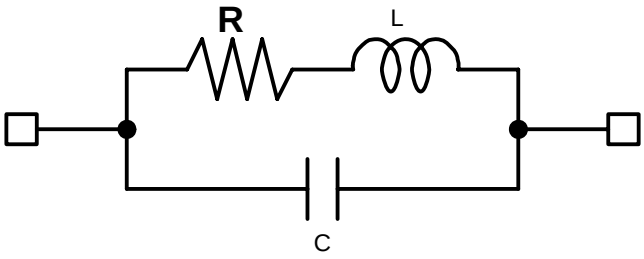
7. TECHNICAL INFORMATION

To find and update technical information relating to this AFE IC, visit the following URL.

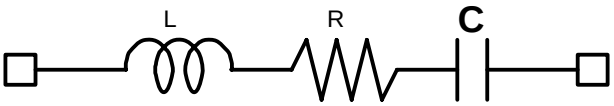
[URL] http://www.epsondevice.com/semicon/index.html
[Analog front-end IC (AFE)] → [AFE Users Site]

8. APPENDIX

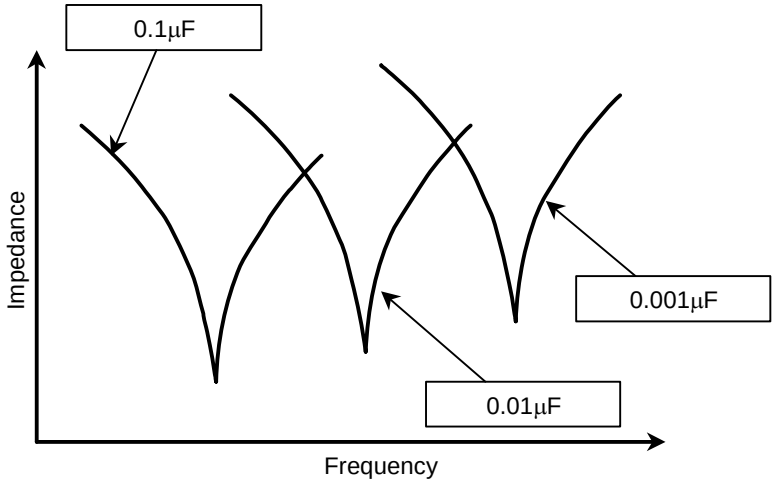
8.1 Equivalent Circuit of Resistors



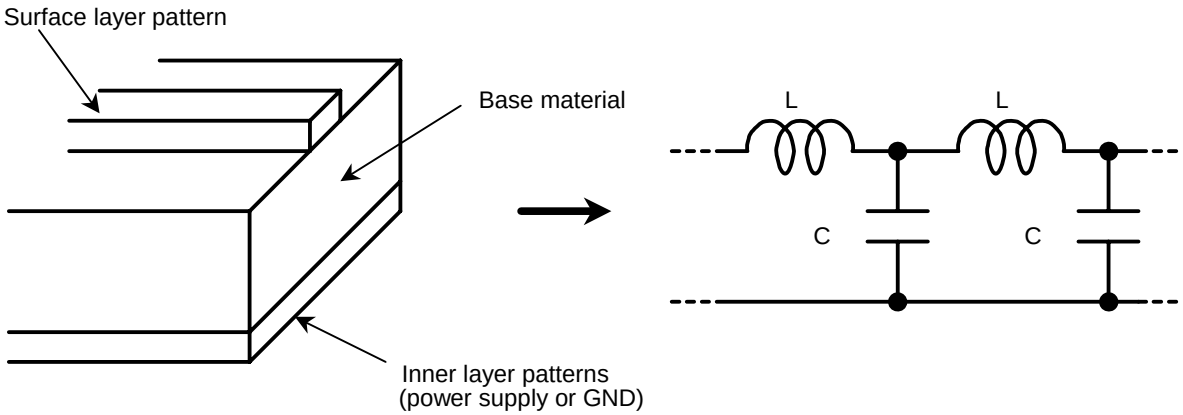
8.2 Equivalent Circuit of Capacitors



8.3 Frequency Characteristics of Capacitors



8.4 Equivalent Circuit of Patterns



9. REVISION HISTORY

Rev	Revision date	Description of revisions
1.0	2007/10/03	First version released.

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