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S1R72U16
Development Support Manual

SEIKO EPSON CORPORATION

Rev.2.00

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Scope

This document applies to the S1R72U16 IDE device - USB 2.0 host bridge LSI.

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1. Function Overview

This LSI includes two functions to support product (system) development. They are controlled by a PC via the serial interface.

- History display function
- USB logo certification support function

The History display function enables the viewing from a PC of various details, including IDE/USB status, detected USB device type, transfer history, and error information. It also enables connection verification between the main CPU and the LSI, as well as simple debugging using transfer history and error information.

The USB logo certification support function is used to switch to the test mode corresponding to the electrical test as part of certification testing. For detailed information, refer to the *S1R72U16 Embedded Host Compliance Guide*.

Note the following precautions for history information.

- HS devices connected via an FS USB hub will be recognized as FS devices, not HS devices.
- Only Bulk Only Transport Mass Storage Class devices are supported.
  - * UFI subclass(SubClassCode value is 04h) devices are unsupported.
  - ➢ CBI Transport devices such as USB FDDs are unsupported, even if they are Mass Storage Class devices. Likewise, devices manufactured before the implementation of Mass Storage Class standards and not conforming to those standards will not be supported.
- Non-Mass Storage Class devices are not supported.

Note the following precautions regarding operations.

- These functions are disabled if the LSI switches to Sleep mode while functions are underway. Operation will resume on recovery from Sleep mode in the state immediately preceding Sleep mode.

2. Operating Configuration

Fig. 2-1 illustrates the typical hardware configuration when using these functions.

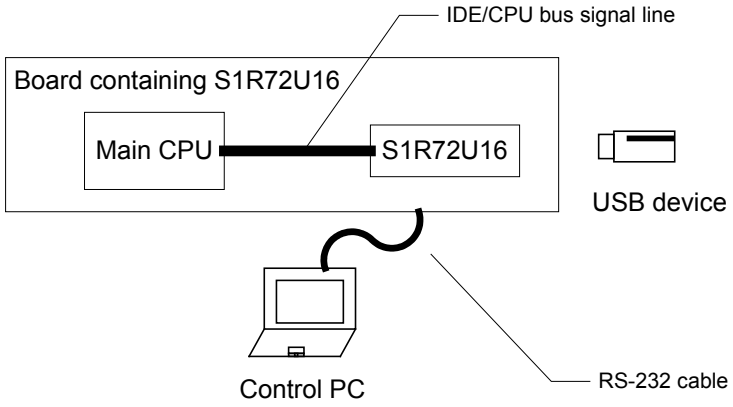

Fig. 2-1 Typical hardware configuration

The blocks shown in Fig. 2-1 are as follows:

- Board containing S1R72U16
  - Corresponds to the product (system) board. These functions are controlled by the control PC.
- Control PC
  - PC used to control these functions via terminal software using the RS-232 interface function.
- USB device
  - A USB device such as USB memory, HDD, CD, DVD, or MO drive. Connect when using the IDE-USB bridge. Not required if only checking (initializing) the connection between the LSI and main CPU.

Table 2-1 shows RS-232 and terminal software settings.

Table 2-1 RS-232 and terminal software settings

Item	Setting
Baud rate	19200bps
Data bit	8bit
Parity	None
Stop bit	1
Flow control	None
Encoding	Shift-JIS
Local echo	On

3. Operating Procedures

Control these functions as shown in Fig. 3-1.

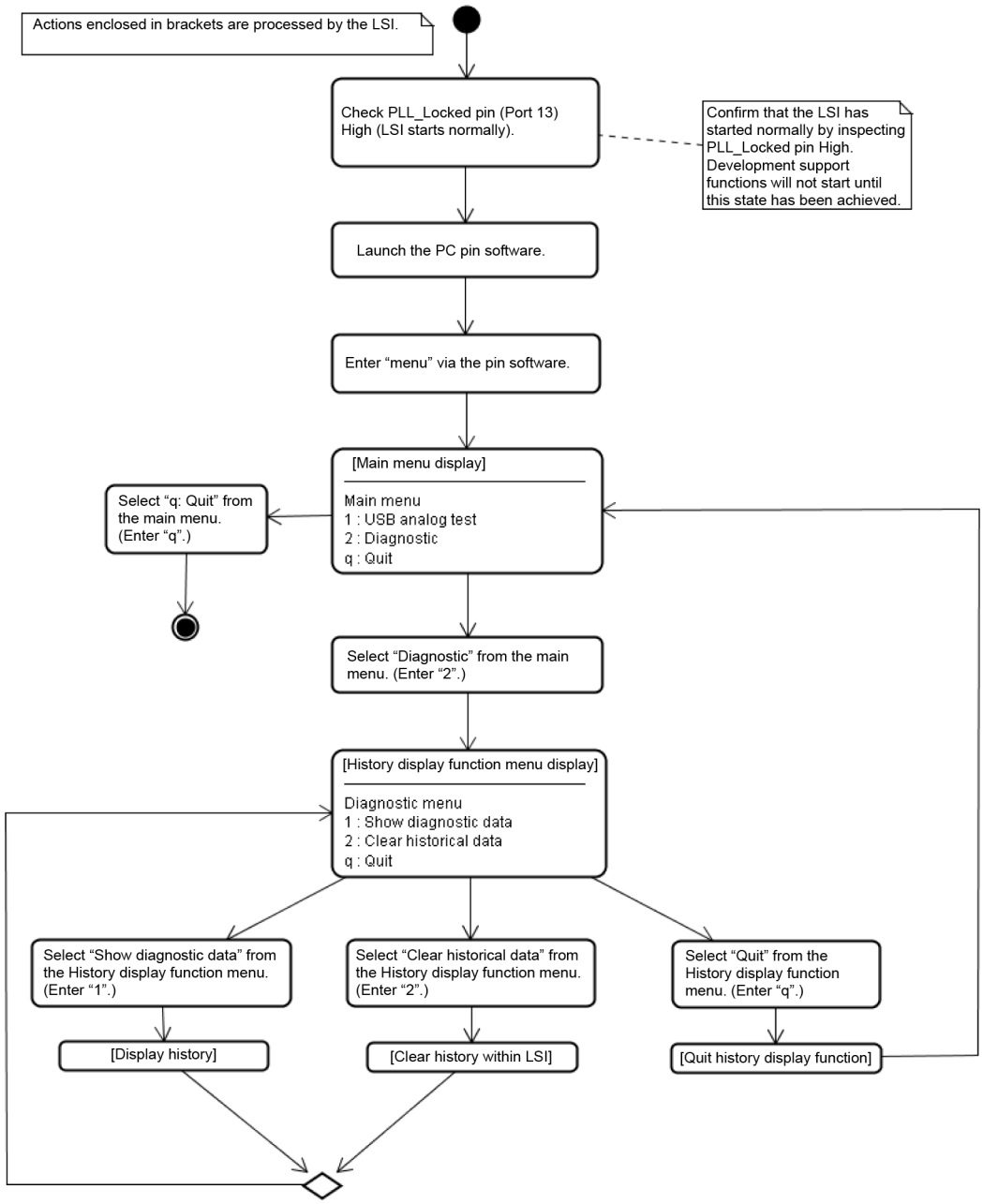

Fig. 3-1 History display function operating procedures

These functions are enabled once the PLL_Locked pin (Port13) switches to High. Confirm that the signal is at High before starting these functions (i.e., before entering "menu").

Consider the following possible causes if the PLL_Locked pin (Port13) fails to switch to High.

- The specified power supply is not provided to the LSI.
- The LSI reset pin (XRESET) is still at Low.

- The clock is not oscillating correctly.

Consider the following possible causes if transfer is not possible even though the PLL_Locked pin (Port13) has switched to High.

- The CLKSEL pin setting does not match the clock frequency.
- The RS-232 cable (cross/straight) used is incorrect for the circuit board wiring.
- The terminal software settings differ from those described in Table 2-1.

3.1 Key Input Specifications

The key input specifications are as follows:

- The Enter key confirms the string entered.
- Only single-byte alphanumeric characters can be entered. Double-byte characters are invalid.
- Input is not case-sensitive.

3.2 Main Menu

Start these functions by entering “menu” via the PC terminal software. This will display the items shown in Table 3-1.

Table 3-1 Main menu list

Key Input	Item	Summary
1	USB analog test	Allows switching to Test mode.
2	Diagnostic	Starts the history display function.
q	Quit	Quits the function.

3.2.1 USB Analog Test

When key input “1” is received, then the operation menu is displayed and to allow switching to Test mode. For detailed information, refer to *S1R72U16 Embedded Host Compliance Guide*.

3.2.2 Diagnostic

When key input “2” is received, then the operation menu is displayed and to start the history display function. For detailed information, refer to “3.3 History Display Function Menu”.

3.2.3 Quit

When key input “q” is received, then this quits the function. The function will be unavailable until the “menu” is invoked once again.

3.3 History Display Function Menu

Table 3-2 shows the items that can be used with the history display function.

Table 3-2 History display function menu list

Key Input	Item	Summary
1	Show diagnostic data	Displays the history data.
2	Clear historical data	Clears the history data recorded.
q	Quit	Quits the history display function.

3.3.1 Show Diagnostic Data

When key input "1" is received, the history data is displayed. Then the menu shown in Table 3-2. History data includes both USB and IDE related data and is displayed in chronological order, starting with the oldest. Up to 63 messages can be displayed. Tables 4-1 and 4-2 show the display details.

3.3.2 Clear Historical Data

When key input "2" is received, recorded history data is all cleared. Then the menu shown in Table 3-2. History data recording resumes after the previous data has been cleared.

3.3.3 Quit

When key input "q" is received, then this quits the history display function and returns to the main menu.

4. History Data Details

This section describes the IDE and USB related history data displayed.

4.1 IDE History Data

Table 4-1 shows the IDE-related history data. The signal descriptions are based on the ATA/ATAPI standard signal naming conventions. Refer to Table A-1 for correspondence to the LSI pin names.

Table 4-1 IDE history data list

History data	Summary
IDE: idle	Idle state
IDE: Hardware reset	Detected hardware reset.
IDE: SRST	Detected software reset.
IDE: command [xxh]	Detected ATA/ATAPI command receipt. “xx” indicates hexadecimal command code (operation code for ATAPI) received.
IDE: PIO (D->H)	Transferred PIO data from device to host.
IDE: PIO (H->D)	Transferred PIO data from host to device.
IDE: Multi Word DMA (D->H)	Transferred Multi Word DMA data from device to host.
IDE: Multi Word DMA (H->D)	Transferred Multi Word DMA data from host to device.
IDE: Ultra DMA (D->H)	Transferred Ultra DMA data from device to host.
IDE: Ultra DMA (H->D)	Transferred Ultra DMA data from host to device.
IDE: CRC error	Detected CRC error during Ultra DMA data transfer.
IDE: INTRQ	Asserted INTRQ.

4.1.1 IDE: idle

This history entry is recorded when in a state that allows commands to be received from the main CPU (when the Status register BSY bit and DRQ bit are both 0), corresponding to the state in which LSI power has been turned on or reset or a command has finished executing. If the main CPU reads the Status register BSY bit as 1 although the history data has not changed from this state, there may be a problem with signal quality or in the signal connections shown below.

- CS0-, DA0 to DA2, DD0 to DD7, **DIOR-**

4.1.2 IDE: Hardware reset

This history entry is recorded when a hardware reset is detected. If this history entry does not appear even after the main CPU has issued a hardware reset, there may be a problem with signal quality or in the signal connection shown below.

- RESET-

4.1.3 IDE: SRST

This history entry is recorded when a software reset is detected. If this history entry does not appear even after the main CPU has issued a software reset, there may be a problem with signal quality or in the signal connections shown below.

- CS1-, DA0 to DA2, DD0 to DD7, **DIOW-**

4.1.4 IDE: command [xxh]

This history entry is recorded when a command is received. The [xxh] part indicates the command code for ATA commands and the operation code for ATAPI commands. If this history entry does not appear even after the main CPU has issued a command or if the command issued by the IDE host does not match the command/operation code in the history, there may be a problem with signal quality or in the signal connections shown below.

- CS0-, CS1-, DA0 to DA2, DD0 to DD7, **DIOW-**

4.1.5 IDE: PIO (D->H)

This history entry is recorded when PIO format data transfer starts. If "IDE: INTRQ" or "IDE: idle" does not appear after the history entry, there may be a problem with signal quality or in the signal connections shown below.

- CS0-, CS1-, DA0 to DA2, **DIOW-**, **DIOR-**

If data is incorrect, there may be a problem with signal quality or in the signal connections shown below.

- **DD0 to DD15**

4.1.6 IDE: PIO (H->D)

Refer to "4.1.5 IDE: PIO (D->H)".

4.1.7 IDE: Multi Word DMA (D->H)

This history entry is recorded when Multi Word DMA format data transfer starts. If "IDE: INTRQ" does not appear after the history entry, there may be a problem with signal quality or in the signal connections shown below.

- **DIOW-**, **DIOR-**, **DMARQ**, **DMACK -**

If data is incorrect, there may be a problem with signal quality or in the signal connections shown below.

- **DD0 to DD15**

4.1.8 IDE: Multi Word DMA (H->D)

Refer to “4.1.7 IDE: Multi Word DMA (D->H)”.

4.1.9 IDE: Ultra DMA (D->H)

This history entry is recorded when Ultra DMA format data transfer starts. If “IDE: INTRQ” or “IDE: CRC error” do not appear after the history entry, there may be a problem with signal quality or in the signal connections shown below.

- **DIOW-, DIOR-, DMARQ, DMACK -, IORDY**

4.1.10 IDE: Ultra DMA (H->D)

Refer to “4.1.9 IDE: Ultra DMA (D->H)”.

4.1.11 IDE: CRC error

This history entry is recorded when a CRC error is detected during Ultra DMA format data transfers. If this history entry appears, there may be a problem with signal quality or in the signal connections shown below.

- **DD0 to DD15**

4.1.12 IDE: INTRQ

This history entry is recorded in spite of the Device Control register nIEN bit when the command issued by the main CPU has finished executing and the status register details have been updated. If the main CPU cannot detect INTRQ even when this history entry appears while the Device Control register nIEN bit is 0, there may be a problem with signal quality or in the signal connection shown below.

- **INTRQ**

  Note that this history entry is not recorded when the following commands, for which the ATA/ATAPI standards specify INTRQ is not to be asserted, terminate normally.

  - IDENTIFY DEVICE
  - IDENTIFY PACKET DEVICE
  - READ SECTOR (S)
  - READ SECTOR (S) EXT
  - READ MULTIPLE
  - READ MULTIPLE EXT

4.2 USB History Data

Table 4-2 shows the USB-related history data.

Table 4-2 USB history data list

History data	Summary
USB: VBUS overcurrent	Detected VBUS overcurrent.
USB: LS device	Detected LS device connection.
USB: FS device	Detected FS device connection.
USB: HS device	Detected HS device connection.
USB: storage device	Detected storage device connection.
USB: unsupported device	Detected unsupported device connection.
USB: more than 3 storage device	Detected connection of 3 or more storage devices.
USB: more than 4 hubs	Detected connection of 4 or more USB hubs.
USB: phase err	Detected phase error.
USB: CBW	Issued CBW.
USB: Data IN	Issued Bulk IN (except CSW).
USB: Data OUT	Issued Bulk OUT (except CBW).
USB: CSW	Received CSW.
USB: cleared STALL	Issued request to clear STALL.
USB: Mass Storage Reset	Issued Mass Storage Reset (specified device reset).

4.2.1 USB: VBUS Overcurrent

This history entry is recorded when an overcurrent is detected in the VBUS. If this history entry appears when an USB device is connected, the current drawn from the VBUS by the USB device may exceed the supply capacity.

4.2.2 USB: LS device

This history entry is recorded when an LS (Low Speed) device is connected. This history entry is not recorded if connected via a USB hub.

4.2.3 USB: FS device

This history entry is recorded when an FS (Full Speed) device is connected. FS devices include USB hubs recognized as FS. This history entry is not recorded if connected via a USB hub.

4.2.4 USB: HS device

This history entry is recorded when an HS (High Speed) device is connected. HS devices include USB hubs recognized as HS. This history entry is not recorded if connected via a USB hub.

4.2.5 USB: storage device

This history entry is recorded if a supported storage device connection is detected.

4.2.6 USB: unsupported device

This history entry is recorded if an unsupported storage device connection is detected.

4.2.7 USB: more than three storage devices

This history entry is recorded if a third or subsequent supported storage devices are detected. Up to two storage devices may be connected to the LSI.

4.2.8 USB: more than four hubs

This history entry is recorded if a fourth or subsequent USB hubs are detected. Up to three USB hubs may be connected to the LSI.

4.2.9 USB: phase err

This history entry is recorded if a problem occurs in the protocol with the storage device.

4.2.10 USB: CBW

This history entry is recorded when a command-issuing CBW is issued as defined for Mass Storage Class.

4.2.11 USB: Data IN

This history entry is recorded when Bulk IN is issued at the start of the data transfer (USB device to USB host) for a command issued using CBW. A single history entry is recorded for the entire data stream rather than for individual packets.

4.2.12 USB: Data OUT

This history entry is recorded when Bulk OUT is issued at the start of the data transfer (USB host to USB device) for a command issued using CBW. A single history entry is recorded for the entire data stream rather than for individual packets.

4.2.13 USB: CSW

This history entry is recorded on receiving a command status reception CSW as defined for Mass Storage Class. This is the status for commands issued using CBW and indicates that the protocol is complete.

4.2.14 USB: cleared STALL

This history entry is recorded when the LSI requests the clearing of (issuing request to clear) the STALL after returnning STALL from a device.

4.2.15 USB: Mass Storage Reset

This history entry is recorded when Mass Storage Reset is issued to a device.

4.3 Connection Verification Methods

This section describes methods for verifying connections between the main CPU and the LSI and between USB devices and the LSI.

4.3.1 Main CPU and LSI Connection Verification Method

This section describes the method for verifying connections between the main CPU and the LSI. Individual IDE signals can be checked via control from the main CPU, as shown below.

- RESET signal confirmation method

  1. Confirm that the "IDE: Hardware reset" history entry appears when the main CPU issue a Hardware Reset.

- CS1 signal confirmation method

  1. Confirm that the "IDE: SRST" history entry appears when the main CPU issues an SRST.

The following signals should be checked, depending on the transfer mode used. The signals used for Multi Word DMA and PIO transfer can be checked simultaneously using Ultra DMA transfer. The signals used for PIO transfer can be checked simultaneously using Multi Word DMA transfer. Set the Device Control register nIEN bit to 0 when issuing commands.

- Method for confirming CS0-, CS1-, DA0 to DA2, DIOW-, DIOR-, INTRQ, and DD0 to DD15 signals
  [When using PIO transfer only]
  Confirm by issuing a command from the main CPU and by using PIO transfer.

  1. Issue the SET FEATURE command and set PIO transfer.
  2. Issue the WRITE SECTOR(S) command. Confirm that the command ends normally and that the history entry appears as "IDE: command [30h]" – "IDE: PIO (H->D)" – "IDE: INTRQ" – "IDE: idle".
  3. Issue the READ SECTOR(S) command and read the data written in 2. Confirm that the command ends normally and that the history entry appears as "IDE: command [20h]" – "IDE: PIO (D->H)" – "IDE: idle".

  This enables evaluation of the CS0-, CS1-, DA0 to DA2, DIOW-, DIOR-, and INTRQ signals.

  4. Compare the data written by the WRITE SECTOR(S) command against the data read by the READ SECTOR(S) command. Confirm that they match.

  This enables evaluation of the DD0 to DD15 signals.

* In ATAPI mode, issue the WRITE command in place of the WRITE SECTOR(S) command and the READ command in place of the READ SECTOR(S) command.

- Method for confirming CS0-, CS1-, DA0 to DA2, DIOW-, DIOR-, INTRQ, DMARQ, DMACK-, DD0 to DD15 signals
  [When using Multi Word DMA transfer]
  Confirm by issuing a command from the main CPU and by using Multi Word DMA transfer.

  1. Issue the SET FEATURE command. Set Multi Word DMA transfer.
  2. Issue the WRITE DMA command. Confirm that the command ends normally and that the history entry appears as "IDE: command [CAh]" – "IDE: Multi Word DMA (H->D)" – "IDE: INTRQ" – "IDE: idle".
  3. Issue the READ DMA command and read the data written in 2. Confirm that the command ends normally and that the history entry appears as "IDE: command [C8h]" – "IDE: Multi Word DMA (D->H)" – "IDE: INTRQ" – "IDE: idle".

  This enables evaluation of the CS0-, CS1-, DA0 to DA2, DIOW-, DIOR-, INTRQ, DMARQ, and DMACK- signals.

  4. Compare the data written by the WRITE DMA command against the data read by the READ DMA command. Confirm that they match.

  This enables evaluation of the DD0 to DD15 signals.

  * In ATAPI mode, issue the WRITE command instead of the WRITE DMA command and the READ command instead of the READ DMA command.

- Method for confirming CS0-, CS1-, DA0 to DA2, DIOW-, DIOR-, INTRQ, DMARQ, DMACK-, IORDY, and DD0 to DD15 signals
  [When using Ultra DMA transfer]
  Confirm by issuing a command from the main CPU and by using Ultra DMA transfer.

  1. Issue the SET FEATURE command. Set Ultra DMA transfer.

  The subsequent control and confirmation methods are the same as for Multi Word DMA. Transfer except that the history information will contain "Ultra DMA" instead of "Multi Word DMA."

4.3.2 USB Device and LSI Connection Verification Method

This section describes method for verifying connections between USB devices and the LSI.

- Checking the initial state of the VBUS supply control circuit

  1. Confirm that "USB: VBUS overcurrent" does not appear in the history without connecting a USB device.

     * Otherwise, there may be a problem in the VBUS supply control circuit.

- Checking the VBUS supply control circuit and the interface peripheral circuits

  1. Connect a USB device (not USB hub) to the LSI and confirm that “USB: VBUS overcurrent” does not appear in the history.

     * Otherwise, there may be a problem in the VBUS supply control circuit.

  2. Confirm that “USB: LS device”, “USB: FS device”, or “USB: HS device” in the history match the speed mode of the USB device connected.

     * If not, there may be a problem in the interface peripheral circuit or with signal quality.

  3. Confirm that the history entry appears as shown below according to the type of USB device connected.

     - Confirm that “USB: storage device” appears in the history if the USB device connected is a storage device.
     - Confirm that “USB: unsupported device” appears in the history if the USB device connected is an unsupported device.

       * If not, there may be a problem with signal quality.

- Checking USB hub operation

  1. Connect a USB hub to the LSI. Confirm that “USB: VBUS overcurrent” does not appear in the history.

     * Otherwise, there may be a problem in the VBUS supply control circuit.

  2. Confirm that “USB: FS device” or “USB: HS device” appears in the history and matches the speed mode of the USB hub connected.

     * If not, there may be a problem with signal quality.

  3. Connect a USB device to the USB hub connected, and check that the history entry appears as shown below, depending on the type of USB device connected.

     - Confirm that the “USB: storage device” appears in the history if the USB device connected is a storage device.
     - Confirm that “USB: unsupported device” appears in the history if the USB device connected is an unsupported device.

       * If not, there may be a problem with signal quality.

4.3.3 Potential Communication Problems with USB Devices

This section describes communication problems with USB devices that can be inferred from history data.

If the following history data appears, the current drawn from the VBUS by the USB device may exceed the supply capacity.

- "USB: VBUS overcurrent"

If the following history data appears, there may be a problem in the USB device.

- "USB: phase err"

If the USB storage device continues to return NAK, the following history data will appear. As the LSI is executing commands, timeout processing should be performed and an ATA/ATAPI standard reset should be issued by the main CPU.

- "USB: CBW" appears in the history, but "USB: CSW" does not, with no status changes.
- "USB: Mass Storage Reset" or "USB: cleared STALL" appears at the end of the history, without any subsequent changes.

If the following combinations appear in the history data, there may be a conflict in the protocol between the USB host and the device. In this case, since an error status is returned to the main CPU, the error should be processed appropriately at the main CPU. If this state occurs other than when a command is being executed (Status register BSY bit is 1 or DRQ bit is 1), the USB device involved will be treated as an unsupported device.

- "USB: cleared STALL" – "USB: Mass Storage Reset" appear in history.
- "USB: phase err" – "USB: Mass Storage Reset" appear in history.

Appendix A Correspondence between Pins and ATA/ATAPI Standard Signals

Table A-1 indicates the correspondence between LSI pins and ATA/ATAPI standard signals.

Table A-1 Correspondence between terminals and ATA/ATAPI standard signals

BGA	QFP	Pin (IDE mode)	Pin (CPU mode)	ATA/ATAPI-6 standard signal
D8	54	HDA2_T	CA2	DA2
D6	52	HDA1_T	CA1	DA1
D5	51	HDA0_T	CA0	DA0
E6	50	XHCS1_T	XCS	CS1-
E7	49	XHCS0_T	CA3	CS0-
J6	33	XHIOR_T	XRD	DIOR-
G5	31	XHIOW_T	XWR	DIOW-
H5	30	HDMARQ_T	XDREQ	DMARQ
J5	29	XHDMACK_T	XDACK	DMACK-
H6	32	HIORDY_T	-	IORDY
F5	28	HINTRQ_T	XINT	INTRQ
E9	48	XHRESET_T	XHRESET	RESET-
E8	47	XHDASP_T	-	DASP-
F7	46	XHPDIAG_T	-	PDIAG-
F9	45	CSEL_T	CSEL	CSEL
D7	55	HDD15_T	CD15	DD15
C9	56	HDD14_T	CD14	DD14
C8	57	HDD13_T	CD13	DD13
C7	58	HDD12_T	CD12	DD12
B8	59	HDD11_T	CD11	DD11
A8	61	HDD10_T	CD10	DD10
B7	62	HDD9_T	CD9	DD9
A7	63	HDD8_T	CD8	DD8
C6	64	HDD7_T	CD7	DD7
B6	65	HDD6_T	CD6	DD6
C5	67	HDD5_T	CD5	DD5
B5	68	HDD4_T	CD4	DD4
A5	69	HDD3_T	CD3	DD3
D4	70	HDD2_T	CD2	DD2
C4	71	HDD1_T	CD1	DD1
B4	72	HDD0_T	CD0	DD0

Revision History

Date	Revision details			
	Rev.	Page	Type	Details
05/31/2007	0.10	All	New	Newly established
2007/07/01	1.00	1	Add	Added subclass details to history information precautions.
		6	Add	Added DRQ bit conditions to states allowing receipt of commands in Section 4.1.1.
		8	Correct	Corrected details for Section 4.1.12.
		15	Correct	Corrected details for Section 4.3.3.
04/01/2008	2.00	4, 5, 7, 8	Correct	Corrected details for Section 3.2, 3.3, 4.1.5 to 4.1.10.

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Document Code: 411136401
First Issue July 2007
Printed April 2008 in JAPAN