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S1R72U16
Application Note

SEIKO EPSON CORPORATION

Rev.2.00

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Scope

This document applies to the S1R72U16 IDE device - USB 2.0 host bridge LSI.

Notice

Before using the S1R72U16, carefully read the sections “Special use case for S1R72U16” and “S1R72U16 Errata.”

Table of Contents

1. Introduction

This LSI is designed to enable control of USB storage devices from the main CPU in compliance with the ATA/ATAPI-6 standards without a USB driver. Nor does it require modification of the ATA/ATAPI driver, provided the USB device is connected via this LSI and the IDE bus and not connected or disconnected as a product (system).

Table 1.1 shows the correspondence between the chapters of this document and the various development phases.

Table 1.1 Correspondence between chapters and development phases

Development phase	Chapter
Product concept	
System study	1. Introduction 2. System Configuration Examples 3. Driver Selection 4. Use with CPU 16-bit Local Bus (Memory Bus) Connections
System specification design	5. Data Transfer User Notifications Procedures
Software design	6. Initialization Procedure 7. Storage Device Control 8. Error Processing 9. Driver Changes for CPU Bus Connection 10. Connection/Disconnection Support 11. Download
Board design	
Evaluation	12. Interface Connection Verification 13. Development Support Functions

Note the following precautions when using the LSI. They are also included in the relevant sections of the *S1R72U16 Technical Manual*.

- Mode settings
  - Set the CSEL pin to Master (= Low) when using in two-device mode
- Device control
  - The maximum data size that can be transferred with a single command is 800000h bytes for Ultra DMA transfers in the DATA-OUT (Write) direction.
  - Connection/disconnection occurs as storage devices are temporarily disconnected while processing the DOWNLOAD MICROCODE command.
- USB devices
  - The supported USB devices are Bulk Only Transport Mass Storage Class, and Hub Class.
    - * Subclass UFI (SubClassCode value 04h) is not supported.
  - Up to two storage devices and up to three USB hubs may be connected. Any additional devices will be ignored.

- Connection/disconnection
  - The main CPU interrupt detection should be set to level detection when using the XChgInt pin as an interrupt signal in two-device mode.
  - Main CPU interrupt detection should be set to both rising and falling edge detection when using the XCD0 and XCD1 pins as interrupt signals.
- Clock selection
  - Make sure the CLKSEL pin settings match the frequency of the crystal oscillator used.

2. System Configuration Examples

Fig. 2.1 shows system configuration examples and LSI settings for various storage device connection methods.

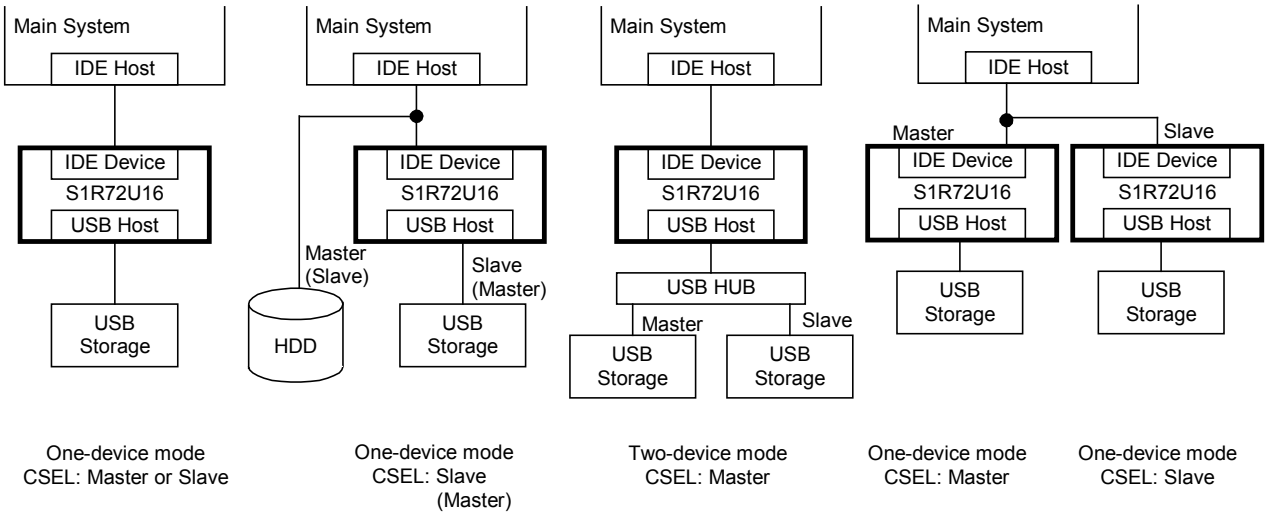


Fig. 2.1 System configuration examples and settings

3. Driver Selection

Storage devices such as Flash memory or HDDs with 512 bytes per sector can be controlled using ATA or CF (True IDE mode) drivers.

* Since this LSI does not implement attribute memory, the CF (True IDE mode) driver must always see this LSI as a CF without attribute memory. If the CF driver in use checks for the presence of a CF with attribute memory, add a modification to make such a CF appear present at all times to enable use of the LSI.

An ATAPI driver is required to control optical disk devices such as CD, DVD, or MO drives. Flash memory and HDD devices can also be controlled in ATAPI mode; use the ATAPI driver if unrestricted control of storage devices is needed.

4. Use with CPU 16-bit Local Bus (Memory Bus) Connections

This LSI offers the highest performance when used with IDE bus connections, but also includes a control mode using a CPU 16-bit local bus (hereafter "CPU bus") to enable use with CPUs that lack an IDE bus. This section describes use with CPU bus connections.

The following drivers can be used when the LSI is connected to a CPU bus.

- ATA/ATAPI driver
- CF (True IDE mode) driver
  * Since this LSI does not implement attribute memory, the CF (True IDE mode) driver must always see this LSI as a CF without attribute memory. If the CF driver in use checks for the presence of a CF with attribute memory, add a modification to make such a CF appear present at all times to enable use of the LSI.

These drivers can be obtained as follows:

- Use the drivers provided with the CPU or file system.
- Purchased from a software company.
- Use the sample ATA/ATAPI (CF (True IDE mode)) driver provided by Seiko Epson.
  * Use of software provided by Seiko Epson requires acceptance of the terms of the license agreement.

Using this LSI with these drivers requires the following modifications:

- Change I/O register address

The following changes may also be necessary.

- Change data transfer method if using DMA transfer for data transfers.
- Change interrupt processing if using interrupts from a device.

For details of the changes required, refer to 9. Driver Changes for CPU Bus Connection

5. Data Transfer User Notifications Procedures

The DASP signal may be used to notify to the user that the system is currently transferring data.

The DASP signal is used by the master device to detect the presence of a slave device during initialization processing. But after initialization is complete, it operates at Low during command processing (when the Status register BSY bit or DRQ bit is 1) and High at all other times. This means it may be used, for example, for access lamps, when data is being transferred.

For more information on signal operations, refer to the *S1R72U16 Technical Manual*.

6. Initialization Procedure

Fig. 6.1 illustrates the initialization sequence performed by the LSI after power is turned on.

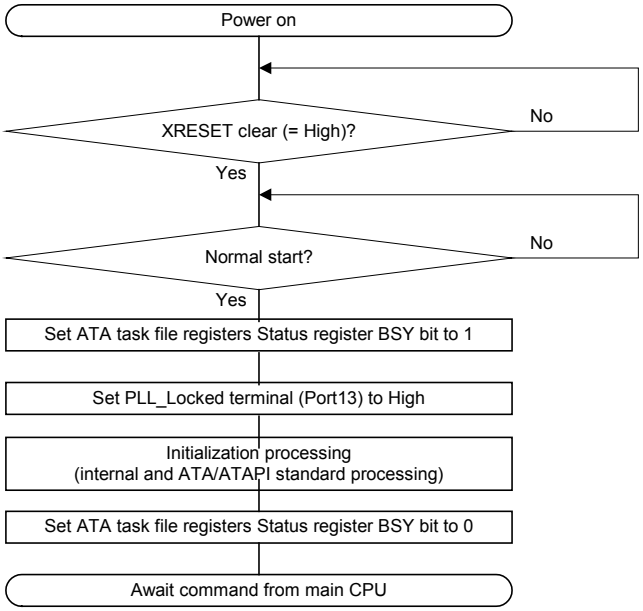


Fig. 6.1 LSI initialization sequence

The Status register BSY bit is set to 1 and the PLL_Locked pin (Port13) to High before initialization starts if the LSI starts up normally after the XRESET (chip reset) signal is cleared. The BSY bit is set to 0 once initialization is complete. This allows control of the LSI by the main CPU.

The main CPU should initiate the ATA/ATAPI standard initialization sequence after the BSY bit has switched to 0. Table 6.1 shows command examples for initialization.

Table 6.1 Commands used in initialization

Command type	Command Code	ATA protocol	Command Code/Operation Code	ATAPI protocol	Details
ATA command	ECh	IDENTIFY DEVICE	A1h	IDENTIFY PACKET DEVICE	Obtains device information
	EFh	SET FEATURES	EFh	SET FEATURES	Sets transfer mode, etc.
ATAPI command			12h	INQUIRY	Obtains device information
			25h	READ CAPACITY	Obtains record details

7. Storage Device Control

The LSI complies with *AT Attachment with Packet Interface – 6 (ATA/ATAPI – 6)*. Thus, storage devices should be controlled in compliance with these standards. It also complies with *AT Attachment with Packet Interface – 4, 5 (ATA/ATAPI – 4, 5)* to ensure backward compatibility, enabling control using CHS (Cylinder Header Sector).

Support for optical disk devices consists of compliance with the *Multi-Media Commands – 5 (MMC – 5)* CD/DVD commands, allowing control of CD, CD-RW, DVD, DVD±RW, and MO devices.

For more information on supported ATA/ATAPI commands, refer to the *S1R72U16 Technical Manual*.

8. Error Processing

This section describes the error specifics and appropriate corrective measures.

8.1 Command Errors

The main CPU should perform error processing when the LSI returns an error status in response to ATA/ATAPI commands issued by the main CPU. Tables 8.1 and 8.2 list errors.

Table 8.1 ATA command errors (when Status register ERR bit is 1)

Error data (Error register bit))	Meaning	Corrective action
ABRT=1	Command not supported by storage device.	Issue a different command or change the storage device.
	Storage device returns an error.	
	Storage device is disconnected.	Refer to “10. Connection/Disconnection Support.”
ABRT=1、IDNF=1	Main CPU specified non-accessible LBA/CHS.	Re-obtain storage device information and issue command specifying accessible LBA/CHS.
ABRT=1、ICRC=1	CRC error was detected during Ultra DMA transfer.	Potential problem with IDE signal quality. Check wiring.
MC=1	Media or storage device was changed.	Refer to “10. Connection/Disconnection Support.”
NM=1	Media or storage device does not exist.	Refer to “10. Connection/Disconnection Support.”

Table 8.2 ATAPI command errors (when Status register CHK bit is 1)

Error data (REQUEST SENSE value)			Connect/disconnect notification	Meaning	Corrective action
Sense Key	ASC	ASCQ			
04h	08h	00h	–	Error occurred in USB protocol.	Problem with storage device. Change storage device.
			–	No response from storage device.	
06h	28h	00h	Yes	Storage device was connected.	Perform storage device mounting processing.
			No	Media was changed.	Process in accordance with ATA/ATAPI standards.
02h	3Ah	00h	Yes	Storage device was disconnected.	Perform storage device unmounting processing.
			No	Media was removed.	Process in accordance with ATA/ATAPI standards.
In other cases			Process in accordance with ATA/ATAPI standards.		

8.2 Remain in Busy State

The LSI remains in Busy state (Status register BSY bit or DRQ bit is 1) while the storage device continues to return NAK on the USB bus protocol. Timeout processing should be performed at the main CPU when using such storage devices. Issuing an ATA/ATAPI standard Hardware Reset as part of the timeout processing will result in a reset from Busy state.

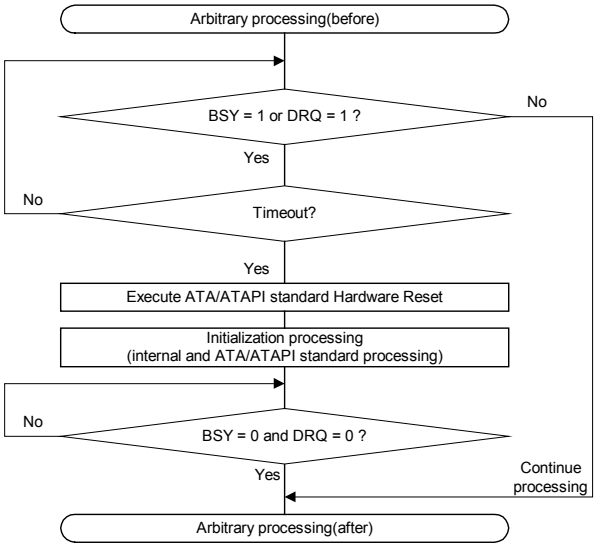


Fig. 8.1 Typical timeout processing

9. Driver Changes for CPU Bus Connection

9.1 Register Mapping for CPU Bus Connection

The ATA/ATAPI driver of the main CPU exerts controls by accessing the IDE control registers normally found in the main CPU. For connections via a CPU bus, the control registers will be the ATA task file registers themselves mapped to the main CPU memory map. Accordingly, the I/O register access section of the driver must be modified for CPU bus connections.

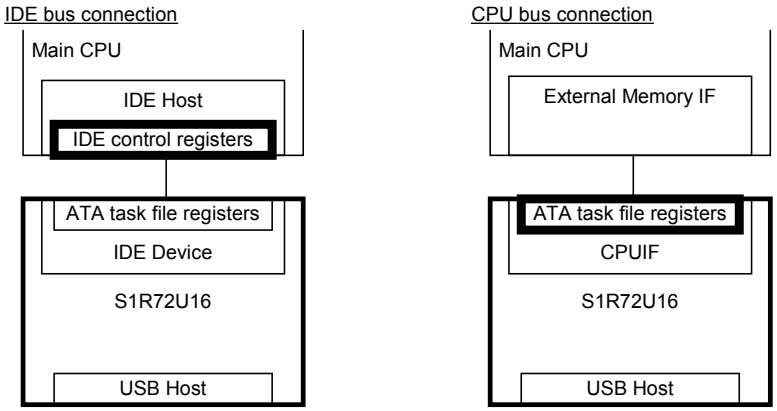


Fig. 9.1 Control register outline

9.2 Register Access and Endian for CPU Bus Connections

The data bus is a little endian 16-bit bus. The data register only allows 16-bit access. Other register values are valid only for lower addresses.

The 16-bit data obtained from the data bus must be swapped if the main CPU is big endian.

Table 9.1 CPU mode ATA task file register map

OFFSET	ATA task file registers	
	READ	WRITE
00h	Data (16bit)	
01h		
02h	Error	Feature
03h		
04h	Sector Count	
05h		
06h	LBA Low	
07h		
08h	LBA Mid	
09h		
0Ah	LBA High	
0Bh		
0Ch	Device	
0Dh		
0Eh	Status	Command
0Fh		

OFFSET	ATA task file registers	
	READ	WRITE
10h	none	
11h		
12h	none	
13h		
14h	none	
15h		
16h	none	
17h		
18h	none	
19h		
1Ah	none	
1Bh		
1Ch	Alternate Status	Device Control
1Dh		
1Eh	none	
1Fh		

* OFFSET is the first address of the memory area assigned for the LSI I/O register.

9.3 I/O Register Address Changes

The driver accesses the registers shown in Table 9.2 to control the device.

Table 9.2 I/O Registers

ATA task file registers (*1)		
Operation	**READ**	**WRITE**
Register	Data	
	Error	Features
	Sector Count	
	LBA Low (Sector Number *2, *3)	
	LBA Mid (Cylinder Low *2, *3)	
	LBA High (Cylinder High *2, *3)	
	Device (Device/Head *2) (Select Card/Head *3)	
	Status	Command
	Alternate Status	Device Control

*1 Registers are referred to as ATA Task File registers or Task File registers.

*2 Register names defined in standards predating *AT Attachment with Packet Interface – 5 (ATA/ATAPI-5)*

*3 Register names defined in *CompactFlash Specifications*

The registers shown in Table 9.2 are mapped onto the CPU memory area shown in Table 9.1 when the LSI is connected to the CPU bus. The I/O register address defined by the driver should be modified to the I/O register address for the LSI mapped onto the CPU memory area.

9.4 Changing Data Transfer Method

The PIO transfer and DMA transfer are available in CPU bus connection. As for the DMA setting of this LSI, please use Multi Word DMA. (Ultra DMA is not able to use it)

A DMA controller capable of transferring data between the device and memory connected via the CPU bus should be used for DMA transfers with the LSI. For detailed information on DMA controller control methods, refer to the manual for the CPU used or contact the CPU manufacturer.

9.5 Changing Interrupt Processing

To use interrupts from this LSI in the driver, use the XINT signal and modify the interrupt handler to ensure interrupts are notified to the driver.

10. Connection/Disconnection Support

For supporting storage device connection/disconnection, a software in the main CPU should correspond to the processing (e.g. detecting connection/discconection, mount/unmount proccessing by application software). The LSI includes the pins (connection/disconnection pins) and registers shown in Table 10.1. Their use allows the main CPU to detect storage device connection and disconnection. For more information on connection/disconnection pins and register, refer to the *S1R72U16 Technical Manual*.

Table 10.1 Connection/disconnection pins and registers

Pin/register	Description
XCD0 pin	Indicates the storage device connection status.
XCD1 pin	
XchgInt pin	Indicates the occurrence of a storage device connection or disconnection.
ChgInt bit (ATA task file registers Status register bit1)	

If the main CPU lacks free pins for connecting the connection/disconnection pins, the connection status of storage devices can be obtained by issuing ATA/ATAPI commands. For detailed information, refer to “10.2.5 When Using Only ATA/ATAPI Commands.”

Note that media connection and disconnection cannot be detected using the connection/disconnection pins or ChgInt bit for CD/DVD drives or multi-card reader devices. Detect media status by issuing commands for obtaining their status.

10.1 Storage Device Mounting/Unmounting

Fig. 10.1 shows a typical status transition when the main CPU supports connection and disconnection.

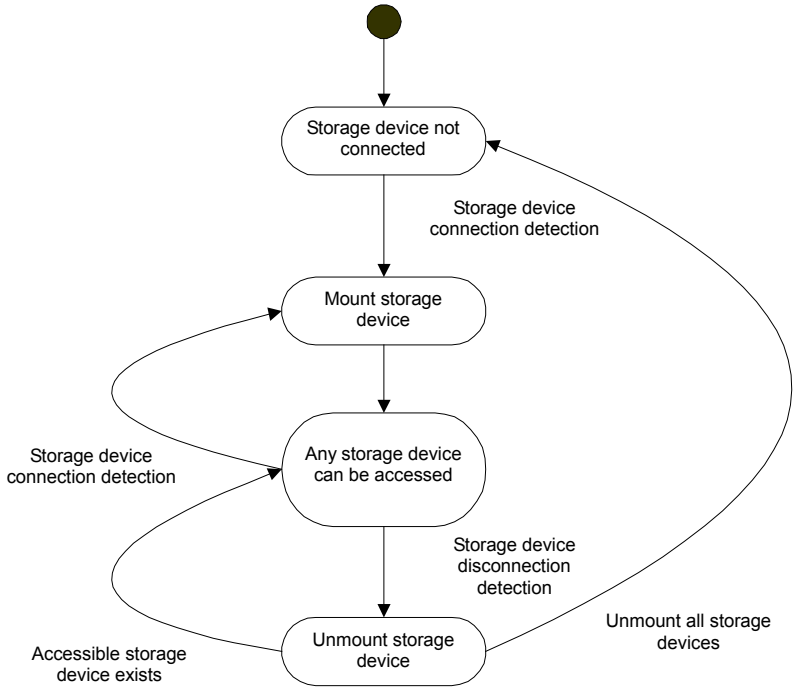


Fig. 10.1 Typical status transition when connection/disconnection is supported

The main CPU should perform mounting processing on detecting storage device connection and unmounting processing on detecting disconnection. The main CPU should issue the commands shown in Table 10.2 to the LSI for mounting and unmounting processing. Connection and disconnection notification will not be issued correctly to the LSI if these commands are not issued by the main CPU. There is no need to issue the commands in Table 10.2 when not using the XchgInt pin or ChgInt bit.

Table 10.2 Commands required for storage device mounting and unmounting

ATA/ATAPI mode	Command for mounting	Command for unmounting
ATA mode	IDENTIFY DEVICE	Any command in ATA mode listed in Table 10.3
ATAPI mode	INQUIRY	Any command in ATAPI mode listed in Table 10.3
	READ CAPACITY	

The main CPU connection/disconnection detection methods are described below.

10.2 Storage Device Connection/Disconnection Detection Methods

The main CPU should detect storage device connection or disconnection by one of the following methods and perform the appropriate mounting or unmounting processing.

10.2.1 When Using Only XCD0/XCD1 Pins

The XCD0/XCD1 pins are monitored to detect storage device connection or disconnection. These pins can also be used for interrupts or polling. The pins indicate the connection status of the storage device regardless of IDENTIFY DEVICE or IDENTIFY PACKET DEVICE commands received or ATA/ATAPI standard resets (Hardware Reset, SRST, or DEVICE RESET command).

When using an interrupt signal, read the pin status when an interrupt occurs and perform mounting processing if Low and unmounting processing if High. When using a polling, perform mounting processing when the status changes from High to Low and unmounting processing when the status changes from Low to High.

10.2.2 When Using XchgInt and XCD0/XCD1 Pins

The XchgInt pin is used to detect connection or disconnection. XCD0/XCD1 pins are used to obtain the storage device connection status. The XchgInt pin may be used for either interrupts or polling. When the XchgInt pin is used as an interrupt signal, the XCD0/XCD1 pins status should be read when an interrupt occurs, followed by mounting processing if Low and unmounting processing if High. When the XchgInt pin is used for polling, the XCD0/XCD1 pins status should be read when the status changes from High to Low.

10.2.3 When Using XchgInt Pin and Commands

Connection or disconnection is detected by the XchgInt pin. The storage device connection status is obtained by issuing commands. The main CPU should issue the commands shown in Table 10.3 to obtain the storage device connection status before performing mounting or unmounting processing, depending on storage device status. The XchgInt pin is used in the same way as described in “10.22 When Using XchgInt and XCD0/XCD1 Pins.”

In two-device mode, issue commands to both master and slave devices, since the XchgInt pin is not capable of determining whether a connection or disconnection occurred in the master or the slave storage device.

Table 10.3 Connection status obtainable by issuing commands

ATA/ATAPI mode	Command	Data position	Value	Status
ATAPI mode	IDENTIFY PACKET DEVICE	Word0: bit8 to 12 (Device Type)	Except 1Fh	Connected
			1Fh	Disconnected
	INQUIRY	Byte0: bit0 to 4 (Device Type)	Except 1Fh	Connected
			1Fh	Disconnected
ATA mode	IDENTIFY DEVICE	Word60～61 (Total LBA)	Except 0000h	Connected
			0000h	Disconnected
	GET MEDIA STATUS	Error register	Except 02h or 20h	Connected
			20h (MC: Media Change)	Connected: Single notification immediately after device connection
			02h (NM: No Media)	Disconnected
	READ/WRITE commands READ SECTOR(S) READ SECTOR(S) EXT READ DMA READ DMA EXT READ MULTIPLE READ MULTIPLE EXT READ VERIFY SECTOR(S) READ VERIFY SECTOR(S) EXT WRITE SECTOR(S) WRITE SECTOR(S) EXT WRITE DMA WRITE DMA EXT WRITE MULTIPLE WRITE MULTIPLE EXT	Error register	Except 02h or 20h	Connected
			20h (MC: Media Change)	Connected: Single notification immediately after device connection
			02h (NM: No Media)	Disconnected

* Media Change and No Media are bits in the ATA task file register Error register. For detailed information, see the ATA/ATAPI-4, -5, -6 standards.

10.2.4 When Using ChgInt Bit instead of XchgInt Pin

The ChgInt bit (ATA task file registers Status register bit) may be used instead of the XchgInt pin. This bit operates in the same way as the XchgInt pin, except that the logic is reversed. The ChgInt bit may be used for polling only. The ChgInt bit may be used replacing the XchgInt pin described in “10.2.2 When Using XchgInt and XCD0/XCD1 Pins” and “10.2.3 When Using XchgInt Pin and Commands.” The ChgInt bit value changing from 0 to 1 indicates that a connection or disconnection has occurred.

10.2.5 When Using Only ATA/ATAPI Commands

The main CPU can obtain the storage device connection status by periodically issuing ATA/ATAPI commands. The confirmation methods are described below for different command system settings.

10.2.5.1 ATA Mode Checking Method

In ATA mode, the main CPU can obtain the storage device connection status by periodically issuing the GET MEDIA STATUS command. In two-device mode, the command should be issued to both master and slave devices. Table 10.4 shows the information returned by the LSI in response to the GET MEDIA STATUS command.

Table 10.4 Information returned for GET MEDIA STATUS command

Data position	Value	Status
Error register	00h (No error)	Storage device connected
	20h (MC: Media Change)	Storage device connected: Single notification immediately after device connection
	02h (NM: No Media)	Storage device not connected

10.2.5.2 ATAPI Mode Checking Method

In ATAPI mode, the main CPU can obtain the storage device connection status by issuing the TEST UNIT READY and REQUEST SENSE commands. In two-device mode, the commands should be issued to both master and slave devices.

The TEST UNIT READY command should be issued periodically. The REQUEST SENSE command should be issued to obtain error information when the LSI returns an error status in response to the TEST UNIT READY command. The storage device connection status can then be obtained from the error information obtained using the REQUEST SENSE command, together with the ChgInt bit value. Table 10.5 shows the error information returned by the REQUEST SENSE command and the ChgInt bit values.

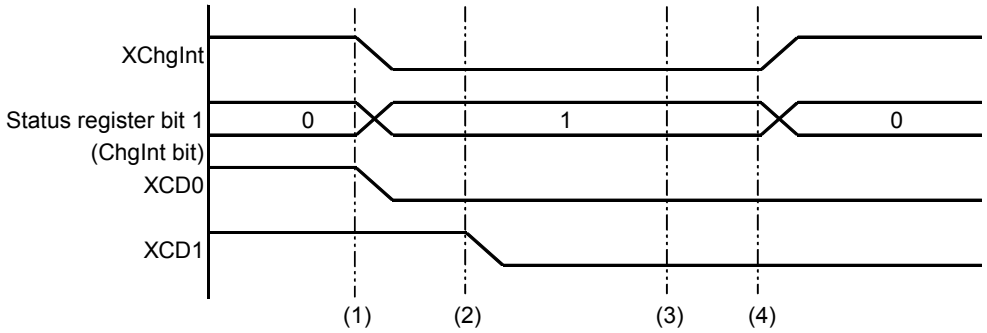
Table 10.5 Error information returned by REQUEST SENSE command and ChgInt bit values

Error information			ChgInt value	Status
Sense Key	ASC	ASCQ		
06h	28h	00h	1	Storage device was connected
			0	Storage device connection unchanged Storage device media was changed
02h	3Ah	00h	1	Storage device was disconnected
			0	Storage device connection unchanged Storage device media was removed

10.2.6 Precautions When Using XchgInt Pin as Interrupt Signal

The XchgInt pin must be used in conjunction with the XCD0 or XCD1 pins or commands, since it is not capable of determining storage device connection status alone. Take the following precautions for interrupt detection methods when using this pin as an interrupt.

- One-device mode
  - Use falling detection or Low level detection for interrupt detection.
- Two-device mode
  - Use Low level detection for interrupt detection.
    Fig. 10.2 illustrates operations when a slave storage device is connected while the XchgInt pin is Low with a master storage device connected. In this case, Low level detection is necessary for interrupt detection to detect connection or disconnection of both the master and slave devices.



(1) Master storage device is connected.

(2) Slave storage device is connected.
XchgInt pin is Low, and ChgInt bit remains at 1.

(3) Receipt of command for master satisfies conditions for XchgInt pin to change to High.
XchgInt pin is Low and ChgInt bit remains at 1, since conditions are not satisfied for slave.

(4) Receipt of command for slave satisfies conditions to change the XchgInt pin to High.
XchgInt pin changes to High and ChgInt bit changes to 0, since conditions are satisfied for both master and slave.

Fig. 10.2 Pin operations for connection/disconnection when XchgInt pin is Low in two-device mode

11. Download

The LSI features a download function and uses the ATA command DOWNLOAD MICROCODE (92h). For more information on the download function and TPL, refer to the *S1R72U16 Technical Manual*.

11.1 Download Command

Table 11.1 shows DOWNLOAD MICROCODE command parameters. Data transfer phase shall use PIO transfer, since this is a PIO Data Out command. The Sector count field uses the sector size to set the transfer size for data downloaded to the LSI. This is an ATA standard command; one sector corresponds to 512 bytes. The data should therefore be padded with 00h if the download data byte size is not a multiple of the sector size.

The main CPU can issue DOWNLOAD MICROCODE commands as required. The data downloaded remains valid until LSI power is turned off. The command should be issued during system initialization (after the Status register BSY bit changes to 0) after power is turned on, since the LSI operation will vary depending on the data downloaded before and after downloading. Download data applies for a single DOWNLOAD MICROCODE command issued to either master or slave in two-device mode. There is no problem even if the command is repeatedly issued..

Download data includes TPL data and Update data. Only one download data item can be downloaded each time a DOWNLOAD MICROCODE command is issued. To use both TPL data and Update data in the LSI, the DOWNLOAD MICROCODE command must be issued separately for each set of data.

Table 11.1 DOWNLOAD MICROCODE parameters

Register	7	6	5	4	3	2	1	0
Features	Subcommand code = 01h							
Sector Count	Sector count (low order)							
LBA Low	Sector count (high order)							
LBA Mid	00h							
LBA High	00h							
Device	obs	na	obs	DEV	0	0	0	0
Command	92h							

* obs (discontinued bit) and na (bits not requiring setting) can be set to 0.

11.2 TPL Data

TPL data is used when the parameters shown in Table 11.2 are used to restrict storage devices supported by the product (system). Downloading TPL data disables support for devices other than the specified storage devices and USB hubs. Support for USB hubs cannot be disabled.

Table 11.2 lists the values that can be specified with TPL data and the default values for the LSI. Parameters not flagged as enabled will be set to default values.

TPL data can be generated easily using tools provided by Seiko Epson.

If connection (or disconnection) processing is not performed until TPL data is enabled, ignore connection/disconnection notifications by connection/disconnection pins until the DOWNLOAD MICROCODE command has finished executing.

Table 11.2 TPL data parameters and specifiable values

Parameter	Details	Values specifiable by TPL data	Default value
idVendor	Vendor ID	0000h to FFFFh	Support all values
idProduct	Product ID	0000h to FFFFh	Support all values
bcdDevice	Device revision	0000h to FFFFh	Support all values
bClass	Class ID	08h	08h
bSubClass	Subclass ID	01h, 02h, 03h, 05h, 06h	Support all except 04h
bProtocol	Protocol ID	50h	50h
Flag	Parameter enable flag	0xxx0xxxb (3rd and 7th bits are disabled)	–

11.3 Update Data

Update data is used when updating LSI functions.

12. Interface Connection Verification

This LSI's serial interface may be used to verify the connection between the main CPU and the LSI and between the USB device and the LSI. For detailed information, refer to the *S1R72U16 Development Support Manual*.

13. Development Support Functions

The LSI includes the following two functions to support product (system) development.

- History display function
- USB logo certification support function

These functions may be used once the PORT13 pin (PLL_Locked) is set to High.

The History display function enables viewing, on a PC, of various details, including LSI internal IDE/USB status, detected USB devices, and transfer history. It also enables connection verification between the main CPU and the LSI, as well as simple debugging using transfer history. For detailed information, refer to the *S1R72U16 Development Support Manual*.

The USB logo certification support function is used to switch to the test mode corresponding to the electrical test as part of certification testing. For detailed information, refer to the *S1R72U16 Embedded Host Compliance Guide*.

Revision History

Date	Revision details			
	Rev.	Page	Type	Details
05/31/2007	0.10	All	New	Newly established
07/01/2007	1.00	1	Correct/ add	Corrected Table 1.1 to incorporate changes to section, and add subclass details to precautions.
		4	Correct	Changed Driver Selection from Section 4 to Section 3.
		5	Add	Added “Use with CPU 16-bit Local Bus (Memory Bus) Connections” as Section 4.
		5	Add	Added details of Status bit to Section 5 indicating that command is being processed.
		8	Add	Added details of Status bit to Section 8.2 indicating Busy state.
		9 to 11	Add	Added “Driver Changes for CPU Bus Connection” as Section 9.
		12 to 21	Correct	Renumbered sections from Section 10 onward.
		18	Correct	Revised Fig. 10.2 to correspond to Technical Manual.
		19	Add	Added details of Download command and Update data.
		20	Correct	Changed order within Section 11.2.
10/15/2007	1.10	Scope	Add	Added “notice.”
		3 and 4	Correct	Changed “CF” to “CF (True IDE mode)”; added restrictions on CF driver.
04/01/2008	2.00	3, 5, 6, 7, 9, 10, 14, 16, 19	Correct	Corrected details for Fig. 2.1, 8.1. Corrected details for Table 6.1, 8.1, 9.1, 10.3, 10.5, 11.2. Corrected details for Section 9.4.

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