S1C17803

EPSON
EXCEED YOUR VISION

CMOS 16-bit Application Specific Controller

- 16-bit RISC CPU Core S1C17 (Max. 33 MHz operation)
- 128K-Byte Flash ROM
- 16K-Byte RAM (IVRAM are shared by CPU and LCDC)
- DSP function (Multiply, Multiply and Accumulation, Division)
- 10-bit ADC
- I^2S Audio DAC Interface
- Infrared Remote Control Circuit
- Multi DMA circuit (for standard DMA and LCD driver DMA)
- USI (Universal Serial Interface)
  (UART/SPI/I^2C)
- Built-in STN LCD Controller
  Support QVGA (320 × 240) in 1 bpp Mode using IVRAM
  Support QVGA (320 × 240) in 4 bpp Mode or VGA (640 x 480) in 1bpp Mode using External VRAM
  NAND Flash Card Interface
- 5V single power operation can be realized by 3V to 5V regulator.

■ DESCRIPTIONS

Many kinds of machine like white goods (eg. Washing machine, rice cooker, and coffee maker) can be improved User Interface using display, music, voice, touch panel and etc.
It can be operated by 5V single power supply using built-in 5V to 3V regulator.
It is separated three groups IO, each group can be set arbitrarily voltage by Multi voltage IO (MVIO).It can be realized the system which mixed 3V and 5V devices easier without level shifter.
Internal LCDC supports QVGA panel (Black and white) without external memory, and it supports to display VGA STN LCD panel (Black and white) or QVGA STN LCD panel (16-gray scale) with external SRAM .
It also supports an LCD driver DMA function to interface with an EPSON S1D15xxx built-in RAM LCD driver and a driver with an SPI. Therefore, it can connect with many kind of LCD driver.
DSP function has 16×16bits MUL (Multiply) instruction, 16×16＋32bits MAC (Multiply and Accumulation) instruction, and 16÷16bits DIV (Division) instruction. As a result, load of CPU in the voice reproduction processing etc. is reduced.
RTC and BBRAM can operated in an independent power supply.
Great Energy-saving can be attempted by stopping the power supply to other circuits.

LINEUP

	Flash ROM	RAM	PKG
1	128K bytes	16K bytes (shared with VRAM)	TQFP14-100pin (0.4mm pitch)
2	128K bytes	16K bytes (shared with VRAM)	TQFP15-128pin (0.4mm pitch)
3	128K bytes	16K bytes (shared with VRAM)	QFP5-128pin (0.5mm pitch)

■ FEATURES

● Technology

0.35 µm AL-4-layers mixed analog low power CMOS process technology

● CPU

Seiko Epson original 16-bit RISC processor S1C17 Core
Internal 3-stage pipeline
Instruction set
- 16-bit fixed length
- 111 basic instructions (184 including variations)

- Compact and fast instruction set optimized for development in C language

Registers

- Eight 24-bit general-purpose registers
- Three special registers (24-bit × 2, 8-bit × 1)

Memory space

- Up to 16M bytes accessible (24-bit address)

● **DSP**

MUL (Multiply)	16 × 16bits (1 cycle)
MAC (Multiply and Accumulation)	16 × 16 + 32bits (1 cycle)
DIV (Division)	16 ÷ 16bits (17 to 20 cycles)

● **Internal Memories**

Flash EEPROM	128K bytes
RAM	16K bytes (shared with VRAM)
BBRAM	16 bytes (for Battery Backup)

● **Operating Clock**

Main clock

- 1 to 33 MHz (can be divided by 1 to 32) or 32.768 kHz
- On-chip oscillator (crystal or ceramic) or external clock input

Sub clock

- 32.768 kHz (typ.) for the RTC
- On-chip oscillator (crystal)

● **Interrupt Controller**

Four non-maskable interrupts

- Reset (#RESET pin or watchdog timer)
- Address misaligned
- Debug
- NMI (#NMI pin or watchdog timer)

18 maskable interrupts TBD

- Port inputs (two systems)
- DMA (one system)
- 16bits timer (one system)
- 8bits timer (one system)
- USI (one system)
- ADC (one system)
- PWM (one system)
- I^2S (one system)
- LCDC (one system)
- 16-bit timers of clock generator (one system)
- 8-bit timers of clock generator (one systems)
- UART (one system)
- I^2C Master (one system)
- I^2C Slave (one system)
- RTC (one system)
- REMC (one system)
- The interrupt level (priority) of each maskable interrupt system is configurable (levels 0 to 7).

● **SRAM Controller**

Provides a 23-bit external address bus, an 8- or 16-bit width selectable data bus, and four chip enable signals to support a maximum of 16M-byte external memory space.
Provides an SRAM UMA feature to access an external VRAM for supporting up to 16-grayscale QVGA LCD panel.

● **PSC (Prescaler)**

Generates the source clocks for the clock generator.

● **CLG (Clock Generator)**

1 channel of 8-bit timer and 2 channels of 16-bit timer are available
These timers are for UART, SPI, I^2C and multi SIO.
Each timer can generate an underflow interrupt.

● **PWM Control Capture 16-bit Timer/Counter**

2 channels of 16-bit timer/counter with PWM output function is available.
Each timer can generate 2 compare-match interrupts.
3 type Bit division function is available (10bits + 6bits, 9bits + 7bits, 8bits + 8bits)
PWM function for sound supports 8bits and 16bits PCM data.
Can output monaural sound without external DAC

● **T8 (8-bit Timer)**

3 channels of 8-bit timer (pre-settable down counter) are available.
Clock generated with the counter underflow can be output to external devices.
Can be used as an interval timer to trigger the ADC and the USI.
Each timer can generate an underflow interrupt.

● **T16A (16-bit Timer)**

1 channels of advanced 16-bit timer (pre-settable down counter) are available.
Capture function is available.
Can use 2 compare value at the same time

● **Watchdog Timer**

30-bit watchdog timer to generate a reset or an NMI
The watchdog timer overflow period (reset or NMI interrupt period) is programmable.
The watchdog timer overflow signal can be output outside the IC.

● **RTC**

Contains time counters (second, minute, and hour) and calendar counters (day, day of the week, month, and year).
The power source separated with the system power supply (LVDD/HVDD) can be used.
Provides the WAKEUP output pin and #STBY input pin to control standby mode.
Periodic interrupts are possible.

● **UART**

1 channels of UART is available.
Supports IrDA 1.0 interface.
2-byte receive data buffer and one-byte transmit buffer are built in to support full-duplex communication.
Transfer rate: 150 to 460800 bps, character length: seven or eight bits, parity mode: even, odd, or no parity, stop bit: one or two bits

Parity error, framing error, and overrun error detectable
Each channel can generate receive buffer full, transmit buffer empty, and receive error interrupts.

● **SPI**

Supports both master and slave modes.
One-byte receive data buffer and one-byte transmit buffer are built in.
Data length: eight bits fixed (MSB first)
Data transfer timing (clock phase and polarity variations) is selectable from among 4 types.
Can generate receive buffer full and transmit buffer empty interrupts.

● **I^2C**

Supports 1 of master and 1 of slave mode.
Data format: 8 bits (MSB first)
Addressing mode: 7-bit addressing (10-bit addressing is not supported.)
Supports the noise reject function controlled by a register.
Can generate an I^2C interrupt.

● **USI**

2 channels of Multi serial interface is available for UART, SPI or I^2C.
SPI and I^2C master or slave mode can be selected
Can generate an USI interrupt.

● **I^2S**

Supports universal audio I^2S Bus Interface.
One I^2S output channel in 16-bits resolution.
Operates as the master to generate the bit clock, word-select signal, data and master clock.
Can generate an I^2S interrupt.

● **CARD Interface**

Generates 8- or 16-bit NAND Flash interface signals.
The ECC function should be implemented in the application program.

● **REMC (Infrared Remote Controller)**

Outputs a modulated carrier signal and inputs remote control pulses.
Embedded carrier signal generator and data length counter.
Can generate REMC interrupts.

● **DMA**

4 channels table DMA
Reload and pause function is available.
DMA function for LCD driver interface is available.
Trigger source

- USI (SPI/I^2C) data receive and transmit.
- I^2S
- PWM
- ADC

● **LCD Controller**

STN LCD controller
Supports up to 16 gray shades using FRM (Frame Rate Modulation).

1/2/4 bpp (2/4/16 grayscale) monochrome LCD interface (bpp: bit-per-pixel)
16K-byte IVRAM (internal VRAM)
- Can be used to display up to 320 × 240 LCD panels in 1 bpp mode.
- The IVRAM arbiter is provided allowing the CPU and LCD controller to access the IVRAM via the SRAM controller.

The UMA feature allows use of an external SRAM as the VRAM.
- Expands the display size up to QVGA (320 × 240) panels in 4 bpp (16-grayscale) mode or VGA (640 x 480) panels in 1 bpp mode.

Supports 16-bit SRAMs for the external VRAM. (8-bit SRAMs are not supported.)
- The EVRAM arbiter is provided allowing the CPU and LCD controller to access the external VRAM via the SRAM controller.

Supports an LCD driver DMA function
- Allows display data transfer to the external LCD driver with no software control.

Supported displays

- Single panel
- Single drive passive display
- Monochrome/grayscale STN LCD panel with a 4/8-bit data bus width SLA or MLA type LCD driver
- LCD panels with a 4/8-bit parallel MCU interface LCD driver
  (LCD segment/common driver with controller)
  The 80 series parallel MCU interface is supported.
  This interface allows writing to and reading from the external LCD driver.
- LCD panels with an LCD driver that supports 8/9-bit SPI
  Supports 8-bit SPI with 4 lines (SCK, SDA, D/#C, #CS: 8-bit data).
  Supports 9-bit SPI with 3 lines (SCK, SDA, #CS: 8-bit data + D/#C).
- LCD panels with a built-in RAM LCD driver that supports 8/9-bit SPI
  Supports 8-bit SPI with 4 lines (SCK, SDA, D/#C, #CS: 8-bit data).
  Supports 9-bit SPI with 3 lines (SCK, SDA, #CS: 8-bit data + D/#C).
  This interface allows only writing to the external LCD driver (it does not support reading from the LCD driver).

Supported drivers

- EPSON S1D15xxx built-in RAM LCD drivers
- STN LCD drivers with a 4/8-bit parallel MCU interface
  (LCD segment/common driver with controller)
  The 80 series parallel MCU interface is supported.
  This interface allows writing to and reading from the external LCD driver.
- STN LCD drivers that support SPI
  Supports 8-bit SPI with 4 lines (SCK, SDA, D/#C, #CS: 8-bit data).
  Supports 9-bit SPI with 3 lines (SCK, SDA, #CS: 8-bit data + D/#C).
  This interface allows only writing to the external LCD driver
  (it does not support reading from the LCD driver).

● **ADC**

10-bit A/D converter with up to 4 analog input ports
Can generates an end of conversion interrupt and an out of range interrupt.

● **GPIO (General-Purpose I/O Ports)**

Maximum 93 I/O ports and 4 input ports are available. (TBD)

Can generate input interrupts from the 29 ports selected with software.(P2x, P4x, P8x, PAx)

*The GPIO ports are shared with other peripheral function pins (UART, PWM etc.). Therefore, the number of GPIO ports depends on the peripheral functions used.

● **Regulator**

5V to 3V conversion

5V single power supply operation

● **Multi I/O voltage**

The each IO group of three (IO1, IO2, Bus) can be selected interface voltage.

● **Operating Voltage**

IOVDD1:	2.70～5.50V
IOVDD2:	2.70～5.50V
BUSVDD:	2.70～5.50V
LVDD:	2.70～3.60V
RTCVDD:	2.70～3.60V
AVDD(I/O):	2.70～5.50V
RGVDD:	4.50～5.50V

● **Operating Temperatures**

-40 to 70°C (Flash memory Erase/Write)

-40 to 85°C (Excluding the above-mentioned)

● **Power Consumption**

Battery Backup (for memory): 0.085 µA

Battery Backup (for clock, memory): 3.7µA

Sleep mode: 6 µA

Halt mode (33MHz): 11 mA

Operating (33 MHz): 32 mA

* By controlling the clocks through the Clock-Gear (CMU), power consumption can be reduced.

*These figures are for reference only, based on 3.3V usage without a regulator. Actual figures will depend on circuit operation and core CPU processing.

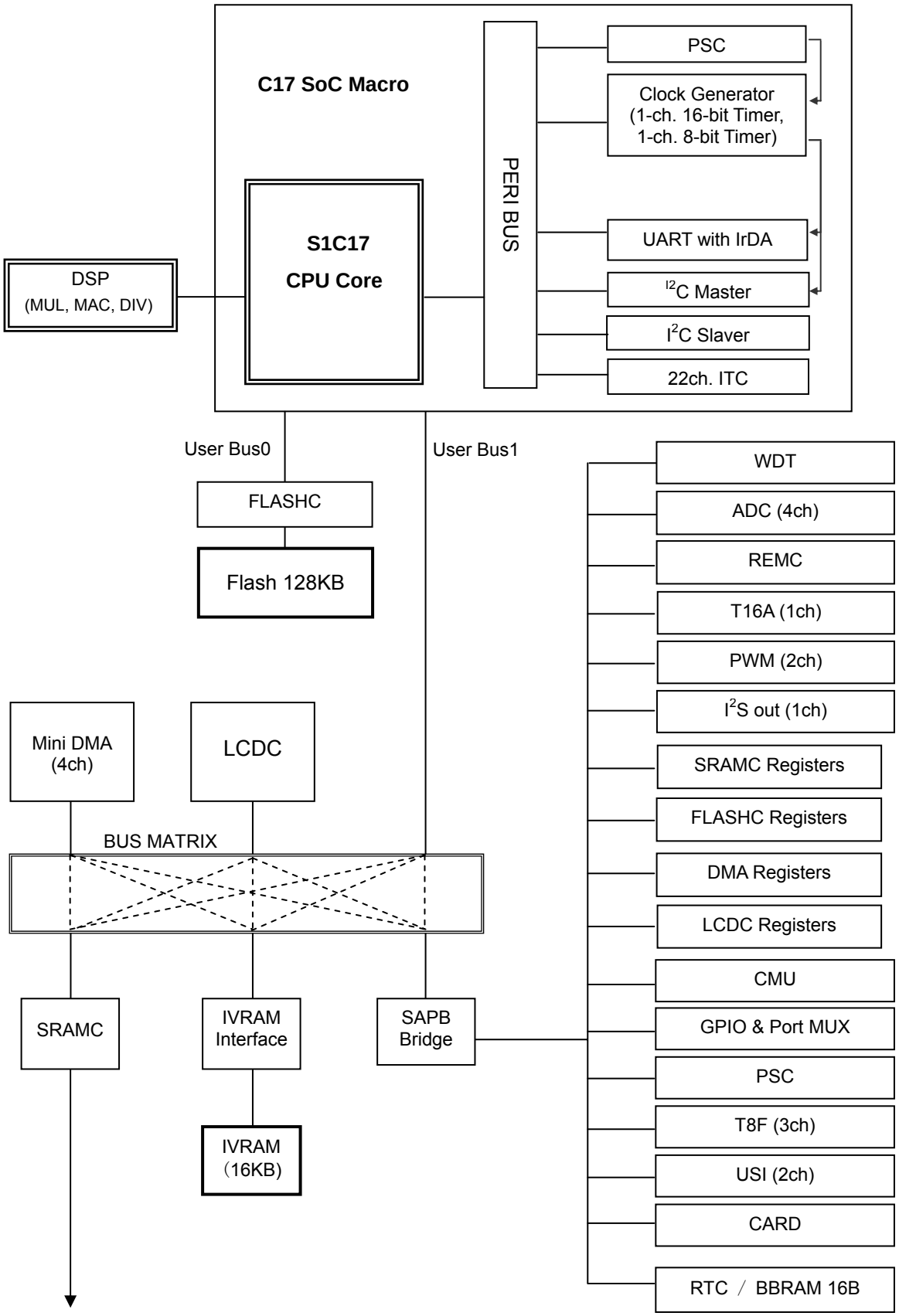
● **Shipping Form**

Package: TQFP14-100pin (12 mm × 12 mm × 1.2 mm, 0.4 mm pin pitch)

Package: TQFP15-128pin (14 mm × 14 mm × 1.2 mm, 0.4 mm pin pitch)

Package: QFP5-128pin (14 mm × 20 mm × 3.5 mm, 0.5 mm pin pitch)

■ Block diagram



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