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35bits Channel Link LVDS receiver

S1R77082F00A000
Technical Manual

SEIKO EPSON CORPORATION

Rev.0.2

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Table of Contents

1. DESCRIPTION

This IC “S1R77082” is a LVDS receiver IC.

S1R77082 recieves the 5 channels LVDS data stream and restore it to 35 bits CMOS/TTL data.

When transmitter clock frequency is 115 MHz, 35 bits CMOS/TTL data is transferred at 805Mbps per channel. When using 115 MHz clock, total throughput is 4,025Gbps (503 Mbytes/s).

“S1R77092” is recommended to use for LVDS transmitter IC.

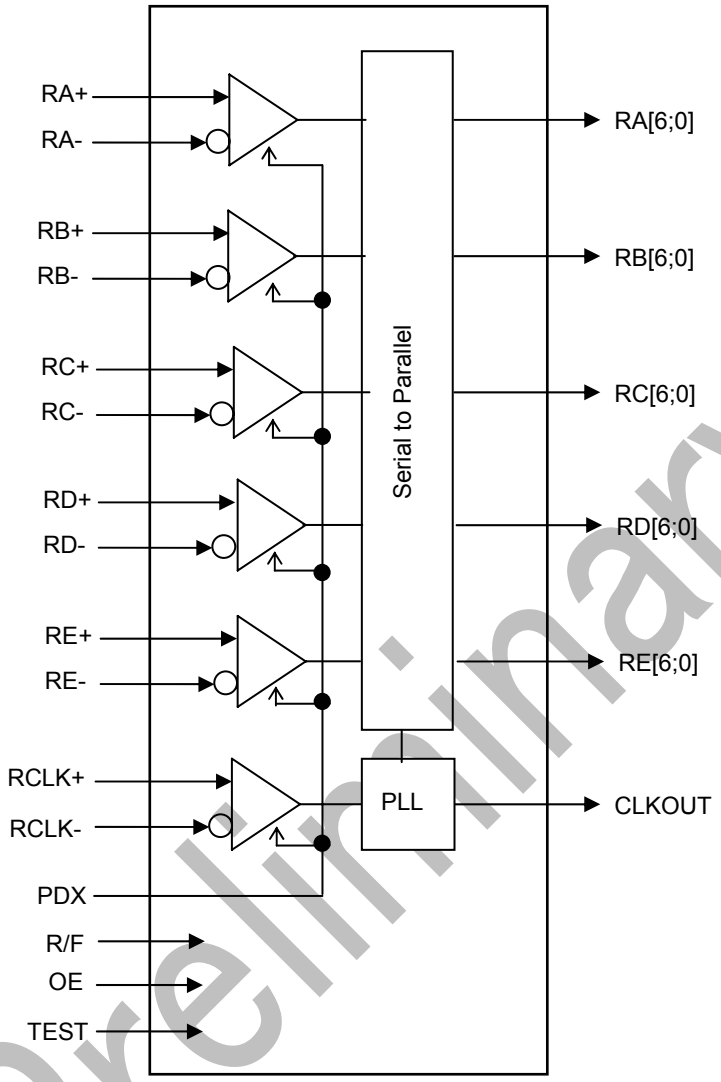
Used in combination with “Analog front-end IC”, this IC enables you to provide the optimal chipset for a high-speed scanner system.

2. FEATURES

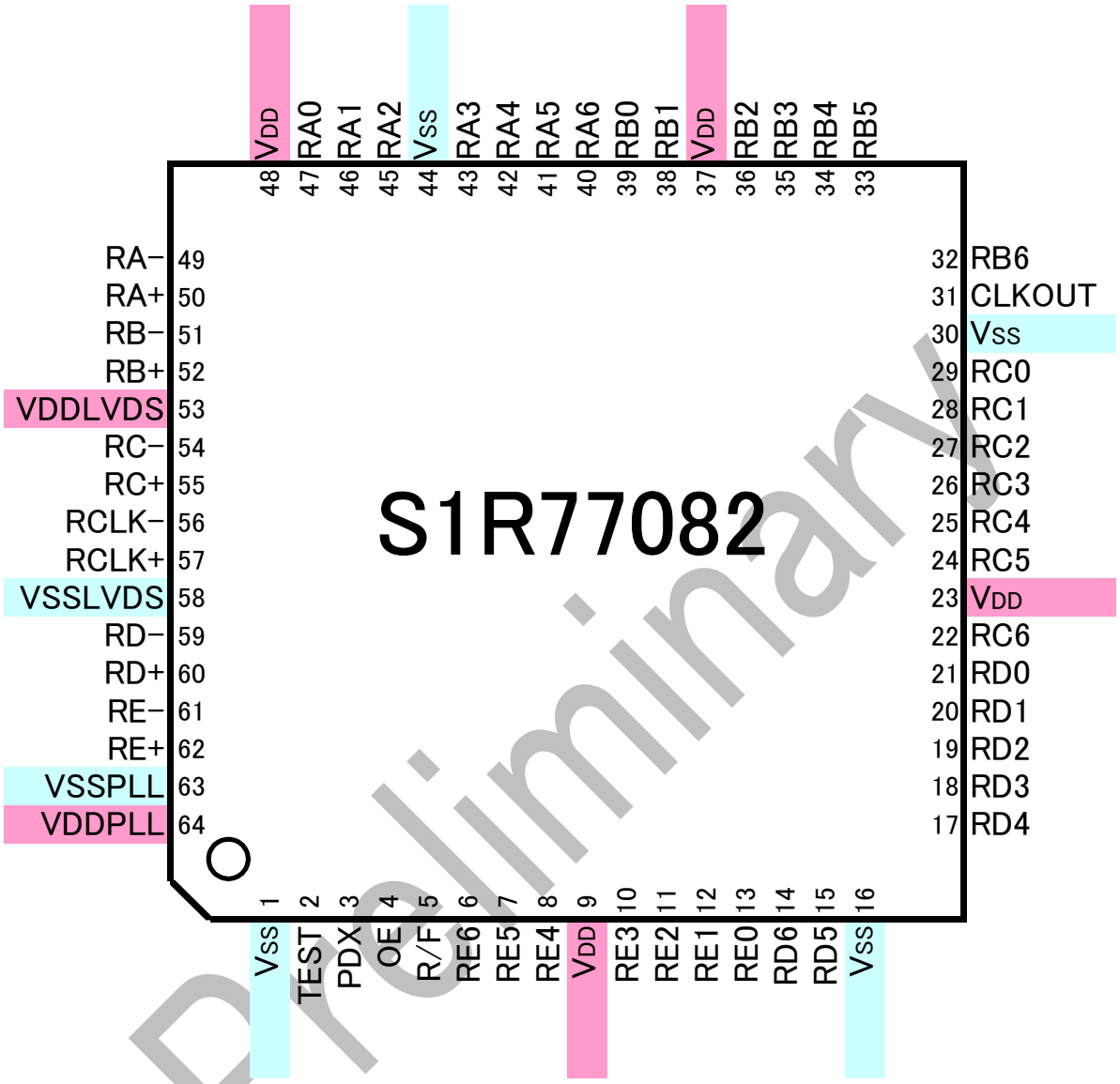
- Converts 5 channels LVDS input into 35 bits CMOS/TTL output
- Wide range clock frequency: 20 MHz to 115 MHz
- 503 Mbytes/s throughput
- 3.3V single power supply
- Power-Down Function
- Low-power CMOS process
- QFP-64 pin package

✧ Radiation shield not included.

3. BLOCK DIAGRAM



4. PIN ASSIGNMENT



5. PIN DESCRIPTION

5.1 LVDS input pin

Pin Name	I/O	No.	Description	Number of Pins
RA+/-	I	50, 49	LVDS differential data input pin. Insert the termination resistor between the positive and negative pins.	2
RB+/-	I	52, 51	LVDS differential data input pin. Insert the termination resistor between the positive and negative pins.	2
RC+/-	I	55, 54	LVDS differential data input pin. Insert the termination resistor between the positive and negative pins.	2
RD+/-	I	60, 59	LVDS differential data input pin. Insert the termination resistor between the positive and negative pins.	2
RE+/-	I	62, 61	LVDS differential data input pin. Insert the termination resistor between the positive and negative pins.	2
RCLK+/-	I	57, 56	LVDS differential clock input pin. Insert the termination resistor between the positive and negative pins.	2

5.2 LVDS output pin

Pin Name	I/O	No.	Description	Number of Pins
RA[6;0]	O	40, 41, 42, 43, 45, 46, 47	LVDS parallel data output pin.	7
RB[6;0]	O	32, 33, 34, 35, 36, 38, 39	LVDS parallel data output pin.	7
RC[6;0]	O	22, 24, 25, 26, 27, 28, 29	LVDS parallel data output pin.	7
RD[6;0]	O	14, 15, 17, 18, 19, 20, 21	LVDS parallel data output pin.	7
RE[6;0]	O	6, 7, 8, 10, 11, 12, 13	LVDS parallel data output pin.	7
CLKOUT	O	31	LVDS clock output pin.	1

5.3 Setting pin

Pin Name	I/O	No.	Description	Number of Pins
PDX	I	3	Power-down setting input pin. H: Normal operation L: Power down	1
OE	I	4	Output-enable setting input pin. H: Output enable (normal operation) L: Output disable (Hi-Z)	1
R/F	I	5	Trigger edge setting input pin for clock output. H: Rising Edge L: Falling Edge	1
TEST	I	2	Input pin used exclusive for shipping test. Locked to Low under normal conditions.	1

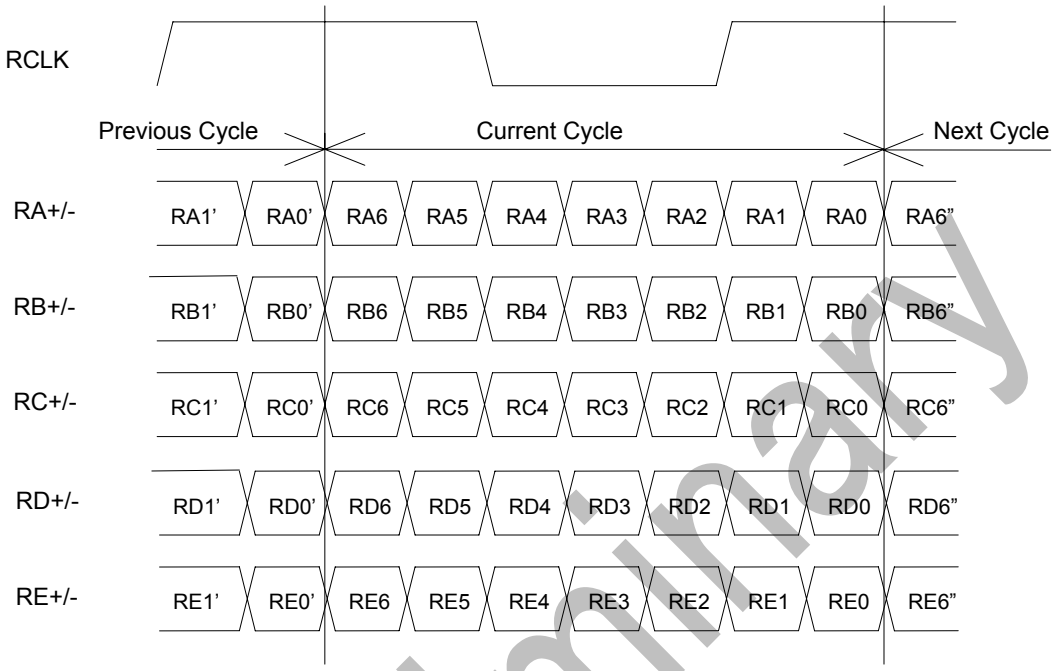
5.4 Pins associated with power supply

Pin Name	I/O	No.	Description	Number of Pins
VDDLVDS	Power supply	53	Power supply pin for LVDS analog circuit. Supply external power 3.3 V to this pin. Separate this pin from other power supply pins.	1
VDDPLL	Power supply	64	Power supply pin for PLL analog circuit. Supply external power 3.3 V to this pin. Separate this pin from other power supply pins.	1
VSSLVDS	Power supply	58	Ground pin for LVDS analog circuit. This is the 0V pin connected to GND. Separate this pin from other ground pins.	1
VSSPLL	Power supply	63	Ground pin for PLL analog circuit. This is the 0V pin connected to GND. Separate this pin from other ground pins.	1
V_{DD}	Power supply	9, 23, 37, 48	Power supply pin for digital circuit. Supply external power 3.3 V to this pin. Separate this pin from other power supply pins.	4
V_{SS}	Power supply	1, 16, 30, 44	Ground pin for digital circuit. This is the 0V pin connected to GND. Separate this pin from other ground pins.	4

6. FUNCTIONAL DESCRIPTION

6.1 LVDS data mapping

LVDS signal is a 7-bit serial data. Input/output mapping is as follows.

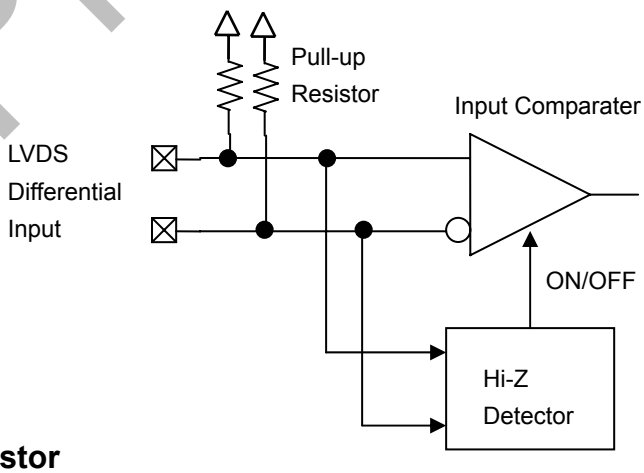


6.2 LVDS input Hi-Z detect circuit

Hi-Z detect circuit is provided to prevent the internal circuit from becoming unstable when LVDS differential input signal is Hi-Z.

The pull-up resistor is connected to LVDS differential input pin. When the differential input signal becomes Hi-Z, this pull-up resistor turns the differential line to High/High state.

Then the circuit detects the High/High level (the differential line is abnormal state), and stops the internal circuit.



6.3 Termination resistor

Connect a 100Ω termination resistor to a point close to the incoming channel external pin. The outgoing channel must also be terminated with 100Ω at a position close to an input pin of the receiving device.

"Cautions as to restrictions"

We recommend use of the termination resistor with ±1.0% or less tolerance.

The resistor and this IC must be mounted on the same side of the board without passing the leads through holes.

7. ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Item	Symbol	Min	Unit
Supply Voltage	Vdd	-0.3 to 4.0	V
Storage Temperature	Tstg	-65 to 150	°C
Input Voltage	Vin	-0.5 to V_{DD}+0.5	V

7.2 Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	Vdd1	VDDLVDS, VDDPLL, VDD	3.0	3.3	3.6	V
Supply Voltage	Vdd2	VDDLVDS, VDDPLL, VDD	2.7	3.0	3.3	V
Operating Temperature	Topr	—	-40	25	85	°C
Input Clock Frequency	Fin1	V_{DD}=3.3±0.3V	20	—	115	MHz
Input Clock Frequency	Fin2	V_{DD}=3.0±0.3V	20	—	85	MHz

7.3 CMOS input/output characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
High Level Input Voltage	Vih	V_{DD}=Max.	2.0	—	—	V
Low Level Input Voltage	Vil	V_{DD}=Min.	V_{SS}	—	0.8	V
High Level Output Voltage	Voh	Ioh=-2mA (Data) Ioh=-6mA (Clock)	V_{DD}-0.4	—	—	V
Low Level Output Voltage	Vol	Ioh=2mA (Data) Ioh=6mA (Clock)	—	—	0.4	V
Input Leak Current	Iil	—	-1	—	1	uA

7.4 LVDS input characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Differential Input High Threshold	Vth	Vcm=1.25V	—	—	+100	mV
Differential Input Low Threshold	Vtl	Vcm=1.25V	-100	—	—	mV
Differential Input Voltage	Vid	—	100	350	600	mV
Common Mode Voltage	Vcm1	V_{DD}>3.0V	0 + |Vid|/2	1.25	2.0	V
Common Mode Voltage	Vcm2	V_{DD}<3.0V	0 + |Vid|/2	1.25	1.8	V
Input Pull-up Resistor	Rpu	—	100	200	600	kΩ

7.5 LVDS Input Timing Characteristics

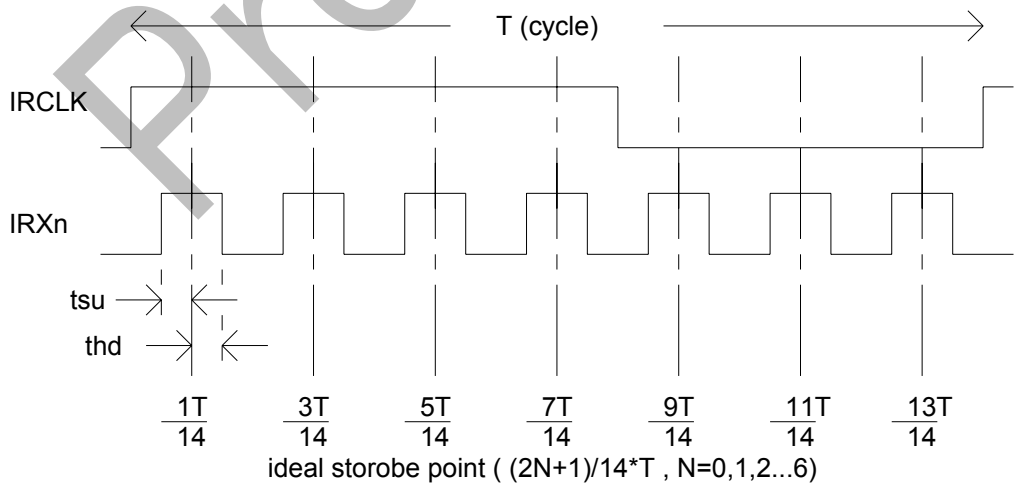
V_{DD}=3.3V±0.3V, Ta=-40 to +85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Data Setup Time1	tsu1	Tin=9ns,Vcm=1.25V	250	—	—	ps
Data Hold Time1	thd1	Tin=9ns,Vcm=1.25V	400	—	—	ps
Data Setup Time2	tsu2	Tin=12ns,Vcm=1.25V	350	—	—	ps
Data Hold Time2	thd2	Tin=12ns,Vcm=1.25V	350	—	—	ps
Data Setup Time3	tsu3	Tin=15ns,Vcm=1.25V	400	—	—	ps
Data Hold Time3	thd3	Tin=15ns,Vcm=1.25V	400	—	—	ps
Data Setup Time4	tsu4	Tin=18ns,Vcm=1.25V	550	—	—	ps
Data Hold Time4	thd4	Tin=18ns,Vcm=1.25V	550	—	—	ps
Data Setup Time5	tsu5	Tin=25ns,Vcm=1.25V	1050	—	—	ps
Data Hold Time5	thd5	Tin=25ns,Vcm=1.25V	1050	—	—	ps

V_{DD}=3.0V±0.3V, Ta=-40 to +85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Data Setup Time1	tsu1	Tin=9ns,Vcm=1.25V	—	—	—	ps
Data Hold Time1	thd1	Tin=9ns,Vcm=1.25V	—	—	—	ps
Data Setup Time2	tsu2	Tin=12ns,Vcm=1.25V	350	—	—	ps
Data Hold Time2	thd2	Tin=12ns,Vcm=1.25V	350	—	—	ps
Data Setup Time3	tsu3	Tin=15ns,Vcm=1.25V	400	—	—	ps
Data Hold Time3	thd3	Tin=15ns,Vcm=1.25V	400	—	—	ps
Data Setup Time4	tsu4	Tin=18ns,Vcm=1.25V	550	—	—	ps
Data Hold Time4	thd4	Tin=18ns,Vcm=1.25V	550	—	—	ps
Data Setup Time5	tsu5	Tin=25ns,Vcm=1.25V	1150	—	—	ps
Data Hold Time5	thd5	Tin=25ns,Vcm=1.25V	1150	—	—	ps

Note: The operations of Tin=9ns is not guaranteed when V_{DD} is below 3.0 V.

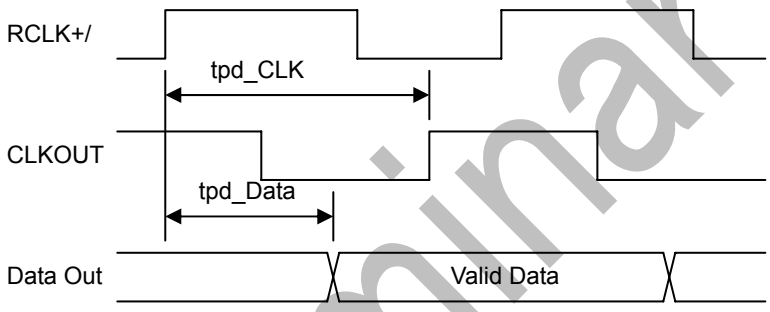


7.6 Clock input/output delay characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
CLKOUT Delay	tpd_CLK	3.3V±0.3V, 0~+70°C	1.98+(T/14) × 8	3.31+(T/14) × 8	5.29+(T/14) × 8	ns
		3.0V±0.3V, 0~+70°C	2.19+(T/14) × 8	3.59+(T/14) × 8	5.89+(T/14) × 8	ns
		3.3V±0.3V, -40~+85°C	1.92+(T/14) × 8	3.31+(T/14) × 8	5.52+(T/14) × 8	ns
		3.0V±0.3V, -40~+85°C	2.08+(T/14) × 8	3.59+(T/14) × 8	6.10+(T/14) × 8	ns

7.7 Clock input/data output delay characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Data Output Delay	tpd_Data	3.3V±0.3V, 0~+70°C	2.37+(T/14) × 4	3.95+(T/14) × 4	6.32+(T/14) × 4	ns
		3.0V±0.3V, 0~+70°C	2.62+(T/14) × 4	4.29+(T/14) × 4	7.04+(T/14) × 4	ns
		3.3V±0.3V, -40~+85°C	2.29+(T/14) × 4	3.95+(T/14) × 4	6.59+(T/14) × 4	ns
		3.0V±0.3V, -40~+85°C	2.49+(T/14) × 4	4.29+(T/14) × 4	7.30+(T/14) × 4	ns

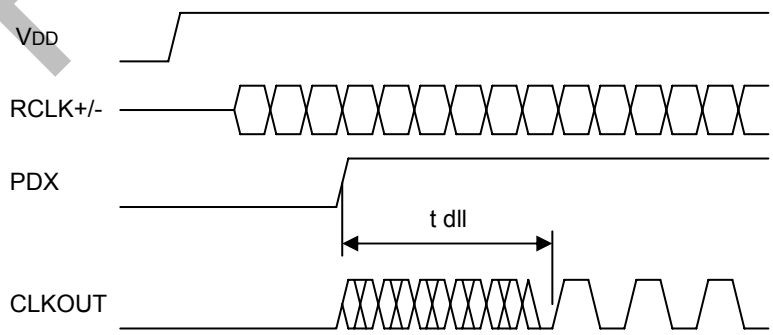


7.8 Output clock duty

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
CLKOUT Duty	Duty_CLK	—	45	50	55	%

7.9 DLL lockup time characteristics

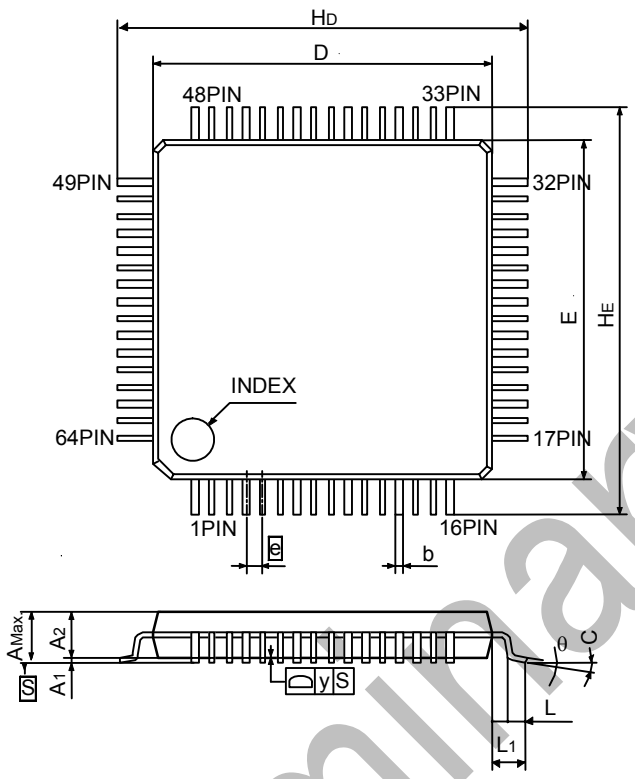
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
DLL Lock Time	tdll	—	—	1	10	ms



7.10 Current Consumption

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current Consumption	Pd_VDDLVDS	Tin=15nS, VDDLVDS=VDDPLL= VDD=3.3V	—	TBD	—	mA
	Pd_VDDPLL		—	TBD	—	
	Pd_VDD		—	TBD	—	

8. EXTERNAL DIMENSIONS



Symbol	Dimension in Milimeters		
	Min.	Nom.	Max.
E	—	10	—
D	—	10	—
Amax	—	—	1.7
A_1	—	0.1	—
A_2	—	1.4	—
e	—	0.5	—
b	0.13	—	0.27
c	0.09	—	0.2
θ	0°	—	10°
L	0.3	—	0.75
L_1	—	1	—
H_E	—	12	—
H_D	—	12	—
y	—	—	0.08

Unit:mm

LQFP13-64PIN

9. REVISION HISTORY

Y/M/D	Rev.No.	Description of revision				
		Scope	Page	Item	Previous	Revised
’07/ 6/25	Rev.0.1	New	All	—	—	New establishment
’07/11/22	Rev.0.2	Revision	P1	Overview	This IC “S1R77082” is a LVDS receiver IC which receives LVDS signals. Used in combination with an analog front-end IC installing CCD-driven clock, this IC enables you to easily provide a high-speed scanner system with excellent EMI characteristics.	“This IC “S1R77082” is a LVDS receiver IC. SIR77082 revices the 5 channels LVDS data stream and restore it to 35 bits CMOS/TTL data.” (excerpted)
				Features	5 LVDS channels incorporated Power-Down Function 3.3V single power supply Low-power CMOS process QFP-64 pin package	Converts 5 channels LVDS input into 35 bits CMOS/TTL output Wide range Clock frequency: 20 MHz to 115 MHz 503 Mbytes/s throughput 3.3V single power supply Power-Down Function Low-power CMOS process QFP-64 pin package
		Added	P4	Added	—	6.3 Termination resistor

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