S1R72U16
Connection Guide
For connecting to local 16-bit
CPU bus (memory bus)

NOTICE

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1. Requirements for using the S1R72U16 connected to a local 16-bit CPU bus (memory bus)

The following drivers can be used when the S1R72U16 is connected to a local 16-bit CPU bus (hereafter "CPU bus").

- ATA/ATAPI driver

- CF (True IDE mode) driver

   ※ Since this LSI does not implement attribute memory, the CF (True IDE mode) driver must always see this LSI as a CF without attribute memory. If the CF driver in use checks for the presence of a CF with attribute memory, add a modification to make such a CF appear present at all times to enable use of the LSI.

These drivers can be obtained from the following sources:

- Use drivers included with the CPU, operating system, or file system.

- Purchase drivers from a software developer.

- Use the sample ATA/ATAPI (CF (True IDE mode)) driver provided by Seiko Epson.*

   * Use of software provided by Seiko Epson requires acceptance of the terms of the license agreement.

   * The sample ATA/ATAPI (CF (True IDE mode)) driver is based on μITRON specifications. There are no plans to implement support for other operating systems.

Using S1R72U16 with these drivers requires the following modifications:

- Change I/O register addresses.

The following modifications may also be required:

- Changes in data transfer method for data transfers via DMA.

- Changes in interrupt processing for device interrupts.

Complete these modifications, as follows:

2. Modifying I/O register addresses, and endian

Drivers access the registers indicated in Table 2-1 for device control.

Table 2.1   I/O registers

ATA task file registers (*1)		
Operation	**READ**	**WRITE**
Register name	Data	
	Error	Features
	Sector Count	
	LBA Low（Sector Number *2, *3)	
	LBA Mid (Cylinder Low *2, *3)	
	LBA High (Cylinder High *2, *3)	
	Device (Device/Head *2) (Select Card/Head *3)	
	Status	Command
	Alternate Status	Device Control

*1   These registers are known collectively as "ATA task file registers." They are sometimes referred to as "task file registers."

*2   Register names as defined in specifications prior to *AT Attachment with Packet Interface—5 (ATA/ATAPI-5)*.

*3   Register names as defined in the *CompactFlash Specifications*.

When the S1R72U16 is connected to a CPU bus, the registers indicated in Table 2.1 are mapped to CPU memory area as shown in Table 2.2.

Modify I/O register addresses defined by the driver so that they correspond to the S1R72U16 I/O register addresses mapped to CPU memory area.

The data bus is a little endian 16-bit bus. The data register only allows 16-bit access. Other register values are valid only for lower addresses.

The 16-bit data obtained from the data bus must be swapped if the main CPU is big endian.

Table 2.2   S1R72U16 register map

OFFSET (*)	ATA task file registers	
	READ	WRITE
00h	Data（16bit）	
01h		
02h	Error	Feature
03h		
04h	Sector Count	
05h		
06h	LBA Low	
07h		
08h	LBA Mid	
09h		
0Ah	LBA High	
0Bh		
0Ch	Device	
0Dh		
0Eh	Status	Command
0Fh		

OFFSET (*)	ATA task file registers	
	READ	WRITE
10h	none	
11h		
12h	none	
13h		
14h	none	
15h		
16h	none	
17h		
18h	none	
19h		
1Ah	none	
1Bh		
1Ch	Alternate Status	Device Control
1Dh		
1Eh	none	
1Fh		

*   OFFSET: Start addresses of the memory area allocated for S1R72U16 I/O registers.

3. Changing the data transfer method

For data transfers with the S1R72U16 via DMA,* use a DMA controller capable of transferring data between the device connected to the CPU bus and memory. For information on DMA controller control methods, consult the CPU documentation or contact the CPU manufacturer.

* When the S1R72U16 is connected to the CPU bus, you cannot use Ultra DMA as defined in *AT Attachment with Packet Interface—4 (ATA/ATAPI-4)* or later specifications. Use multi-word DMA instead.

4. Changing interrupt processing

To use S1R72U16 interrupts with the driver, use an XINT signal and modify an interrupt handler or the like to notify the driver of interrupts.

Revision History

Date	Revision details			
	Rev.	**Page**	**Type**	**Details**
06/29/2007	0.80	All	New	Newly established
08/22/2007	1.00	2	Correct	Corrected Section 2 title and note, and Added explanation, and Corrected Table 2-2.
		5	Add	Added Revision History.
10/15/2007	1.10	1	Correct	Changed "CF" to "CF (True IDE mode)"; added restrictions on CF driver.

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