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PCB Design Guidelines for S1R72V Series USB 2.0 High-Speed Devices

SEIKO EPSON CORPORATION

Rev.2.3

NOTICE

Scope

These guidelines apply to the S1R72V series of Seiko Epson products and derivatives (hereafter the USB 2.0 Controller IC).

Note that names for signals and power supply in the USB 2.0 transceiver macro component reflect the names used during development at Seiko Epson. The corresponding pin names in the actual USB 2.0 Controller IC vary from product to product.
Diagrams, components, and values in these guidelines are provided for reference purposes only. They do not represent guaranteed performance parameters for specific applications.

These guidelines may change without prior notice.

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1. Purpose

This document is intended for use as guidelines for the USB 2.0 transceiver macro peripheral component, serving as a reference for users of the S1R72V series of Seiko Epson products and derivatives when designing the boards in question. This document focuses on the implementation of USB 2.0 functions. It omits general precautions for board design.

We recommend referring to the documented board artwork and verification test procedures published by the USB Implementers Forum (USB-IF) in addition to these Guidelines.

2. Board Design Guidelines

2.1. DP/DM Signal Wiring

Consider the following points when designing the DP/DM signal wiring:

(1) The differential impedance of DP/DM must be 90 Ω.
(2) The signal lines must be routed to the shortest distance possible to keep board signal propagation delays under 1 ns.
(3) To prevent signal skews and to stabilize differential impedance, the signal lines must be routed in equal lengths and kept parallel.
(4) The internal layer directly below the signal lines must be a contiguous solid GND plane with no separation.
(5) Avoid routing other signals near the signal lines. In particular, route high-speed signals and clock signals at some distance from the signal lines to ensure maintenance of stable characteristic impedance values.
(6) When wiring needs to be bent, it must be R-processed to minimize signal reflections.
(7) The VBUS line must be routed at a sufficient distance from the DP/DM signal lines to avoid effects upon differential impedance.
(8) If the wiring length is extended or other connectors are inserted between the IC and USB connector, take special care to ensure that characteristic impedances are matched.
(9) We recommend preparing a chip capacitor-mounting pattern between the DP-GND and DM-GND pins to adjust the transmission waveform. This can be done using a static and surge protective chip varistor, as described below.

2.1.1. Common Mode Choke Coils (CMCC)

Although CMCCs help improve skews and reduce unwanted electromagnetic noise, they can also degrade differential signal characteristics (e.g., FS transmit waveforms). But since CMCCs in the USB 2.0 Controller IC have negligible adverse effects on differential signal characteristics, CMCCs may be used where necessary.
We recommend using the following CMCC products.
However, note that the user must confirm that the CMCCs used actually reduce unwanted electromagnetic noise to the extent necessary. We also recommend that the user consult with the vendor on issues related to CMCC mounting position and other technical matters.

[Common mode filter ACM2012-900-2P made by TDK]

[Chop common mode choke coil DLW21SN900SQ2 made by Murata Mfg.]

[Common mode choke 985BH-1007 made by TOKO]

2.1.2. Using the Chip Varistor

Use a chip varistor to protect the DP/DM pins from static electricity and surges.
You can use one of the following products as a chip varistor for USB2.0 High-Speed transfers. The chip varistor is generally mounted near a connector. For more information on mounting positions, please consult with the supplier of the product in question.

[AVR-series chip varistors made by TDK]

[EZJZ-series chip varistors made by Matsushita Electric Industrial Co., Ltd.]

2.1.3. About External Parts for the DP/DM Pins

The differential signal characteristics (e.g., HS transmit waveform) of DP/DM pins may be degraded in the following cases, adversely affecting the quality of eye pattern waveforms. Carefully consider the need for each part in the user product and perform an overall evaluation of product functions and differential signal characteristics with respect to such parts.

- When uncertified receptacles or cables and connectors are used
- When multiple receptacles are used for a pair of DP/DM signal lines

The 72V**-series USB controller LSIs from Seiko Epson boast High-Speed waveform quality as one of their distinguishing features, providing superior connectivity. In High-Speed communications, signal relays or board-to-board connections with flexible cables or addition of protective devices, etc. to the PCB tends to degrade transmission waveforms, making it difficult to maintain communication.
Based on the assumption that parasitic capacitance will occur, as in this case, in the DP/DM lines, the transmission characteristics in the 72V**-series USB controller LSIs from Seiko Epson are adjusted with relatively steep waveform slopes to provide adjustment latitude on the PCB. Keep in mind that this may result in a failure to meet the rated Tr/Tf values [Note] in USB compliance tests depending on PCB board design. Seiko Epson has confirmed that the measurement environment significantly influences Tr/Tf measured values and concluded that the issue cannot be fully resolved in the LSI.
Thus, we recommend providing a land pattern that permits the mounting of a varistor for waveform adjustments, even when no static protective varistors are used.

[Note]: 500 ps (min.) under USB2.0 standard 7.1.2.2

2.1.4. Example Board Layout

An example DP/DM wiring between the USB 2.0 Controller IC and a receptacle is shown below. The dimensions shown here are based on performance records for the evaluation board produced to verify Seiko Epson USB 2.0 characteristics (boards made by Kyoden Co.). When manufacturing user boards, consult the board manufacturer to confirm the processing conditions required to match differential impedance characteristics.

The layout examples here omit external components such as CMCs and chip varistors. Please confirm that the CMCs are located in the DP/DM lines linearly and that chip varistors are mounted at the shortest possible distances from the DP/DM lines.

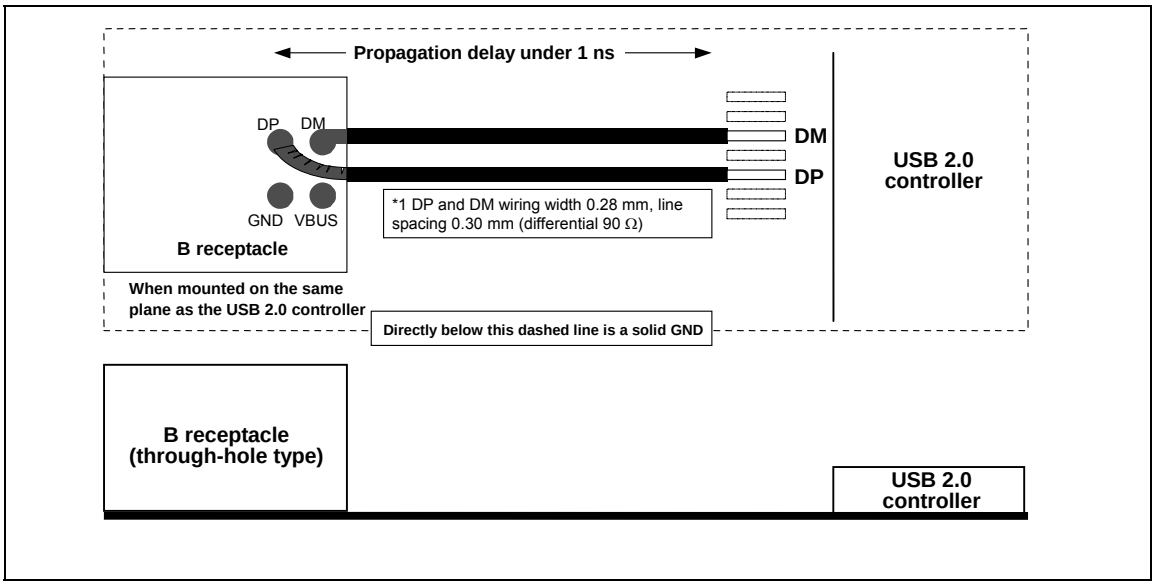


Figure 2-1. Board Layout Example [B Receptacle (Through-Hole Type): Mounted on same plane]

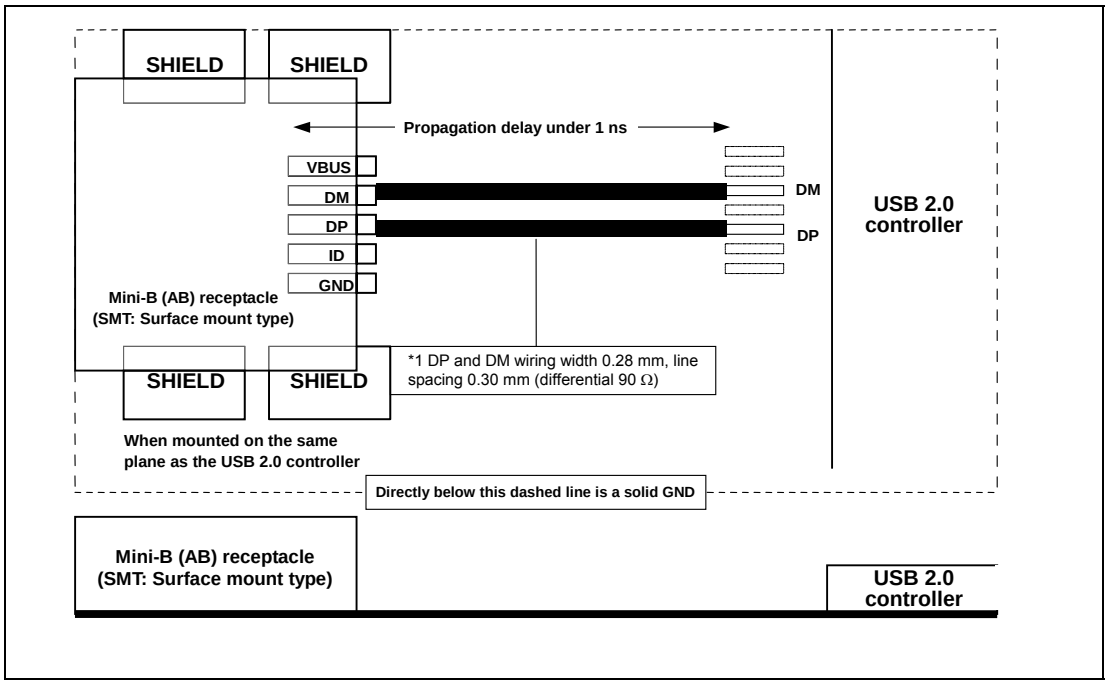


Figure 2-2. Example Board Layout [Mini-B or Mini-AB Receptacle (SMT Type): Mounted on same plane]

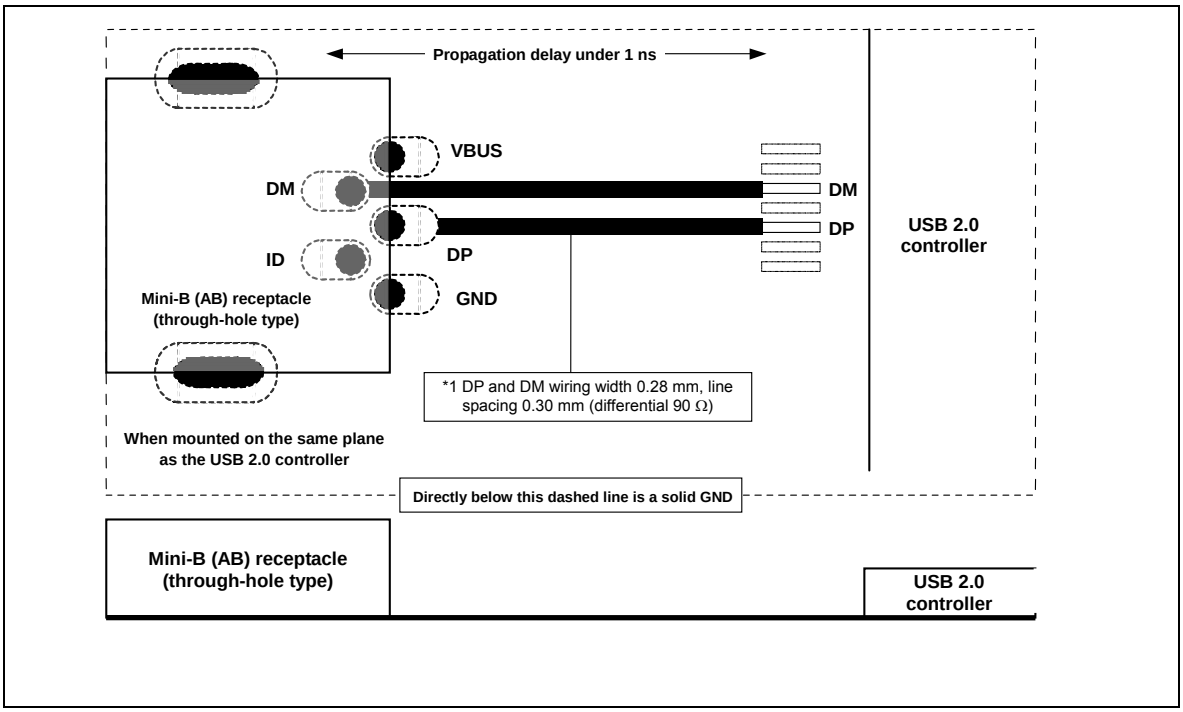


Figure 2-3. Board Layout Example [Mini-B or Mini-AB Receptacle (Through-Hole Type): Mounted on same plane]

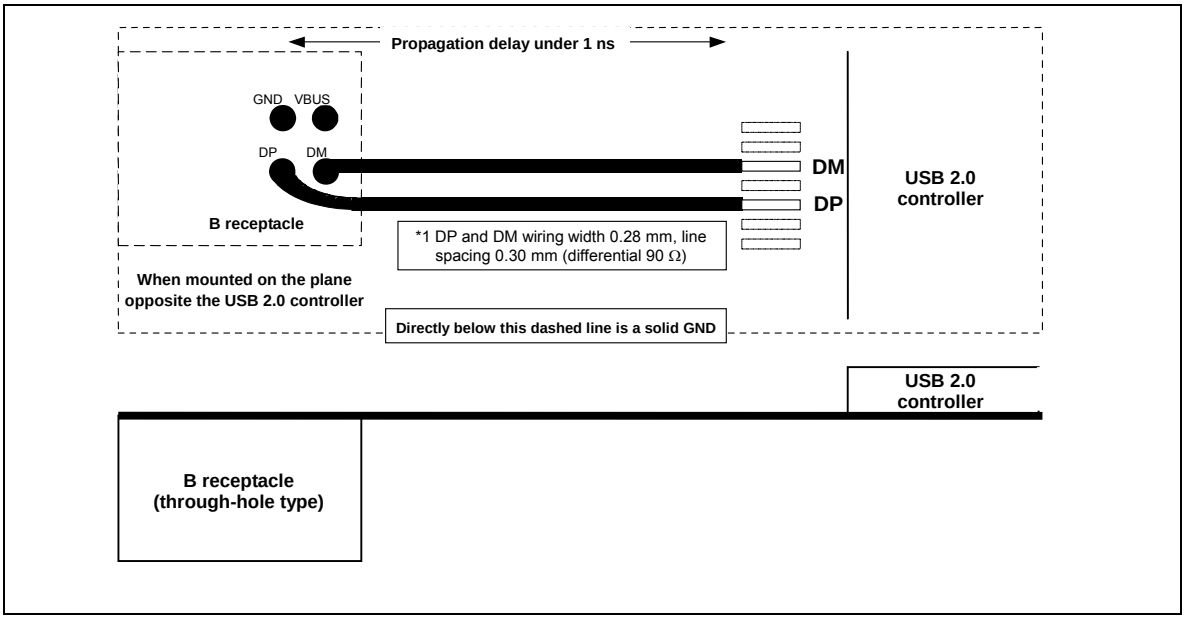


Figure 2-4. Board Layout Example [B Receptacle (Through-Hole Type): Mounted on opposite plane]

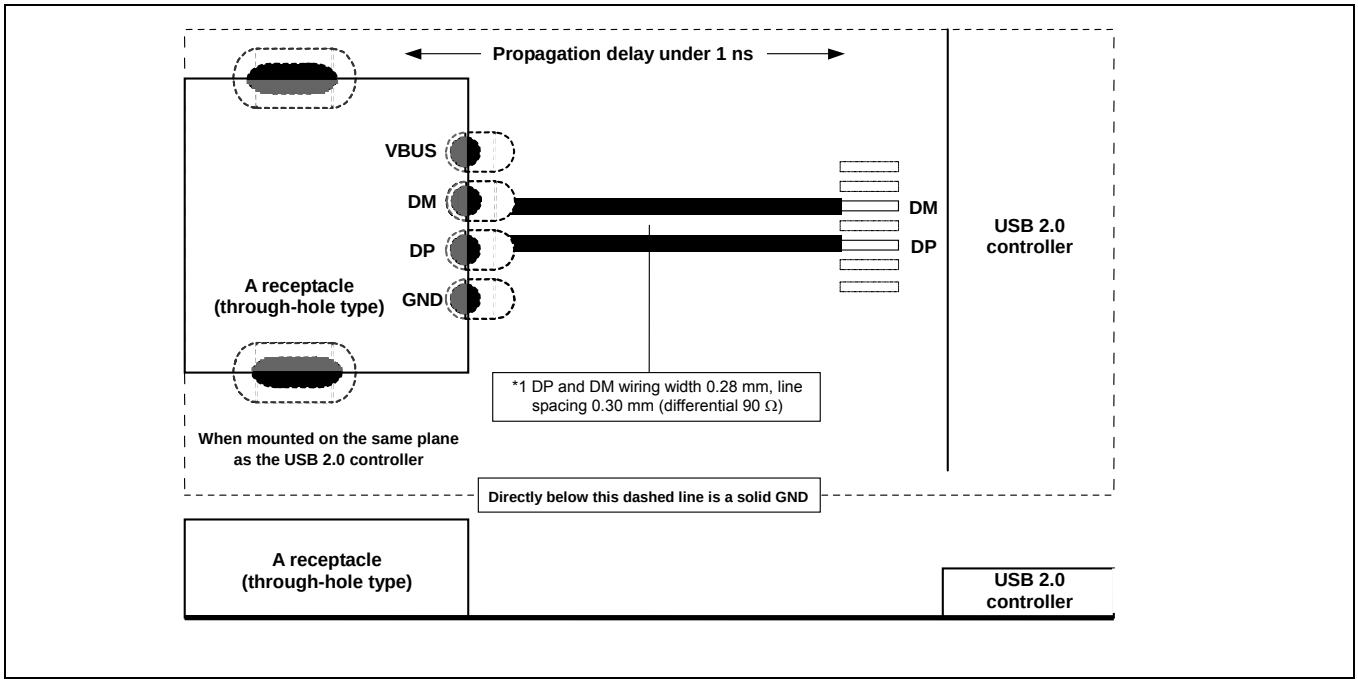
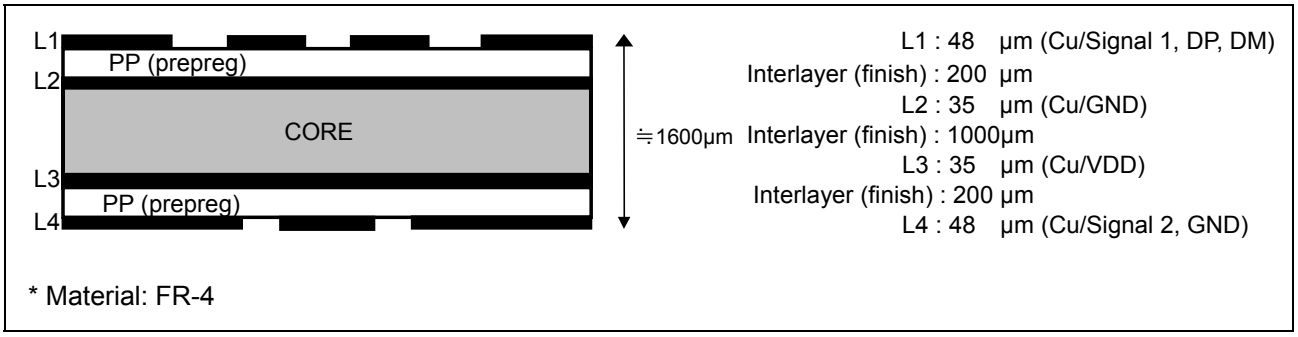


Figure 2-5. Board Layout Example [A Receptacle (Through-hole Type): Mounted on same plane]

2.1.5. Example Structure of Board Layers

A typical board layer structure is shown below, using as an example of a 4- or 6-layered 1.6-mm thick printed circuit board.

The dimensions shown here are based on performance records for the evaluation board produced to verify Seiko Epson USB 2.0 characteristics (boards made by Kyoden Co.). When manufacturing user



boards, consult the board manufacturer to confirm the processing conditions required to match differential impedance characteristics.

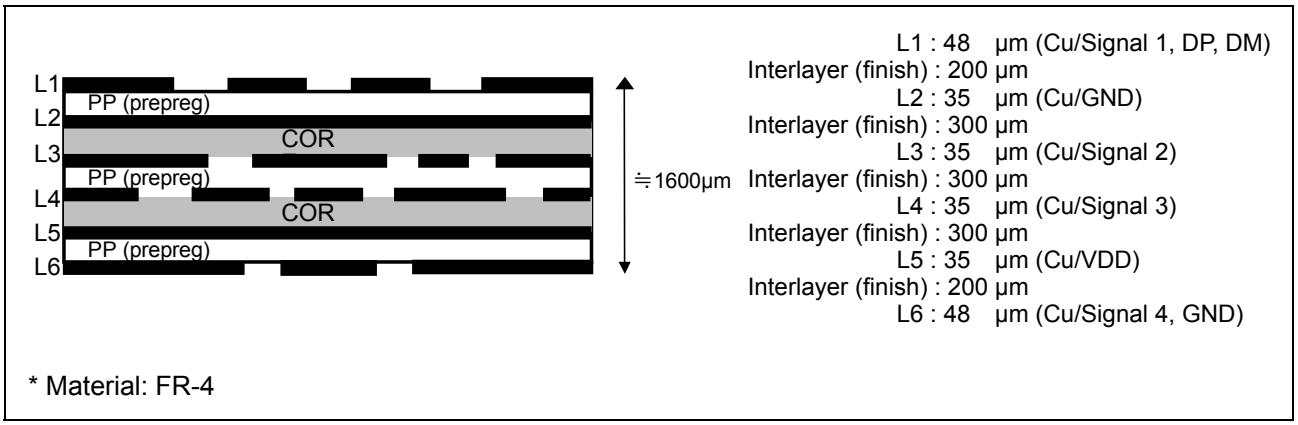


Figure 2-6. Structure of 4-layered Printed Circuit Board

Figure 2-7. Structure of a 6-layered Printed Circuit Board

2.2. USB Peripheral Circuit

Consider the following points when connecting or inserting peripheral circuit components of the USB 2.0 Controller IC.

- The 6.2 kΩ ± 1% resistor to be connected to the R1 pin must be placed as close to the R1 pin as possible.
- The VSSs for the USB 2.0 transceiver macro component must be connected at low impedance to the common GND, not separately.
- Each decoupling capacitor must be placed close to the corresponding power supply pin (recommended).
- Use C3 and C5 as necessary. (For more information, refer to Section 2.2.1, “Inter-Power Supply Decoupling Capacitance And VDD-GND Planes.”)

Figure 2-8 shows an example of a USB peripheral circuit.
Since the actual pin placement and pin names in the product used may not be the same as those shown here, refer to the example USB connections in the development specifications for each product for more information on component placement and component-to-pin connections.

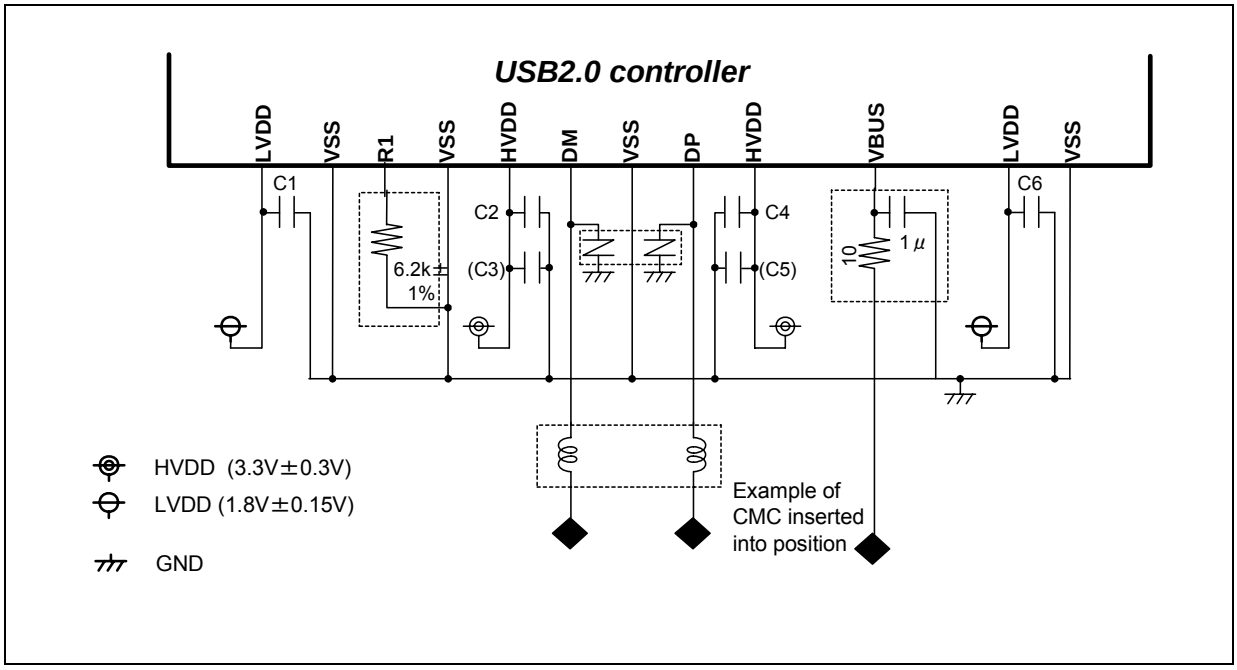


Figure 2-8. USB Peripheral Circuit Example

2.2.1. Inter-Power Supply Decoupling Capacitance And VDD-GND Planes

Reference values for the capacitance of each inter-power supply decoupling capacitor are given below.

Table 2-1. Capacitances of Inter-Power Supply Decoupling Capacitors

Capacitor name (**Figure 2-8**)	C1	C2, C4	C6
Reference value	1 µF	0.1 µF	1 µF

Good VDD plane vs. GND plane characteristics are required to prevent adverse effects on differential signal characteristics due to increased jitter or other factors. Keep in mind the following to avoid this problem.

- Carefully examine the effects of noise from the switching regulator, where applicable. Consider ways to reduce switching noise when designing a printed circuit board.
- Depending on the printed circuit board in question, you may be able to resolve the jitter problem by placing capacitors with larger capacitances than C2 and C4 at the C3 and C5 locations. If so, make sure that C2 and C4 are placed closer to the HVDD pin than C3 and C5.
- Consider the circuit board, component placement, component count, anticipated cost, and signal quality to determine the optimal capacitance for the capacitors.

2.2.2. VBUS Protective Circuit

When the USB 2.0 Controller IC operates as a USB device, connecting the USB cable may result in a voltage that significantly exceeds the rated VBUS voltage (5 V) at the VBUS pin, thereby exceeding the absolute maximum rating and causing the VBUS pin to fail. To prevent this, always use a protective circuit similar to the one shown below.

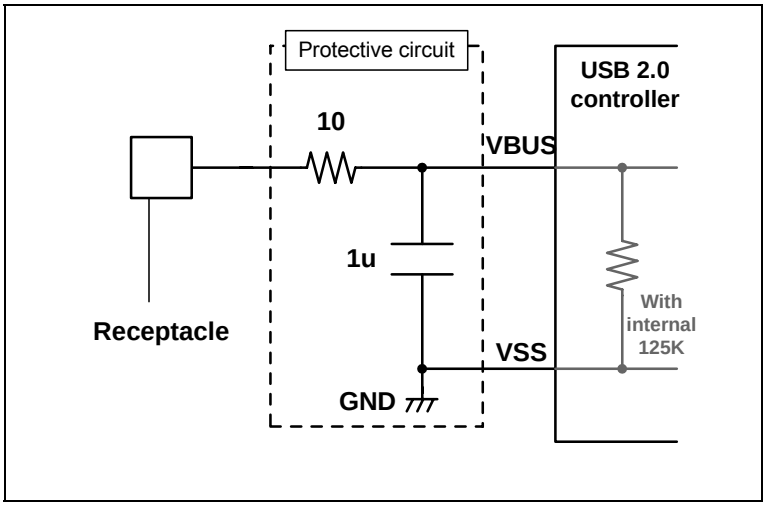
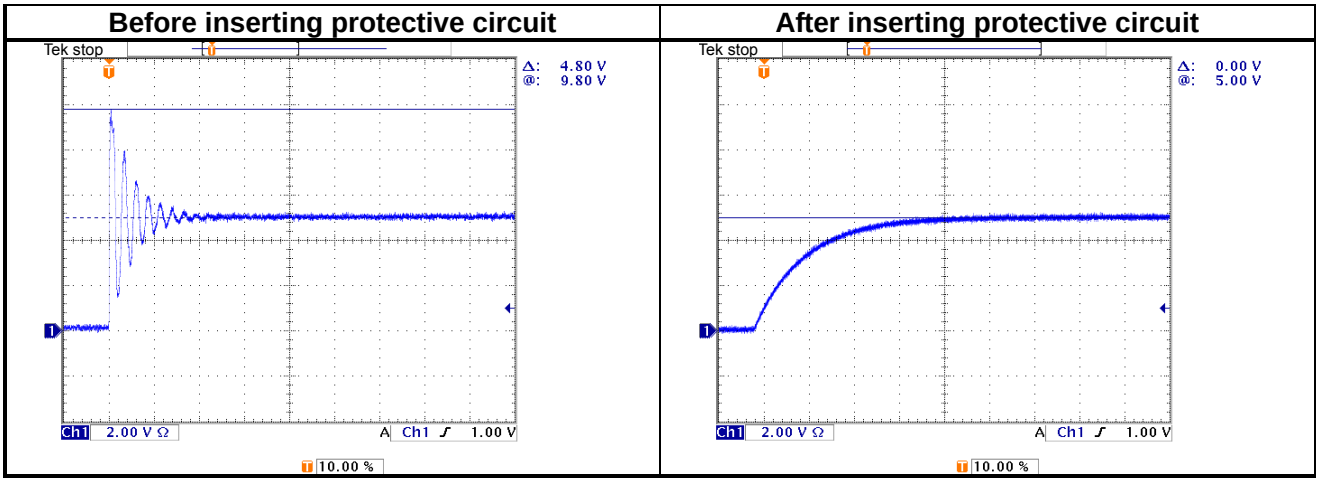


Figure 2-9. VBUS Protective Circuit



Blue color ——— : VBUS pin voltage

Figure 2-10. Rising Waveform of the Applied Voltage on VBUS Pin

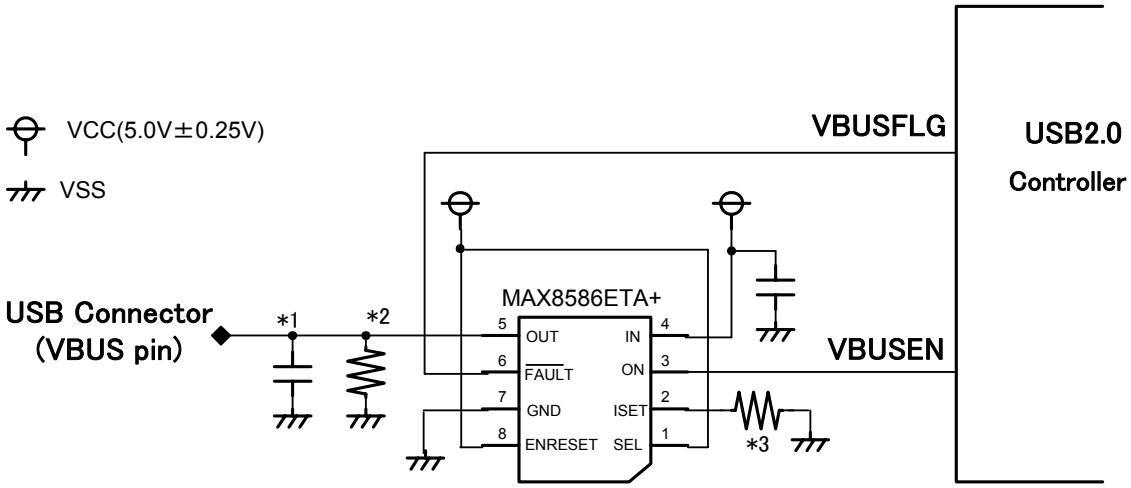
2.2.3. VBUS Supply Circuit

An example shown here is the circuit for the VBUS power supply (+5V) from the USB connector when using the Epson USB2.0 controller IC with the USB host function. In this example, Maxim MAX8586ETA+ is used as a USB power switch IC with Over-current and Reverse-current Protection features*. However, this does not guarantee the circuit operation on your system. In practice, you need to fully study the specification of the power switch IC to use and the way of Over-current Protection when selecting components and circuit designs suitable for your system.

*When using a USB power switch IC without Reverse-current Protection feature, care must be taken for the following point: For example, if external voltage is applied to the VBUS pins of the USB connector while the equipment is powered off Reverse-current Protection may flow from the OUT terminal to the IN terminal of the USB power switch IC. This may cause unexpected power-on of the equipment.

For the circuit configuration that allows both USB host and device functions, two sample circuits are shown: One using the USB host−only connector and the other using the USB connector shared by the host and device.

The sample circuit for using the USB host−only connector



*1: The Universal Serial Bus Specification (Revision 2.0) 7.2.4 calls for a minimum of 120µF for bypassing the VBUS line on the USB downstream port. Capacitance equivalent to 122µF is mounted on the Epson evaluation board.

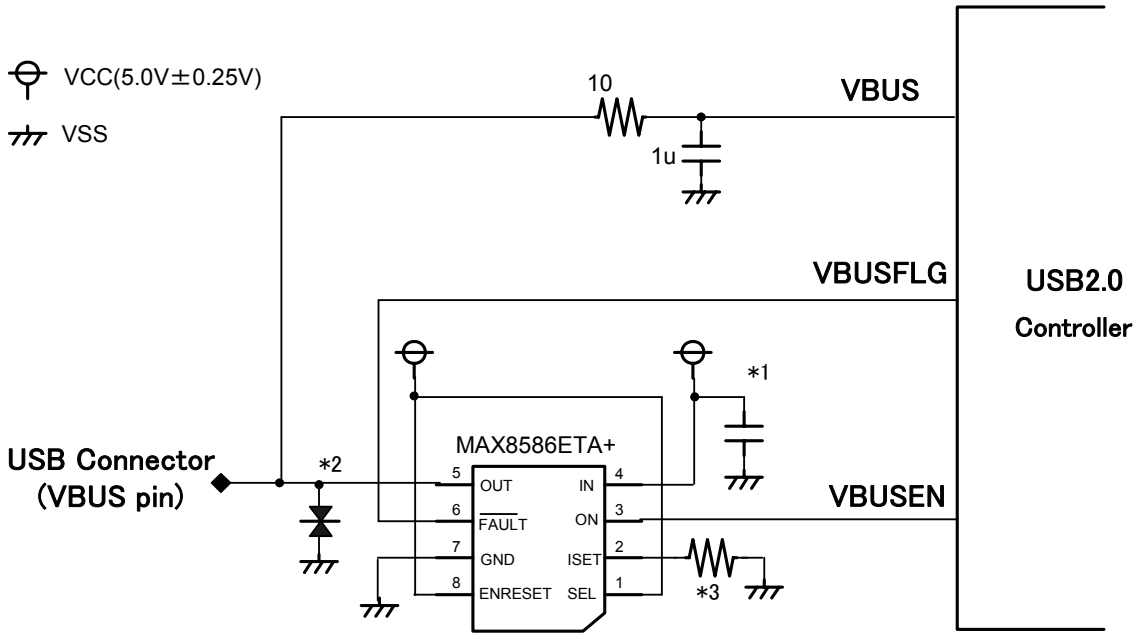
*2: Resistor to discharge the capacitor of over 120µF mentioned above. 100KΩ is mounted on the Epson evaluation board.

*3: Resistor that determines the overcurrent detection value. For more information, refer to the

specification of the USB power switch IC.

Figure 2-11 VBUS Supply Circuit sample_1

The sample circuit for using the USB connector shared by the host and device



*1: The Universal Serial Bus Specification (Revision 2.0) 7.2.4 calls for a minimum of 120µF for bypassing the VBUS line on the USB downstream port. Capacitance equivalent to 122µF is mounted on the Epson evaluation board.

*2: It is to protect the USB power switch IC when connected to the equipment where VBUS voltage greater than the rated value is supplied through the USB connector.

*3: Resistor that determines the overcurrent detection value. For more information, refer to the specification of the USB power switch IC.

Figure 2-12 VBUS Supply Circuit sample_2

2.3. Oscillator Circuit

Noise-induced disturbances in the oscillation clock waveform will cause the IC to operate erratically. Keep in mind the following:

- Do not place high-current signal lines or high-speed signal lines near the oscillator circuit.
- XI and XO signals must be routed by the shorted distance possible.
- The crystal resonator used for the oscillator circuit must have a frequency accuracy of close to 100 ppm.

Figure 2-13 and Table 2-2 show a typical configuration of an oscillator circuit, using as an example the FA-128 crystal resonator made by Epson Toyocom Corp.

However, since oscillation characteristics depend on various other factors (e.g., components used and board pattern), consult the resonator manufacturer to evaluate peripheral circuit constants. This will make it possible to determine the appropriate constants for each board.

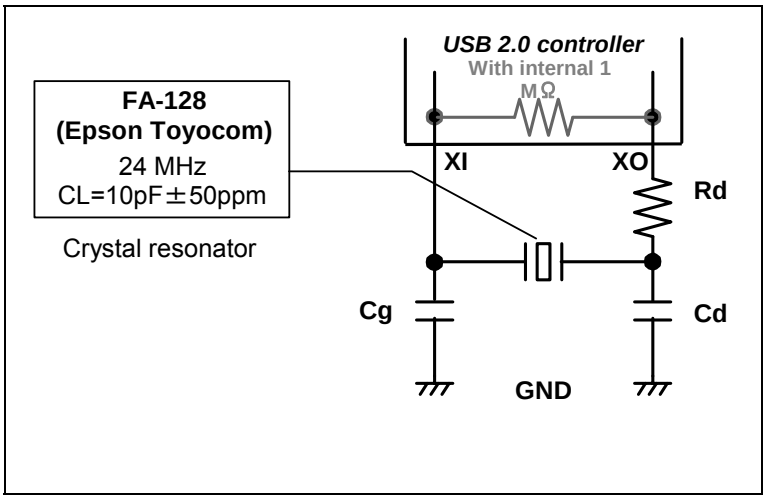


Figure 2-13. Example of Connecting a Crystal Resonator

Table 2-2. Circuit Constants in Seiko Epson EVA Board

Crystal resonator made by Epson Toyocom Corp. (CL = 10 pF ± 50 ppm)	Oscillation frequency (MHz)	Recommended circuit constants		
		Cg (pF)	Cd (pF)	Rd (Ω)
FA-128	24	15	15	470

3. Example Differential Signal Characteristics (Eye Diagram)

Figure 3-1 shows an example of the Hi-Speed eye pattern observed on the USB 2.0 Controller IC Evaluation Board designed according to these guidelines.

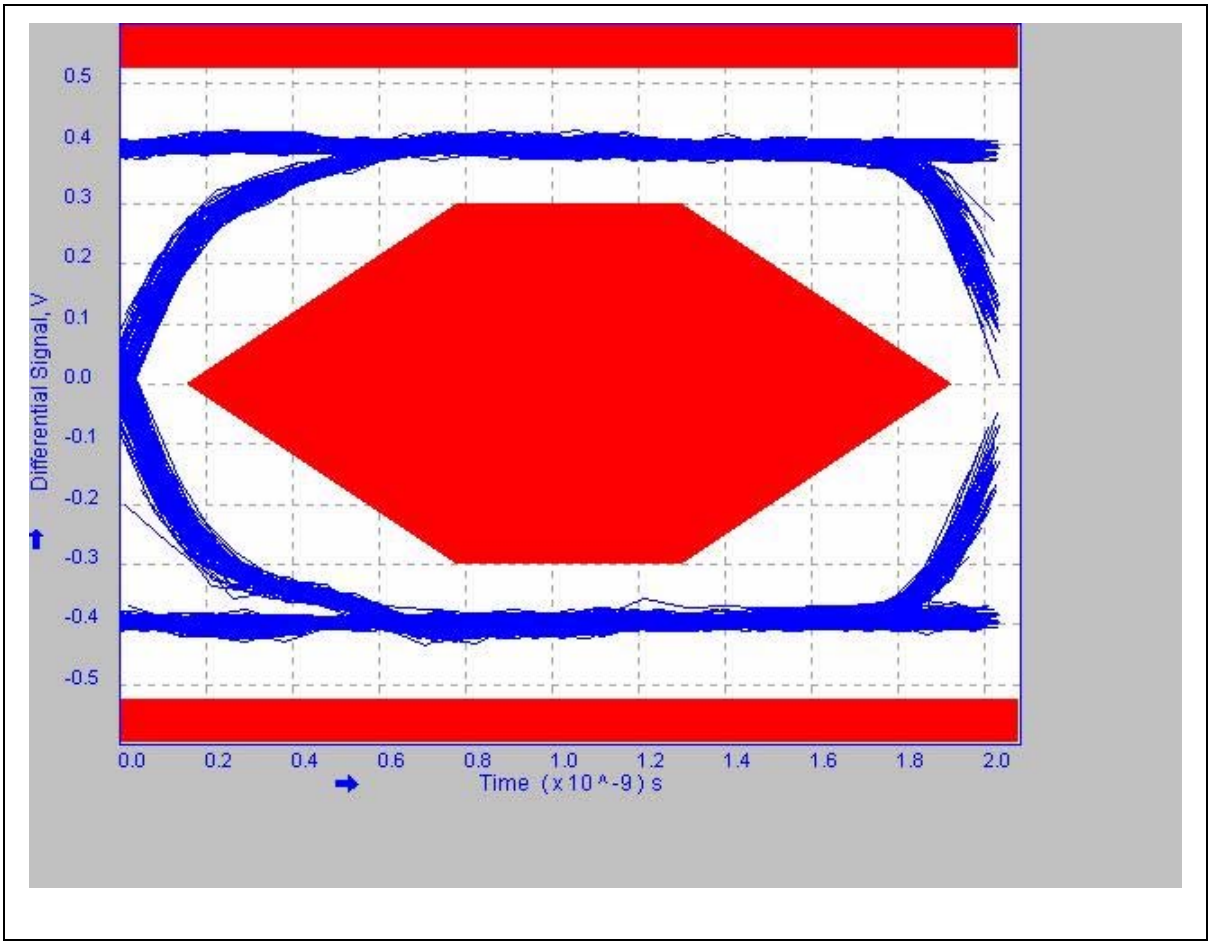


Figure 3-1. Eye Pattern Waveform (Hi-Speed)

* The eye pattern waveforms observed will differ with transmission lines, board power supply characteristics, and the measurement environment, among other factors.

Revision History

day/month/Year	Content of revision			
	Rev.	Section (old version)	Category	Content
10/14/05	2.0	All sections	New	Newly created
03/01/06	2.1	2.2	Correction	Description of C2 and C4 deleted.
			Correction	Description of C3 and C5 added.
			Correction	C3 and C5 in Figure 2-8 changed to (C3) and (C5), respectively.
		2.2.1	Correction	C3 and C5 in Table 2-1 deleted.
			Correction	Note added: when using C3 and C5.
			Correction	Note added: determining capacitor capacitance.
04/10/06	2.2	2.1	Addition	Description of waveform adjustment added.
		2.1.2	Addition	New section 2.1.2 on chip varistors added.
		2.1.3	Correction	Section numbers updated pursuant to the above. Notes partly deleted. Description of waveform adjustment added.
		2.1.4	Addition	Note on external components added.
		2.2	Addition	Varistor and CMC added to the diagram.
05/11/07	2.3	2.2.3	Addition	New section 2.2.3 VBUS Supply Circuit added.
		2.3	Correction	Crystal resonator updated from FA-365 to FA-128. Figure numbers updated from Figure 2-11 to Figure 2-13.

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